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January 2000
Revised January 2000

74LVTH16646
Low Voltage 16-Bit Transceiver/Register with 3-STATE Outputs

General Description

The LVTH16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition (see Functional Description).

The LVTH16646 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

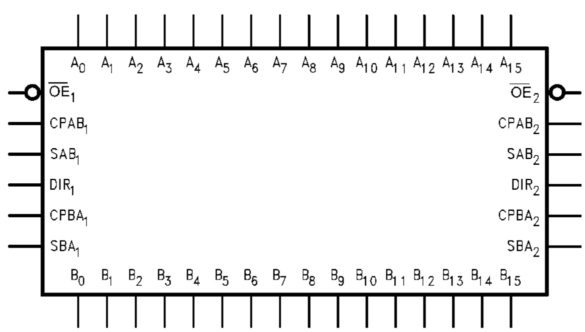
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA

Ordering Code:

Order Number	Package Number	Package Description
74LVTH16646MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LVTH16646MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Logic Symbol



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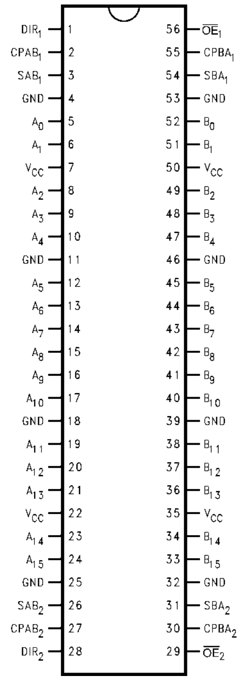
Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/3-STATE Outputs
B_0–B_{15}	Data Register B Inputs/3-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs
DIR_n	Direction Control Inputs

Truth Table (Note 1)

Inputs						Data I/O		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	↑	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data Into B Register
L	H	X	X	L	X			A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Clock A_n Data to A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n into B Register and Output to A_n

H = HIGH Voltage Level
X = Immaterial
L = LOW Voltage Level
↑ = LOW-to-HIGH Transition.

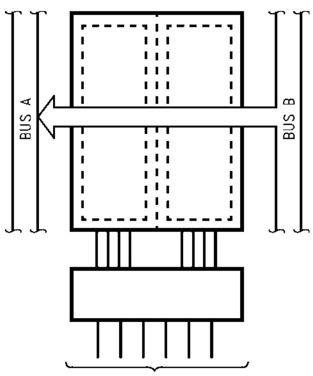
Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB_n, SBA_n) controls can multiplex stored and real-time. The examples shown below demonstrate the four fundamental bus-management functions that can be performed.

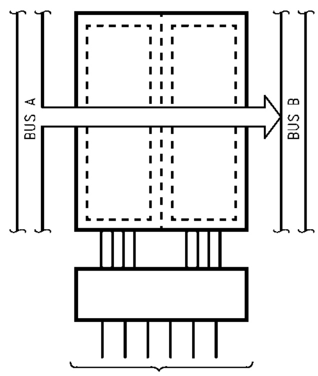
The direction control (DIR_n) determines which bus will receive data when $\overline{OE}_n$ is LOW. In the isolation mode ($\overline{OE}_n$ HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.

Real-Time Transfer
Bus B to Bus A



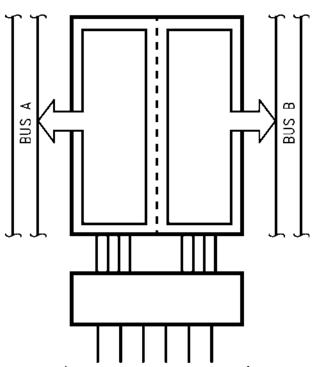
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B



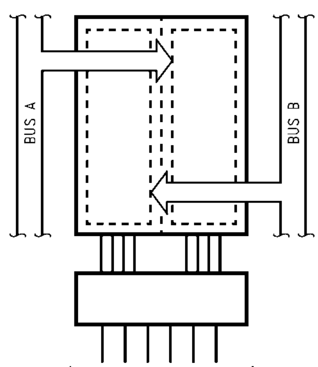
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

Transfer Storage
Data to A or B



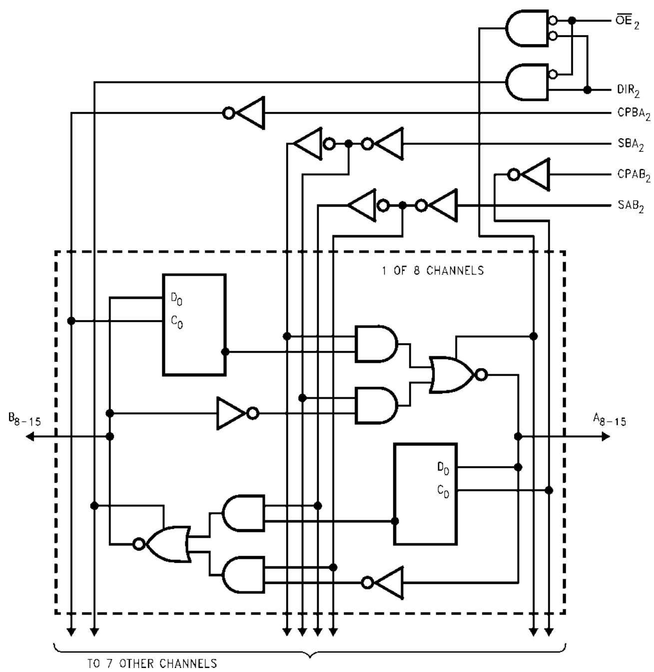
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

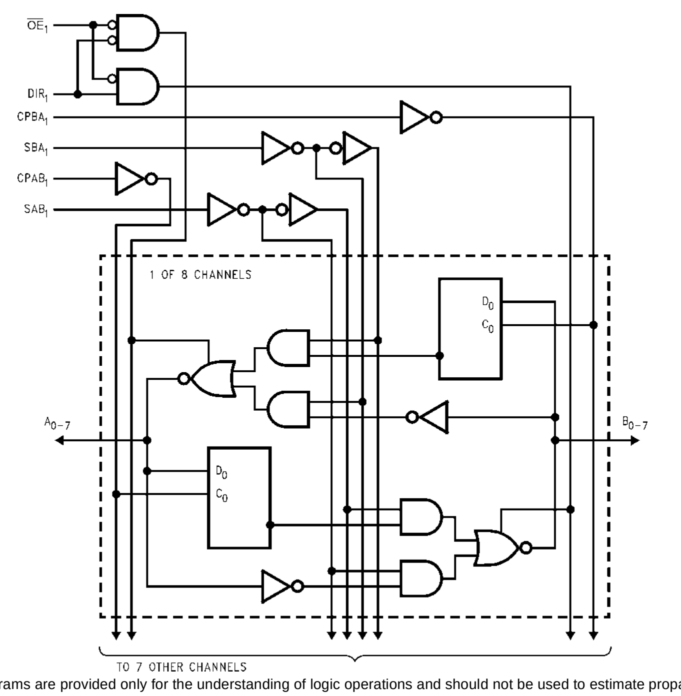
Storage



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	↑	X	L	X
L	L	X	↑	X	L
H	X	↑	X	X	X
H	X	X	↑	X	X

Logic Diagrams





Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−32	mA
I_{OL}	LOW-Level Output Current		64	
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V–2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
				Min	Max		
V_{IK}	Input Clamp Diode Voltage		2.7		–1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \leq 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8		$V_O \geq V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ µA
			2.7	2.4		V	$I_{OH} = -8$ mA
			3.0	2.0		V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	$I_{OL} = 100$ µA
			2.7		0.5	V	$I_{OL} = 24$ mA
			3.0		0.4	V	$I_{OL} = 16$ mA
			3.0		0.5	V	$I_{OL} = 32$ mA
			3.0		0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	$V_I = 0.8V$
				–75		µA	$V_I = 2.0V$
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 4)
				–500		µA	(Note 5)
I_I	Input Current		3.6		10	µA	$V_I = 5.5V$
		Control Pins	3.6		±1	µA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		–5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current		0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$ $V_I = GND$ or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		–5	µA	$V_O = 0.0V$
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.6V$
$I_{OZH}+$	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current		3.6		0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 6)		3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 8)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		–0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$, $V_{CC} = 3.3 \pm 0.3V$ Min	$V_{CC} = 3.3 \pm 0.3V$ Max	$V_{CC} = 2.7V$ Min	$V_{CC} = 2.7V$ Max	Units
f_{MAX}	Maximum Clock Frequency		150		150		MHz
t_{PLH}	Propagation Delay		1.3	5.4	1.3	5.9	ns
t_{PHL}	CPAB or CPBA to A or B		1.3	5.2	1.3	5.8	
t_{PLH}	Propagation Delay		1.0	4.4	1.0	4.7	ns
t_{PHL}	Data to A or B		1.0	4.6	1.0	5.1	
t_{PLH}	Propagation Delay		1.0	4.6	1.0	5.4	ns
t_{PHL}	SBA or SAB to A or B		1.0	4.8	1.0	5.6	
t_{PZH}	Output Enable Time		1.0	4.7	1.0	5.4	ns
t_{PZL}	$\overline{OE}$ to A or B		1.0	5.1	1.0	6.0	
t_{PHZ}	Output Disable Time		2.0	5.6	2.0	6.1	ns
t_{PLZ}	$\overline{OE}$ to A or B		2.0	5.4	2.0	6.1	
t_{PZH}	Output Enable Time		1.0	4.9	1.0	5.4	ns
t_{PZL}	DIR to A or B		1.0	5.4	1.0	6.4	
t_{PHZ}	Output Disable Time		1.5	6.4	1.5	7.1	ns
t_{PLZ}	DIR to A or B		1.5	5.4	1.5	5.9	
t_W	Pulse Duration	CPAB or CPBA HIGH or LOW	3.3		3.3		ns
t_S	Setup Time	A or B before CPAB or CPBA, Data HIGH	1.2		1.5		ns
		A or B before CPAB or CPBA, Data LOW	2.0		2.8		
t_H	Hold Time	A or B after CPAB or CPBA, Data HIGH	0.5		0.0		ns
		A or B after CPAB or CPBA, Data LOW	0.5		0.5		
t_{OSHL}	Output to Output Skew (Note 9)			1.0		1.0	ns
t_{OSLH}				1.0		1.0	

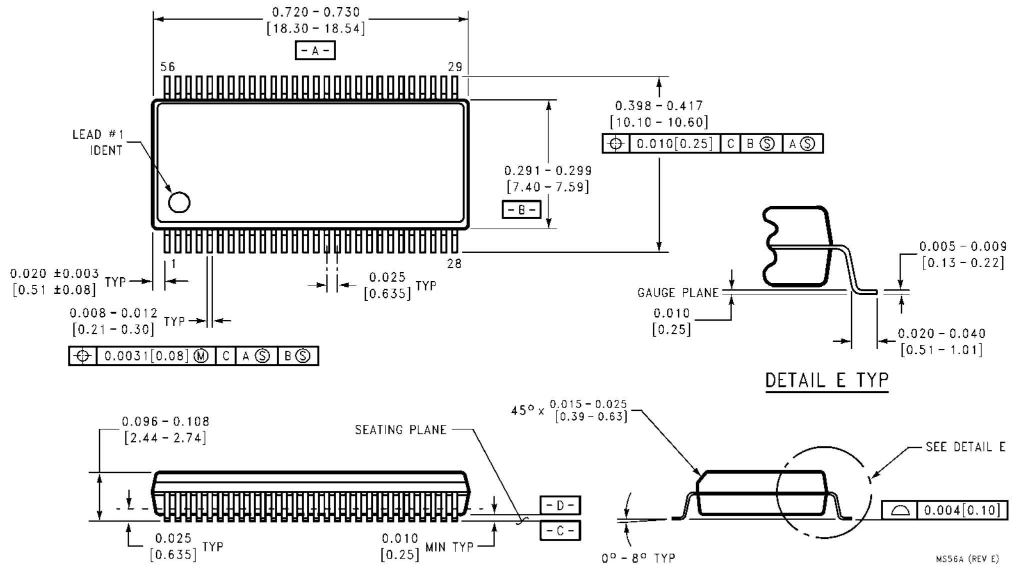
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	8	pF

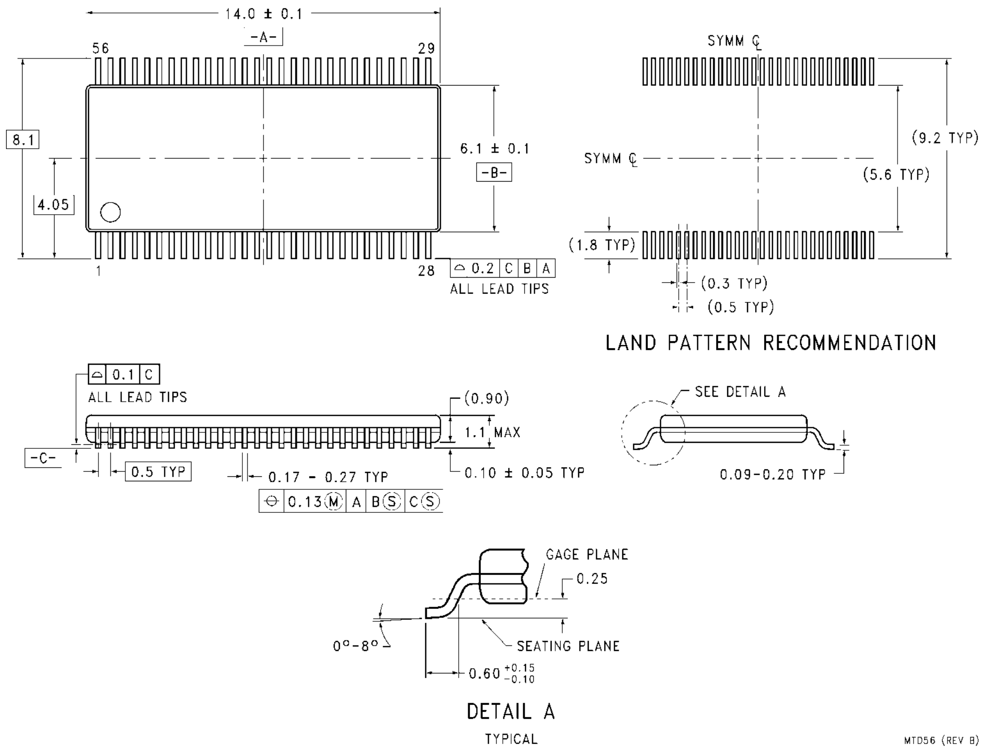
Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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