**signetics**

# TTL 256x1 RAM (54/74S200/201 TRI-STATE) (54/74S301 OPEN COLLECTOR)

# 54/74S200
# 54/74S201
# 54/74S301

FEBRUARY 1975

## DIGITAL 8000 SERIES TTL/MEMORY

## DESCRIPTION

The 54/74S200/201 and 54/74S301 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state outputs options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, three chip enable inputs and PNP input transistors which reduce input loading to 25$\mu$A for a "1" level and $-250\mu$A (S54S200/201/301) or $-100\mu$A (N74S200/201/301) for a "0" level.

The additional feature of output blanking during write ($\overline{D_0}$ terminal "H" or "Hi-Z" state) permits $\overline{D_0}$ and $D_{IN}$ terminals to share a common I/O line to reduce system interconnections. Both devices have fast read access and write cycle times and thus are ideally suited in high speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S200/201/301, B or F. For the military temperature range (−55°C to +125°C) specify S54S200/201/301, F only.

## FEATURES

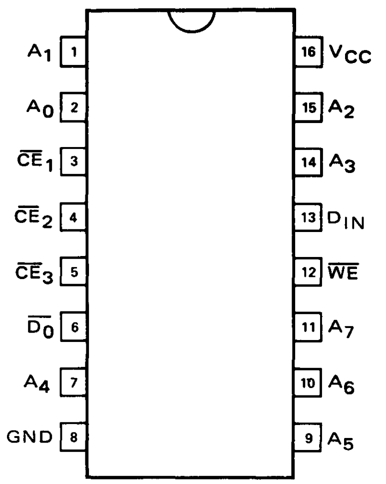
- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
  S54S200/201/301 – 70ns MAXIMUM
  N74S200/201/301 – 50 ns MAXIMUM
- WRITE CYCLE TIME:
  S54S200/201/301 – 60ns MAXIMUM
  N74S200/201/301 – 50ns MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
  S54S200/201/301 – ($-250\mu$A) MAXIMUM
  N74S200/201/301 – ($-100\mu$A) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION:
  TRI-STATE – 54/74S200/201
  OPEN COLLECTOR – 54/74S301
- 16 PIN CERAMIC DIP

## APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

## PIN CONFIGURATION

B, F PACKAGE*



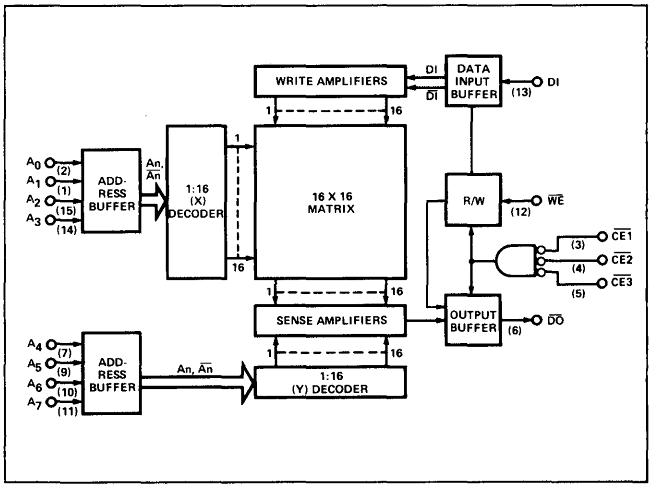
*B – Plastic
F – Cerdip

## TRUTH TABLE

| MODE | $\overline{CE}$* | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | |
|---|---|---|---|---|---|
| | | | | 54/74S301 | 54/74S200/201 |
| READ | 0 | 1 | X | STORED $\overline{DATA}$ | STORED $\overline{DATA}$ |
| WRITE "0" | 0 | 0 | 0 | 1 | High-Z |
| WRITE "1" | 0 | 0 | 1 | 1 | High-Z |
| DISABLED | 1 | X | X | 1 | High-Z |

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | +7 | Vdc |
| $V_{IN}$ | Input Voltage | +5.5 | Vdc |
| $V_{OUT}$ | High Level Output Voltage (54/74S301) | +5.5 | Vdc |
| $V_O$ | Off-State Output Voltage (54/74S200/201) | +5.5 | Vdc |
| $T_A$ | Operating Temperature Range | | |
| | S54S200/201/301 | -55° to +125° | °C |
| | N74S200/201/301) | 0° to +70° | °C |
| $T_{stg}$ | Storage Temperature Range | -65° to +150° | °C |

## ELECTRICAL CHARACTERISTICS

S54S200/201/301 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5V$
N74S200/201/301 $0°C \leqslant T_A \leqslant +70°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

| PARAMETER | | TEST CONDITIONS | S54S200/201/301 | | | N74S200/201/301 | | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP$^2$ | MAX | MIN | TYP$^2$ | MAX | | |
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = MAX | 2.0 | | | 2.0 | | | V | 1 |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = MIN | | | 0.8 | | | 0.85 | V | 1 |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = -18mA | | -0.8 | -1.2 | | -0.8 | -1.2 | V | 1, 8 |
| $V_{OH}$ | High Level Output Voltage (N74S200/201) | $V_{CC}$ = MIN<br>$I_{OH}$ = -10.3mA | | | | 2.4 | | | V | 1, 6 |
| $V_{OH}$ | High Level Output Voltage (S54S200/201) | $V_{CC}$ = MIN<br>$I_{OH}$ = -5.2mA | 2.4 | | | | | | V | 1, 6 |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = MIN<br>$I_{OL}$ = 16mA | | 0.35 | 0.50 | | 0.35 | 0.45 | V | 1, 7 |
| $I_{OLK}$ | Output Leakage Current (54/74S301) | $V_{CC}$ = MIN $V_O$ = 2.4V | | 1 | 50 | | 1 | 40 | µA | 5 |
| | | $V_{IH}$ = 2V $V_O$ = 5.5V | | 1 | 50 | | 1 | 40 | µA | 5 |
| $I_{O(OFF)}$ | Hi-Z State Output Current (54/74S200/201) | $V_{CC}$ = MAX $V_O$ = 5.5V | | 1 | 50 | | 1 | 40 | µA | 5 |
| | | $V_{IH}$ = 2V $V_O$ = 0.4V | | -1 | -50 | | -1 | -40 | µA | 5 |
| $I_I$ | Input Current at $V_{IN}$ MAX | $V_{CC}$ = MAX, $V_{IN}$ = 5.5V | | | 1 | | | 1 | mA | 8 |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = MAX, $V_{IH}$ = 2.7V | | 1 | 25 | | 1 | 25 | µA | 8 |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = MAX, $V_{IL}$ = 0.45V | | -10 | -250 | | -10 | -100 | µA | 8 |
| $I_{OS}$ | Short Circuit Output Current (54/74S200/201) | $V_{CC}$ = MAX $V_O$ = 0V | -30 | | -100 | -30 | | -100 | mA | 3 |
| $I_{CC}$ | $V_{CC}$ Supply Current (54/74S200/201/301) | $V_{CC}$ = MAX | | 80 | 130 | | 80 | 130 | mA | 4 |
| | $V_{CC}$ Supply Current (54S200/201/301) | $V_{CC}$ = MAX, $T_A$ = +125°C | | | 99 | | | | mA | 4 |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V, $V_{CC}$ = 5.0V | | 5 | | | 5 | | pF | |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V, $V_{CC}$ = 5.0V | | 8 | | | 8 | | pF | |

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. $I_{CC}$ is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with $V_{IH}$ applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with logic "0" stored, and $V_{IL}$ applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to $V_{CC}$.
8. Test each input one at the time.

## SWITCHING CHARACTERISTICS

S54S301 $-55°C \leq T_A \leq +125°C, 4.5V \leq V_{CC} \leq 5.5V$
N74S301 $0°C \leq T_A \leq +70°C, 4.75V \leq V_{CC} \leq 5.25V$

| PARAMETER | | TEST CONDITIONS | | S54S301 | | | N74S301 | | | UNIT | NOTES[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | S54S301 | N74S301 | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | | |
| $t_{PLH}$ | Access Time From | $R_{L1} = 270\Omega$<br>$R_{L2} = 1K\Omega$<br>$C_L = 15pF$ | $R_{L1} = 270\Omega$<br>$R_{L2} = 1K\Omega$<br>$C_L = 15pF$ | | 40 | 70 | | 40 | 50 | ns | B, D, E |
| $t_{PHL}$ | Address | | | | 40 | 70 | | 40 | 50 | ns | B, D, E |
| $t_{PHL}$ | Enable Time From Chip Enable | | | | | 45 | | | 35 | ns | C, D, E |
| $t_{PLH}$ | Disable Time From Chip Enable | | | | | 30 | | | 20 | ns | C, D, E |
| $t_{PLH}$ | Disable Time From Write Enable | | | | | 40 | | | 30 | ns | C, D, E |
| $t_{SR}$ | Sense-Recovery Time | | | | | 50 | | | 40 | ns | D |
| $t_W$ | Width of Write Enable Pulse | | | 50 | | | 40 | | | ns | H |
| | **Setup Time:** | | | | | | | | | | D |
| $t_{setup}$ | Address-to-Write Enable | | | 0 | | | 0 | | | ns | |
| | Data-to-Write Enable | | | 50 | | | 40 | | | ns | |
| | Chip Enable-to-Write Enable | | | 0 | | | 0 | | | ns | |
| | **Hold Time:** | | | | | | | | | | |
| $t_{hold}$ | Address-From-Write Enable | | | 10 | | | 10 | | | ns | |
| | Data-From-Write Enable | | | 10 | | | 10 | | | ns | |
| | Chip Enable-From-Write Enable | | | 0 | | | 0 | | | ns | |

## SWITCHING CHARACTERISTICS

S54S200/201 $-55°C \leq T_A \leq +125°C, 4.5V \leq V_{CC} \leq 5.5V$
N74S200/201 $0°C \leq T_A \leq +70°C, 4.75V \leq V_{CC} \leq 5.25V$

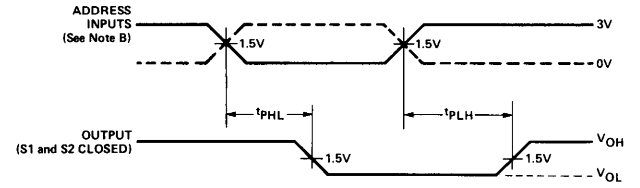
| PARAMETER | | TEST CONDITIONS | | S54S200/201 | | | N74S200/201 | | | UNIT | NOTES[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | S54S200/201 | N74S200/201 | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | | |
| $t_{PLH}$ | Access Time From | $R_L = 270\Omega$<br>$C_L = 15pF$ | $R_L = 270\Omega$<br>$C_L = 15pF$ | | 40 | 70 | | 40 | 50 | ns | B, D, E |
| $t_{PHL}$ | Address | | | | 40 | 70 | | 40 | 50 | ns | B, D, E |
| $t_{ZH}$ | Enable Time From | | | | | 45 | | | 35 | ns | C, D, F, G |
| $t_{ZL}$ | Chip Enable | | | | | 45 | | | 35 | ns | C, D, F, G |
| $t_{HZ}$ | Disable Time From | $R_L = 270\Omega$<br>$C_L = 5pF$ | $R_L = 270\Omega$<br>$C_L = 5pF$ | | | 30 | | | 20 | ns | C, D, F, G |
| $t_{LZ}$ | Chip Enable | | | | | 30 | | | 20 | ns | C, D, F, G |
| $t_{HZ}$ | Disable Time From | | | | | 40 | | | 30 | ns | D, G |
| $t_{LZ}$ | Write Enable | | | | | 40 | | | 30 | ns | D, G |
| $t_{ZH}$ | Sense-Recovery Time | $R_L = 270\Omega$<br>$C_L = 15pF$ | $R_L = 270\Omega$<br>$C_L = 15pF$ | | | 50 | | | 40 | ns | D, F |
| $t_{ZL}$ | | | | | | 50 | | | 40 | ns | D, F |
| $t_W$ | Width of Write Enable Pulse | | | 50 | | | 40 | | | ns | H |
| | **Setup Time:** | | | | | | | | | | D |
| $t_{setup}$ | Address-to-Write Enable | | | 0 | | | 0 | | | ns | |
| | Data-to-Write Enable | | | 50 | | | 40 | | | ns | |
| | Chip Enable-to-Write Enable | | | 0 | | | 0 | | | ns | |
| | **Hold Time:** | | | | | | | | | | |
| $t_{hold}$ | Address-From-Write Enable | | | 10 | | | 10 | | | ns | |
| | Data-From-Write Enable | | | 10 | | | 10 | | | ns | |
| | Chip Enable-From-Write Enable | | | 0 | | | 0 | | | ns | |

NOTES: 1. All typical values are $V_{CC} = 5V$, $T_A = 25°C$. 2. See Notes on Switching Parameter Measurement Information.

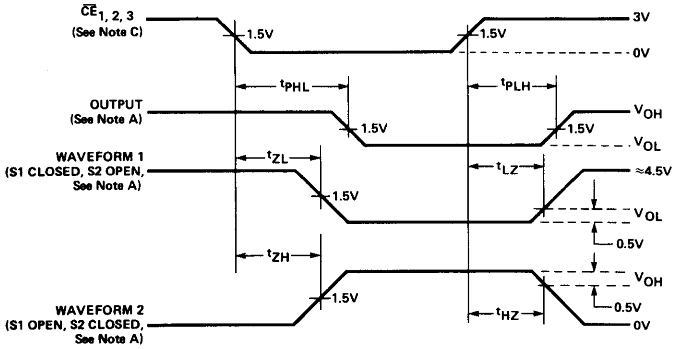
## SWITCHING PARAMETER MEASUREMENT INFORMATION

### READ CYCLE

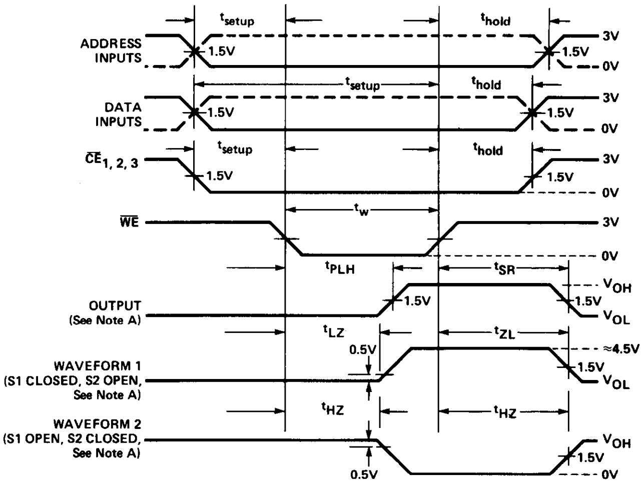
#### ACCESS TIME FROM ADDRESS



#### CHIP ENABLE AND DISABLE TIME

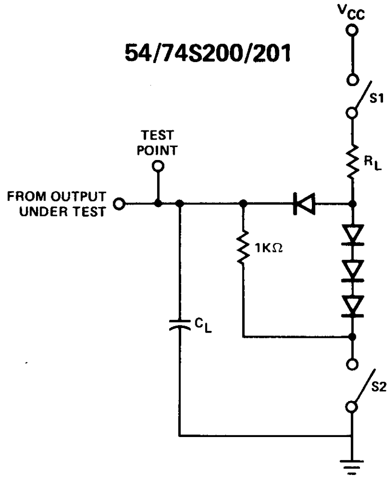


### WRITE CYCLE

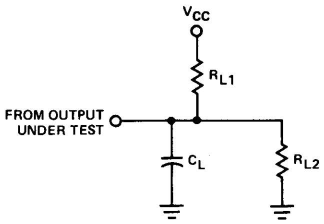


## AC TEST LOAD

**54/74S200/201**



**54/74S301**



$C_L$ INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.

NOTES:

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5ns$, $t_f \leqslant 2.5ns$, PRR $\leqslant$ 1MHz, and $Z_{out} \approx 50\Omega$.
E. $t_{PLH}$ propagation delay time, low-to-high-level output, $t_{PHL}$ propagation delay time, high-to-low-level output.
F. $t_{ZH}$ propagation delay time, hi-Z to high-level output, $t_{ZL}$ propagation delay time, hi-Z to low-level output.
G. $t_{HZ}$ propagation delay time, high-level to hi-Z output, $t_{LZ}$ propagation delay time, low-level to hi-Z output.
H. Minimum required to guarantee a WRITE into the slowest bit.