National Semiconductor

November 1990

DM74S473
(512 x 8) 4096-Bit TTL PROM

General Description

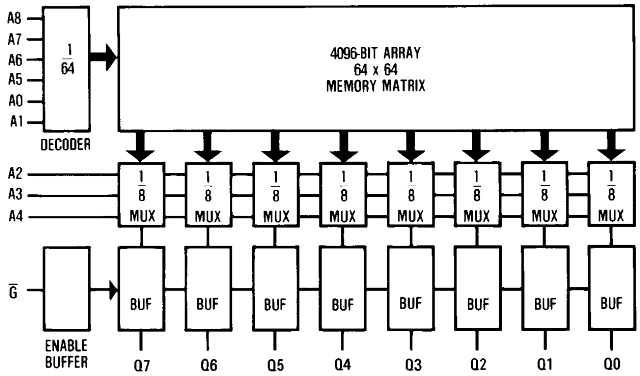
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9715–1

Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

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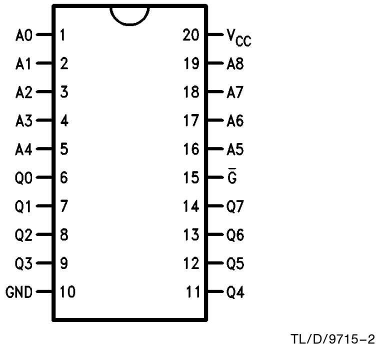
Connection Diagrams

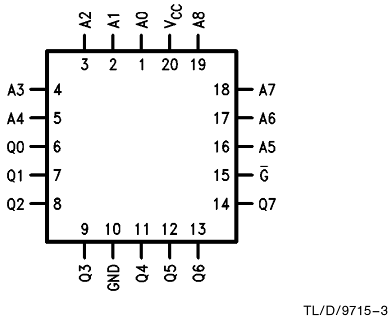
Dual-In-Line Package



Top View

Order Number DM74S473J, 473AJ,
DM74S473N or 473AN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



Top View

Order Number DM74S473V or 473AV
See NS Package Number V20A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S473AN	45
DM74S473N	60
DM74S473AJ	45
DM74S473J	60
DM74S473AV	45
DM74S473V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S473			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	µA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	µA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50	µA
		V_{CC} = Max, V_{CEX} = 5.5V			100	µA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP. RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S473			DM74S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

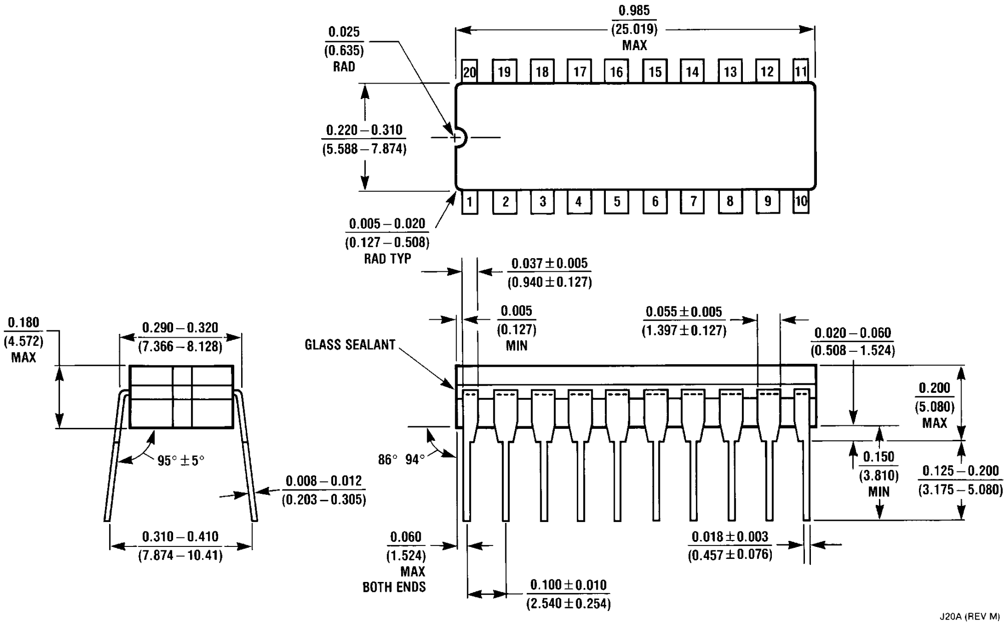
As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

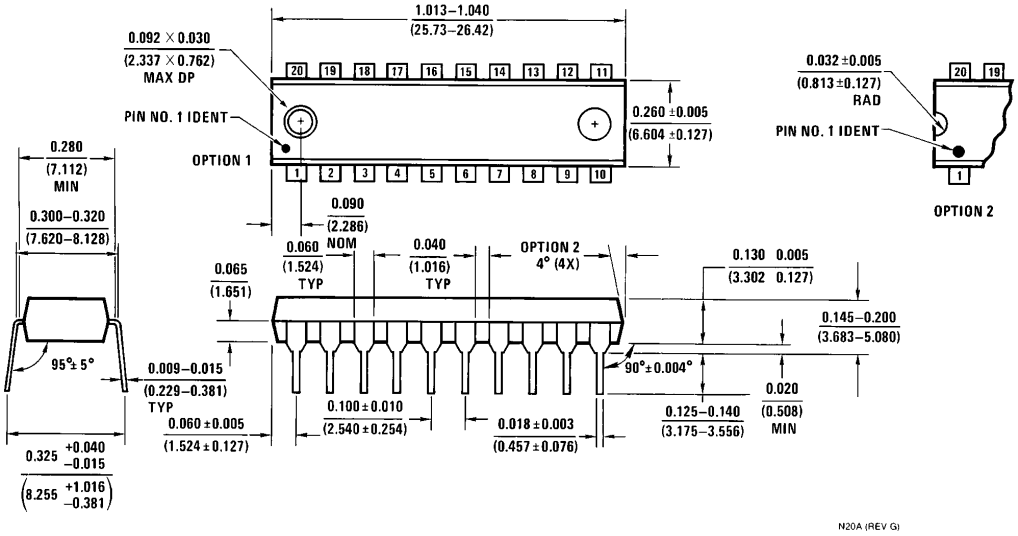
National's Programmable Read-Only Memories (PROMs) feature titanuim-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

Physical Dimensions inches (millimeters)

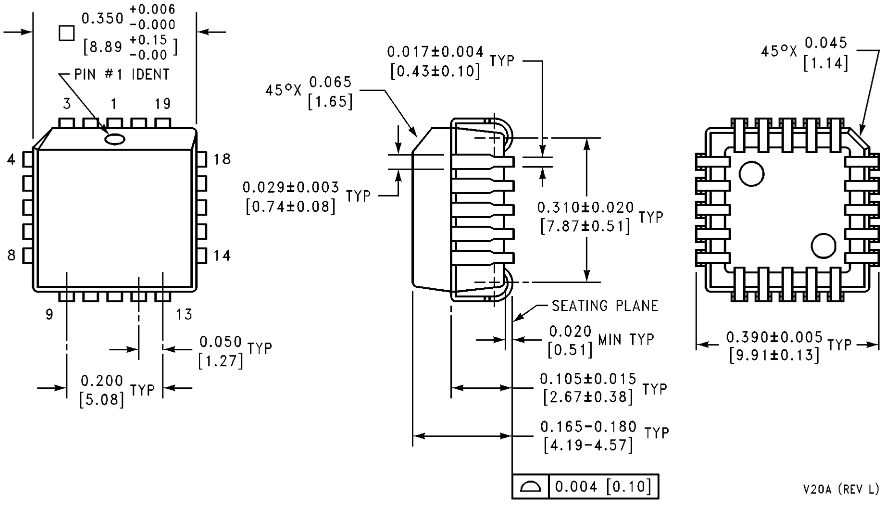


Ceramic Dual-In-Line Package (J)
Order Number DM74S473J or 473AJ
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number DM74S473N or 473AN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Plastic Leaded Chip Carrier (V)
Order Number DM74S473V or 473AV
See NS Package Number V20A

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