

74VCX32500

Low Voltage 36-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The VCX32500 is an 36-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in a high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active HIGH and OEBA is active LOW).

The VCX32500 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX32500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
 - 2.9 ns max for 3.0V to 3.6V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ± 24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model >200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, OEBA should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

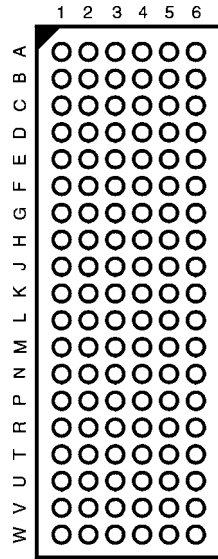
Order Number	Package Number	Package Description
74VCX32500G (Note 2)(Note 3)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 2: Ordering Code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74VCX32500 Low Voltage 36-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	1A ₂	1A ₁	LEAB ₁	CLKAB ₁	1B ₁	1B ₂
B	1A ₄	1A ₃	OEAB ₁	GND	1B ₃	1B ₄
C	1A ₆	1A ₅	GND	GND	1B ₅	1B ₆
D	1A ₈	1A ₇	V _{CC}	V _{CC}	1B ₇	1B ₈
E	1A ₁₀	1A ₉	GND	GND	1B ₉	1B ₁₀
F	1A ₁₂	1A ₁₁	GND	GND	1B ₁₁	1B ₁₂
G	1A ₁₄	1A ₁₃	V _{CC}	V _{CC}	1B ₁₃	1B ₁₄
H	1A ₁₅	1A ₁₆	GND	GND	1B ₁₆	1B ₁₅
J	1A ₁₇	1A ₁₈	OEBA ₁	CLKBA ₁	1B ₁₈	1B ₁₇
K	NC	LEAB ₂	LEBA ₁	GND	CLKAB ₂	NC
L	2A ₂	2A ₁	OEAB ₂	GND	2B ₁	2B ₂
M	2A ₄	2A ₃	GND	GND	2B ₃	2B ₄
N	2A ₆	2A ₅	V _{CC}	V _{CC}	2B ₅	2B ₆
P	2A ₈	2A ₇	GND	GND	2B ₇	2B ₈
R	2A ₁₀	2A ₉	GND	GND	2B ₉	2B ₁₀
T	2A ₁₂	2A ₁₁	V _{CC}	V _{CC}	2B ₁₁	2B ₁₂
U	2A ₁₄	2A ₁₃	GND	GND	2B ₁₃	2B ₁₄
V	2A ₁₅	2A ₁₆	OEBA ₂	CLKBA ₂	2B ₁₆	2B ₁₅
W	2A ₁₇	2A ₁₈	LEBA ₂	GND	2B ₁₈	2B ₁₇

Pin Descriptions

Pin Names	Description
OEAB _n	Output Enable Input for A to B Direction (Active HIGH)
OEBA _n	Output Enable Input for B to A Direction (Active LOW)
LEAB _n , LEBA _n	Latch Enable Inputs
CLKAB _n , CLKBA _n	Clock Inputs
1A ₁ –1A ₁₈ 2A ₁ –2A ₁₈	Side A Inputs or 3-STATE Outputs
1B ₁ –1B ₁₈ 2B ₁ –2B ₁₈	Side B Inputs or 3-STATE Outputs

Function Table (Note 4)

Inputs				Outputs
OEAB _n	LEAB _n	CLKAB _n	A _n	B _n
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ (Note 5)
H	L	L	X	B ₀ (Note 6)

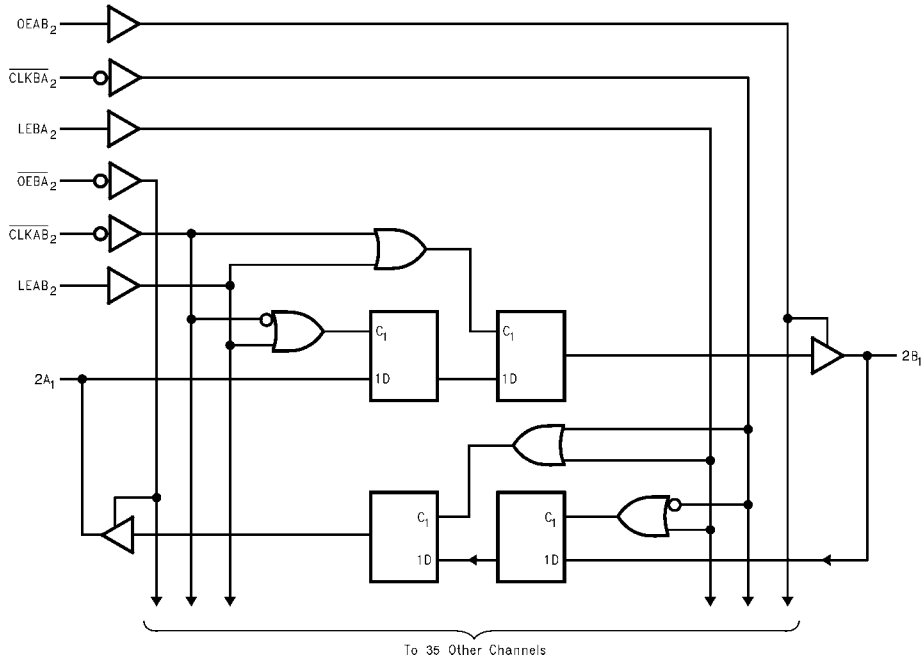
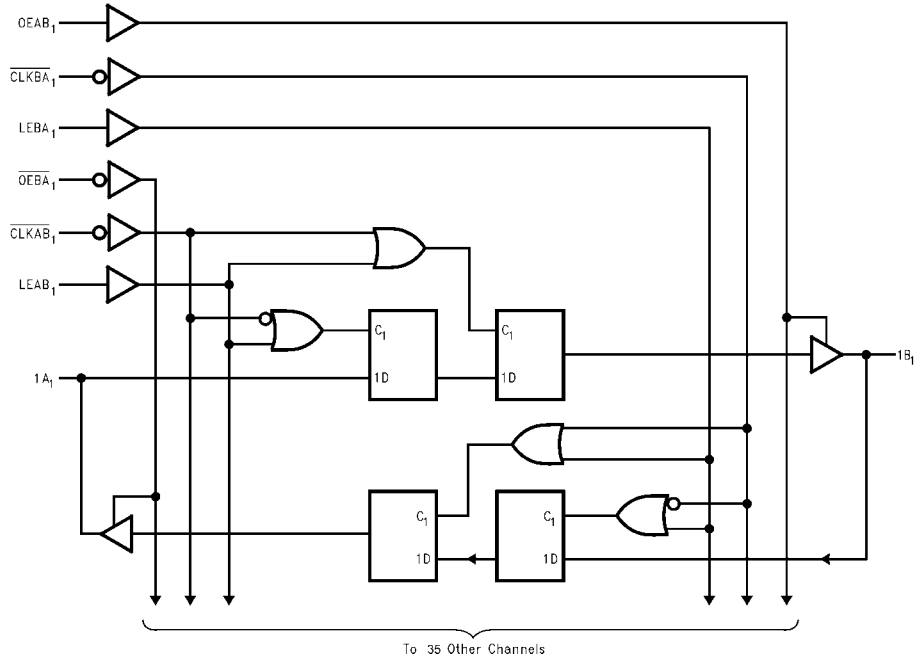
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Note 4: A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA and CLKBA. OEBA is active LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

Logic Diagrams



Absolute Maximum Ratings (Note 7)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 8)	-0.5 to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 9)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
$V_{CC} = 1.4V$ to 1.6V	± 2 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 7: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
		$I_{OH} = -12 \text{ mA}$	3.0	2.4		
			3.0	2.2		
		$I_{OH} = -18 \text{ mA}$	2.3 - 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
		$I_{OH} = -6 \text{ mA}$	2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		
			1.65	1.25		
$I_{OH} = -100 \mu A$	1.4 - 1.6	$V_{CC} - 0.2$				
	1.4	1.05				
$I_{OH} = -2 \text{ mA}$						

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7	0.4		
		I _{OL} = 18 mA	3.0	0.4		
		I _{OL} = 24 mA	3.0	0.55		
		I _{OL} = 100 μA	2.3 - 2.7	0.2		
		I _{OL} = 12 mA	2.3	0.4		
		I _{OL} = 18 mA	2.3	0.6		
		I _{OL} = 100 μA	1.65 - 2.3	0.2		
	I _{OL} = 6 mA	1.65	0.3			
	I _{OL} = 100 μA	1.4 - 1.6	0.2			
	I _{OL} = 2 mA	1.4	0.35			
I _I	Input Leakage Current	0V ≤ V _I ≤ 3.6V	1.4 - 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0V ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.4 - 3.6		±10.0	μA
I _{OFF}	Power Off Leakage Current	0V ≤ (V _I , V _O) ≤ 3.6V	0		10.0	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.4 - 3.6		40.0	μA
		V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 10)	1.4 - 3.6		±40.0	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA

Note 10: Outputs disabled or 3-STATE only.**AC Electrical Characteristics** (Note 11)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{MAX}	Setup Time	C _L = 30 pF	3.3 ± 0.3	250		MHz	
			2.5 ± 0.2	200			
			1.8 ± 0.15	100			
		C _L = 15 pF	1.5 ± 0.1	80.0			
t _{PHL}	Propagation Delay	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	2.7	ns	Figures 1, 2
t _{PLH}	Bus-to-Bus		2.5 ± 0.2	0.8	3.5		
			1.8 ± 0.15	1.5	7.0		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	14.0		Figures 7, 8
t _{PHL}	Propagation Delay	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	4.2	ns	Figures 1, 2
t _{PLH}	Clock-to-Bus		2.5 ± 0.2	0.8	5.3		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t _{PHL}	Propagation Delay	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.8	ns	Figures 1, 2
t _{PLH}	LE-to-Bus		2.5 ± 0.2	0.8	4.9		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t _{PZL}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.8	ns	Figures 1, 3, 4
t _{PZH}			2.5 ± 0.2	0.8	4.9		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t _{PLZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.7	ns	Figures 1, 3, 4
t _{PHZ}			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	7.6		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	15.2		Figures 7, 9, 10

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _S	Setup Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 6
			2.5 ± 0.2	1.5			
		C _L = 15 pF, R _L = 500Ω	1.8 ± 0.15	2.5			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	3.0			Figures 7, 8
t _H	Hold Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
		C _L = 15 pF, R _L = 500Ω	1.8 ± 0.15	1.0			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	2.0			Figures 7, 6
t _W	Pulse Width	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 5
			2.5 ± 1.2	1.5			
		C _L = 15 pF, R _L = 500Ω	1.8 ± 0.15	4.0			
		C _L = 15 pF, R _L = 500Ω	1.5 ± 0.1	4.0			Figures 5, 7

Note 11: For C_L = 50pF, add approximately 300ps to the AC maximum specification.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
C _{IN}	Input Capacitance	V _I = 0V or V _{CC} V _{CC} = 1.8V, 2.5V, or 3.3V,	6.0	pF
C _{I/O}	Output Capacitance	V _I = 0V, or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7.0	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz V _{CC} = 1.8V, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms ($V_{CC} 3.3V \pm 0.3V$ to $1.8V \pm 0.15V$)

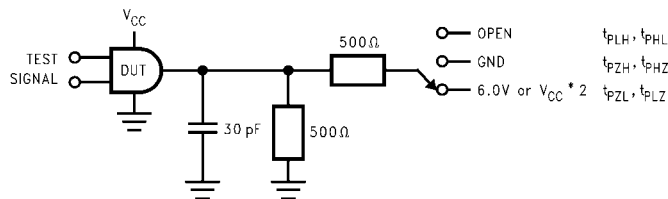


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8 \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

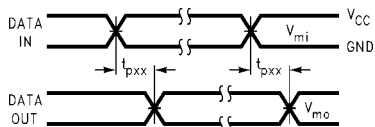


FIGURE 2. Waveform for Inverting and Non-inverting Functions

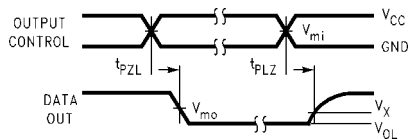


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

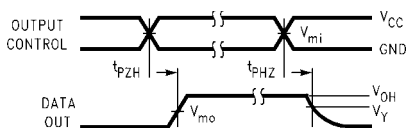


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

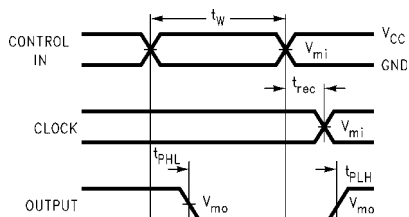


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

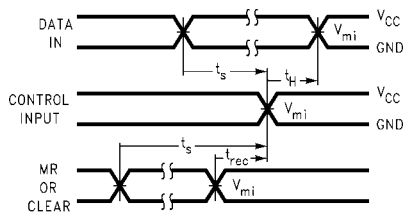
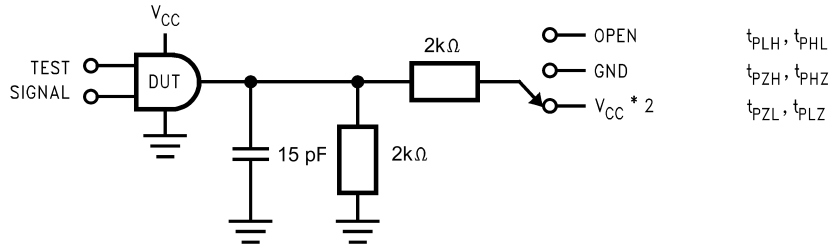


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8 \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5V \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

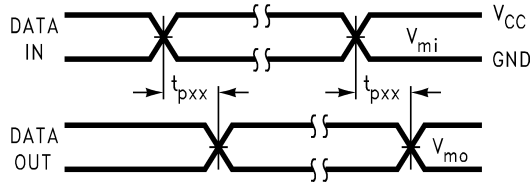


FIGURE 8. Waveform for Inverting and Non-Inverting Functions

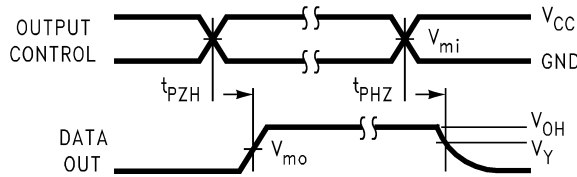


FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

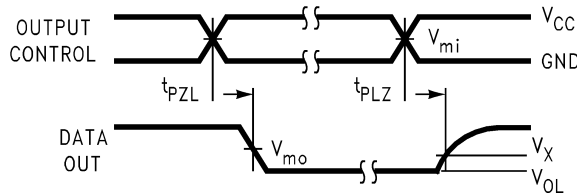
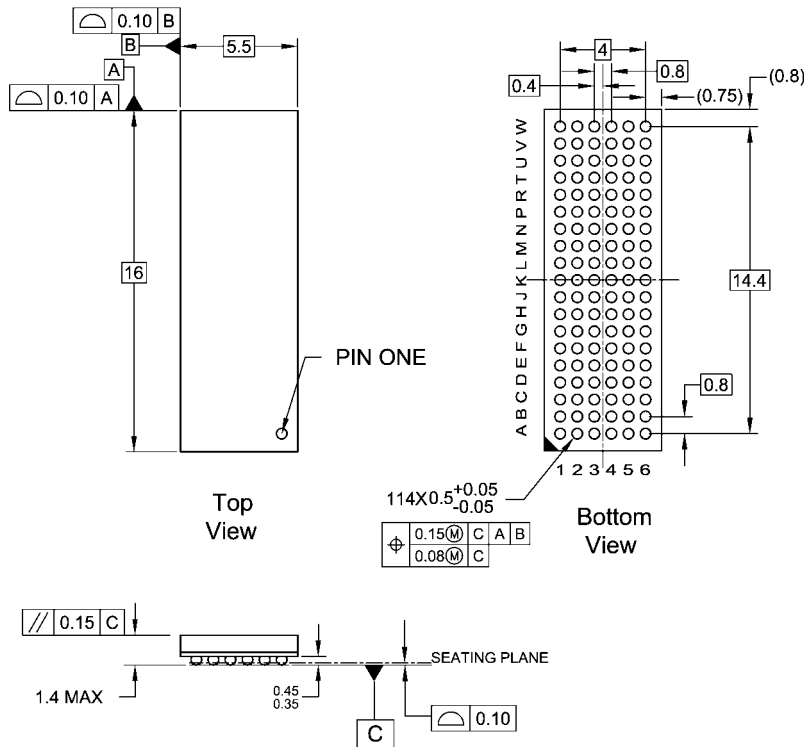


FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_x	$V_{OL} + 0.1V$
V_y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
 - B. ALL DIMENSIONS IN MILLIMETERS
 - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
 - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

**114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A**

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