74VCX16374

Low-Voltage 1.8/2.5/3.3V 16-Bit D-Type Flip-Flop

With 3.6 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

ON Semiconductor®

http://onsemi.com

The 74VCX16374 is an advanced performance, non−inverting 16−bit D−type flip−flop. It is designed for very high−speed, very low−power operation in 1.8 V, 2.5 V or 3.3 V systems. The VCX16374 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for a full 16−bit operation.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be overvoltage tolerant to 3.6 V.

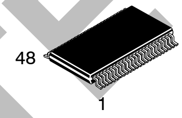
The 74VCX16374 consists of 16 edge−triggered flip−flops with individual D−type inputs and 3.6 V−tolerant 3−state outputs. The clocks (CPn) and Output Enables ($\overline{\text{OEn}}$) are common to all flip−flops within the respective byte. The flip−flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW−to−HIGH Clock (CP) transition. With the $\overline{\text{OE}}$ LOW, the contents of the flip−flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. The $\overline{\text{OE}}$ input level does not affect the operation of the flip−flops.

Features

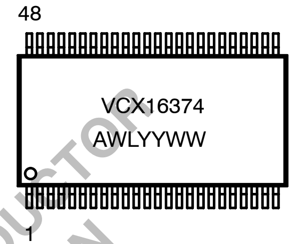
- Designed for Low Voltage Operation: V_{CC} = 1.65 V − 3.6 V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.0 ns max for 3.0 V to 3.6 V
  3.9 ns max for 2.3 V to 2.7 V
  7.8 ns max for 1.65 V to 1.95 V
- Static Drive: ±24 mA Drive at 3.0 V
  ±18 mA Drive at 2.3 V
  ±6 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V
  Machine Model >200 V
- All Devices in Package TSSOP are Inherently Pb−Free*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



TSSOP−48
DT SUFFIX
CASE 1201



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

Pins	Function
OEn	Output Enable Inputs
CPn	Clock Pulse Inputs
D0−D15	Inputs
O0−O15	Outputs

ORDERING INFORMATION

Device	Package	Shipping†
74VCX16374DT	TSSOP (Pb−Free)	39 / Rail
74VCX16374DTR	TSSOP (Pb−Free)	2500 / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

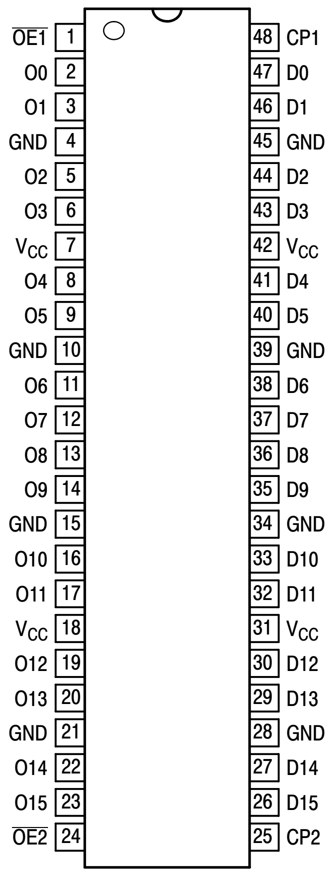


Figure 1. 48–Lead Pinout
(Top View)

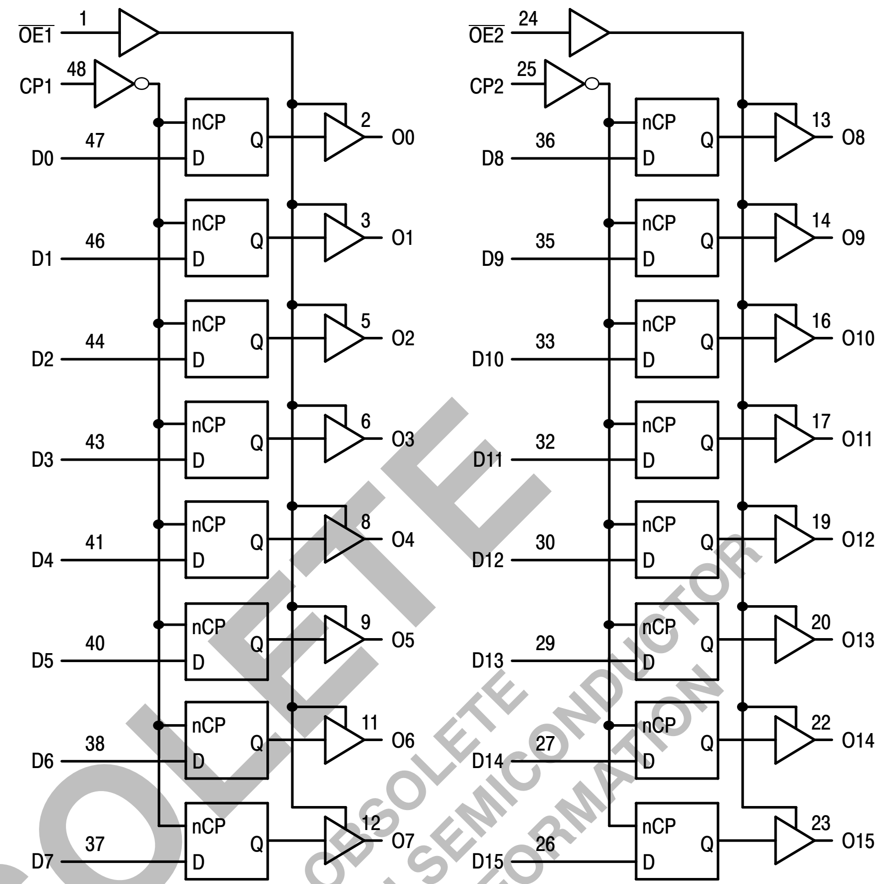


Figure 2. Logic Diagram

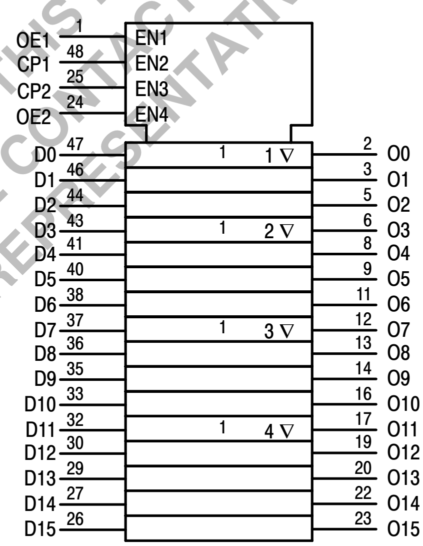


Figure 3. IEC Logic Diagram

TRUTH TABLE

Inputs			Outputs	Inputs			Outputs
CP1	OE1	D0:7	O0:7	CP2	OE2	D8:15	O8:15
↑	L	H	H	↑	L	H	H
↑	L	L	L	↑	L	L	L
X	L	X	O0	X	L	X	O0
X	H	X	Z	X	H	X	Z

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
↑ = Low−to−High Transition
X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs
O0 = No Change

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +4.6$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +4.6$	Output in 3−State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Note 1; Outputs Active	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		−0.3		3.6	V
V_O	Output Voltage	(Active State) (3−State)	0 0		V_{CC} 3.6	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0 V − 3.6 V				−24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0 V − 3.6 V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.3 V − 2.7 V				−18	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.3 V − 2.7 V				18	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 1.65 V − 1.95 V				−6	mA
I_{OL}	LOW Level Output Current, V_{CC} = 1.65 V − 1.95 V				6	mA
T_A	Operating Free−Air Temperature		−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2)	1.65 V ≤ V_{CC} < 2.3 V	0.65 x V_{CC}		V
		2.3 V ≤ V_{CC} ≤ 2.7 V	1.6		
		2.7 V < V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	1.65 V ≤ V_{CC} < 2.3 V		0.35 x V_{CC}	V
		2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	
		2.7 V < V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 μA	V_{CC} − 0.2		V
		V_{CC} = 1.65 V; I_{OH} = −6 mA	1.25		
		V_{CC} = 2.3 V; I_{OH} = −6 mA	2.0		
		V_{CC} = 2.3 V; I_{OH} = −12 mA	1.8		
		V_{CC} = 2.3 V; I_{OH} = −18 mA	1.7		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 1.65 V; I_{OL} = 6 mA		0.3	
		V_{CC} = 2.3 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 2.3 V; I_{OL} = 18 mA		0.6	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 18 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	1.65 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_I ≤ 3.6 V		±5.0	μA
I_{OZ}	3−State Output Current	1.65 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_O ≤ 3.6 V; V_I = V_{IH} or V_{IL}		±10	μA
I_{OFF}	Power−Off Leakage Current	V_{CC} = 0 V; V_I or V_O = 3.6 V		10	μA
I_{CC}	Quiescent Supply Current (Note 3)	1.65 V ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		20	μA
		1.65 V ≤ V_{CC} ≤ 3.6 V; 3.6 V ≤ V_I, V_O ≤ 3.6 V		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 V < V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		750	μA

2. These values of V_I are used to test DC electrical characteristics only.
3. Outputs disabled or 3−state only.

AC CHARACTERISTICS (Note 4; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	$T_A = -40°C$ to $+85°C$						Unit
			$V_{CC} = 3.0$ V to 3.6 V		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} = 1.65$ V to 1.95 V		
			Min	Max	Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	1	250		200		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP−to−On	1	0.8 0.8	3.0 3.0	1.0 1.0	3.9 3.9	1.5 1.5	7.8 7.8	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	4.6 4.6	1.5 1.5	9.2 9.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	3.8 3.8	1.5 1.5	6.8 6.8	ns
t_s	Setup Time, High or Low Dn−to−CP	3	1.5		1.5		2.5		ns
t_h	Hold Time, High or Low Dn−to−CP	3	1.0		1.0		1.0		ns
t_w	CP Pulse Width, High	3	1.5		1.5		4.0		ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 5)			0.5 0.5		0.5 0.5		0.75 0.75	ns

4. For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.
5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

AC CHARACTERISTICS ($t_R = t_F = 2.0$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	$T_A = -40°C$ to $+85°C$				Unit
			$V_{CC} = 3.0$ V to 3.6 V		$V_{CC} = 2.7$ V		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	4	150		150		MHz
t_{PLH} t_{PHL}	Propagation Delay CP−to−On	4	1.0 1.0	4.2 4.2		4.9 4.9	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	5	1.0 1.0	4.8 4.8		5.9 5.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	5	1.0 1.0	4.3 4.3		4.7 4.7	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 6)			0.5 0.5		0.5 0.5	ns

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

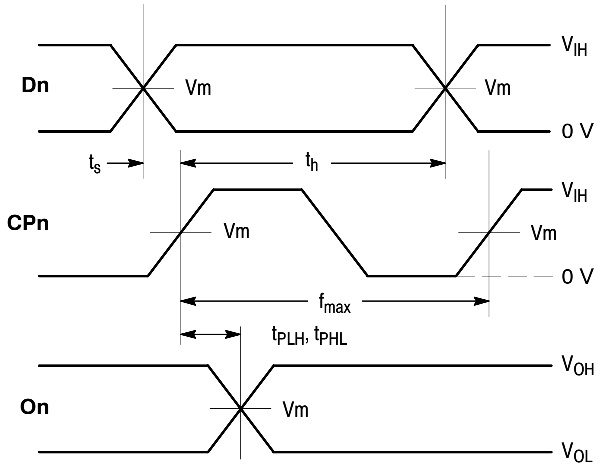
Symbol	Characteristic	Condition	T_A = +25°C	Unit
			Typ	
V_{OLP}	Dynamic LOW Peak Voltage (Note 7)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	0.25	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	0.6	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	0.8	
V_{OLV}	Dynamic LOW Valley Voltage (Note 7)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	−0.25	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	−0.6	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	−0.8	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 8)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.5	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.9	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	2.2	

7. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.
8. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

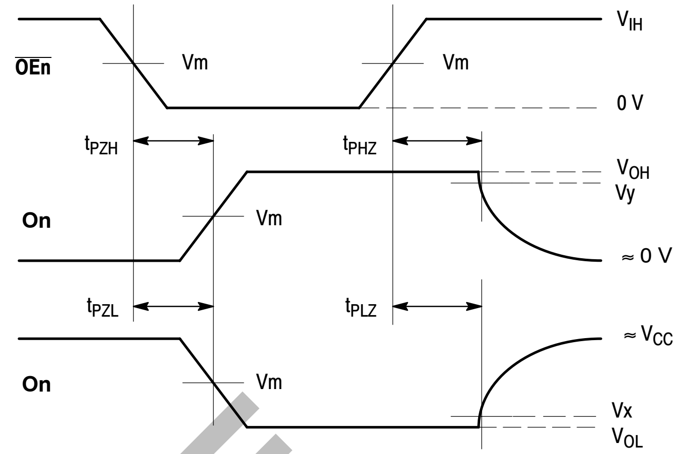
Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 9	6	pF
C_{OUT}	Output Capacitance	Note 9	7	pF
C_{PD}	Power Dissipation Capacitance	Note 9, 10 MHz	20	pF

9. V_{CC} = 1.8 V, 2.5 V or 3.3 V; V_I = 0 V or V_{CC}.



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES

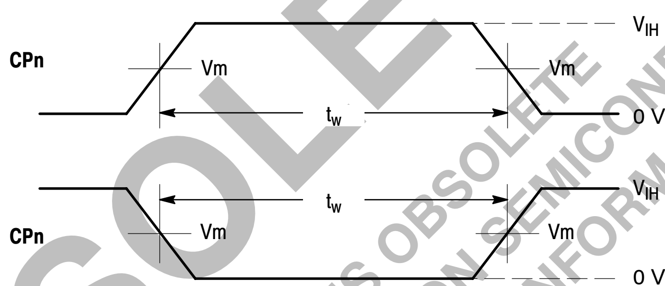
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

Figure 4. AC Waveforms



WAVEFORM 3 – PULSE WIDTH

$t_R = t_F = 2.0$ ns (or fast as required) from 10% to 90%

Figure 5. AC Waveforms

Table 1. AC WAVEFORMS

Symbol	V_{CC} 3.3 V ± 0.3 V	V_{CC} 2.5 V ± 0.2 V	V_{CC} 1.8 V ± 0.15 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_m	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_x	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_y	V_{OH} – 0.3 V	V_{OH} – 0.15 V	V_{OH} – 0.15 V

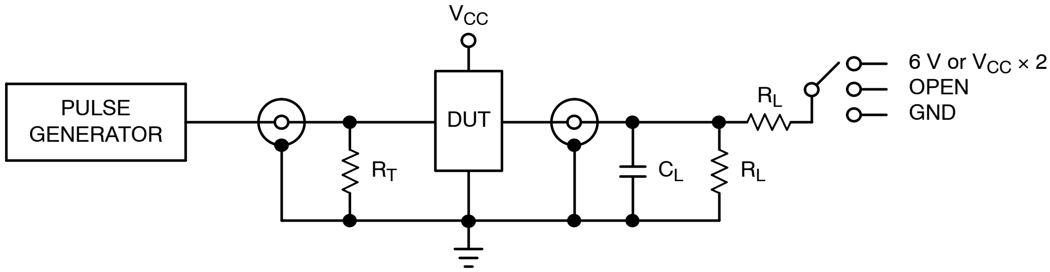
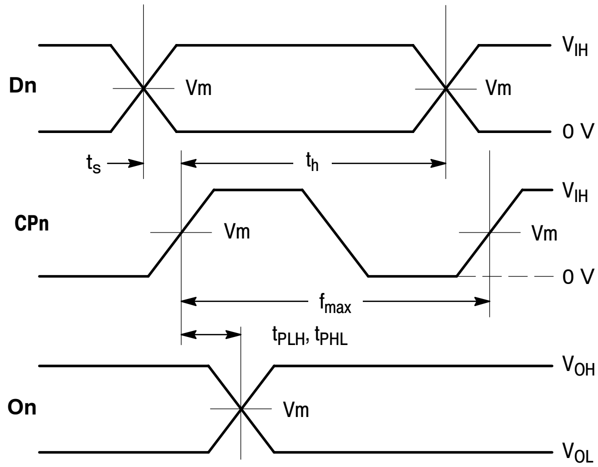


Figure 6. Test Circuit

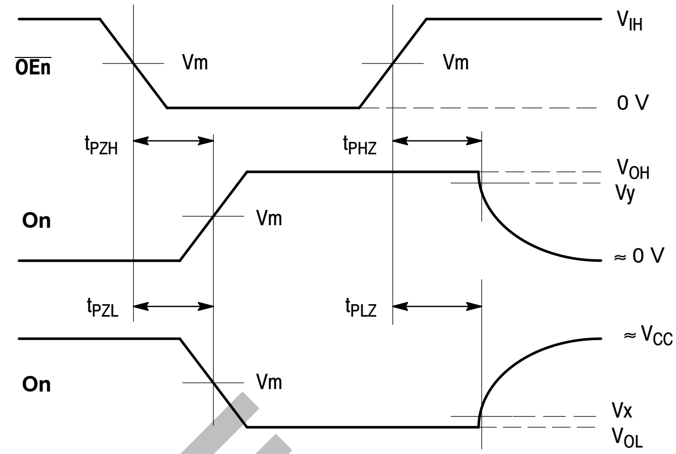
Table 2. TEST CIRCUIT

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V; V_{CC} × 2 at V_{CC} = 2.5 ± 0.2 V; 1.8 ± 0.15 V
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (Includes jig and probe capacitance)
R_L = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

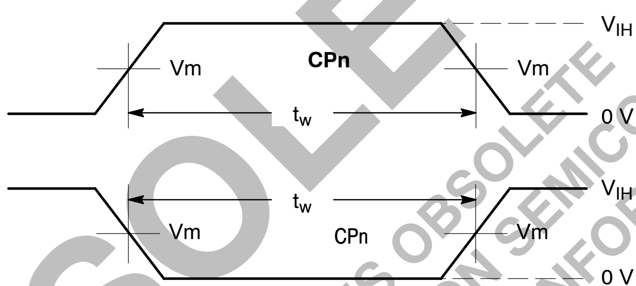


WAVEFORM 4 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns



WAVEFORM 5 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

Figure 7. AC Waveforms



WAVEFORM 6 – PULSE WIDTH
$t_R = t_F = 2.0$ ns (or fast as required) from 10% to 90%

Figure 8. AC Waveforms

Table 3. AC WAVEFORMS

Symbol	V_{CC}	
	3.3 V ± 0.3 V	**2.7 V**
V_{IH}	2.7 V	2.7 V
V_m	1.5 V	1.5 V
V_x	V_{OL} + 0.3 V	V_{OL} + 0.3 V
V_y	V_{OH} – 0.3 V	V_{OH} – 0.3 V

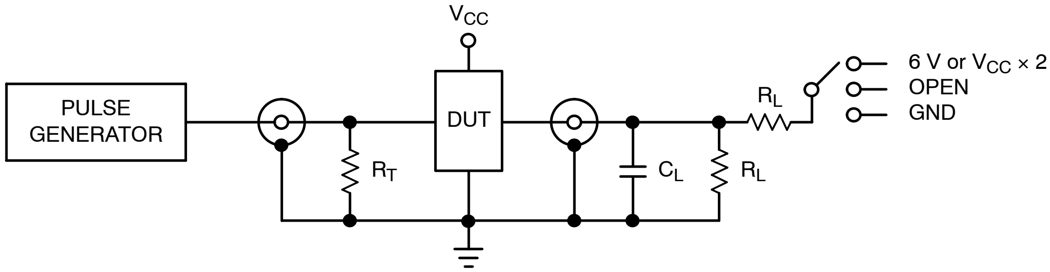


Figure 9. Test Circuit

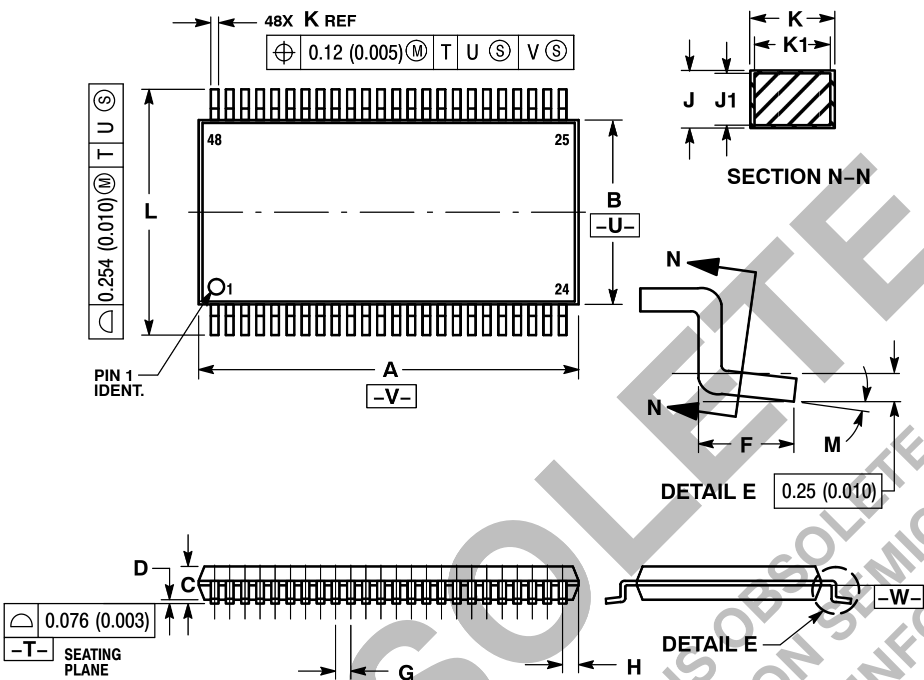
Table 4. TEST CIRCUIT

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V; V_{CC} × 2 at V_{CC} = 2.5 ± 0.2 V; 1.8 ± 0.15 V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF or equivalent (Includes jig and probe capacitance)
R_L = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative