FAIRCHILD

SEMICONDUCTOR ™

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74VCX16821
Low Voltage 20-Bit D-Type Flip-Flops with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16821 contains twenty non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications.

The 74VCX16821 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX16821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
    3.5 ns max for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
    ±24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
   Human body model > 2000V
    Machine model > 200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX16821MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
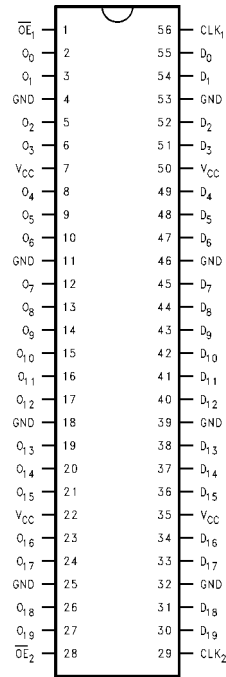
Logic Symbol
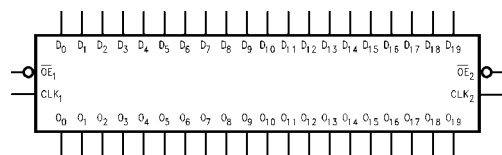
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CLK_n	Clock Input
D_0–D_{19}	Inputs
O_0–O_{19}	Outputs

Connection Diagram

$\overline{OE}_1$	1		56	CLK_1
O_0	2		55	D_0
O_1	3		54	D_1
GND	4		53	GND
O_2	5		52	D_2
O_3	6		51	D_3
V_{CC}	7		50	V_{CC}
O_4	8		49	D_4
O_5	9		48	D_5
O_6	10		47	D_6
GND	11		46	GND
O_7	12		45	D_7
O_8	13		44	D_8
O_9	14		43	D_9
O_{10}	15		42	D_{10}
O_{11}	16		41	D_{11}
O_{12}	17		40	D_{12}
GND	18		39	GND
O_{13}	19		38	D_{13}
O_{14}	20		37	D_{14}
O_{15}	21		36	D_{15}
V_{CC}	22		35	V_{CC}
O_{16}	23		34	D_{16}
O_{17}	24		33	D_{17}
GND	25		32	GND
O_{18}	26		31	D_{18}
O_{19}	27		30	D_{19}
$\overline{OE}_2$	28		29	CLK_2

Truth Tables

Inputs			Outputs
CLK_1	$\overline{OE}_1$	D_0–D_9	O_0–O_9
X	H	X	Z
⟋	L	L	L
⟋	L	H	H
L or H	L	X	O_0

Inputs			Outputs
CLK_2	$\overline{OE}_2$	D_{10}–D_{19}	O_{10}–O_{19}
X	H	X	Z
⟋	L	L	L
⟋	L	H	H
L or H	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance
O_0 = Previous O_0 before LOW-to-HIGH transition of Clock
⟋ = LOW-to-HIGH transition

Functional Description

The VCX16821 contains twenty D-type flip-flops with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of each other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the flip-flops.

Logic Diagrams
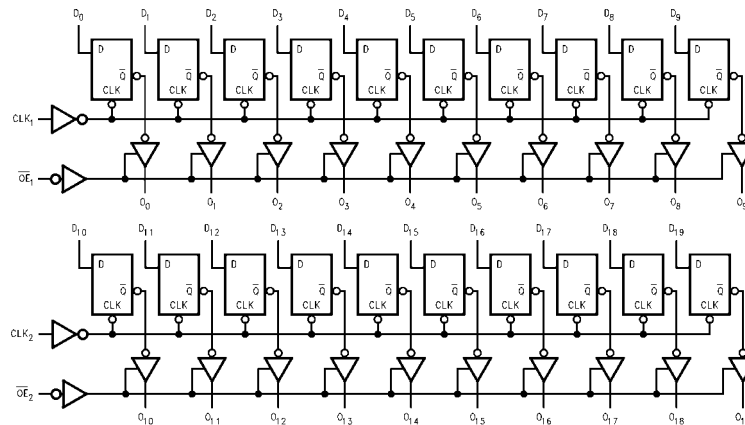
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})   −0.5V to +4.6V
DC Input Voltage (V_I)   −0.5V to +4.6V
Output Voltage (V_O)
   Outputs 3-STATE   −0.5V to +4.6V
   Outputs Active (Note 3)   −0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V   −50 mA
DC Output Diode Current (I_{OK})
   V_O < 0V   −50 mA
   V_O > V_{CC} +50 mA
DC Output Source/Sink Current
   (I_{OH}/I_{OL})   ±50 mA
DC V_{CC} or GND Current per
   Supply Pin (I_{CC} or GND)   ±100 mA
Storage Temperature Range (T_{STG})   −65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply
   Operating   1.4V to 3.6V
Input Voltage   −0.3V to +3.6V
Output Voltage (V_O)
   Output in Active States   0V to V_{CC}
   Output in 3-STATE   0.0V to 3.6V
Output Current in I_{OH}/I_{OL}
   V_{CC} = 3.0V to 3.6V   ±24 mA
   V_{CC} = 2.3V to 2.7V   ±18 mA
   V_{CC} = 1.65V to 2.3V   ±6 mA
   V_{CC} = 1.4V to 1.6V   ±2 mA
Free Air Operating Temperature (T_A)   −40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)
   V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V   10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		
			1.4 - 1.6	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	
			1.4 - 1.6		0.35 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
		I_{OH} = −100 µA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.8		
		I_{OH} = −18 mA	2.3	1.7		
		I_{OH} = −100 µA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −6 mA	1.65	1.25		
		I_{OH} = −100 µA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −12 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V$_{CC}$ (V)	Min	Max	Units
V$_{OL}$	LOW Level Output Voltage	I$_{OL}$ = 100 µA	2.7 - 3.6		0.2	V
		I$_{OL}$ = 12 mA	2.7		0.4	
		I$_{OL}$ = 18 mA	3.0		0.4	
		I$_{OL}$ = 24 mA	3.0		0.55	
		I$_{OL}$ = 100 µA	2.3 - 2.7		0.2	
		I$_{OL}$ = 6 mA	2.3		0.4	
		I$_{OL}$ = 12 mA	2.3		0.6	
		I$_{OL}$ = 100 µA	1.65 - 2.3		0.2	
		I$_{OL}$ = 6 mA	1.65		0.3	
		I$_{OL}$ = 100 µA	1.4 - 1.6		0.2	
		I$_{OL}$ = 2 mA	1.4		0.35	
I$_I$	Input Leakage Current	0 ≤ V$_I$ ≤ 3.6V	1.4 - 3.6		±5.0	µA
I$_{OZ}$	3-STATE Output Leakage	0 ≤ V$_O$ ≤ 3.6V V$_I$ = V$_{IH}$ or V$_{IL}$	1.4 - 3.6		±10	µA
I$_{OFF}$	Power-OFF Leakage Current	0 ≤ (V$_I$, V$_O$) ≤ 3.6V	0		10	µA
I$_{CC}$	Quiescent Supply Current	V$_I$ = V$_{CC}$ or GND	1.4 - 3.6		20	µA
		V$_{CC}$ ≤ (V$_I$, V$_O$) ≤ 3.6V (Note 5)	1.4 - 3.6		±20	
ΔI$_{CC}$	Increase in I$_{CC}$ per Input	V$_{IH}$ = V$_{CC}$ −0.6V	2.7 - 3.6		750	µA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Figure Number
f_{MAX}	Maximum Clock Frequency	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	250		MHz	
			2.5 ± 0.2	200			
			1.8 ± 0.15	100			
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	80.0			
t_{PHL} t_{PLH}	Propagation Delay	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	8.8		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	1.0	17.6		Figures 7, 8
t_{PZL} t_{PZH}	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.7	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.7		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t_{PLZ} t_{PHZ}	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.7	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.2		
			1.8 ± 0.15	1.5	7.6		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	1.0	15.2		Figures 7, 9, 10
t_S	Setup Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.5		ns	Figure 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	3.0			
t_H	Hold Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.0		ns	Figure 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	2.0			
t_W	Pulse Width	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	1.5		ns	Figure 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	4.0			
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 7)	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1		1.5		

Note 6: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	
			2.5	0.6	V
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	−0.25	
			2.5	−0.6	V
			3.3	−0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	
			2.5	1.9	V
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8V$, $2.5V$ or $3.3V$, $V_I = 0V$ or V_{CC}	6	pF
C_{OUT}	Output Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, $2.5V$ or $3.3V$	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, $f = 10$ MHz, $V_{CC} = 1.8V$, $2.5V$ or $3.3V$	20	pF

AC Loading and Waveforms (V_{CC} 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)
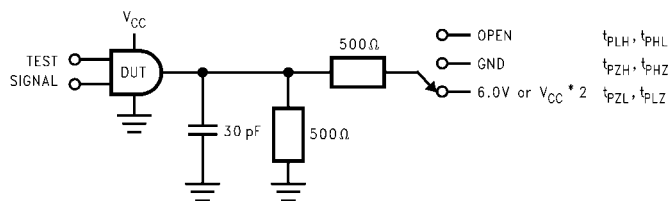
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3V $\pm$ 0.3V; V_{CC} x 2 at V_{CC} = 2.5V $\pm$ 0.2V; 1.8V $\pm$ 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit
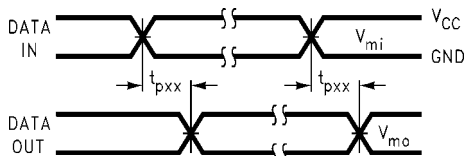
FIGURE 2. Waveform for Inverting and Non-Inverting Functions
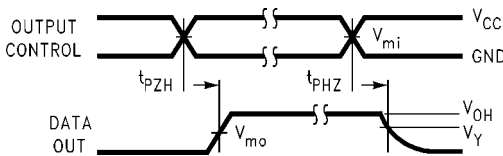
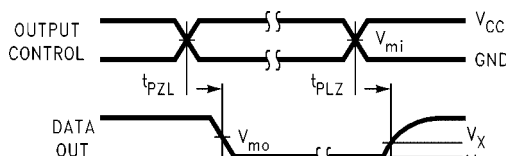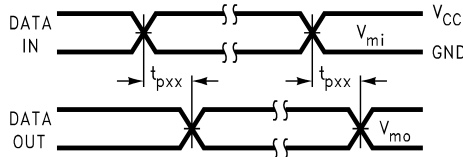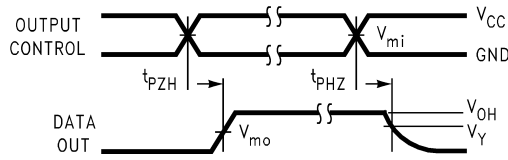**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
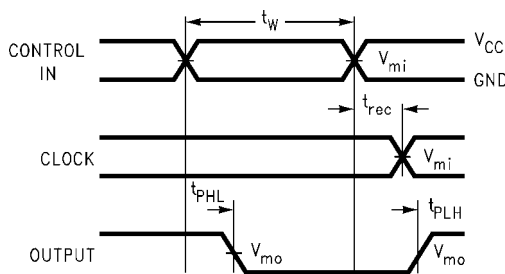
FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms
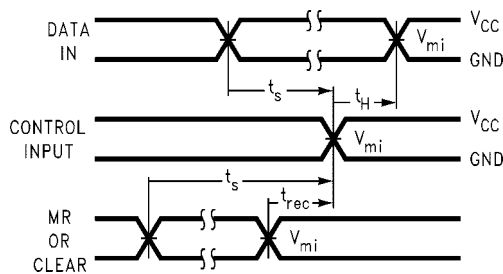
FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

AC Loading and Waveforms (V$_{CC}$ 1.5V $\pm$ 0.1V)
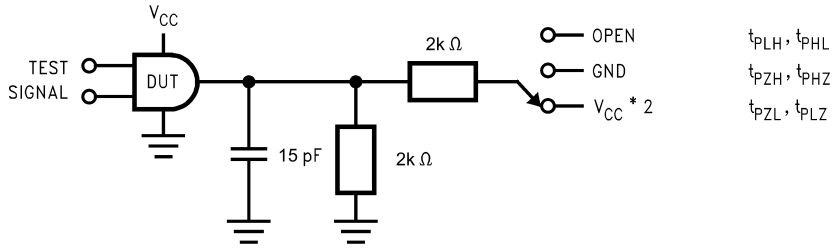
TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	V$_{CC}$ x 2 at V$_{CC}$ = 1.5V $\pm$ 0.1V
t$_{PZH}$, t$_{PHZ}$	GND

FIGURE 7. AC Test Circuit

FIGURE 8. Waveform for Inverting and Non-Inverting Functions

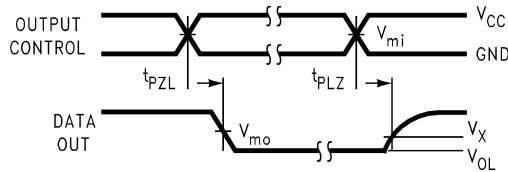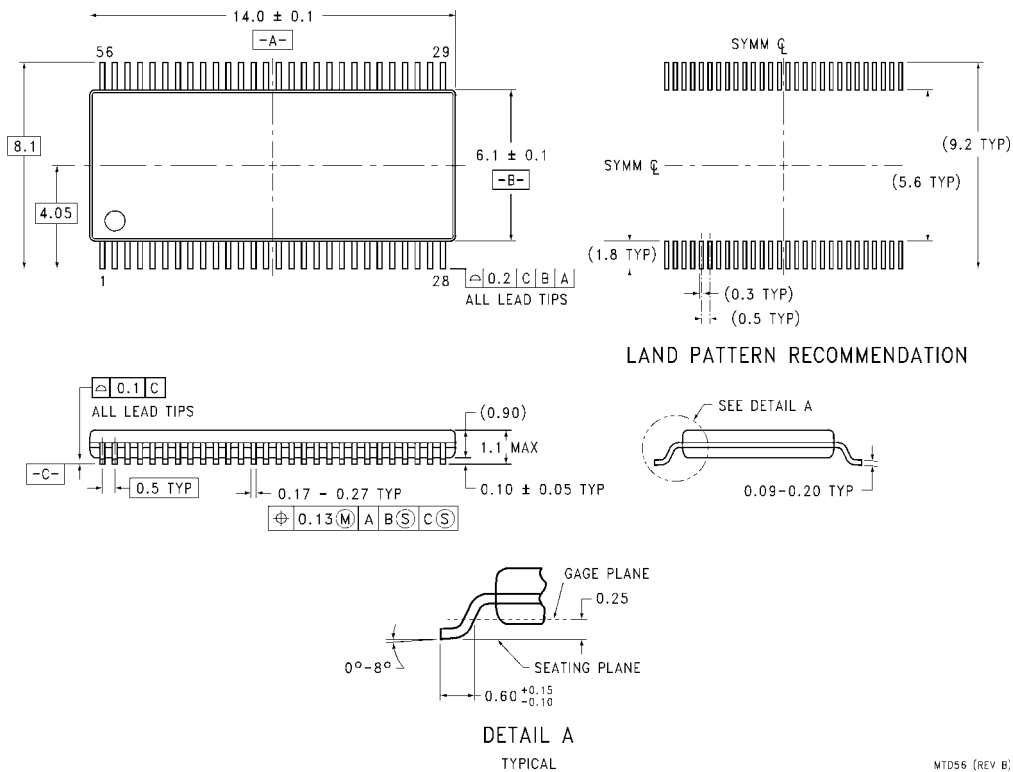**FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V$_{CC}$
	1.5V $\pm$ 0.1V
V$_{mi}$	V$_{CC}$/2
V$_{mo}$	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.1V
V$_Y$	V$_{OH}$ − 0.1V

Physical Dimensions inches (millimeters) unless otherwise noted

**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

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