National Semiconductor

PRELIMINARY
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74VHC299
8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The VHC299 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

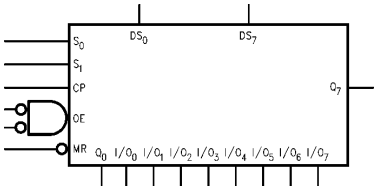
Features

- Low power dissipation: $I_{CC} = 4\ \mu A$ at $T_A = 25°C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%\ V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Low noise: $V_{OLP} = 0.9V$ (typ)
- Pin and function compatible with 74HC299

Commercial	Package Number	Package Description
74VHC299M	M20B	20-Lead Molded JEDEC SOIC
74VHC299SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC299MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC299N	N20A	20-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter 'X' to the ordering code.

Logic Symbols



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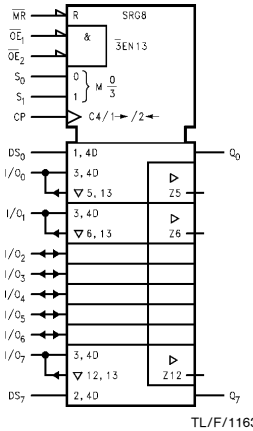
IEEE/IEC



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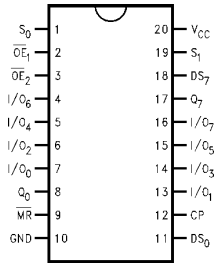
Connection Diagram

Pin Assignment for DIP, TSSOP and SOIC



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TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The VHC299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

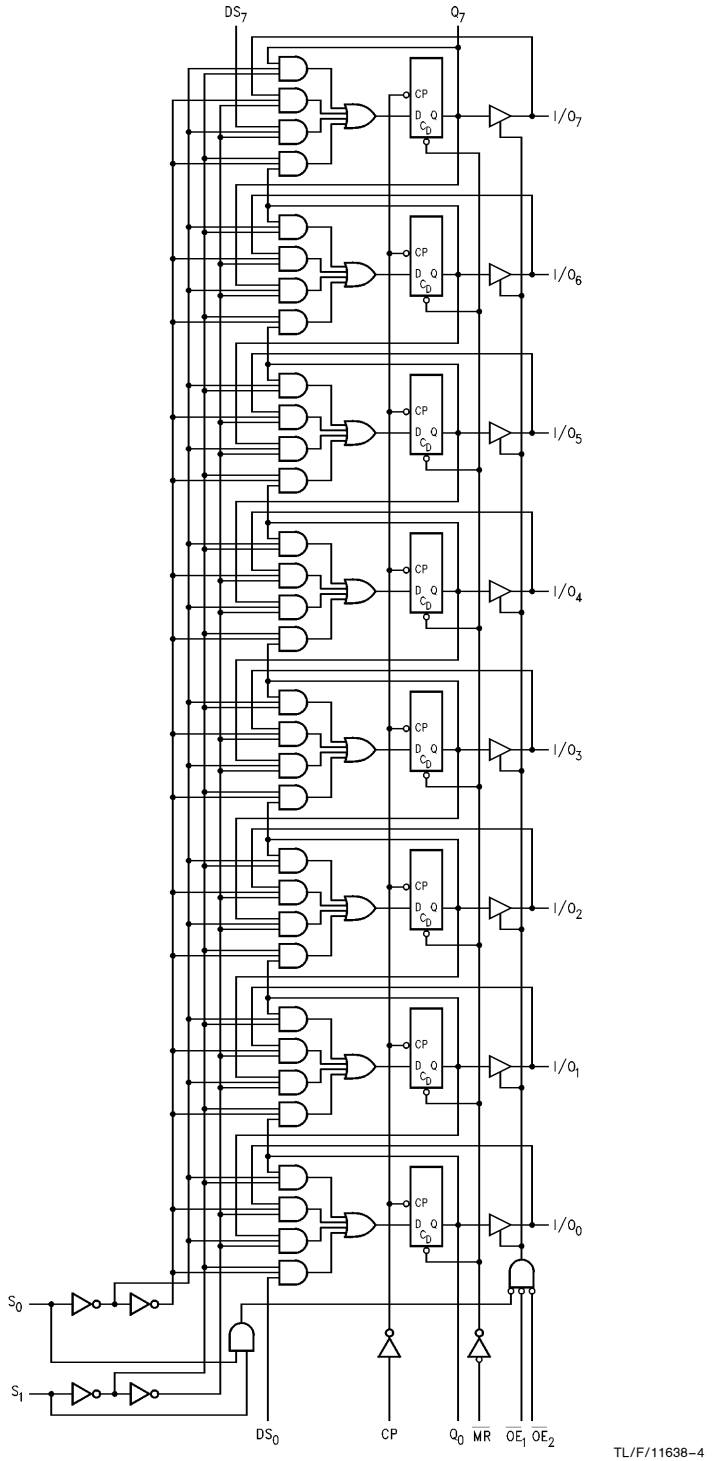
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐⌐	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = +25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices:

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = +25°C$		Units	Conditions
			Typ	Limits		
V_{OLP}**	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	$C_L = 50$ pF
V_{OLV}**	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.9	−1.2	V	$C_L = 50$ pF
V_{IHD}**	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD}**	Maximum High Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices:

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = +25°C$			74VHC $T_A = -40°C$ to $+85°$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Time CP to Q_0 or Q_7 (Shift Left or Right)	3.3 ±0.3		12.2	17.2	1.0	19.8	ns		$C_L = 15$ pF
				14.7	20.7	1.0	23.3			$C_L = 50$ pF
		5.0 ±0.5		8.5	10.8	1.0	12.0	ns		$C_L = 15$ pF
				10.0	12.8	1.0	14.0			$C_L = 50$ pF
t_{PLH} t_{PHL}	Propagation Delay Time (CP − I/O_n)	3.3 ±0.3		10.3	14.3	1.0	16.6	ns		$C_L = 15$ pF
				12.8	17.8	1.0	20.1			$C_L = 50$ pF
		5.0 ±0.5		7.3	9.1	1.0	10.4	ns		$C_L = 15$ pF
				8.8	11.1	1.0	12.4			$C_L = 50$ pF
t_{PHL}	Propagation Delay Time ($\overline{MR}$ to Q_0 or Q_7)	3.3 ±0.3		13.0	19.0	1.0	22.0	ns		$C_L = 15$ pF
				15.5	22.5	1.0	25.5			$C_L = 50$ pF
		5.0 ±0.5		9.1	11.2	1.0	13.5	ns		$C_L = 15$ pF
				10.8	13.2	1.0	15.5			$C_L = 50$ pF
t_{PHL}	Propagation Delay Time ($\overline{MR}$ − I/O_n)	3.3 ±0.3		10.8	17.0	1.0	19.5	ns		$C_L = 15$ pF
				13.3	20.5	1.0	23.0			$C_L = 50$ pF
		5.0 ±0.5		7.7	10.5	1.0	12.0	ns		$C_L = 15$ pF
				9.2	12.5	1.0	14.0			$C_L = 50$ pF
t_{PZL} t_{PZH}	Output Enable Time ($\overline{OE}$ − I/O_n)	3.3 ±0.3		13.3	16.5	1.0	19.2	ns	$R_L = 1$ kΩ	$C_L = 15$ pF
				14.8	19.0	1.0	21.7			$C_L = 50$ pF
		5.0 ±0.5		8.9	9.7	1.0	11.3	ns		$C_L = 15$ pF
				10.4	11.2	1.0	12.6			$C_L = 50$ pF
t_{PZL} t_{PZH}	Output Enable Time (S_0 or S_1 to I/O_n)	3.3 ±0.3		13.3	16.5	1.0	19.2	ns	$R_L = 1$ kΩ	$C_L = 15$ pF
				14.8	19.0	1.0	21.7			$C_L = 50$ pF
		5.0 ±0.5		8.9	9.7	1.0	11.3	ns		$C_L = 15$ pF
				10.4	11.2	1.0	12.6			$C_L = 50$ pF
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{OE}$ − I/O_n)	3.3 ±0.3		18.0	21.3	1.0	24.3	ns	$R_L = 1$ kΩ	$C_L = 50$ pF
		5.0 ±0.5		11.8	13.2	1.0	15.0			$C_L = 50$ pF
t_{PLZ} t_{PHZ}	Output Disable Time (S_0 or S_1 to I/O_n)	3.3 ±0.3		18.0	21.3	1.0	24.3	ns	$R_L = 1$ kΩ	$C_L = 50$ pf
		5.0 ±0.5		11.8	13.2	1.0	15.0			$C_L = 50$ pF
f_{MAX}	Maximum Clock Frequency	3.3 ±0.3	65	100		55		MHz		$C_L = 15$ pF
			55	90		50				$C_L = 50$ pF
		5.0 ±0.5	125	160		110		MHz		$C_L = 15$ pF
			115	150		100				$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			4				pF	$V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance			110				pF	(Note 1)	

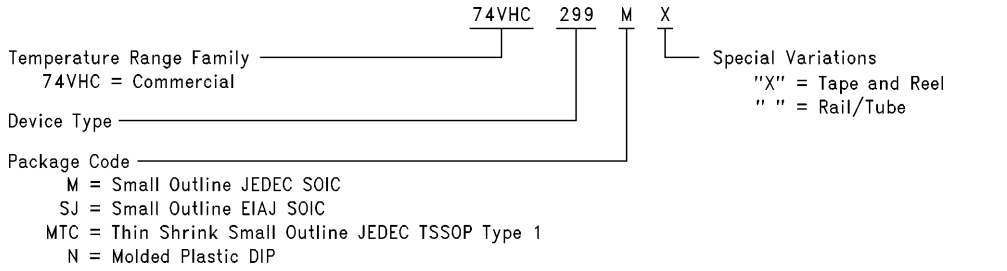
Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

AC Operating Requirements for 'VHC Family Devices:

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = +25°C$		74VHC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
t_S	Minimum Setup Time S_0 or S_1 to CP	3.3 ±0.3 5.0 ±0.5		14.5 7.0	17.0 8.0	ns	
t_S	Minimum Setup Time I/O_n to CP	3.3 ±0.3 5.0 ±0.5		8.0 4.0	9.0 4.0	ns	
t_S	Minimum Setup Time DS_0 or DS_7 to CP	3.3 ±0.3 5.0 ±0.5		8.5 5.0	10.0 5.0	ns	
t_H	Minimum Hold Time S_0 or S_1 to CP	3.3 ±0.3 5.0 ±0.5		0.0 0.5	0.0 0.5	ns	
t_H	Minimum Hold Time I/O_n to CP	3.3 ±0.3 5.0 ±0.5		0.5 1.5	0.5 1.5	ns	
t_H	Minimum Hold Time DS_0 or DS_7 to CP	3.3 ±0.3 5.0 ±0.5		1.0 1.0	1.0 1.0	ns	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CP)	3.3 ±0.3 5.0 ±0.5		7.0 7.0	8.0 8.0	ns	
$t_{W(L)}$	Minimum Pulse Width ($\overline{MR}$)	3.3 ±0.3 5.0 ±0.5		6.0 6.0	7.0 7.0	ns	
t_{rem}	Minimum Removal Time ($\overline{MR}$ to CP)	3.3 ±0.3 5.0 ±0.5		5.0 4.0	6.0 4.0	ns	

Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



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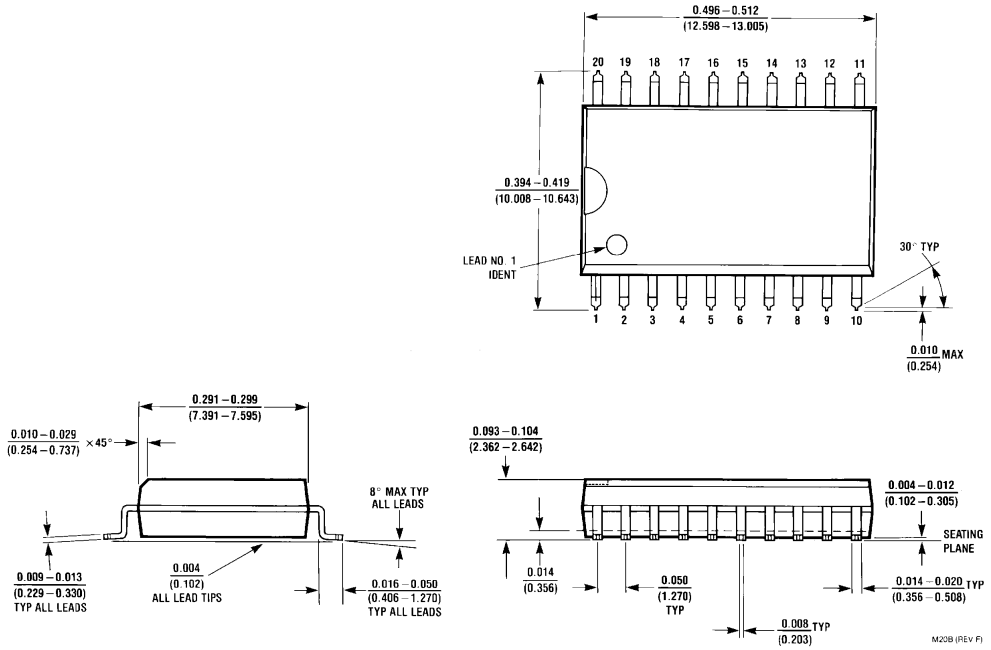
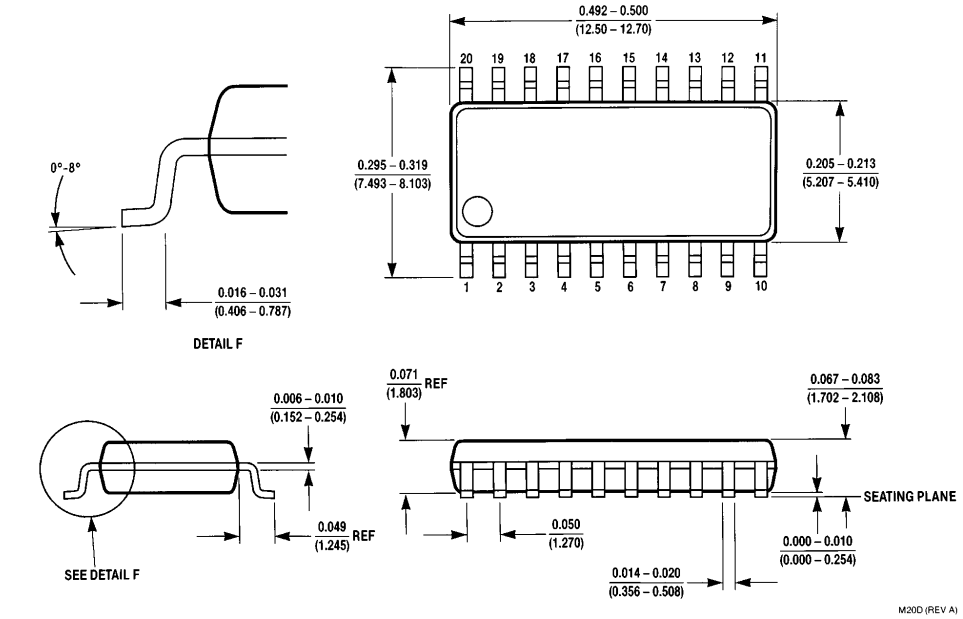
Physical Dimensions inches (millimeters)

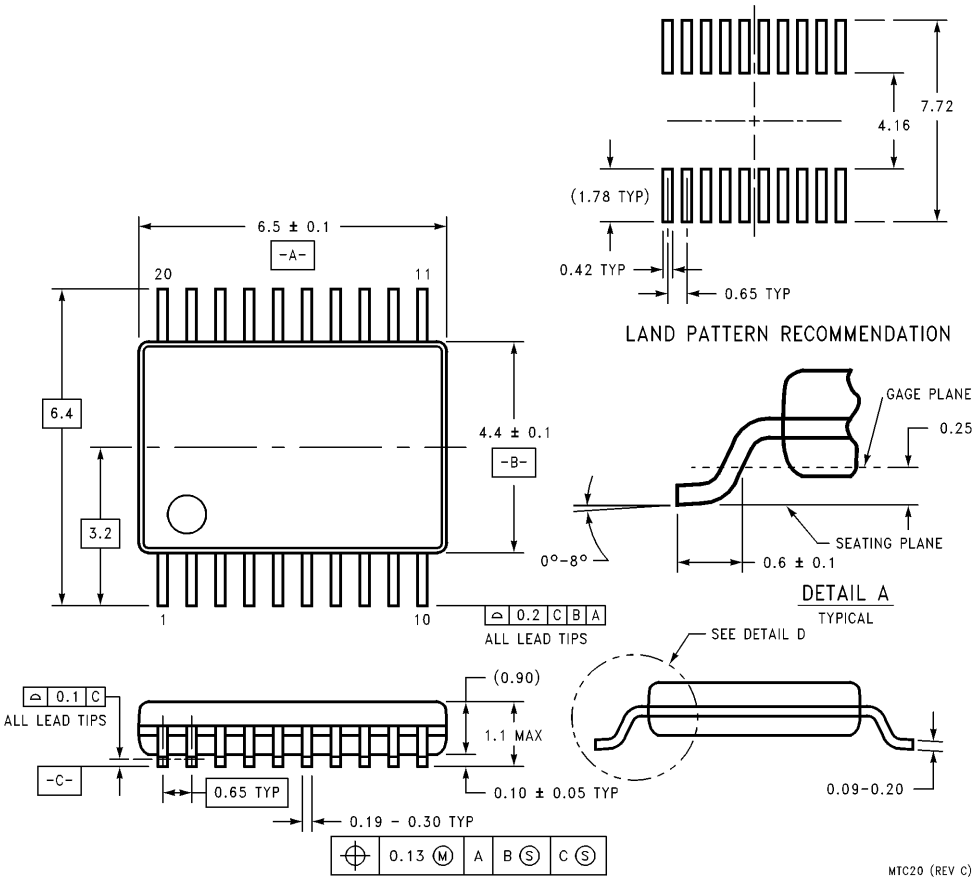


20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
Order Number 74VHC299M or 74VHC299MX
NS Package Number M20B



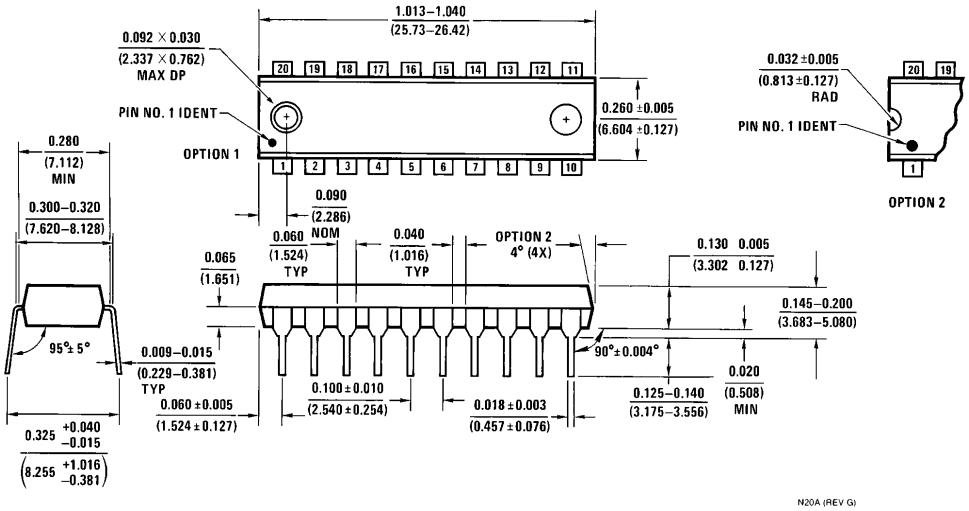
20-Lead Plastic EIAJ SOIC (SJ)
Order Number 74VHC299SJ or 74VHC299SJX
NS Package Number M20D

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Thin Shrink Small Outline JEDEC Type I TSSOP
Order Number 74VHC299MTC
NS Package Number MTC20

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Dual-In-Line Package
Order Number 74VHC299N
NS Package Number N20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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