**FAIRCHILD**
SEMICONDUCTOR®

February 2008

# 74VHCT08A
# Quad 2-Input AND Gate

## Features

- High speed: $t_{PD} = 5.0$ns (typ.) at $T_A = 25°C$
- High noise immunity: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power down protection is provided on all inputs and outputs
- Low noise: $V_{OLP} = 0.8V$ (max.)
- Low power dissipation: $I_{CC} = 2\mu A$ (max.) @ $T_A = 25°C$
- Pin and function compatible with 74HCT08

## General Description

The VHCT08A is an advanced high speed CMOS 2 Input AND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC} = 0V$. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.
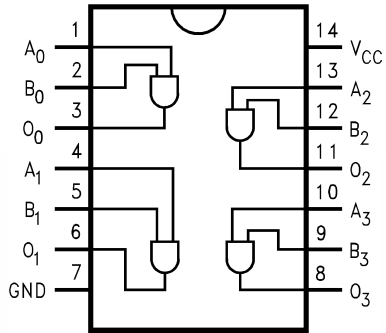
## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| 74VHCT08AM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHCT08ASJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT08AMTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74HCT08AN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
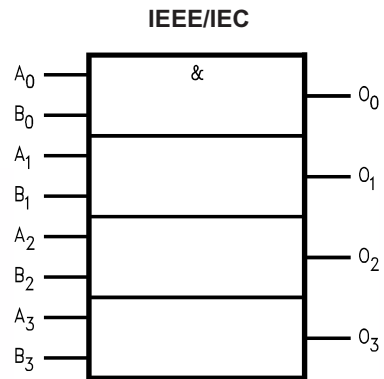
♻ All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram



| | | |
|---|---|---|
| $A_0$ | 1 | 14 | $V_{CC}$ |
| $B_0$ | 2 | 13 | $A_2$ |
| $O_0$ | 3 | 12 | $B_2$ |
| $A_1$ | 4 | 11 | $O_2$ |
| $B_1$ | 5 | 10 | $A_3$ |
| $O_1$ | 6 | 9 | $B_3$ |
| GND | 7 | 8 | $O_3$ |

## Logic Symbol

**IEEE/IEC**



$A_0$
$B_0$
$A_1$
$B_1$
$A_2$
$B_2$
$A_3$
$B_3$

&

$O_0$
$O_1$
$O_2$
$O_3$

## Pin Description

| Pin Names | Description |
|---|---|
| $A_n$, $B_n$ | Inputs |
| $O_n$ | Outputs |

## Truth Table

| A | B | O |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|--------|-----------|--------|
| $V_{CC}$ | Supply Voltage | –0.5V to +7.0V |
| $V_{IN}$ | DC Input Voltage | –0.5V to +7.0V |
| $V_{OUT}$ | DC Output Voltage<br>    HIGH or LOW state, $I_{OUT}$ absolute maximum rating must be observed | –0.5V to $V_{CC}$ + 0.5V |
|  | $V_{CC}$ = 0V | –0.5V to +7.0V |
| $I_{IK}$ | Input Diode Current | –20mA |
| $I_{OK}$ | Output Diode Current, $V_{OUT}$ < GND, $V_{OUT}$ > $V_{CC}$ (Outputs Active) | ±20mA |
| $I_{OUT}$ | DC Output Current | ±25mA |
| $I_{CC}$ | DC $V_{CC}$/GND Current | ±50mA |
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions[1]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|--------|-----------|--------|
| $V_{CC}$ | Supply Voltage | 4.5V to 5.5V |
| $V_{IN}$ | Input Voltage | 0V to +5.5V |
| $V_{OUT}$ | Output Voltage<br>    HIGH or LOW state, $I_{OUT}$ absolute maximum rating must be observed | 0V to $V_{CC}$ |
|  | $V_{CC}$ = 0V | 0V to +5.5V |
| $T_{OPR}$ | Operating Temperature | –40°C to +85°C |
| $t_r$, $t_f$ | Input Rise and Fall Time, $V_{CC}$ = 5.0V ± 0.5V | 0ns/V ~ 20ns/V |

**Note:**

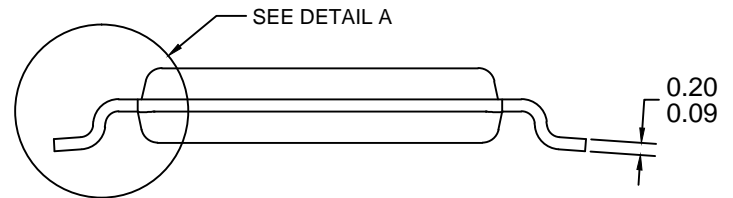1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | | $T_A = 25°C$ Min. | $T_A = 25°C$ Typ. | $T_A = 25°C$ Max. | $T_A = -40°C$ to +85°C Min. | $T_A = -40°C$ to +85°C Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH Level | 4.5 | | | 2.0 | | | 2.0 | | V |
| | Input Voltage | 5.5 | | | 2.0 | | | 2.0 | | |
| $V_{IL}$ | LOW Level | 4.5 | | | | | 0.8 | | 0.8 | V |
| | Input Voltage | 5.5 | | | | | 0.8 | | 0.8 | |
| $V_{OH}$ | HIGH Level | 4.5 | $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -50µA$ | 4.40 | 4.50 | | 4.40 | | V |
| | Output Voltage | | | $I_{OH} = -8mA$ | 3.94 | | | 3.80 | | |
| $V_{OL}$ | LOW Level Output Voltage | 4.5 | $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 50µA$ | | 0.0 | 0.1 | | 0.1 | V |
| | | | | $I_{OL} = 8mA$ | | | 0.36 | | 0.44 | |
| $I_{IN}$ | Input Leakage Current | 0–5.5 | $V_{IN} = 5.5V$ or GND | | | | ±0.1 | | ±1.0 | µA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | $V_{IN} = V_{CC}$ or GND | | | | 2.0 | | 20.0 | µA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | $V_{IN} = 3.4V$, Other Inputs = $V_{CC}$ or GND | | | | 1.35 | | 1.50 | mA |
| $I_{OFF}$ | Output Leakage Current (Power Down State) | 0.0 | $V_{OUT} = 5.5V$ | | | | 0.5 | | 5.0 | µA |

## Noise Characteristics

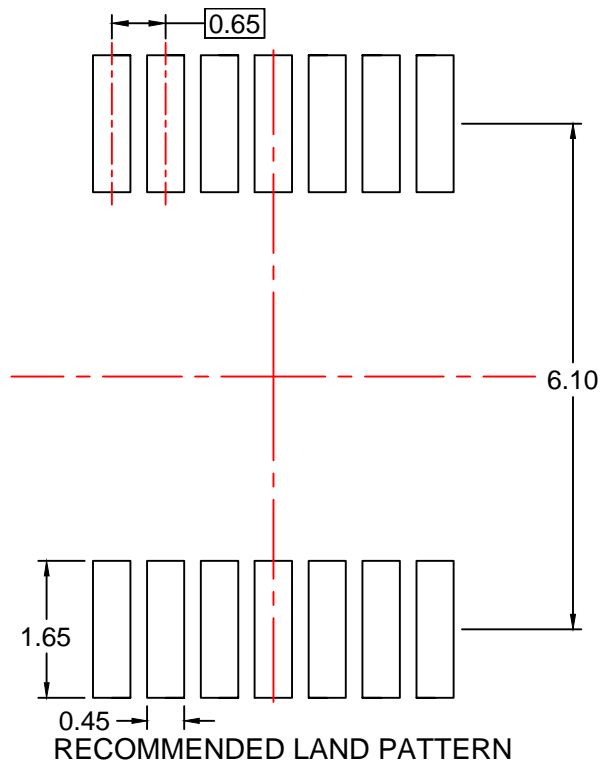| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A = 25°C$ Typ. | $T_A = 25°C$ Limits | Units |
|---|---|---|---|---|---|---|
| $V_{OLP}$[2] | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | $C_L = 50pF$ | 0.4 | 0.8 | V |
| $V_{OLV}$[2] | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | $C_L = 50pF$ | −0.4 | −0.8 | V |
| $V_{IHD}$[2] | Minimum HIGH Level Dynamic Input Voltage | 5.0 | $C_L = 50pF$ | | 2.0 | V |
| $V_{ILD}$[2] | Maximum LOW Level Dynamic Input Voltage | 5.0 | $C_L = 50pF$ | | 0.8 | V |

**Note:**
2. Parameter guaranteed by design.

## AC Electrical Characteristics

| Symbol | Parameter | V$_{CC}$ (V) | Conditions | T$_A$ = 25°C | | | T$_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| t$_{PLH}$, t$_{PHL}$ | Propagation Delay | 5.0 ± 0.5 | C$_L$ = 15pF | | 5.0 | 6.9 | 1.0 | 8.0 | ns |
| | | | C$_L$ = 50pF | | 5.5 | 7.9 | 1.0 | 9.0 | |
| C$_{IN}$ | Input Capacitance | | V$_{CC}$ = Open | | 4 | 10 | | 10 | pF |
| C$_{PD}$ | Power Dissipation Capacitance | | (3) | | 18 | | | | pF |

**Note:**

3. C$_{PD}$ is defined as the value of the internal equivalent capacitance, which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:

$$I_{CC} \text{ (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per gate)}$$

5.00±0.10   □A

0.43TYP

14   8

□B

□6.4   4.40±0.10

□3.2

PIN#1 IDENT   1   TOP VIEW   7   ⌒ | 0.2 | C | B | A
ALL LEAD TIPS

0.65

6.10

1.65

0.45

RECOMMENDED LAND PATTERN

1.2 MAX

0.90 +0.15 -0.10

0.10±0.05

ALL LEAD TIPS
⌒ | 0.1 | C

0.30
0.19

□C

0.65   ⊕ | 0.13Ⓜ | A | BⓈ | CⓈ

FRONT VIEW

SEE DETAIL A

0.20
0.09

12.00° TOP & BOTTOM

0.09 MIN

GAGE PLANE

0°- 8°

0.09 MIN

0.25

0.6±0.1

SEATING PLANE

1.00

DETAIL A
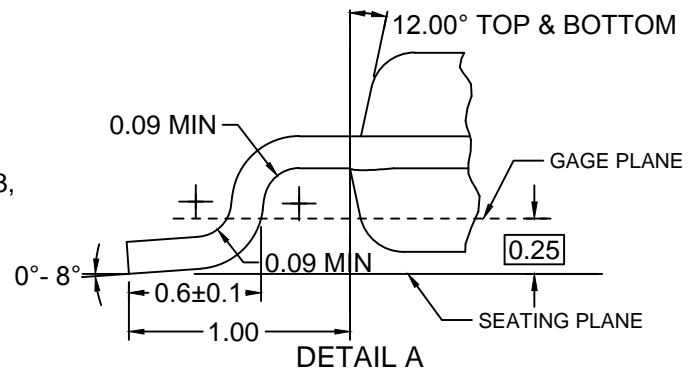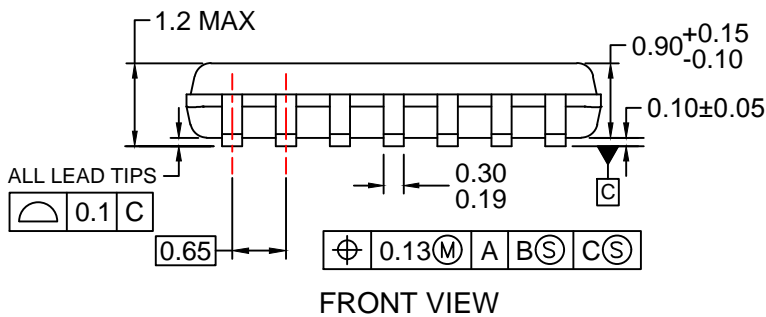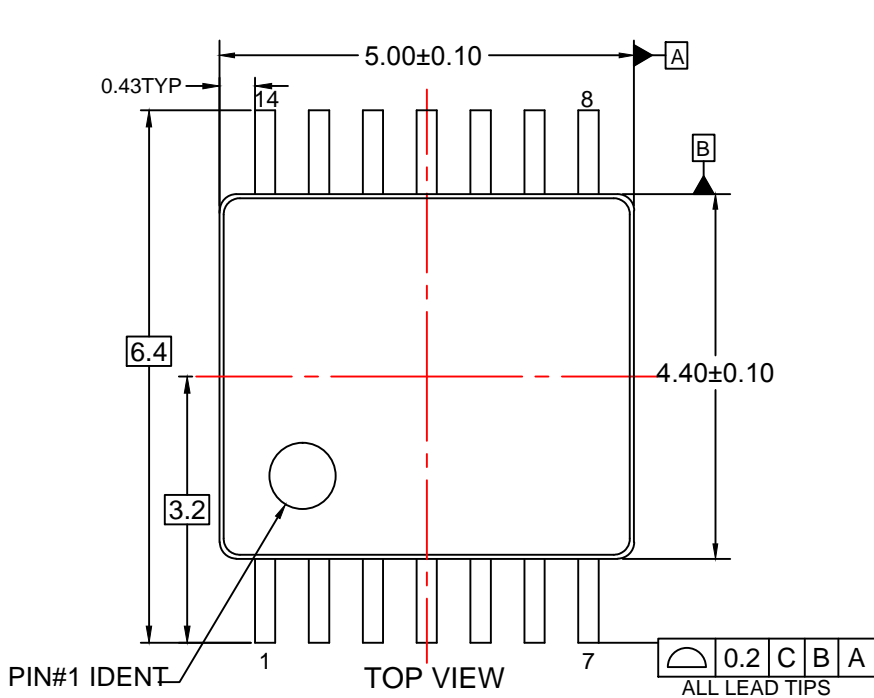
NOTES:
 A. CONFORMS TO JEDEC REGISTRATION MO-153,
    VARIATION AB, REF NOTE 6
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
    MOLD FLASH, AND TIE BAR EXTRUSIONS
 D. DIMENSIONING AND TOLERANCES PER ANSI
    Y14.5M, 2009.
 E. LANDPATTERN STANDARD: SOP65P640X110-14M.
 F. DRAWING FILE NAME: MKT-MTC14rev7.

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## TOP VIEW

8.75
8.50 → A

7.62

14     8    B

6.00

4.00
3.80

PIN #1
IDENT.

1     7

1.27

0.51
0.35

(0.33)

TOP VIEW

⊕ | 0.25 Ⓜ | C | B | A

## LAND PATTERN RECOMMENDATION

14    0.65 →|←    8

5.60

1.70

1     7

1.27

LAND PATTERN RECOMMENDATION

## FRONT VIEW

1.75 MAX

C

1.50
1.25

0.25
0.10

⌓ | 0.10 | C

FRONT VIEW

## SIDE VIEW

A

0.25
0.19

SIDE VIEW
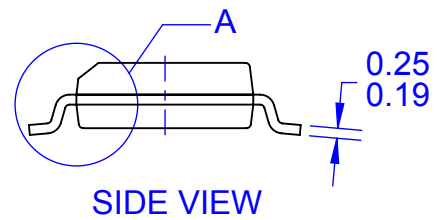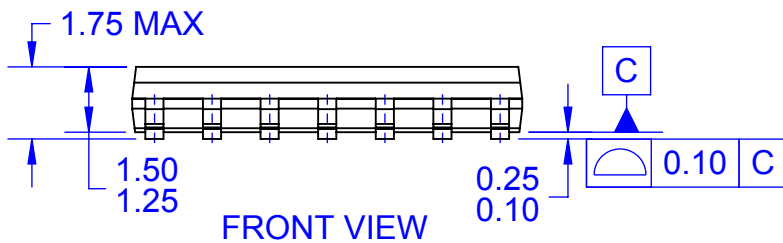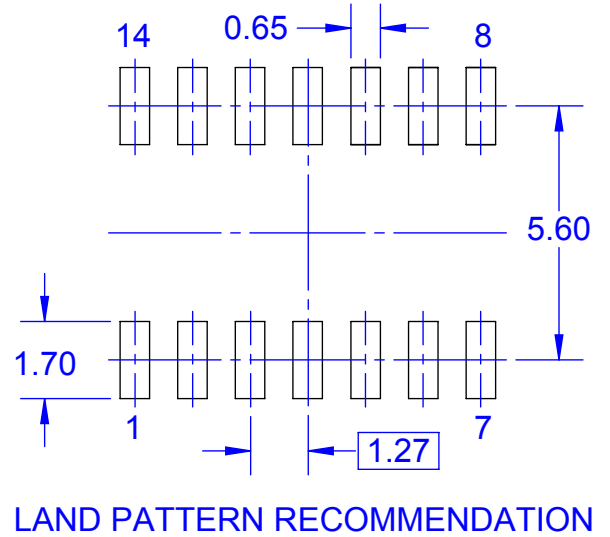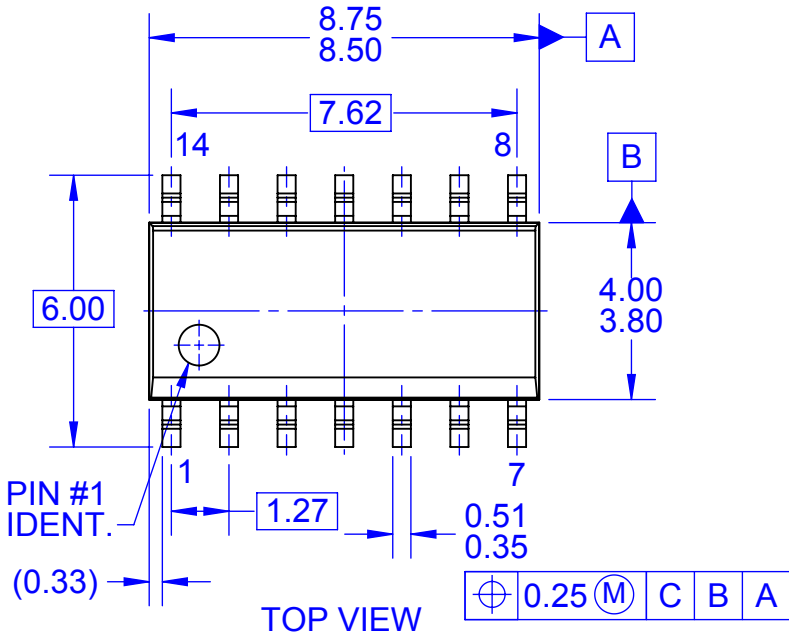
## NOTES:

A. CONFORMS TO JEDEC MS-012,
   VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS
D. LAND PATTERN STANDARD:
   SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

**FAIRCHILD** ™

## DETAIL A

0.50
0.25 X 45°

R0.10

GAGE
PLANE

R0.10

0.36

8°
0°

0.90
0.50

(1.04)

SEATING PLANE

DETAIL A
SCALE 16 : 1

## PUBLICATION ORDERING INFORMATION
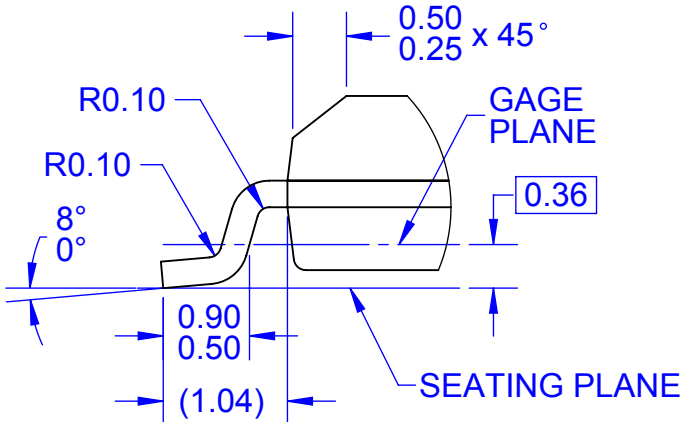
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