



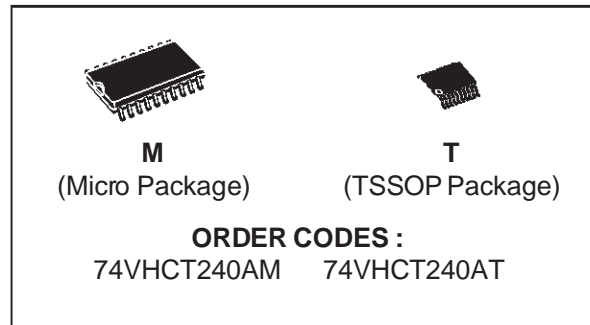
74VHCT240A

OCTAL BUS BUFFER WITH 3 STATE OUTPUTS (INVERTED)

- HIGH SPEED: $t_{PD} = 5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2V$ (MIN), $V_{IL} = 0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 240
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (Max.)

DESCRIPTION

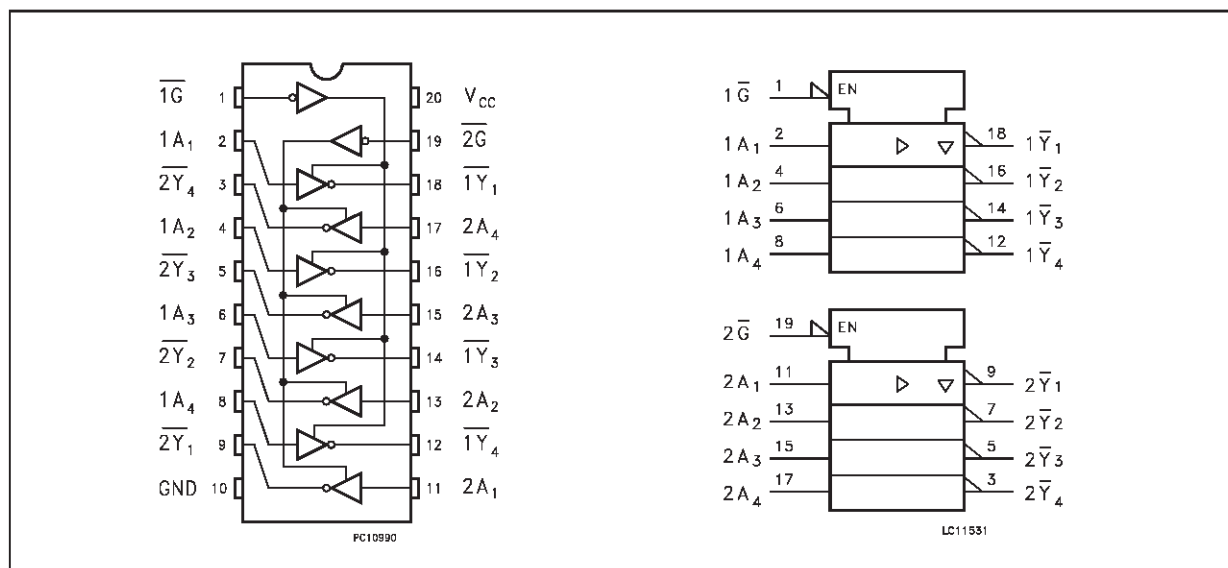
The 74VHCT240A is an advanced high-speed CMOS OCTAL BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2 MOS technology.



\overline{G} output enable governs four BUS BUFFERS. This device is designed to be used with 3 state memory address drivers, etc. Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

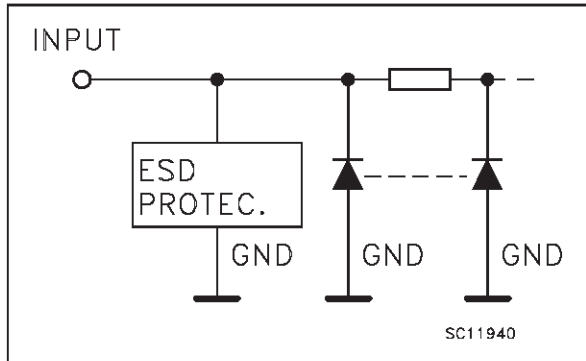
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74VHCT240A

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	$\overline{2Y1}$ to $\overline{2Y4}$	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	$\overline{1Y1}$ to $\overline{1Y4}$	Data Outputs
19	$\overline{2G}$	Output Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		OUTPUT
\overline{G}	A _n	$\overline{Y_n}$
L	L	H
L	H	L
H	X	Z

X: "H" or "L"

Z: High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V _O	DC Output Voltage (see note 2)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	-20	mA
I _{OK}	DC Output Diode Current	±20	mA
I _O	DC Output Current	±25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) Output in OFF State

2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	4.5 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage (see note 1)	0 to 5.5	V
V _O	Output Voltage (see note 2)	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 3) (V _{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) Output in OFF State

2) High or Low State

3) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =50 μA	4.4	4.5		4.4		V
		4.5	I _O =8 mA	3.94			3.8		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44	
I _{OZ}	High Impedance Output Leakage Current	4.5 to 5.5	V _I = V _{IH} or V _{IL} V _O = 0V to 5.5V			±0.25		±2.5	μA
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	5.0 ^(*)	15			5.6	7.8	1.0	9.0	ns
		5.0 ^(*)	50			6.1	8.8	1.0	10.0	
t _{PLZ} t _{PHZ}	Output Disable Time	5.0 ^(*)	15	R _L = 1KΩ		7.7	10.4	1.0	12.0	ns
		5.0 ^(*)	50			8.2	11.4	1.0	13.0	
t _{PZL} t _{PZH}	Output Enable Time	5.0 ^(*)	50	R _L = 1KΩ		8.8	11.4	1.0	13.0	ns

(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			4	10		10	pF
C _{OUT}	Output Capacitance			9				pF
C _{PD}	Power Dissipation Capacitance (note 1)			19				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(OPR)} = C_{PD} • V_{CC} • f_{IN} + I_{CC0}/8 (per Circuit)

DYNAMIC SWITCHING CHARACTERISTICS

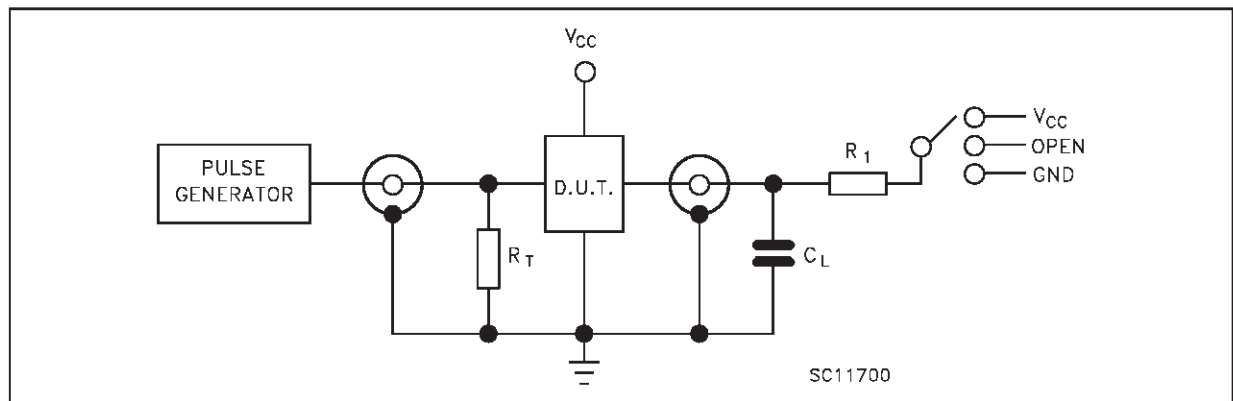
Symbol	Parameter	Test Conditions	Value					Unit	
			V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50pF		0.9	1.1		V	
V _{OLV}				-1.1	-0.9				
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		2.0					
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0			0.8				

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n - 1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching, (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT

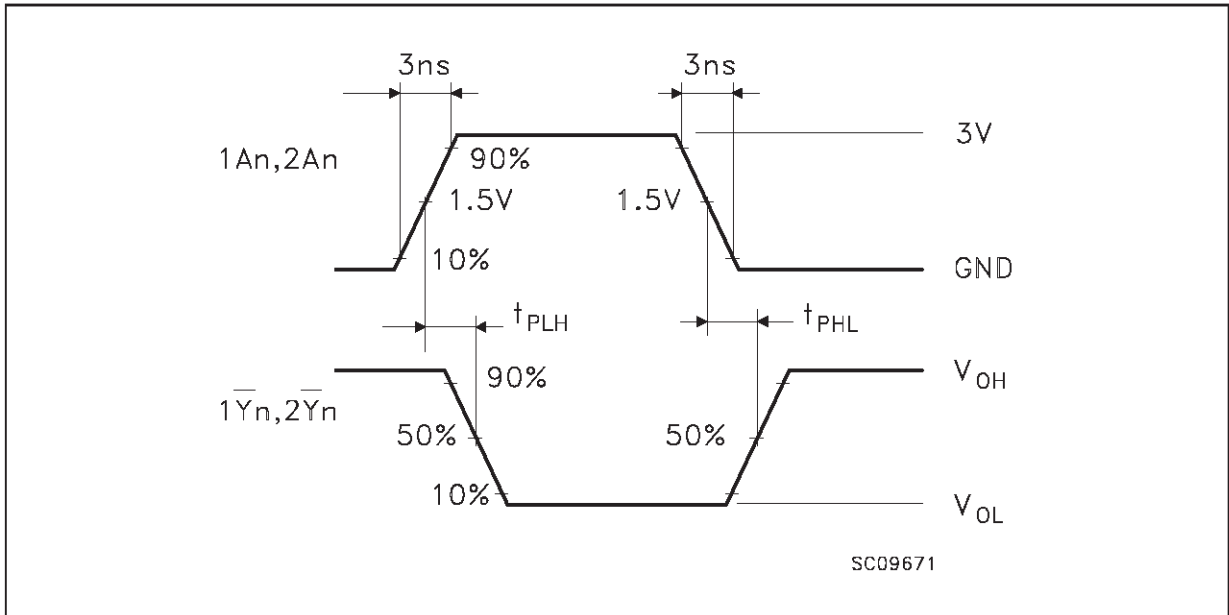
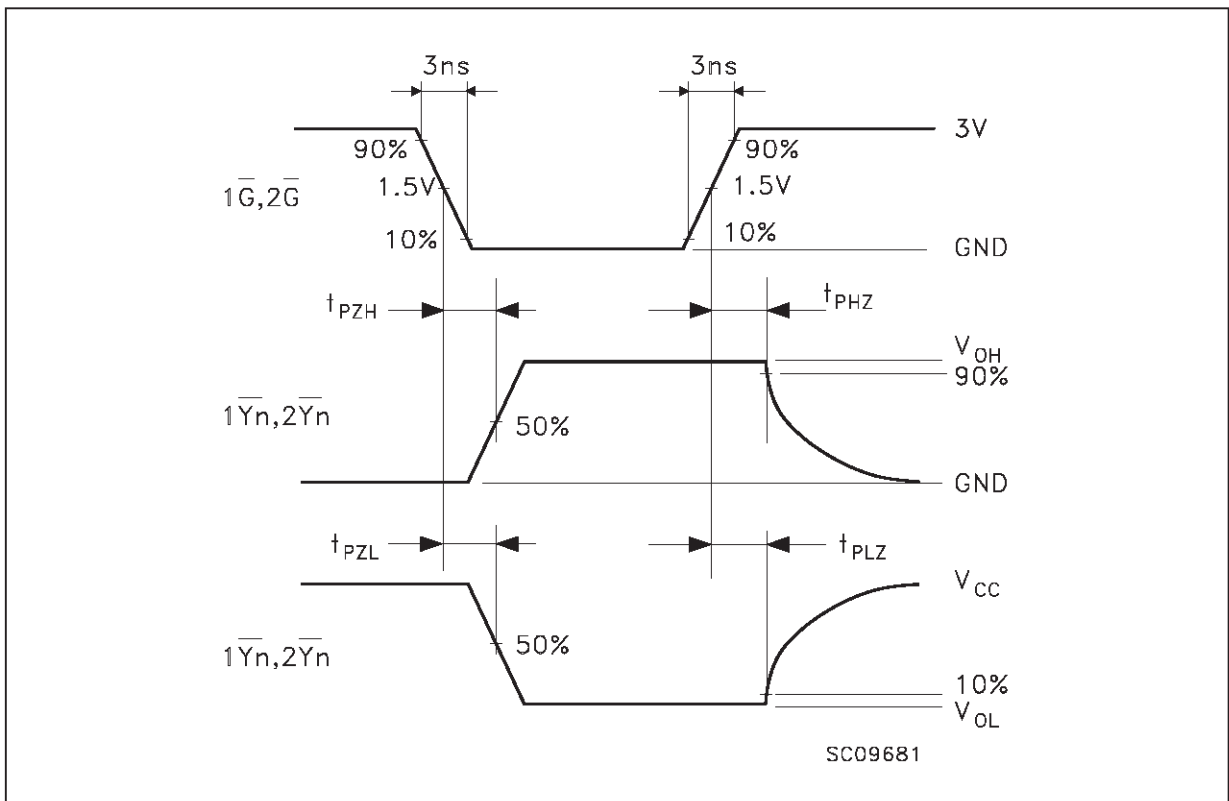


TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 15/50 pF or equivalent (includes jig and probe capacitance)

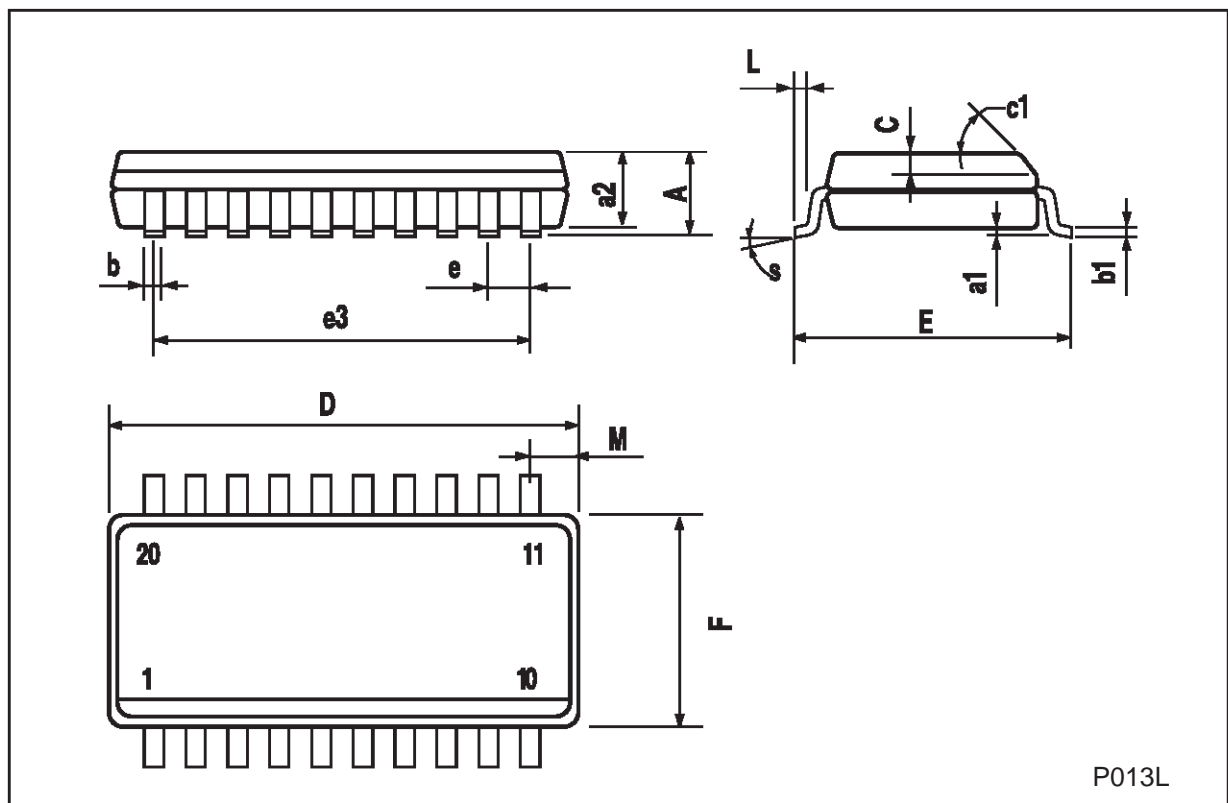
R_L = R₁ = 1KΩ or equivalent

R_T = Z_{out} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** (f=1MHz; 50% duty cycle)

SO-20 MECHANICAL DATA

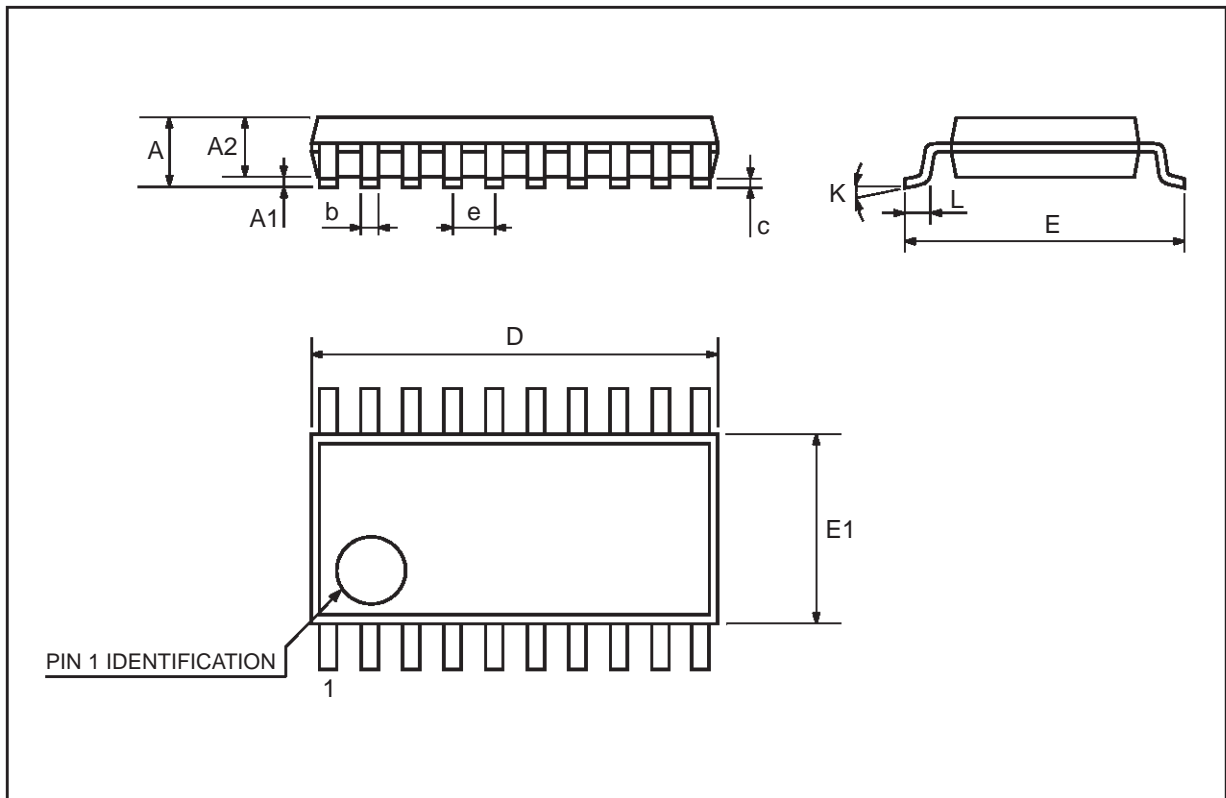
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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