

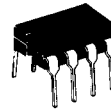

MOTOROLA
**MC75451
MC75452
MC75453
MC75454**
DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

Each of these devices consists of a pair of M TTL gates with the output of each gate internally connected to the base of a transistor.

MC75451 provides the AND function
MC75452 provides the NAND function
MC75453 provides the OR function
MC75454 provides the NOR function

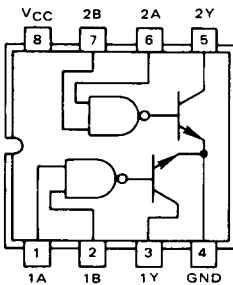
- 300 mA Output Current Capability
- Output Breakdown Voltage – 30 V Min
- M TTL compatible Inputs

**DUAL
PERIPHERAL DRIVERS**
**SILICON MONOLITHIC
INTEGRATED CIRCUITS**


U SUFFIX
CERAMIC PACKAGE
CASE 693



P SUFFIX
PLASTIC PACKAGE
CASE 626

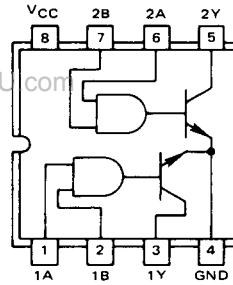
MC75451 – Positive AND


Positive Logic: $Y = AB$

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("off" state)

H = high level, L = low level.

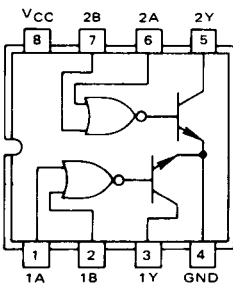
MC75452 – Positive NAND


Positive Logic: $Y = \overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level.

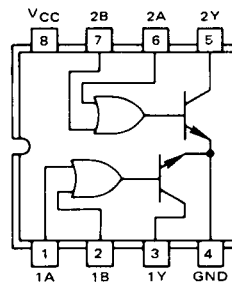
MC75453 – Positive OR


Positive Logic: $Y = A + B$

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level.

MC75454 – Positive NOR


Positive Logic: $Y = \overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

MC75451, MC75452, MC75453, MC75454

MAXIMUM RATINGS ($T_A = 0^\circ\text{C}$ to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Interemitter Voltage(2)	—	5.5	Vdc
Output Voltage(3)	V_O	30	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $T_A = +25^\circ\text{C}$	P_D	830 6.6	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

- (1) Voltage values are with respect to network ground terminal.
- (2) This is the voltage between two emitters of a multiple-emitter transistor.
- (3) This is the maximum voltage which should be applied to any output when it is in the "off" state.
- (4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

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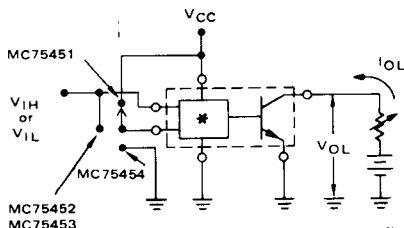
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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $4.75 \geq V_{CC} \geq 5.25$ V and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$)

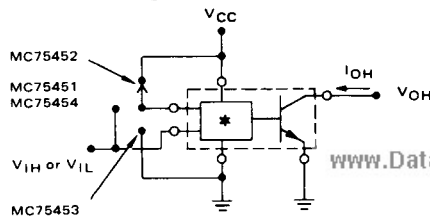
Characteristic	Figure	Symbol	Min	Typ (1)	Max	Unit
Input Voltage — High Logic State	1,2	V_{IH}	2.0	—	—	Vdc
Input Voltage — Low Logic State	1,2	V_{IL}	—	—	0.8	Vdc
Input Clamp Voltage ($V_{CC} = 4.75$ V, $I_I = -12$ mA)	4	V_I	—	-1.2	-1.5	Vdc
Output Current — High Logic State ($V_{CC} = 4.75$ V, $V_{OH} = 30$ V, $V_{IH} = 2.0$ V) ($V_{CC} = 4.75$ V, $V_{OH} = 30$ V, $V_{IL} = 0.8$ V)	2	I_{OH}	—	—	100	μA
Output Voltage — Low Logic State ($V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V) ($V_{CC} = 4.75$ V, $V_{IH} = 2.0$ V) ($I_{OL} = 100$ mA) ($I_{OL} = 300$ mA)	1	V_{OL}	—	0.25 0.5	0.4 0.7	Vdc
Input Current — High Logic State ($V_{CC} = 5.25$ V, $V_I = 2.4$ V) ($V_{CC} = 5.25$ V, $V_I = 5.5$ V)	3	I_{IH}	—	—	40 1.0	μA mA
Input Current — Low Logic State ($V_{CC} = 5.25$ V, $V_I = 0.4$ V)	4	I_{IL}	—	-1.0	-1.6	mA
Power Supply Current — Output High Logic State ($V_{CC} = 5.25$ V, $V_I = 5.0$ V) ($V_{CC} = 5.25$ V, $V_I = 0$) ($V_{CC} = 5.25$ V, $V_I = 5.0$ V) ($V_{CC} = 5.25$ V, $V_I = 0$)	5	I_{CCH}	—	7.0 11 8.0 13	11 14 11 17	mA
Power Supply Current — Output Low Logic State ($V_{CC} = 5.25$ V, $V_I = 0$) ($V_{CC} = 5.25$ V, $V_I = 5.0$ V) ($V_{CC} = 5.25$ V, $V_I = 0$) ($V_{CC} = 5.25$ V, $V_I = 5.0$ V)	5	I_{CCL}	—	52 56 54 61	65 71 68 79	mA

(1) Typical Values Measured with $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$.

TEST CIRCUITS

(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)FIGURE 1 — V_{OL} . V_{IH} — MC75452 and MC75454
 V_{IL} — MC75451 and MC75453

*See Page 1 for specific gate type.

FIGURE 2 — I_{OH} . V_{IH} — MC75451 and MC75453
 V_{IL} — MC75452 and MC75454Each input is tested at V_{IH} and V_{IL} .

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SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx 200\text{ mA}$, $C_L = 15\text{ pF}$, $R_L = 50\text{ ohms}$)						
MC75451						
Low-to-High-Level Output	t_{PLH}	6	—	17	—	ns
High-to-Low-Level Output	t_{PHL}		—	18	—	
MC75452						
Low-to-High-Level Output	t_{PLH}	6	—	18	—	ns
High-to-Low-Level Output	t_{PHL}		—	16	—	
MC75453						
Low-to-High-Level Output	t_{PLH}	6	—	15	—	ns
High-to-Low-Level Output	t_{PHL}		—	17	—	
MC75454						
Low-to-High-Level Output	t_{PLH}	6	—	25	—	ns
High-to-Low-Level Output	t_{PHL}		—	19	—	
Transition Time ($I_O \approx 200\text{ mA}$, $C_L = 15\text{ pF}$, $R_L = 50\text{ ohms}$)						
MC75451						
Low-to-High-Level Output	t_{TLH}	6	—	6.0	—	ns
High-to-Low-Level Output	t_{THL}		—	11	—	
MC75452						
Low-to-High-Level Output	t_{TLH}	6	—	8.0	—	ns
High-to-Low-Level Output	t_{THL}		—	9.0	—	
MC75453						
Low-to-High-Level Output	t_{TLH}	6	—	5.0	—	ns
High-to-Low-Level Output	t_{THL}		—	8.0	—	
MC75454						
Low-to-High-Level Output	t_{TLH}	6	—	5.0	—	ns
High-to-Low-Level Output	t_{THL}		—	8.0	—	

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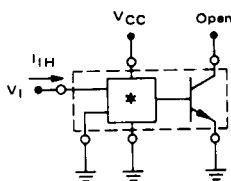
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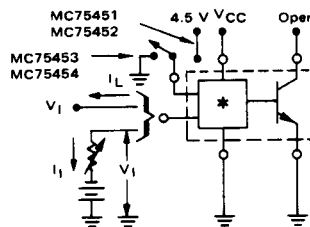
TEST CIRCUITS (Continued)
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 — I_{IH}
(ALL DEVICE TYPES)



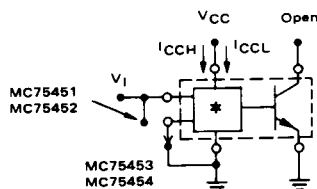
Each input is tested separately.

FIGURE 4 — I_{IL}, V_I
(ALL DEVICE TYPES)



Each input is tested separately.

FIGURE 5 — I_{CCH}, I_{CCL}
(ALL DEVICE TYPES)



Both gates are tested simultaneously.

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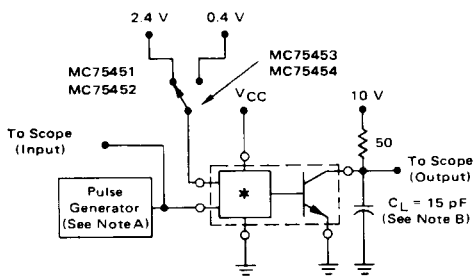
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*See page 1 for specific gate type.

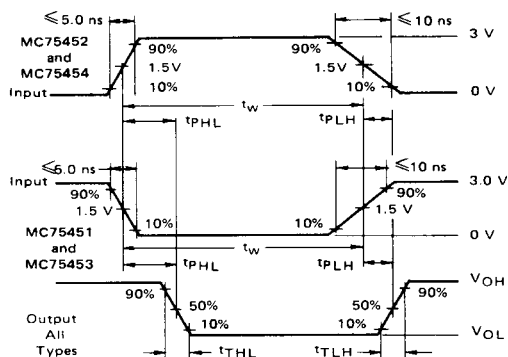
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FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



- NOTES: A. Pulse generator characteristics: $t_w = 0.5 \mu s$,
 PRR = 1.0 MHz, $z_o \approx 50 \Omega$
 B. C_L includes probe and test fixture capacitance.


 REPRESENTATIVE SCHEMATIC DIAGRAMS
 (1/2 Circuits Shown)
