

# MITSUBISHI MICROCOMPUTERS 7560 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The 7560 group is the 8-bit microcomputer based on the 740 family core technology.

The 7560 group has the LCD drive control circuit, an 8-channel A/D-D-A converter, UART and PWM as additional functions.

The various microcomputers in the 7560 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 7560 Group, refer the section on group expansion.

## FEATURES

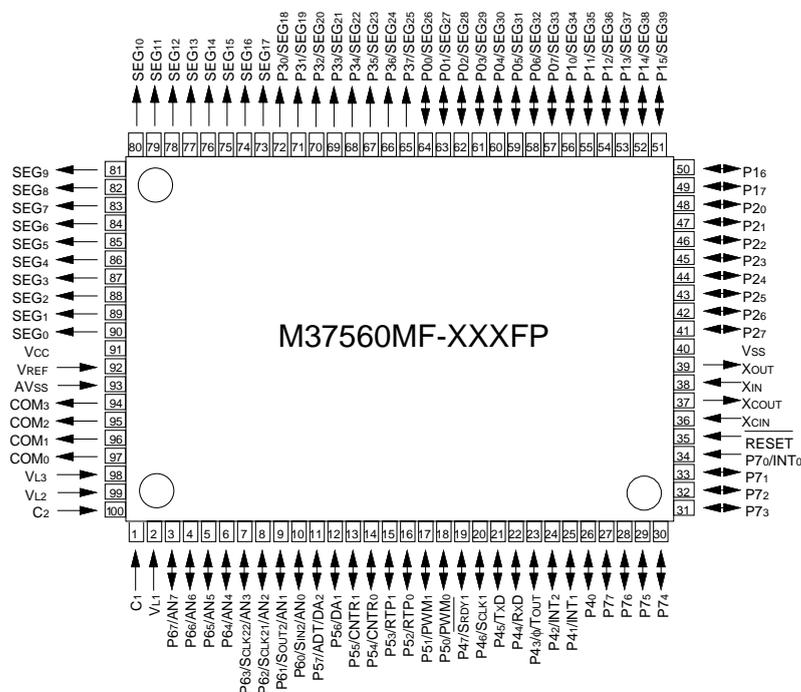
- Basic machine-language instructions ..... 71
- The minimum instruction execution time ..... 0.5  $\mu$ s  
(at 8 MHz oscillation frequency)
- Memory size
  - ROM ..... 32 K to 60 K bytes
  - RAM ..... 1024 to 2560 bytes
- Programmable input/output ports ..... 55
- Software pull-up resistors ..... Built-in
- Output ports ..... 8
- Input ports ..... 1
- Interrupts ..... 17 sources, 16 vectors  
(includes key input interrupt)

- Timers ..... 8-bit X 3, 16-bit X 2
- Serial I/O1 ..... 8-bit X 1 (UART or Clock-synchronous)
- Serial I/O2 ..... 8-bit X 1 (Clock-synchronous)
- PWM output ..... 8-bit X 1
- A-D converter ..... 8-bit X 8 channels
- D-A converter ..... 8-bit X 2 channels
- LCD drive control circuit
  - Bias ..... 1/2, 1/3
  - Duty ..... 1/2, 1/3, 1/4
  - Common output ..... 4
  - Segment output ..... 40
- 2 Clock generating circuits  
(connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer ..... 14-bit X 1
- Power source voltage ..... 2.2 to 5.5 V
- Power dissipation
  - In high-speed mode ..... 40 mW  
(at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 60  $\mu$ W  
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... - 20 to 85°C

## APPLICATIONS

Camera, household appliances, consumer electronics, etc.

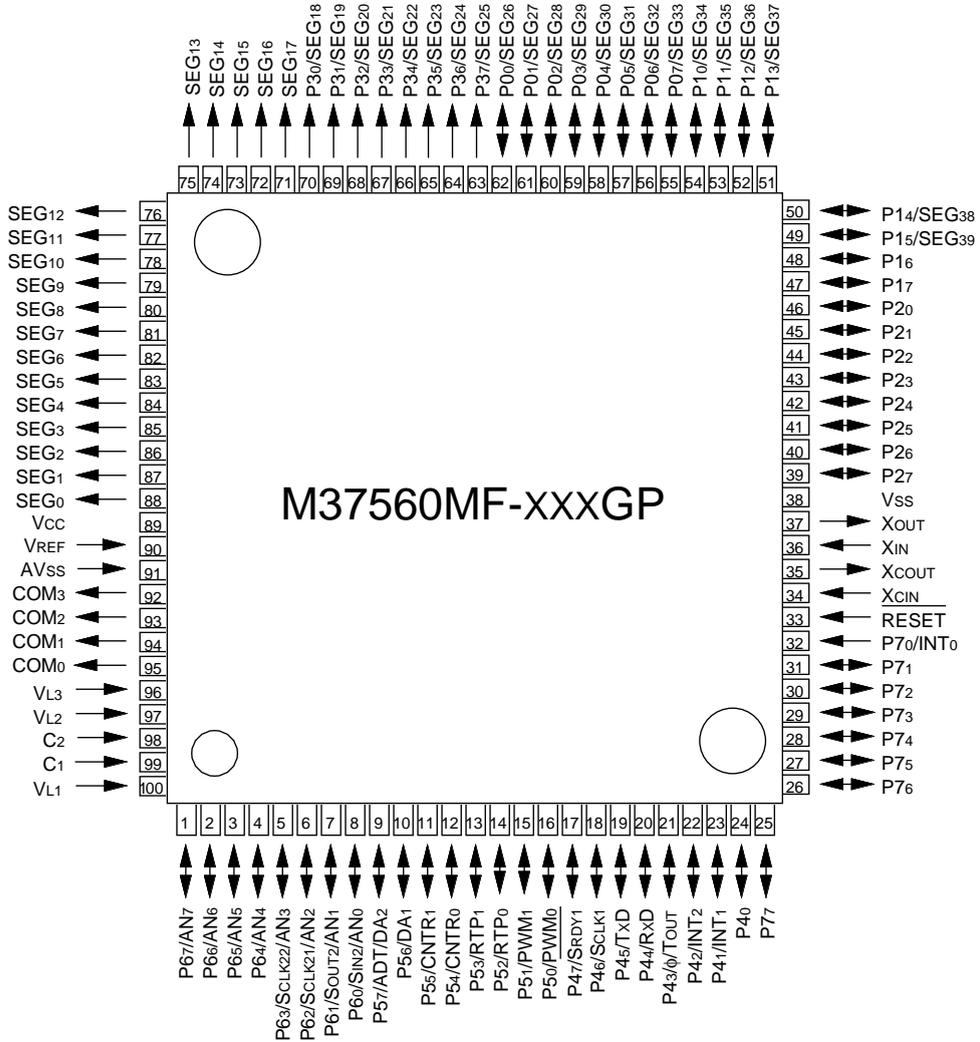
## PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A

Fig. 1 Pin configuration of M37560MF-XXXFP

**PIN CONFIGURATION (TOP VIEW)**



Package type : 100P6Q-A

Fig. 2 Pin configuration of M37560MF-XXXGP

FUNCTIONAL BLOCK DIAGRAM (Package : 100P6S-A)

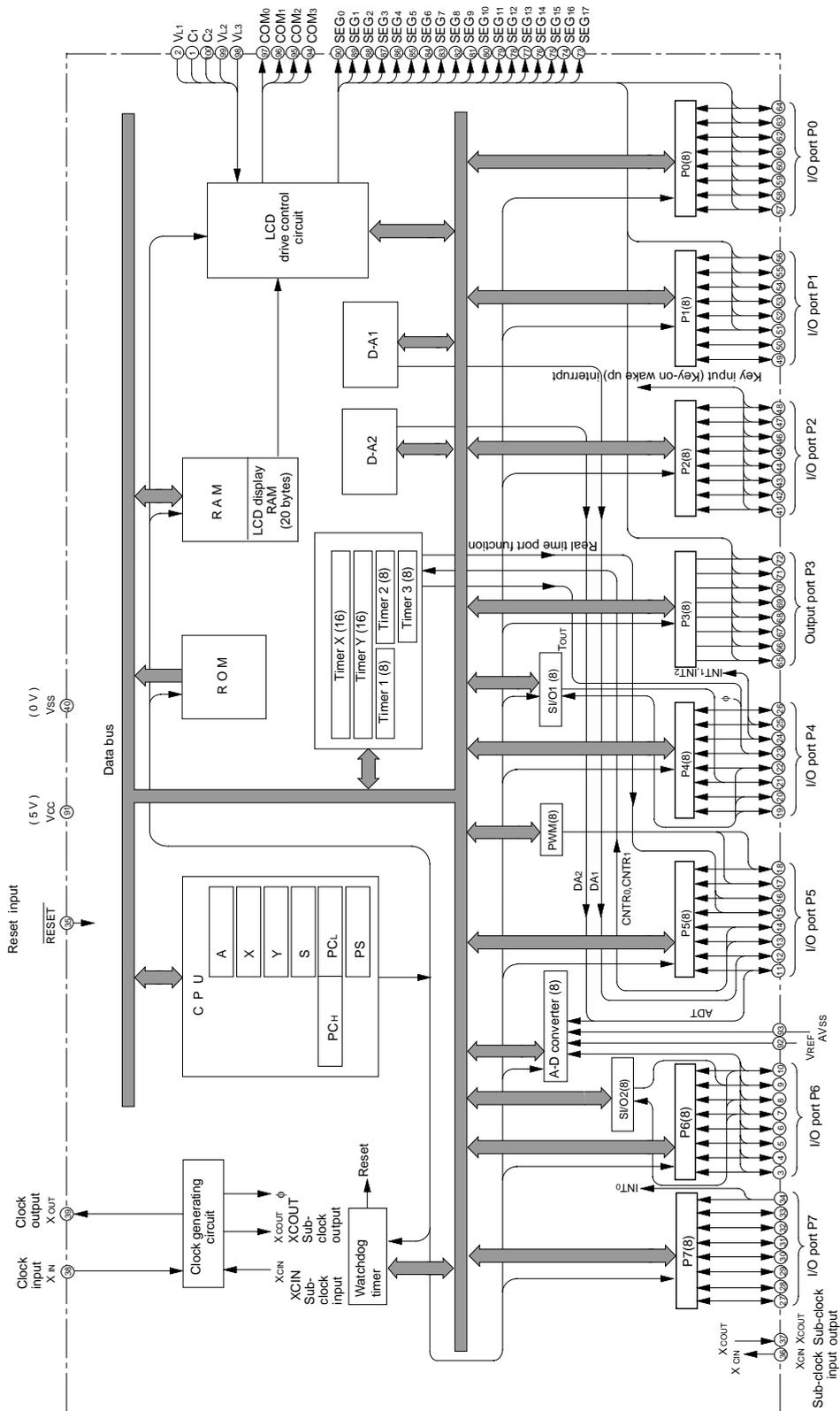


Fig. 3 Functional block diagram

**PIN DESCRIPTION**

**Table 1 Pin description (1)**

Pin	Name	Function	
			Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.2 V to 5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter.	
AVSS	Analog power source	•GND input pin for A-D converter. •Connect to Vss.	
RESET	Reset input	•Reset input pin for active "L".	
XIN	Clock input	•Input and output pins for the main clock generating circuit. •Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	•If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. A feedback resistor is built-in.	
VL1-VL3	LCD power source	•Input $0 \leq VL1 \leq VL2 \leq VL3$ voltage. •Input $0 - VL3$ voltage to LCD. ( $0 \leq VL1 \leq VL2 \leq VL3$ when a voltage is multiplied.)	
C1, C2	Charge-pump capacitor pin	•External capacitor pins for a voltage multiplier (3 times) of LCD control.	
COM0-COM3	Common output	•LCD common output pins. •COM2 and COM3 are not used at 1/2 duty ratio. •COM3 is not used at 1/3 duty ratio.	
SEG0-SEG17	Segment output	•LCD segment output pins.	
P00/SEG26-P07/SEG33	I/O port P0	<ul style="list-style-type: none"> <li>•8-bit I/O port.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•Pull-up control is enabled.</li> <li>•I/O direction register allows each 8-bit pin to be programmed as either input or output.</li> </ul>	•LCD segment output pins
P10/SEG34-P15/SEG39	I/O port P1	<ul style="list-style-type: none"> <li>•6-bit I/O port with same function as port P0.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•Pull-up control is enabled.</li> <li>•I/O direction register allows each 6-bit pin to be programmed as either input or output.</li> </ul>	
P16, P17		<ul style="list-style-type: none"> <li>•2-bit I/O port.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>•Pull-up control is enabled.</li> </ul>	
P20 - P27	I/O port P2	<ul style="list-style-type: none"> <li>•8-bit I/O port with same function as P16 and P17.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•Pull-up control is enabled.</li> </ul>	•Key input (key-on wake-up) interrupt input pins
P30/SEG18 - P37/SEG25	Output port P3	<ul style="list-style-type: none"> <li>•8-bit output port with same function as port P0.</li> <li>•CMOS 3-state output structure.</li> <li>•Port output control is enabled.</li> </ul>	•LCD segment output pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P40	I/O port P4	<ul style="list-style-type: none"> <li>•1-bit I/O port with same function as P16 and P17.</li> <li>•CMOS compatible input level.</li> <li>•N-channel open-drain output structure.</li> </ul>	
P41/INT1, P42/INT2			<ul style="list-style-type: none"> <li>•Interrupt input pins</li> </ul>
P43/φ/TOUT			<ul style="list-style-type: none"> <li>•φ clock output pin</li> <li>•Timer 2 output pin</li> </ul>
P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1			<ul style="list-style-type: none"> <li>•Serial I/O1 I/O pins</li> </ul>
P50/PWM0, P51/PWM1	I/O port P5	<ul style="list-style-type: none"> <li>•8-bit I/O port with same function as P16 and P17.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•Pull-up control is enabled.</li> </ul>	<ul style="list-style-type: none"> <li>•PWM function pins</li> </ul>
P52/RTP0, P53/RTP1			<ul style="list-style-type: none"> <li>•Real time port function pins</li> </ul>
P54/CNTR0, P55/CNTR1			<ul style="list-style-type: none"> <li>•Timer X, Y function pins</li> </ul>
P56/DA1, P57/ADT/DA2			<ul style="list-style-type: none"> <li>•D-A conversion output pins</li> </ul>
P60/AN0/SIN2, P61/AN1/SOUT2, P62/AN2/SCLK21, P63/AN3/SCLK22	I/O port P6	<ul style="list-style-type: none"> <li>•8-bit I/O port with same function as P16 and P17.</li> <li>•CMOS compatible input level.</li> <li>•CMOS 3-state output structure.</li> <li>•Pull-up control is enabled.</li> </ul>	<ul style="list-style-type: none"> <li>•A-D conversion input pins</li> <li>•Serial I/O2 I/O pins</li> </ul>
P64/AN4– P67/AN7			<ul style="list-style-type: none"> <li>•A-D conversion input pins</li> </ul>
P70/INT0	Input port P7	<ul style="list-style-type: none"> <li>•1-bit input port.</li> </ul>	<ul style="list-style-type: none"> <li>•Interrupt input pin</li> </ul>
P71–P77	I/O port P7	<ul style="list-style-type: none"> <li>•7-bit I/O port with same function as P16 and P17.</li> <li>•CMOS compatible input level.</li> <li>•N-channel open-drain output structure.</li> </ul>	
XCOUT	Sub-clock output	<ul style="list-style-type: none"> <li>•Sub-clock generating circuit I/O pins.</li> </ul> (Connect a resonator. External clock cannot be used.)	
XCIN	Sub-clock input		

**PART NUMBERING**

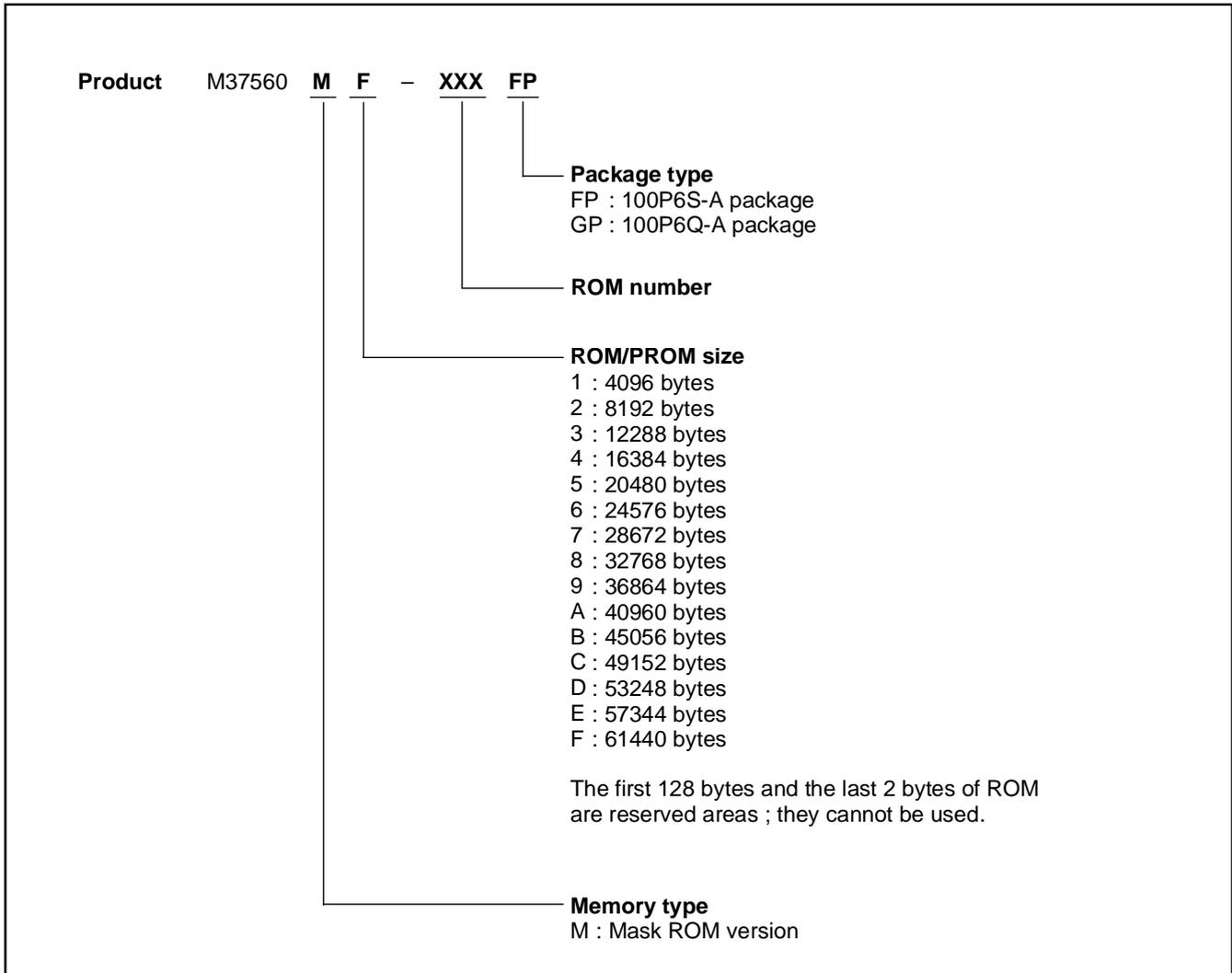


Fig. 4 Part numbering

**GROUP EXPANSION**

Mitsubishi plans to expand the 7560 group as follows.

**Packages**

100P6Q-A ..... 0.5 mm-pitch plastic molded QFP  
 100P6S-A ..... 0.65 mm-pitch plastic molded QFP

**Memory Type**

Support for mask ROM version.

**Memory Size**

ROM size ..... 32 K to 60 K bytes  
 RAM size ..... 1024 to 2560 bytes

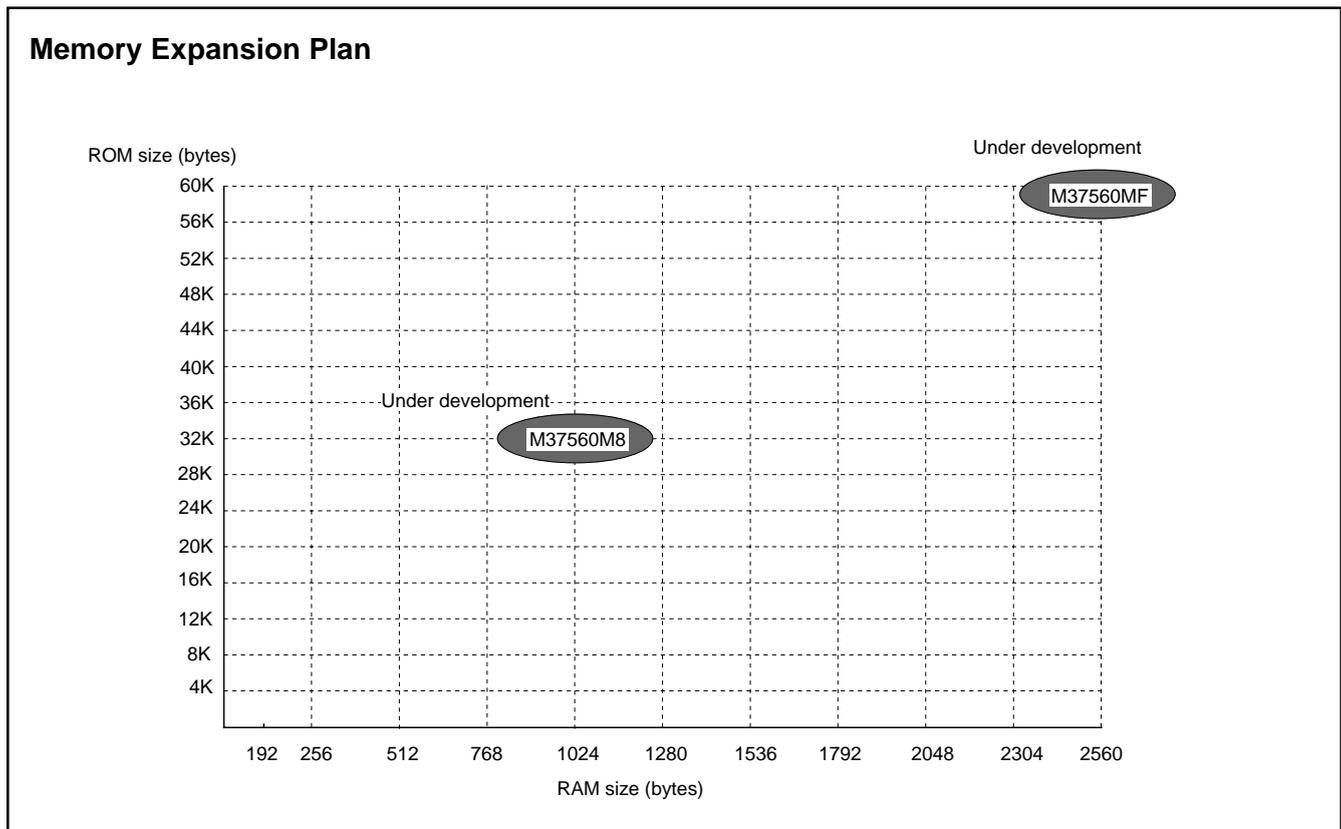


Fig. 5 Memory expansion plan

Currently products are listed below.

Table 3. List of products

As of Mar. 2001

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M37560M8-XXXFP	32768 (32638)	1024	100P6S-A	Mask ROM version
M37560M8-XXXGP			100P6Q-A	Mask ROM version
M37560MF-XXXFP	61440 (61310)	2560	100P6S-A	Mask ROM version
M37560MF-XXXGP			100P6Q-A	Mask ROM version

**FUNCTIONAL DESCRIPTION  
CENTRAL PROCESSING UNIT (CPU)**

The 7560 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:  
The FST and SLW instruction cannot be used.  
The STP, WIT, MUL, and DIV instruction can be used.

**[Accumulator (A)]**

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

**[Index Register X (X)]**

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

**[Index Register Y (Y)]**

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

**[Stack Pointer (S)]**

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

**[Program Counter (PC)]**

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

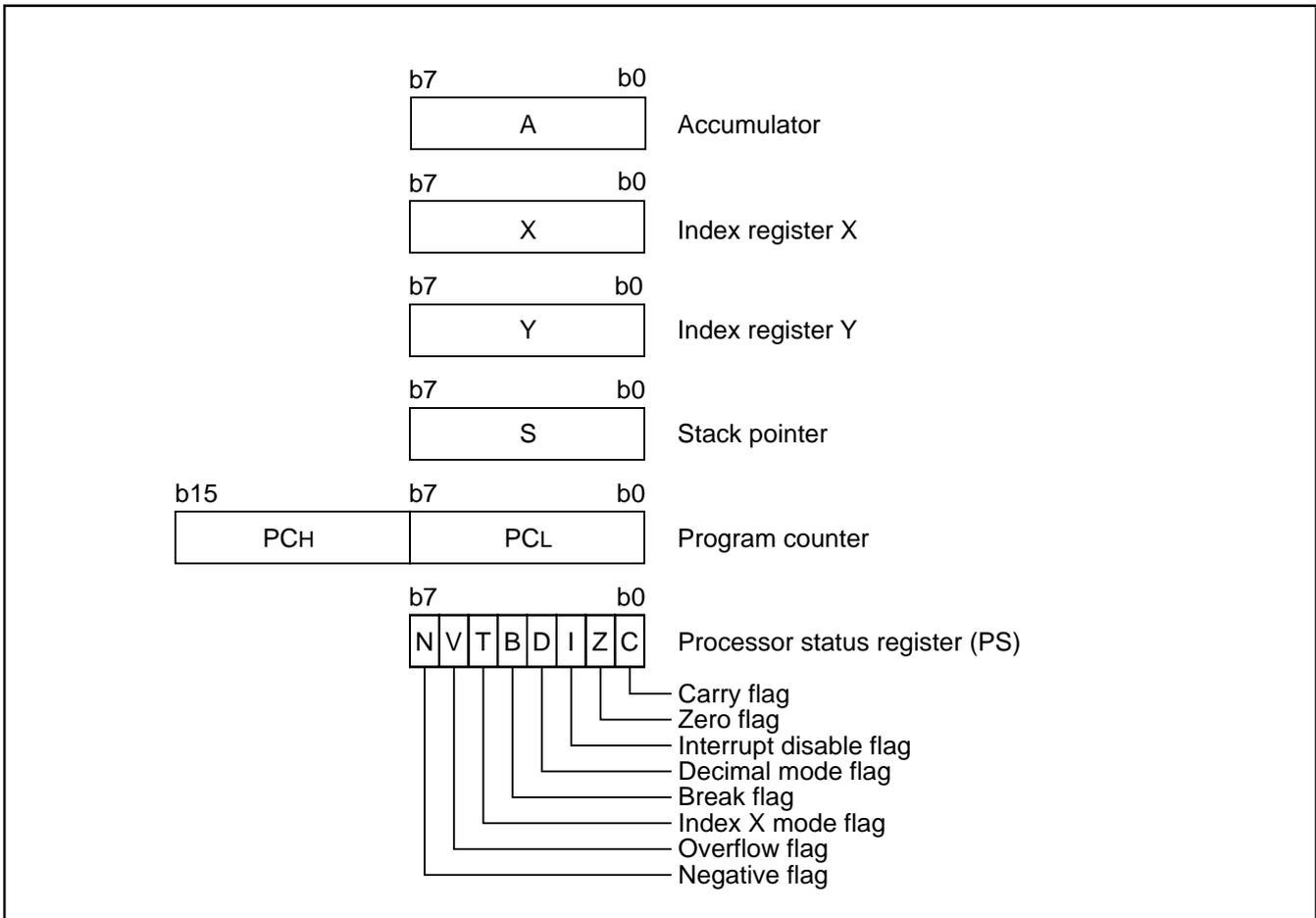


Fig. 6 740 Family CPU register structure

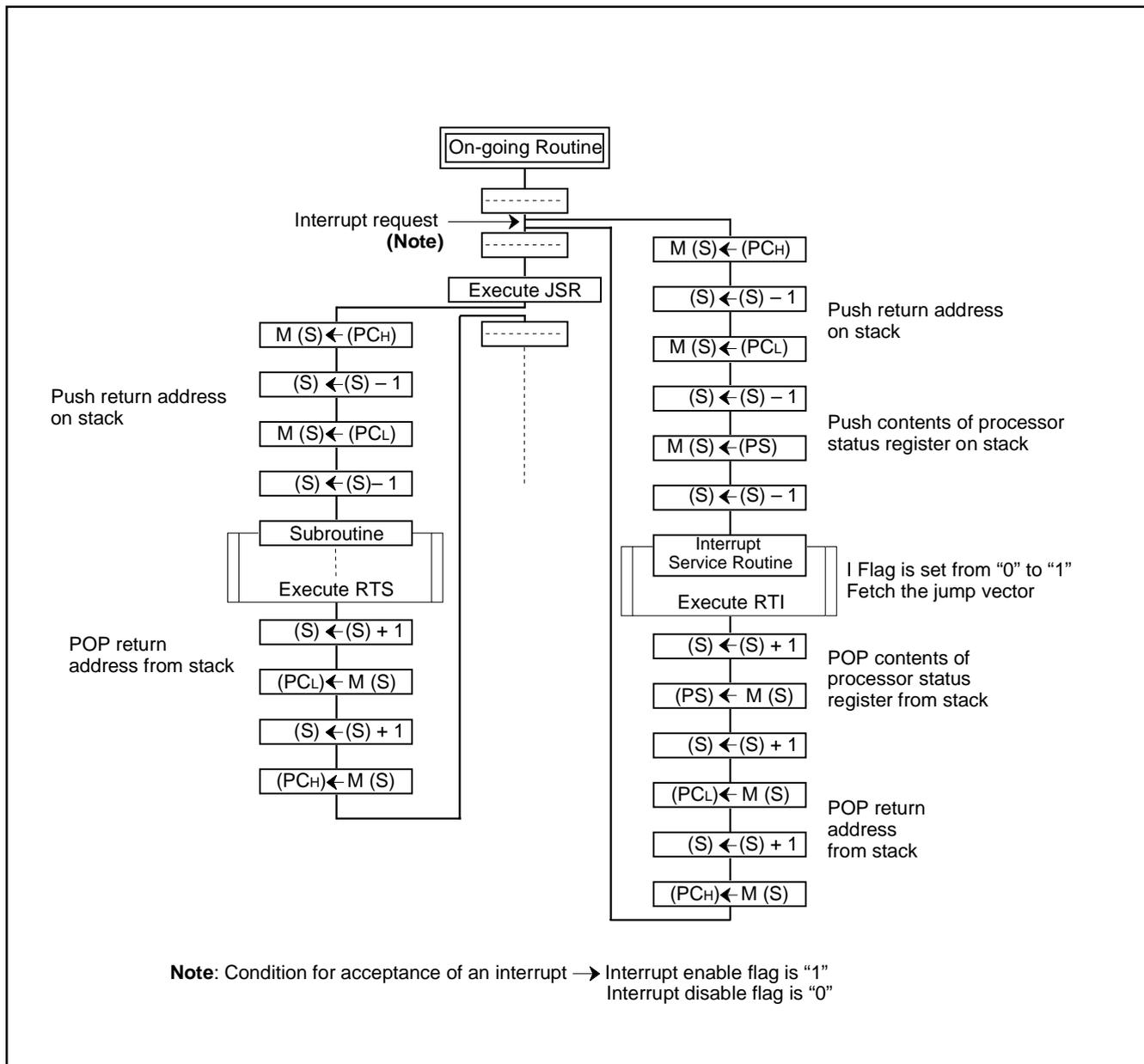


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

**[Processor status register (PS)]**

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

- Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

- Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

- Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

- Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

- Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

- Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

- Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

**Table 5 Set and clear instructions of each bit of processor status register**

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

**[CPU Mode Register (CPUM)] 003B16**

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B16.

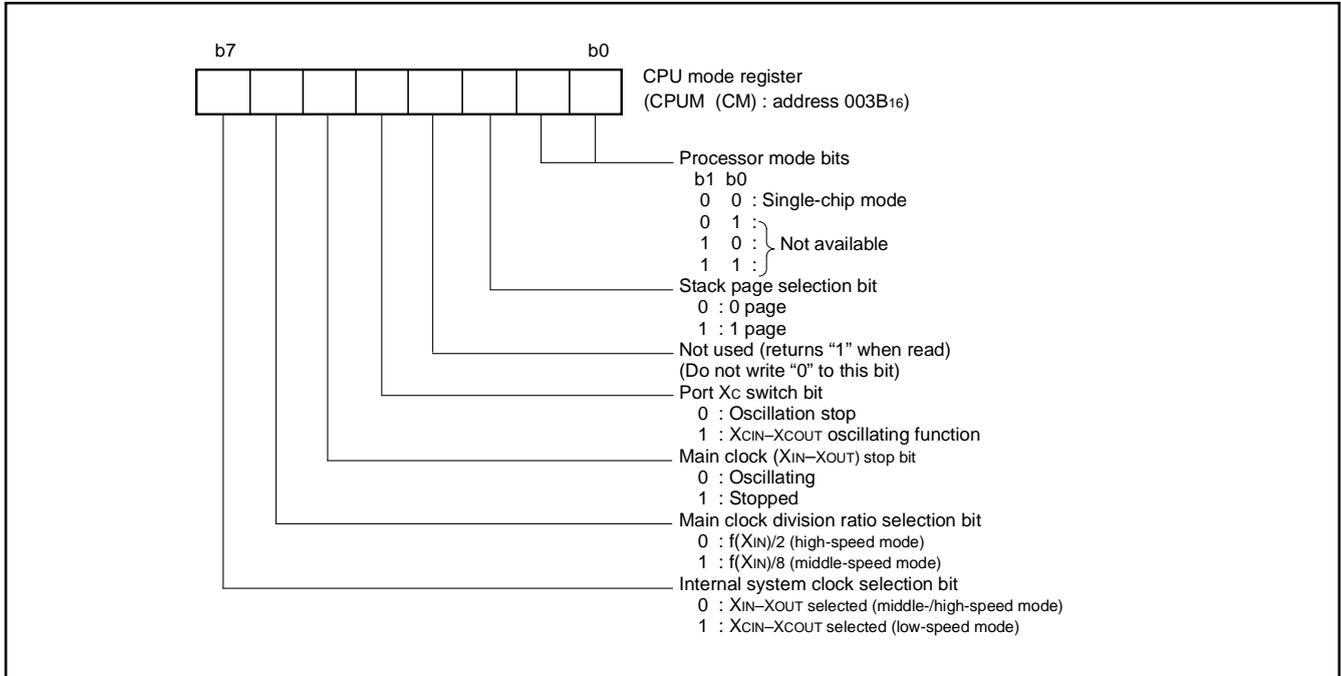


Fig. 8 Structure of CPU mode register

**MEMORY**

**Special Function Register (SFR) Area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

**RAM**

RAM is used for data storage and for stack area of subroutine calls and interrupts.

**ROM**

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

**Interrupt Vector Area**

The interrupt vector area contains reset and interrupt vectors.

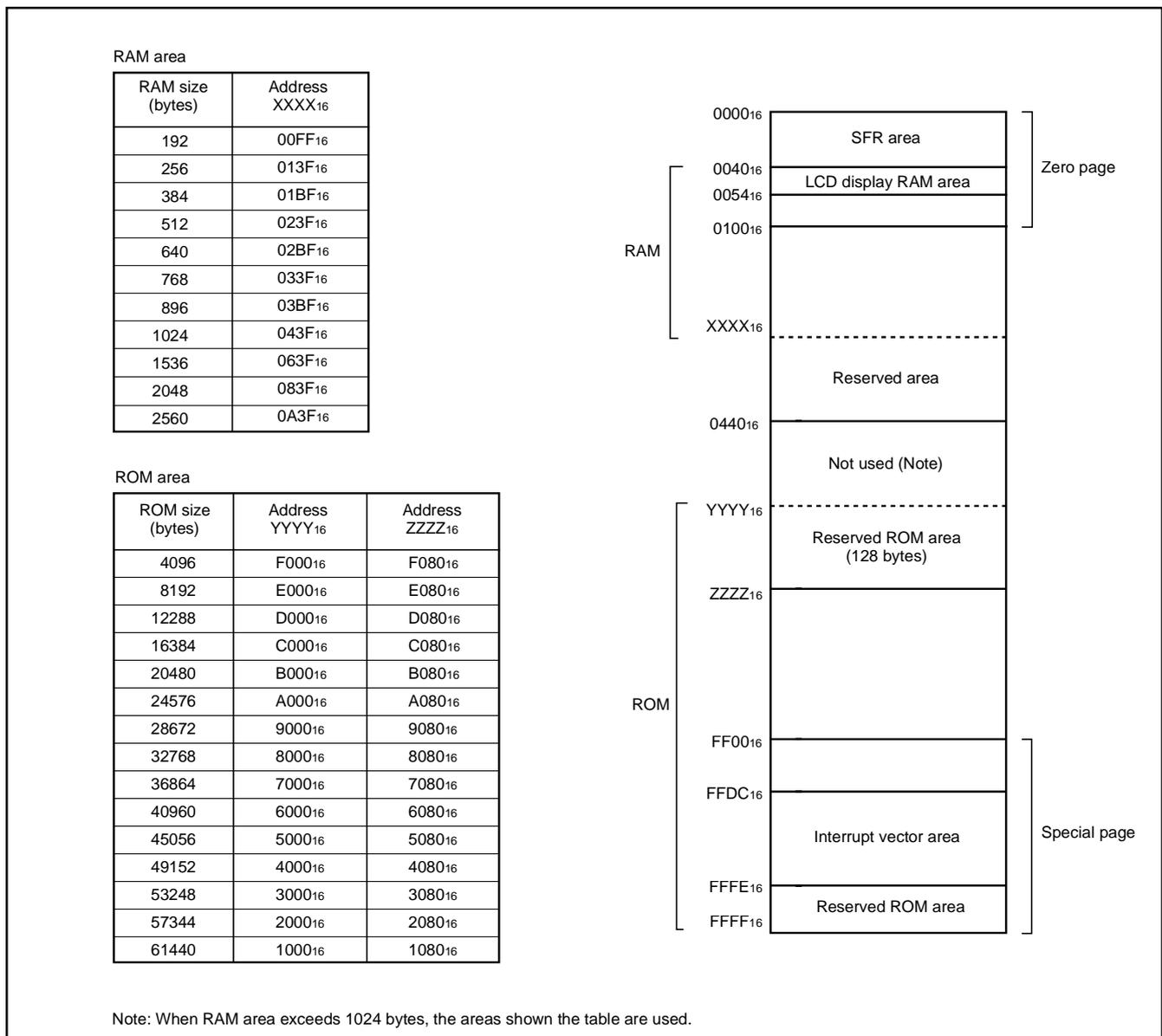
**Zero Page**

The 256 bytes from addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

**Special Page**

The 256 bytes from addresses FF00<sub>16</sub> to FFFF<sub>16</sub> are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



Note: When RAM area exceeds 1024 bytes, the areas shown the table are used.

Fig. 9 Memory map diagram

0000 <sup>16</sup>	Port P0 (P0)	0020 <sup>16</sup>	Timer X (low) (TXL)
0001 <sup>16</sup>	Port P0 direction register (P0D)	0021 <sup>16</sup>	Timer X (high) (TXH)
0002 <sup>16</sup>	Port P1 (P1)	0022 <sup>16</sup>	Timer Y (low) (TYL)
0003 <sup>16</sup>	Port P1 direction register (P1D)	0023 <sup>16</sup>	Timer Y (high) (TYH)
0004 <sup>16</sup>	Port P2 (P2)	0024 <sup>16</sup>	Timer 1 (T1)
0005 <sup>16</sup>	Port P2 direction register (P2D)	0025 <sup>16</sup>	Timer 2 (T2)
0006 <sup>16</sup>	Port P3 (P3)	0026 <sup>16</sup>	Timer 3 (T3)
0007 <sup>16</sup>	Port P3 output control register (P3C)	0027 <sup>16</sup>	Timer X mode register (TXM)
0008 <sup>16</sup>	Port P4 (P4)	0028 <sup>16</sup>	Timer Y mode register (TYM)
0009 <sup>16</sup>	Port P4 direction register (P4D)	0029 <sup>16</sup>	Timer 123 mode register (T123M)
000A <sup>16</sup>	Port P5 (P5)	002A <sup>16</sup>	Tout/φ output control register (CKOUT)
000B <sup>16</sup>	Port P5 direction register (P5D)	002B <sup>16</sup>	PWM control register (PWMCON)
000C <sup>16</sup>	Port P6 (P6)	002C <sup>16</sup>	PWM prescaler (PREPWM)
000D <sup>16</sup>	Port P6 direction register (P6D)	002D <sup>16</sup>	PWM register (PWM)
000E <sup>16</sup>	Port P7 (P7)	002E <sup>16</sup>	Reserved area
000F <sup>16</sup>	Port P7 direction register (P7D)	002F <sup>16</sup>	Reserved area
0010 <sup>16</sup>		0030 <sup>16</sup>	Reserved area
0011 <sup>16</sup>		0031 <sup>16</sup>	Reserved area
0012 <sup>16</sup>		0032 <sup>16</sup>	D-A1 conversion register (DA1)
0013 <sup>16</sup>		0033 <sup>16</sup>	D-A2 conversion register (DA2)
0014 <sup>16</sup>	Reserved area	0034 <sup>16</sup>	A-D control register (ADCON)
0015 <sup>16</sup>	Key input control register (KIC)	0035 <sup>16</sup>	A-D conversion register (AD)
0016 <sup>16</sup>	PULL register A (PULLA)	0036 <sup>16</sup>	D-A control register (DACON)
0017 <sup>16</sup>	PULL register B (PULLB)	0037 <sup>16</sup>	Watchdog timer control register (WDTCON)
0018 <sup>16</sup>	Transmit/Receive buffer register (TB/RB)	0038 <sup>16</sup>	Segment output enable register (SEG)
0019 <sup>16</sup>	Serial I/O1 status register (SIO1STS)	0039 <sup>16</sup>	LCD mode register (LM)
001A <sup>16</sup>	Serial I/O1 control register (SIO1CON)	003A <sup>16</sup>	Interrupt edge selection register (INTEDGE)
001B <sup>16</sup>	UART control register (UARTCON)	003B <sup>16</sup>	CPU mode register (CPUM)
001C <sup>16</sup>	Baud rate generator (BRG)	003C <sup>16</sup>	Interrupt request register 1 (IREQ1)
001D <sup>16</sup>	Serial I/O2 control register (SIO2CON)	003D <sup>16</sup>	Interrupt request register 2 (IREQ2)
001E <sup>16</sup>	Reserved area	003E <sup>16</sup>	Interrupt control register 1 (ICON1)
001F <sup>16</sup>	Serial I/O2 register (SIO2)	003F <sup>16</sup>	Interrupt control register 2 (ICON2)

Fig. 10 Memory map of special function register (SFR)

**I/O PORTS**

**Direction Registers**

The I/O ports (ports P0, P1, P2, P4, P5, P6, P71–P77) have direction registers which determine the input/output direction of each individual pin. (Ports P00–P07 are shared with bit 0 of the port P0 direction register, and ports P10–P15 shared with bit 0 of the port P1 direction register.) Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port. When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

**Port P3 Output Control Register**

Bit 0 of the port P3 output control register (address 000716) enables control of the output of ports P30–P37.

When the bit is set to “1”, the port output function is valid.

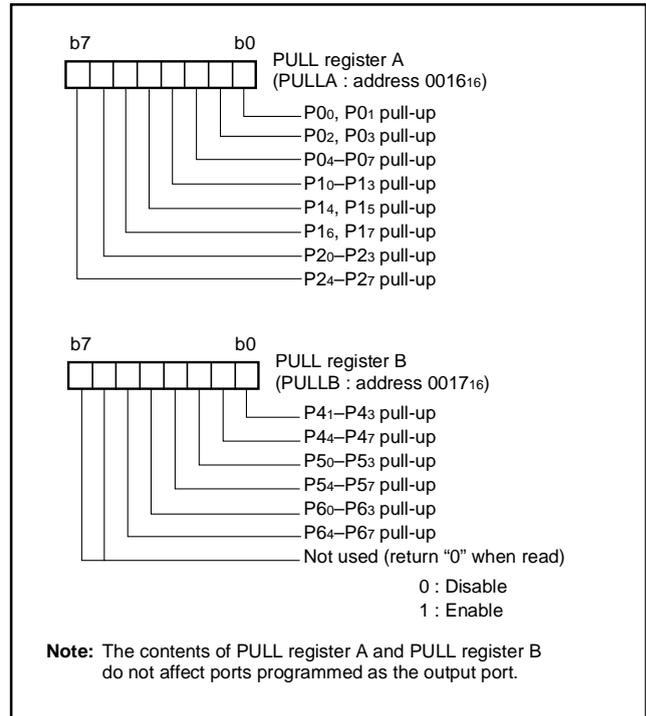
When resetting, bit 0 of the port P3 output control register is set to “0” (the port output function is invalid) and pulled up.

**Pull-up Control**

By setting the PULL register A (address 001616) or the PULL register B (address 001716), ports P0 to P2, P4 to P6 can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

The PULL register A setting is invalid for pins set to segment output with the segment output enable register.



**Fig. 11 Structure of PULL register A and PULL register B**

Table 6 List of I/O port function (1)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.	
P00/SEG26– P07/SEG33	Port P0	Input/output, byte unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)	
P10/SEG34– P15/SEG39	Port P1	Input/output, 6-bit unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)	
P16 , P17		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register A	(4)	
P20–P27	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register2 Key input control register		
P30/SEG18– P37/SEG25	Port P3	Output	CMOS 3-state output	LCD segment output	Segment output enable register P3 output enable register	(3)	
P40	Port P4	Input/output, individual bits	CMOS compatible input level N-channel open-drain output			(13)	
P41/INT1, P42/INT2				CMOS compatible input level	External interrupt input	Interrupt edge selection register	(4)
P43/φ/TOUT				CMOS 3-state output	Timer output φ output	PULL register B Timer 123 mode register TOUT/φ output control register	(12)
P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1				Serial I/O1 function I/O		PULL register B Serial I/O1 control register Serial I/O1 status register UART control register	(5)
							(6)
				(7)			
				(8)			
P50/PWM0, P51/PWM1	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	PWM output	PULL register B PWM control register	(10)	
P52/RTP0, P53/RTP1				Real time port function output	PULL register B Timer X mode register	(9)	
P54/CNTR0				Timer X function I/O	PULL register B Timer X mode register	(11)	
P55/CNTR1				Timer Y function input	PULL register B Timer Y mode register	(14)	
P56/DA1				DA1 output	PULL register B D-A control register	(15)	
P57/ADT/ DA2				DA2 output A-D trigger input	PULL register B D-A control register A-D control register	(15)	

Table 7 List of I/O port function (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P60/SIN2/AN0	Port P6	Input/ output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input Serial I/O2 function I/O	PULL register B A-D control register Serial I/O2 control register	(17)
P61/SOUT2/ AN1						(18)
P62/SCLK21/ AN2						(19)
P63/SCLK22 / AN3						(20)
P64/AN4– P67/AN7				A-D conversion input	A-D control register PULL register B	(16)
P70/INT0	Port P7	Input	CMOS compatible input level	External interrupt input	Interrupt edge selection register	(23)
P71–P77		Input/ output, individual bits	CMOS compatible input level N-channel open-drain output			(13)
COM0–COM3	Common	Output	LCD common output		LCD mode register	(21)
SEG0–SEG17	Segment	Output	LCD segment output			(22)

**Notes1:** How to use double-function ports as function I/O ports, refer to the applicable sections.

**2:** Make sure that the input level at each pin is either 0 V or V<sub>CC</sub> during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow V<sub>CC</sub> to V<sub>SS</sub> through the input-stage gate.

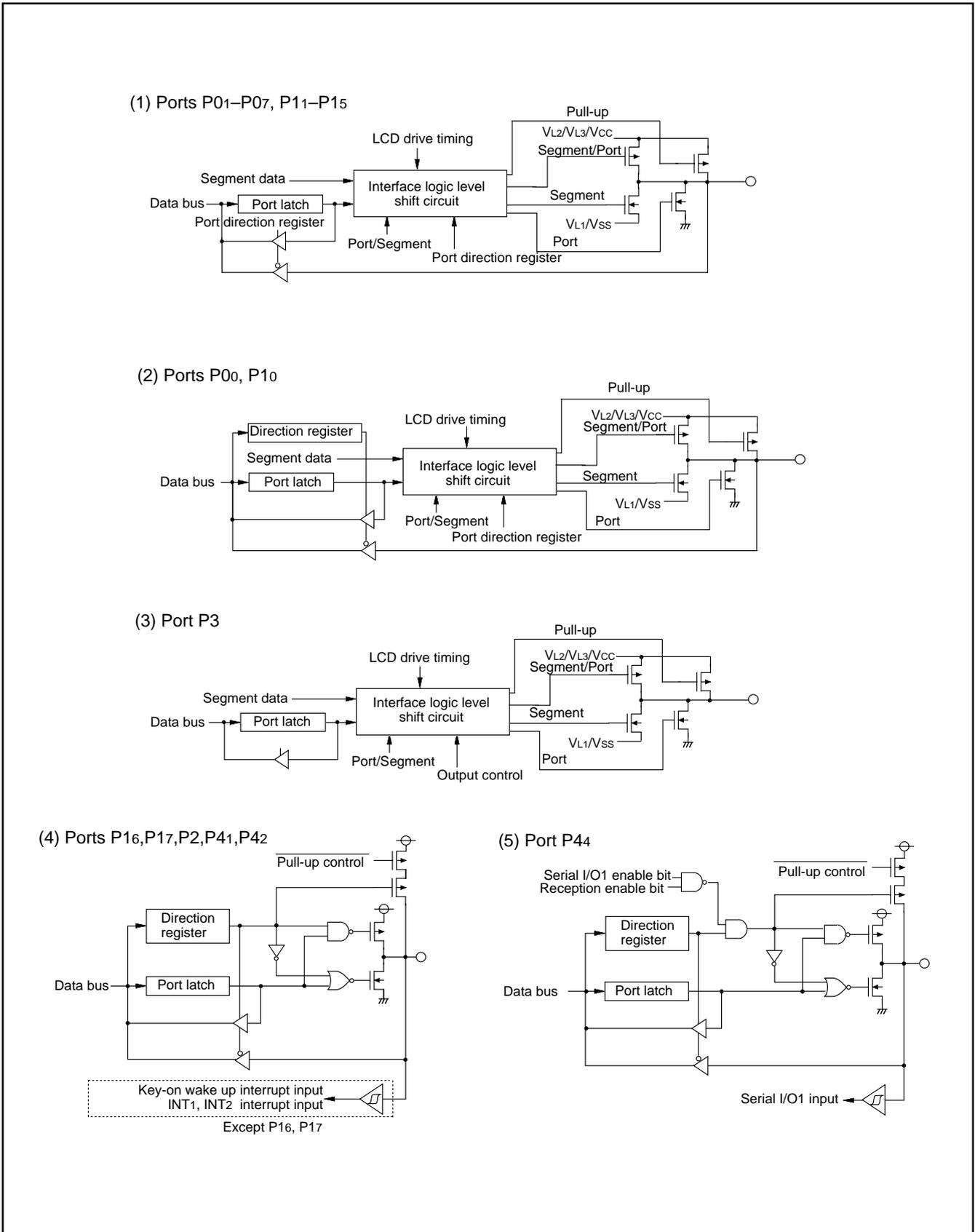


Fig. 12 Port block diagram (1)

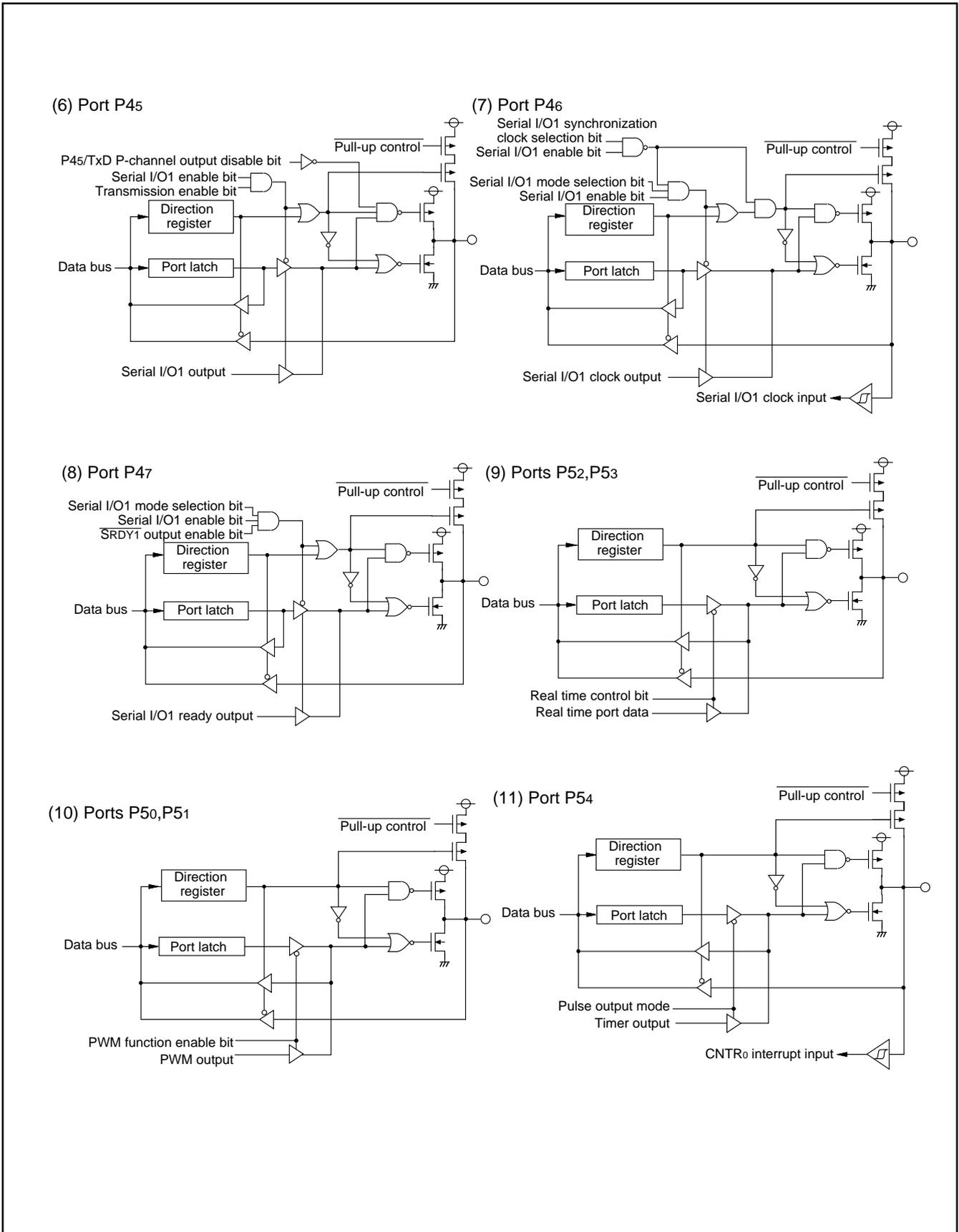


Fig. 13 Port block diagram (2)

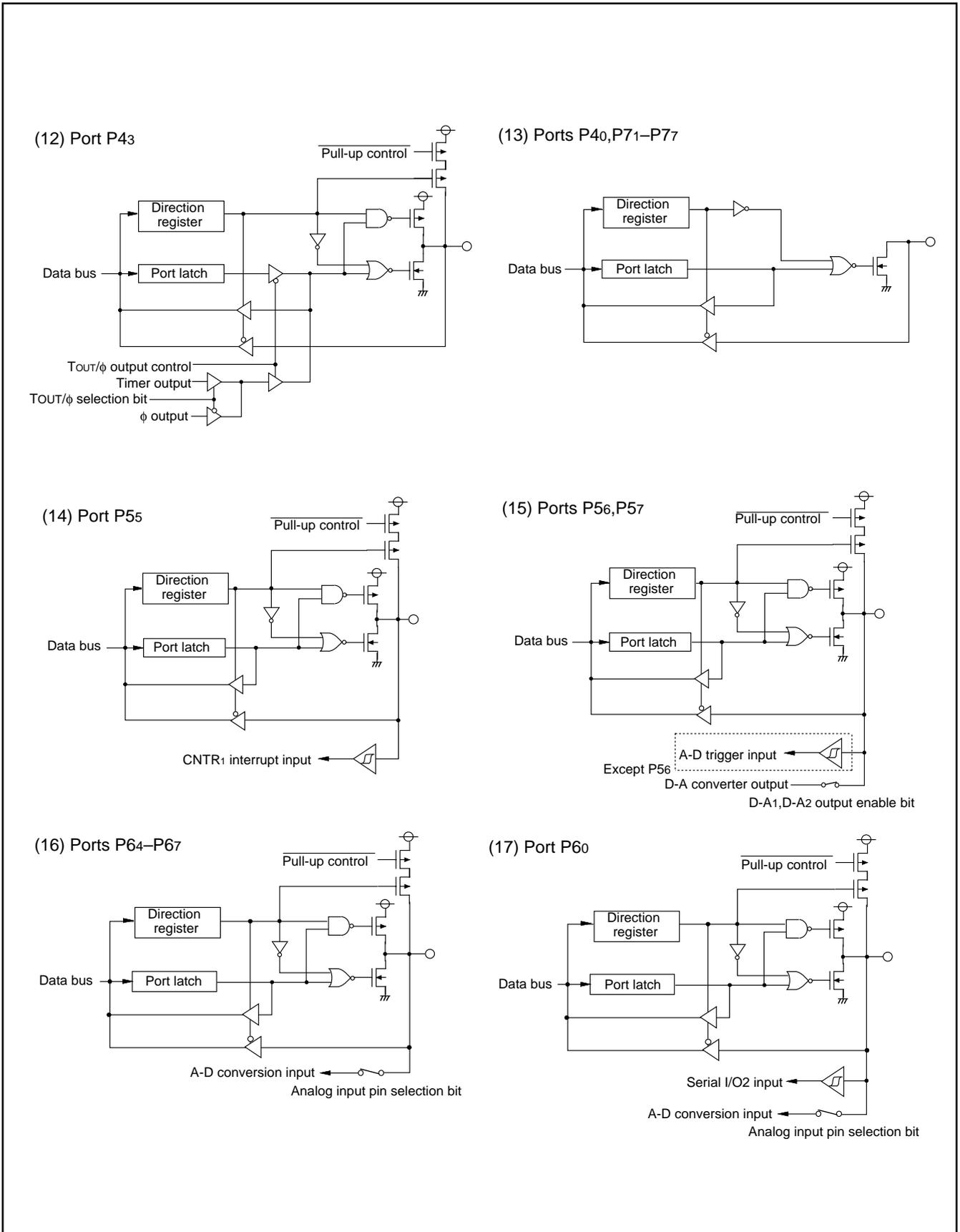


Fig. 14 Port block diagram (3)

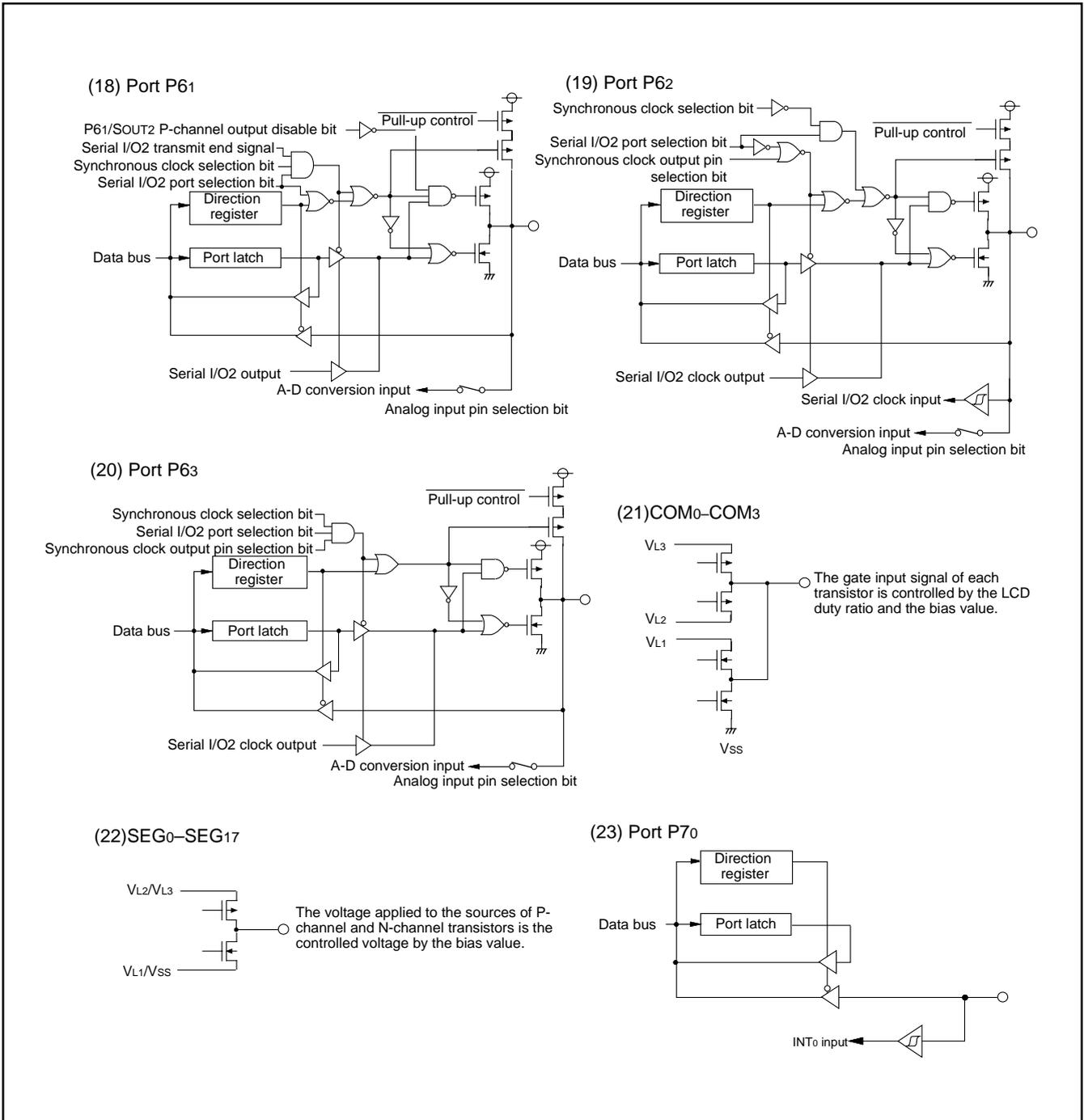


Fig. 15 Port block diagram (4)

**INTERRUPTS**

Interrupts occur by seventeen sources: seven external, nine internal, and one software.

**Interrupt Control**

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

**Interrupt Operation**

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

**Table 8 Interrupt vector addresses and priority**

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset	Non-maskable
INT <sub>0</sub>	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
INT <sub>1</sub>	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O <sub>1</sub> reception	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At completion of serial I/O <sub>1</sub> data reception	Valid when serial I/O <sub>1</sub> is selected
Serial I/O <sub>1</sub> transmission	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At completion of serial I/O <sub>1</sub> transmit shift or when transmission buffer is empty	Valid when serial I/O <sub>1</sub> is selected
Timer X	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At timer X underflow	
Timer Y	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer Y underflow	
Timer 2	8	FFEF <sub>16</sub>	FFEE <sub>16</sub>	At timer 2 underflow	
Timer 3	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At timer 3 underflow	
CNTR <sub>0</sub>	10	FFE <sub>B</sub> <sub>16</sub>	FFE <sub>A</sub> <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>0</sub> input	External interrupt (active edge selectable)
CNTR <sub>1</sub>	11	FFE <sub>9</sub> <sub>16</sub>	FFE <sub>8</sub> <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>1</sub> input	External interrupt (active edge selectable)
Timer 1	12	FFE <sub>7</sub> <sub>16</sub>	FFE <sub>6</sub> <sub>16</sub>	At timer 1 underflow	
INT <sub>2</sub>	13	FFE <sub>5</sub> <sub>16</sub>	FFE <sub>4</sub> <sub>16</sub>	At detection of either rising or falling edge of INT <sub>2</sub> input	External interrupt (active edge selectable)
Serial I/O <sub>2</sub>	14	FFE <sub>3</sub> <sub>16</sub>	FFE <sub>2</sub> <sub>16</sub>	At completion of serial I/O <sub>2</sub> data transmission or reception	Valid when serial I/O <sub>2</sub> is selected
Key input (Key-on wake-up)	15	FFE <sub>1</sub> <sub>16</sub>	FFE <sub>0</sub> <sub>16</sub>	At falling of conjunction of input level for port P <sub>2</sub> (at input mode)	External interrupt (valid at falling)
ADT	16	FFD <sub>F</sub> <sub>16</sub>	FFD <sub>E</sub> <sub>16</sub>	At falling edge of ADT input	Valid when ADT interrupt is selected External interrupt (valid at falling)
A-D conversion				At completion of A-D conversion	Valid when A-D interrupt is selected
BRK instruction	17	FFD <sub>D</sub> <sub>16</sub>	FFD <sub>C</sub> <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

**Notes1:** Vector addresses contain interrupt jump destination addresses.

**2:** Reset function in the same way as an interrupt with the highest priority.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge  
 Related register: Interrupt edge selection register (address 3A16)  
 Timer X mode register (address 2716)  
 Timer Y mode register (address 2816)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated  
 Related register: Interrupt source selection bit of A-D control register (bit 6 of address 3416)

When not requiring for the interrupt occurrence synchronous with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit (polarity switch bit) or the interrupt source select bit to "1".
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

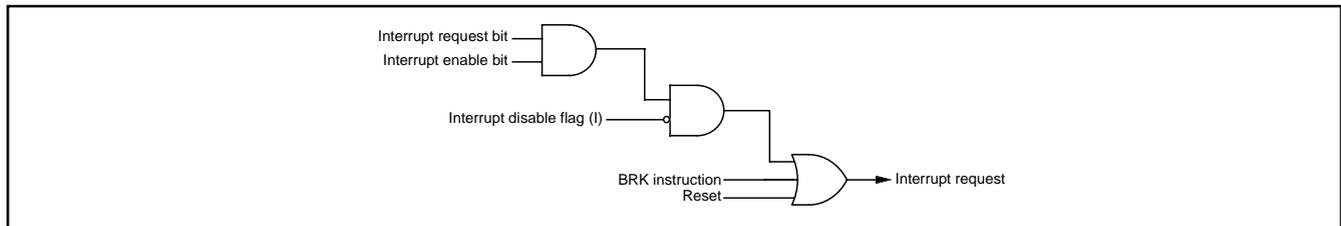


Fig. 16 Interrupt control

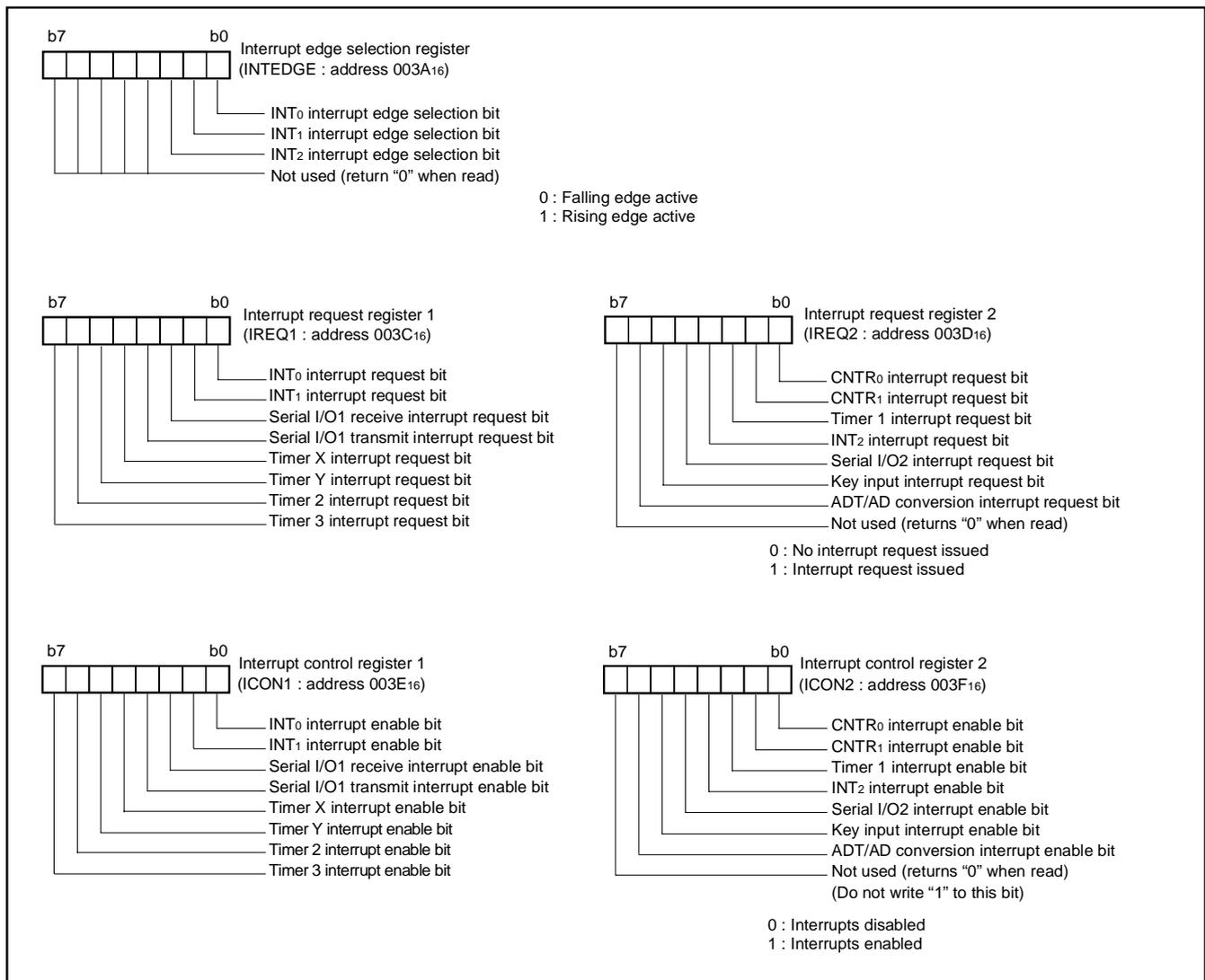


Fig. 17 Structure of interrupt-related registers

**Key Input Interrupt (Key-on Wake Up)**

A Key-on wake up interrupt request is generated by applying "L" level voltage to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level

goes from "1" to "0". An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.

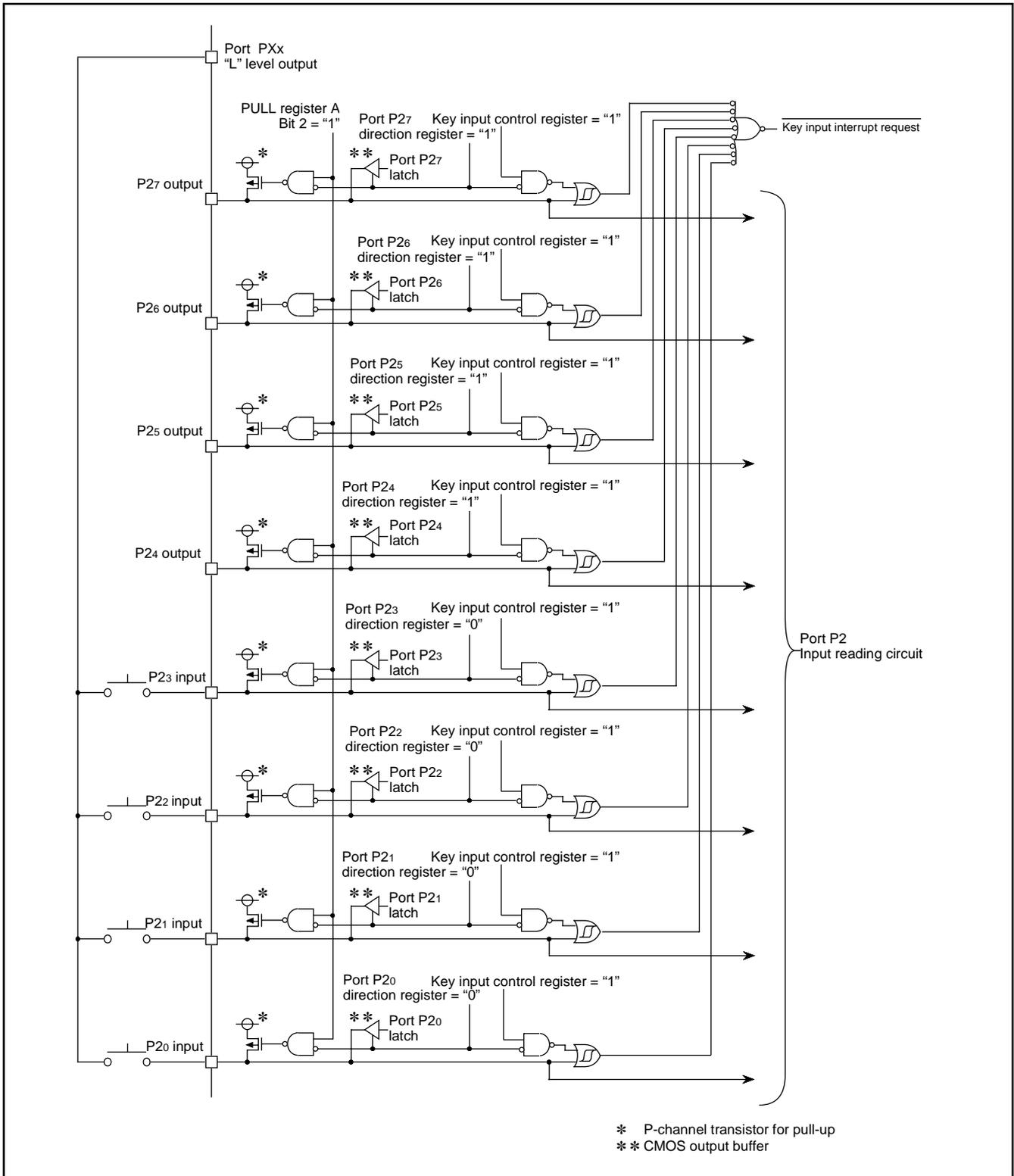


Fig. 18 Connection example when using key input control register, key input interrupt and port P2 block diagram

**TIMERS**

The 7560 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

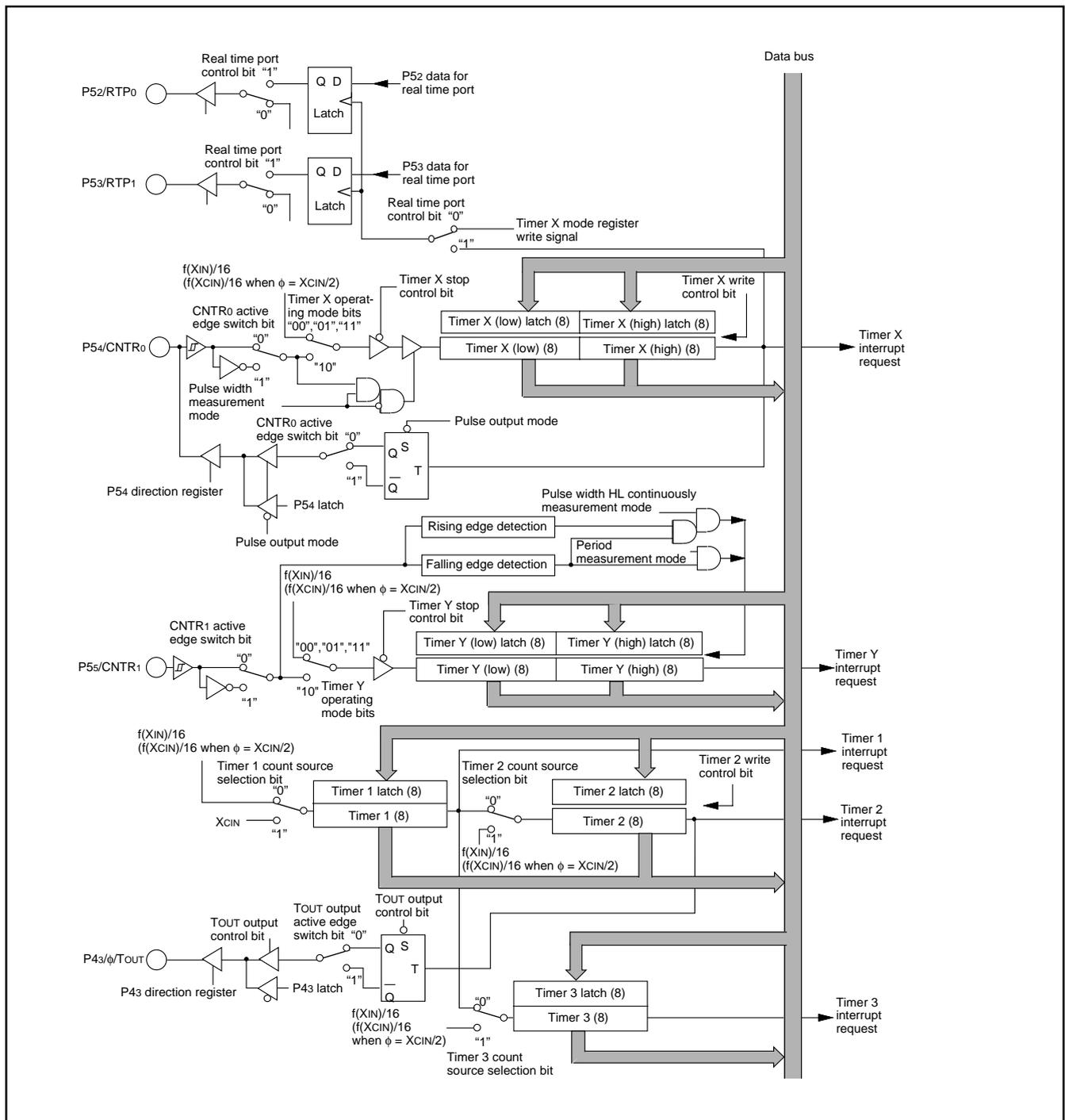


Fig. 19 Timer block diagram

## Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

### (1) Timer mode

The timer counts  $f(X_{IN})/16$  (or  $f(X_{CIN})/16$  in low-speed mode).

### (2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

### (3) Event counter mode

The timer counts signals input through the CNTR0 pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

### (4) Pulse width measurement mode

The count source is  $f(X_{IN})/16$  (or  $f(X_{CIN})/16$  in low-speed mode). If CNTR0 active edge switch bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L". When using a timer in this mode, set the corresponding port P54 direction register to input mode.

#### ●Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

#### ●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1" after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.

Before using this function, set the corresponding port direction registers to output mode.

#### ■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

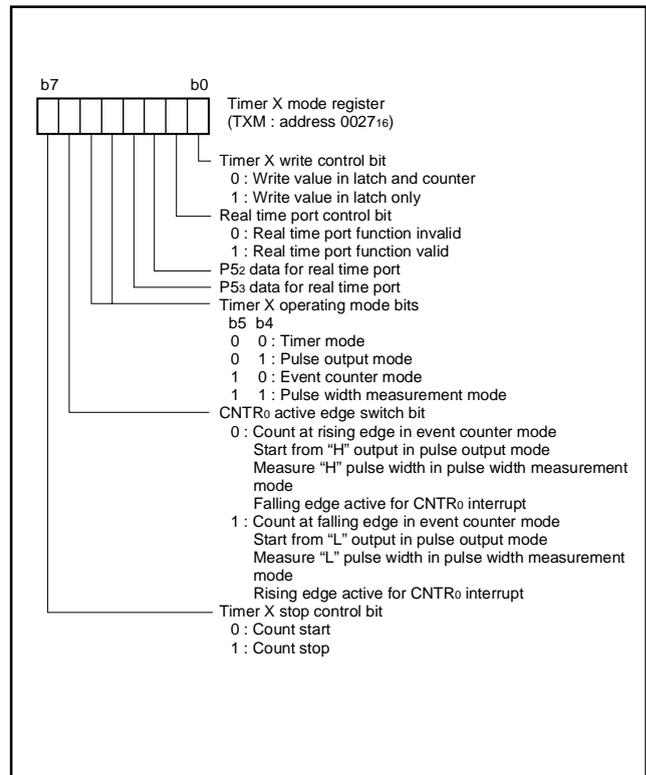


Fig. 20 Structure of timer X mode register

## Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

### (1) Timer mode

The timer counts  $f(X_{IN})/16$  (or  $f(X_{CIN})/16$  in low-speed mode).

### (2) Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

### (3) Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

### (4) Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

### ■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

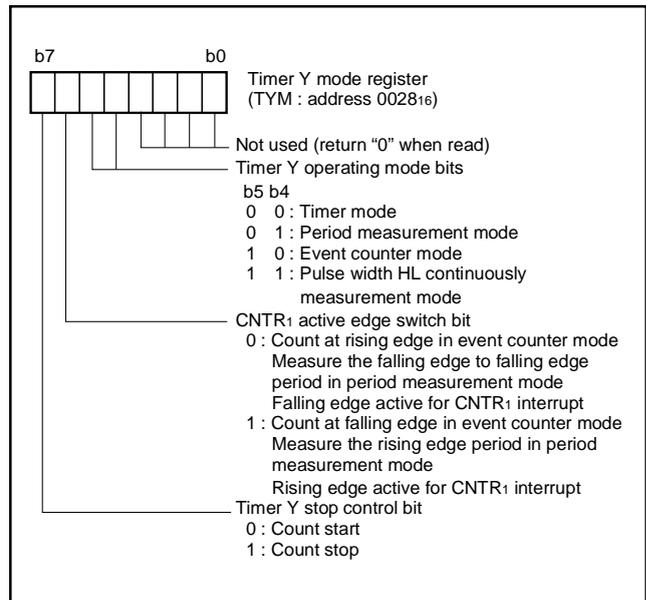


Fig. 21 Structure of timer Y mode register

**Timer 1, Timer 2, Timer 3**

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

**●Timer 2 Write Control**

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

**●Timer 2 Output Control**

When the timer 2 (TOUT) is output enabled, an inversion signal from pin TOUT is output each time timer 2 underflows. In this case, set the port P5<sub>6</sub> shared with the port TOUT to the output mode.

**■Note on Timer 1 to Timer 3**

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output. Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

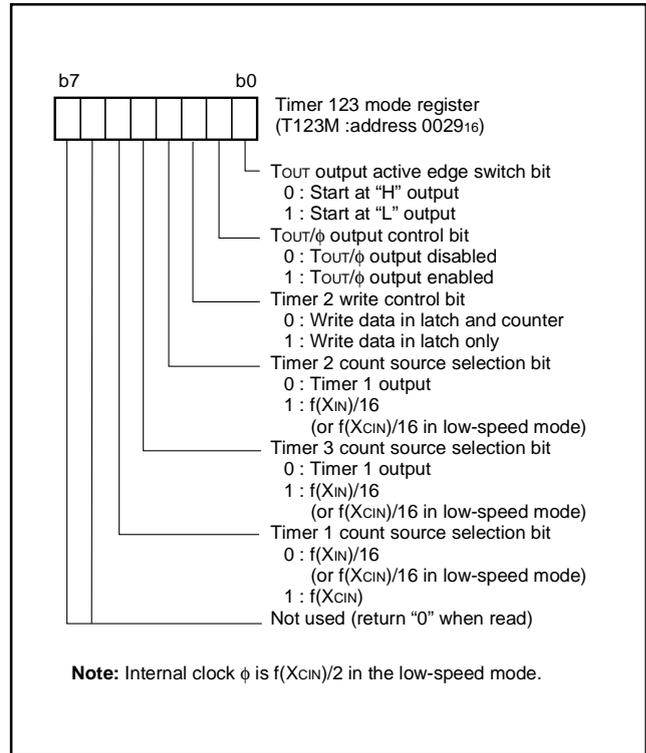


Fig. 22 Structure of timer 123 mode register

**SERIAL I/O  
Serial I/O1**

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

**(1) Clock Synchronous Serial I/O Mode**

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O1 control register to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 001816).

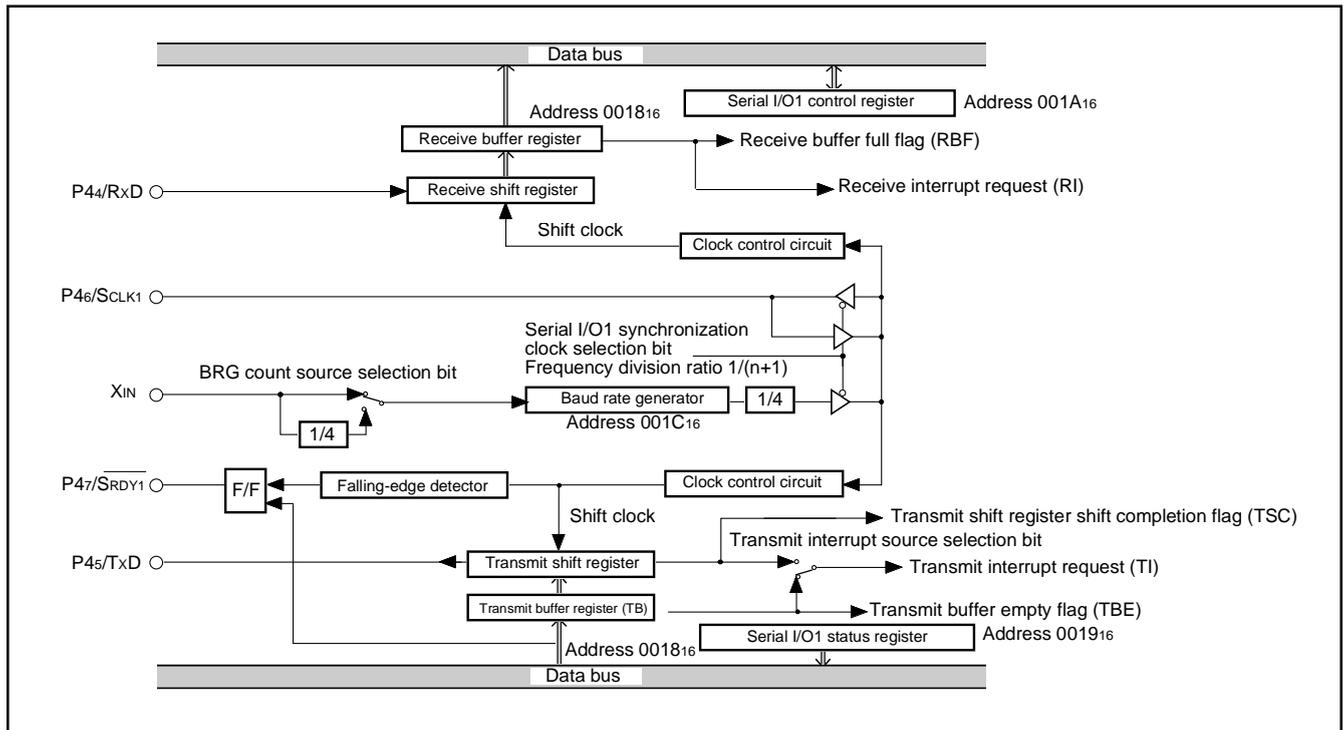


Fig. 23 Block diagram of clock synchronous serial I/O1

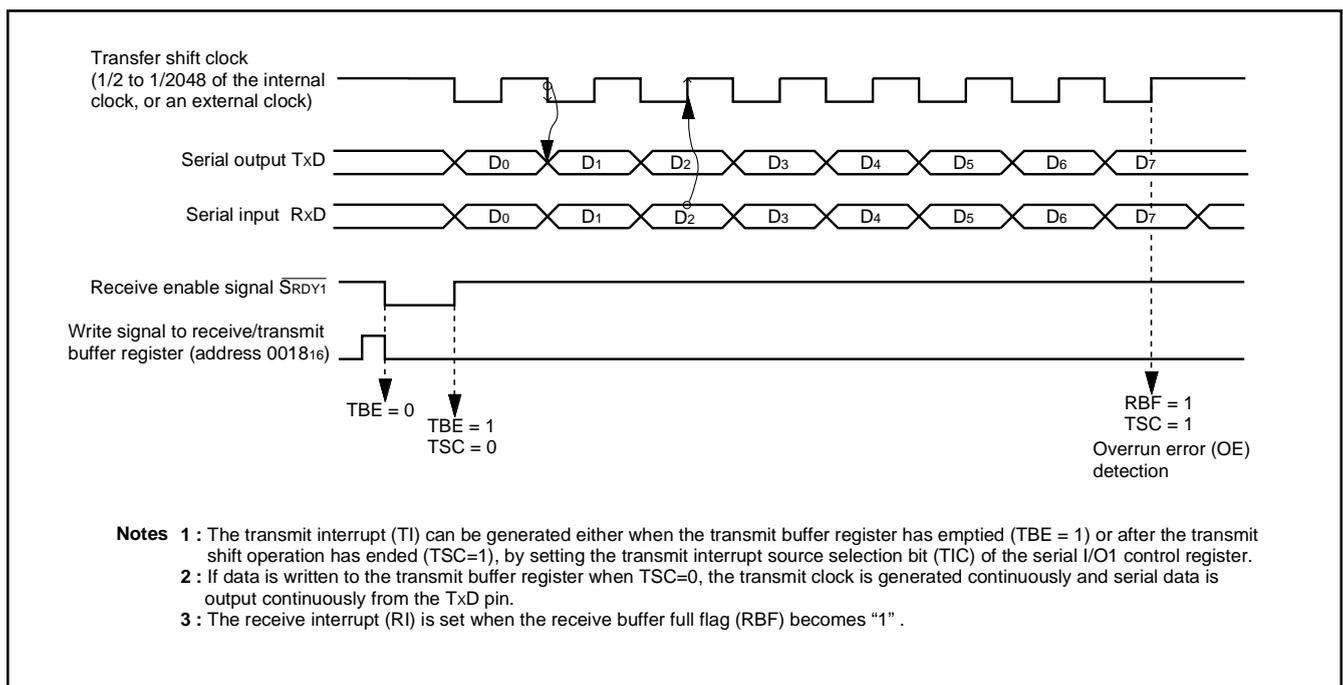


Fig. 24 Operation of clock synchronous serial I/O1 function

**(2) Asynchronous Serial I/O (UART) Mode**

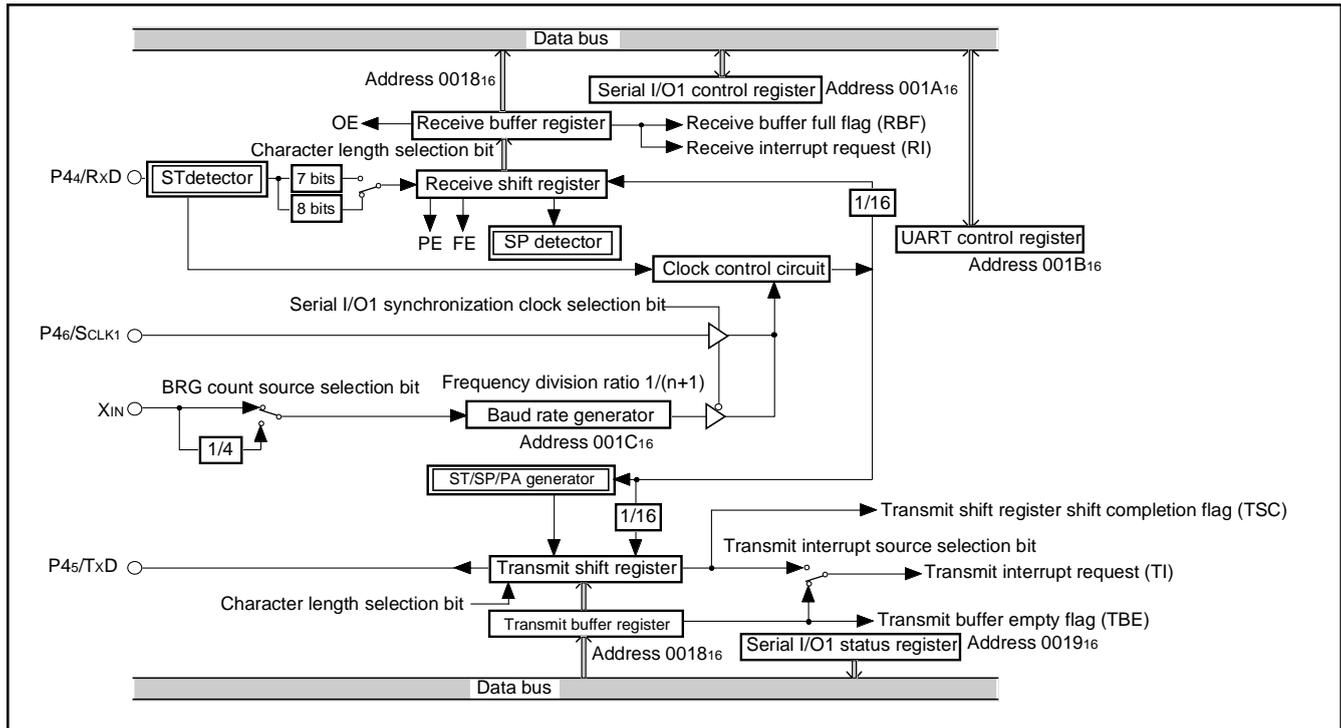
Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

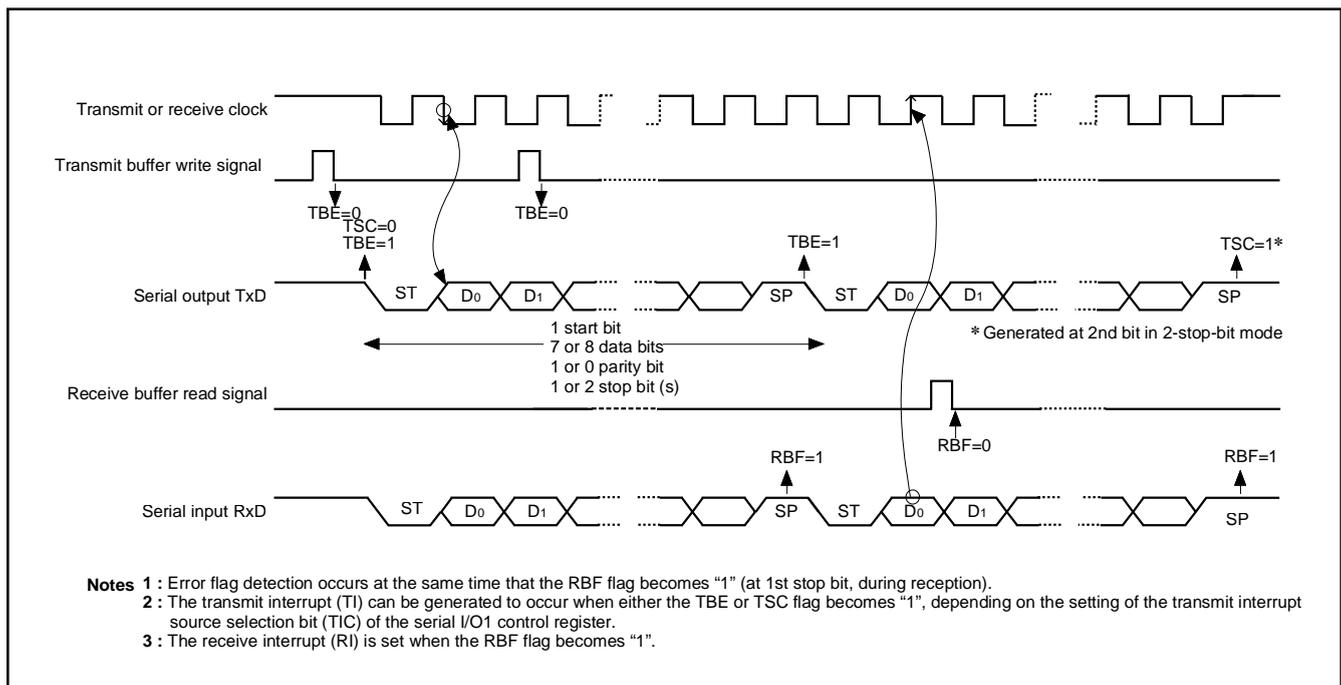
The transmit and receive shift registers each have a buffer regis-

ter, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.



**Fig. 25 Block diagram of UART serial I/O1**



- Notes**
- 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
  - 2 : The transmit interrupt (TI) can be generated to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
  - 3 : The receive interrupt (RI) is set when the RBF flag becomes "1".

**Fig. 26 Operation of UART serial I/O1 function**

**[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018<sub>16</sub>**

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

**[Serial I/O1 Status Register (SIO1STS)] 0019<sub>16</sub>**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the Serial I/O1 Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**[Serial I/O1 Control Register (SIO1CON)] 001A<sub>16</sub>**

The serial I/O1 control register contains eight control bits for the serial I/O1 function.

**[UART Control Register (UARTCON)] 001B<sub>16</sub>**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TXD pin.

**[Baud Rate Generator (BRG)] 001C<sub>16</sub>**

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where n is the value written to the baud rate generator.

**■Notes on serial I/O**

When setting the transmit enable bit to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronous with the transmission enabled, take the following sequence.

- ①Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
- ②Set the transmit enable bit to "1".
- ③Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

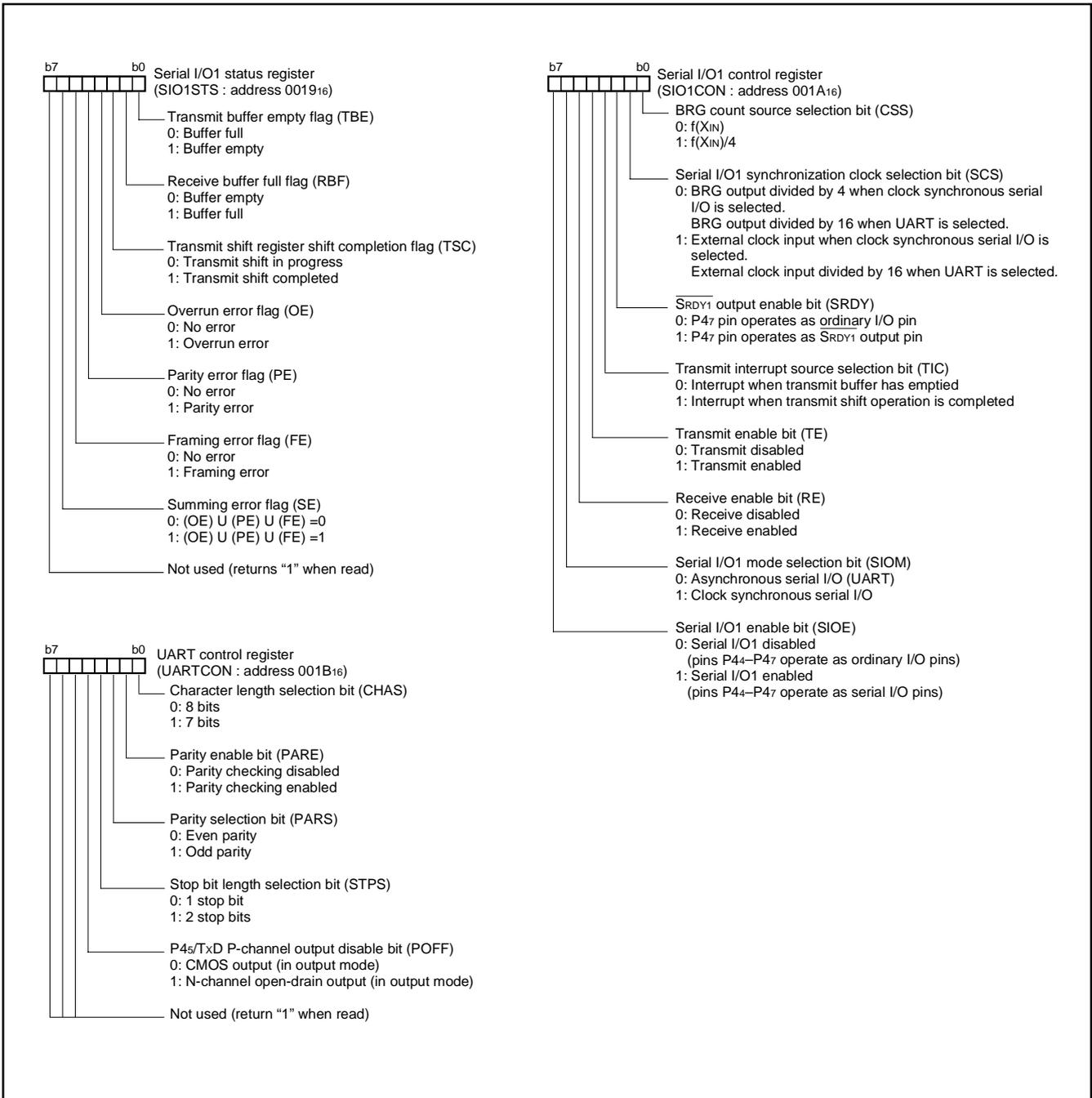


Fig. 27 Structure of serial I/O1 control registers

**Serial I/O2**

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

When an internal clock is selected as the synchronous clock of the serial I/O2, either P62 or P63 can be selected as an output pin of the synchronous clock. In this case, the pin that is not selected as an output pin of the synchronous clock functions as a port.

**[Serial I/O2 Control Register (SIO2CON)] 001D16**

The serial I/O2 control register contains 8 bits which control various serial I/O2 functions.

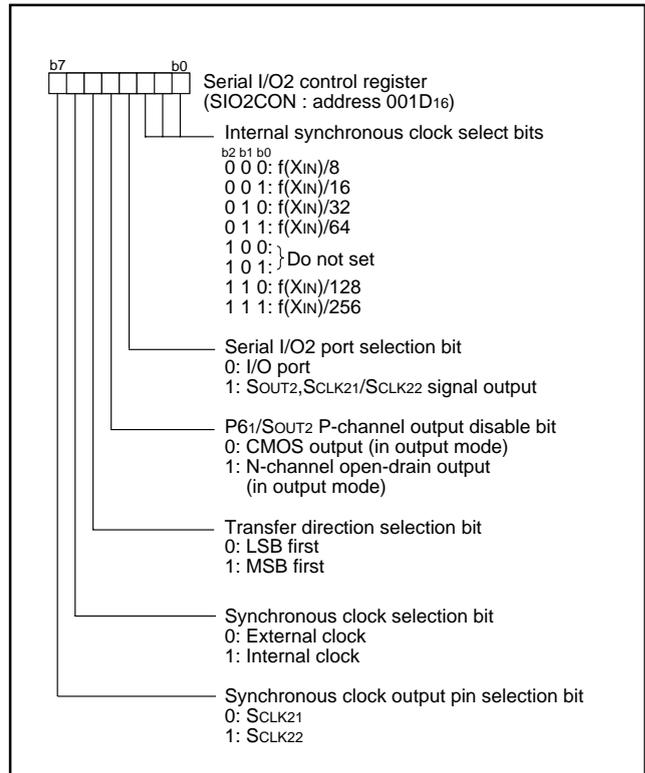


Fig. 28 Structure of serial I/O2 control register

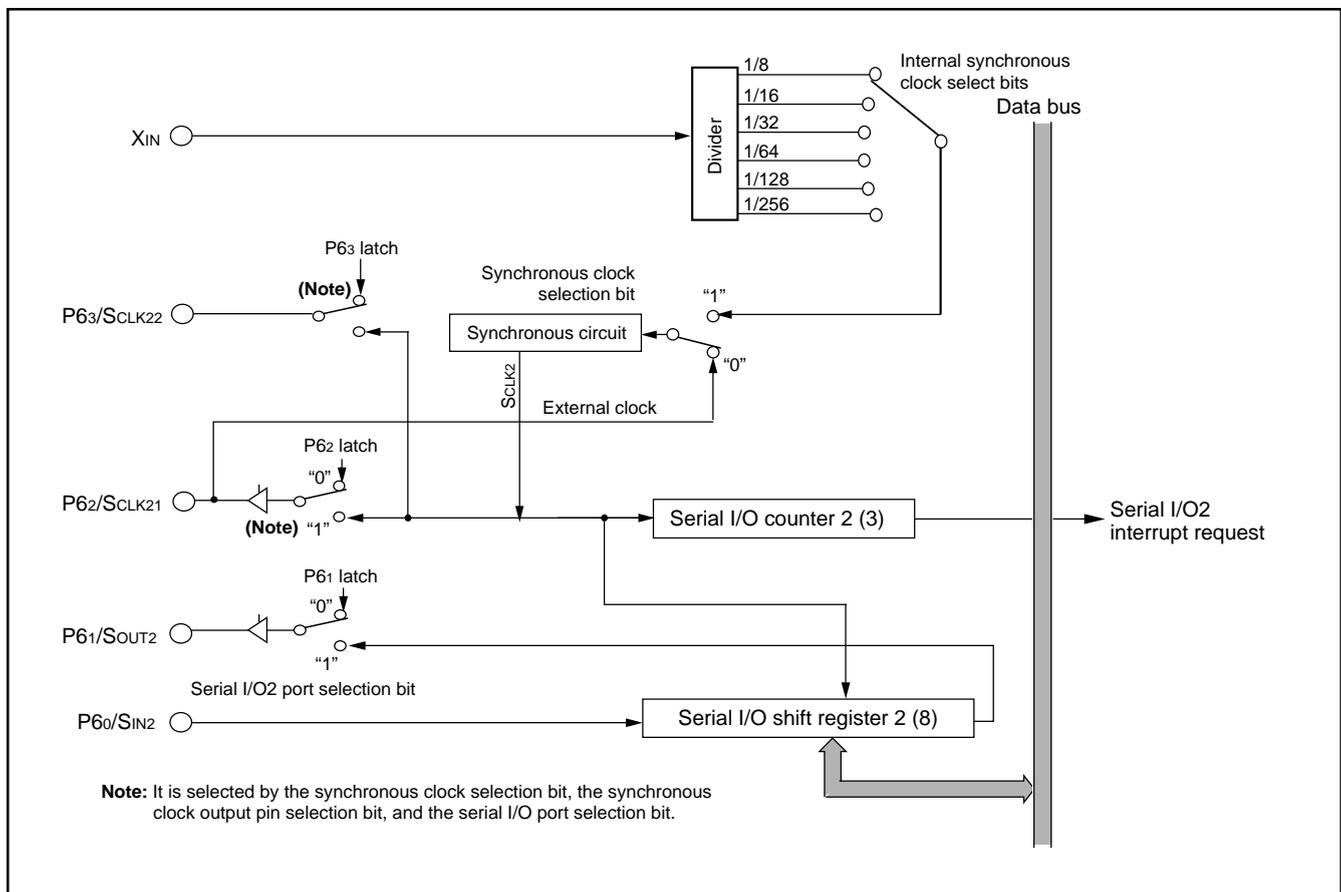


Fig. 29 Block diagram of serial I/O2 function

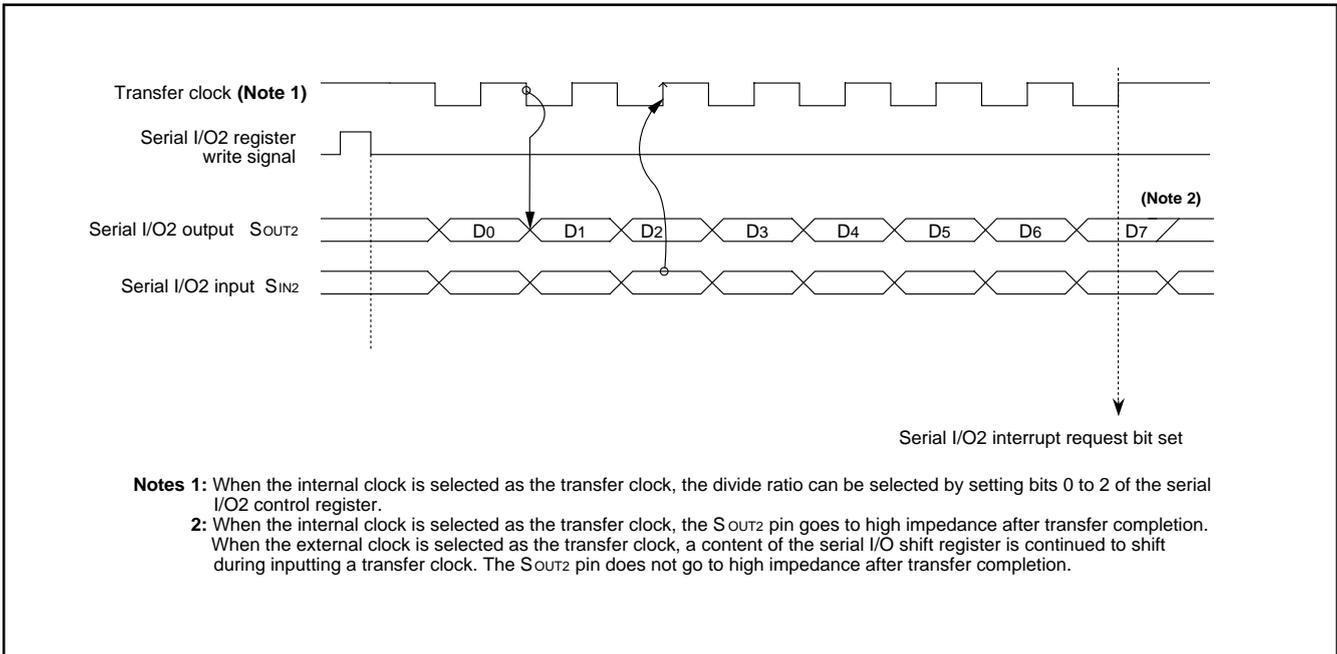


Fig. 30 Timing of serial I/O2 function

**PULSE WIDTH MODULATION (PWM)**

The 7560 group has a PWM function with an 8-bit resolution, based on a signal that is the clock input X<sub>IN</sub> or that clock input divided by 2.

**Data Setting**

The PWM output pin also functions as ports P50 and P51. Set the PWM period by the PWM prescaler, and set the period during which the output pulse is an "H" by the PWM register.

If PWM count source is f(X<sub>IN</sub>) and the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1)/f(X_{IN}) \\ &= 31.875 \times (n+1) \mu\text{s} \quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" period} &= \text{PWM period} \times m/255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

**PWM Operation**

When at least either bit 1 (PWM<sub>0</sub> function enable bit) or bit 2 (PWM<sub>1</sub> function enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H". When one PWM output is enabled and that the other PWM output is enabled, PWM output which is enabled to output later starts pulse output from halfway. When the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

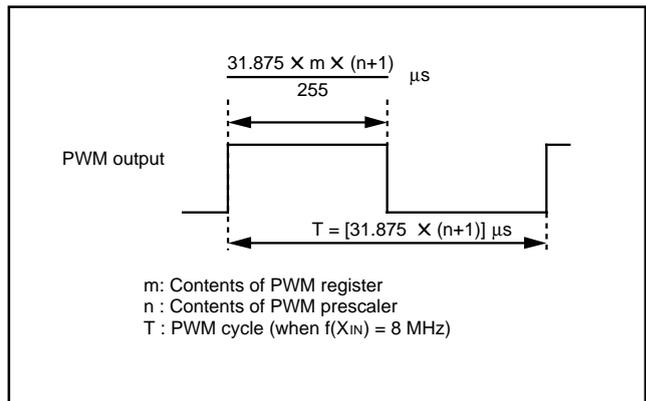


Fig. 31 Timing of PWM cycle

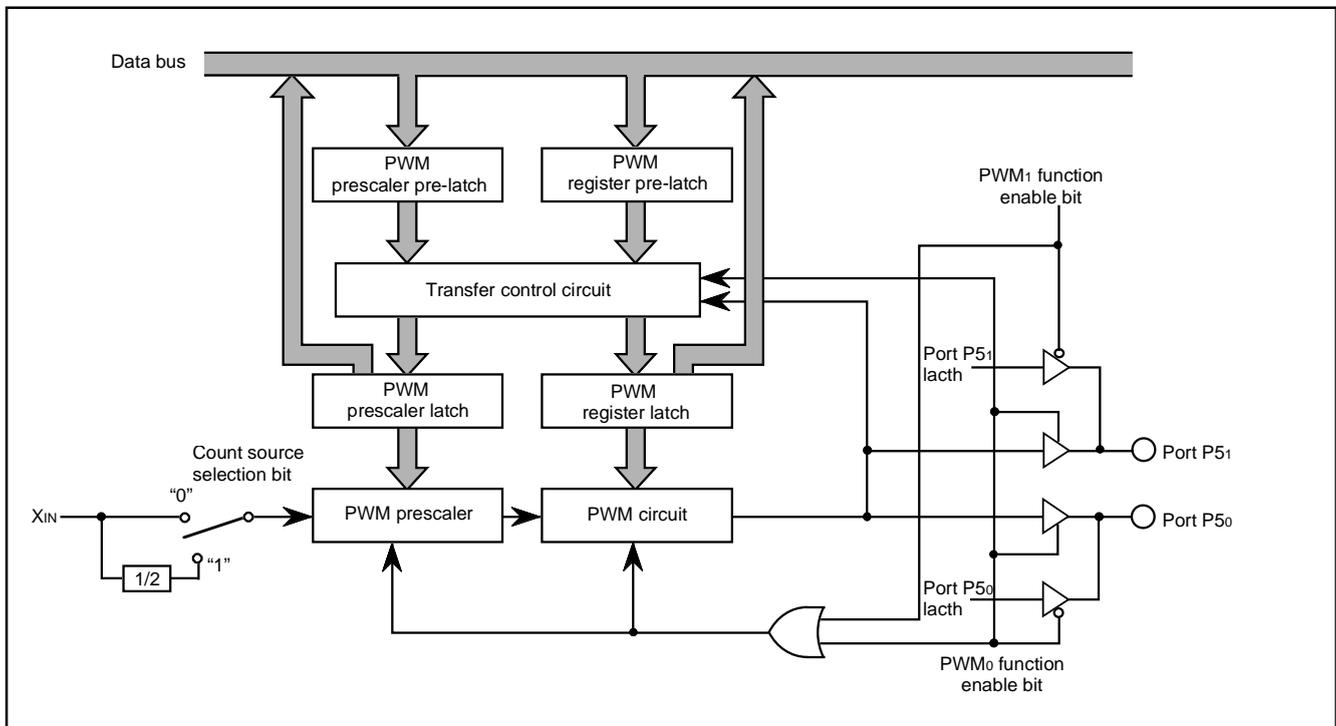


Fig. 32 Block diagram of PWM function

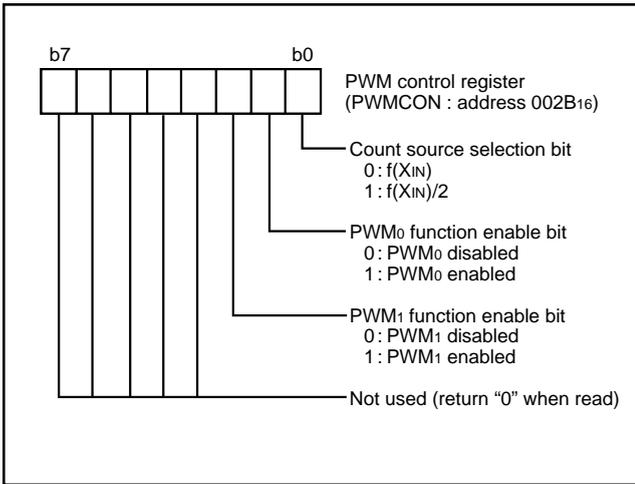


Fig. 33 Structure of PWM control register

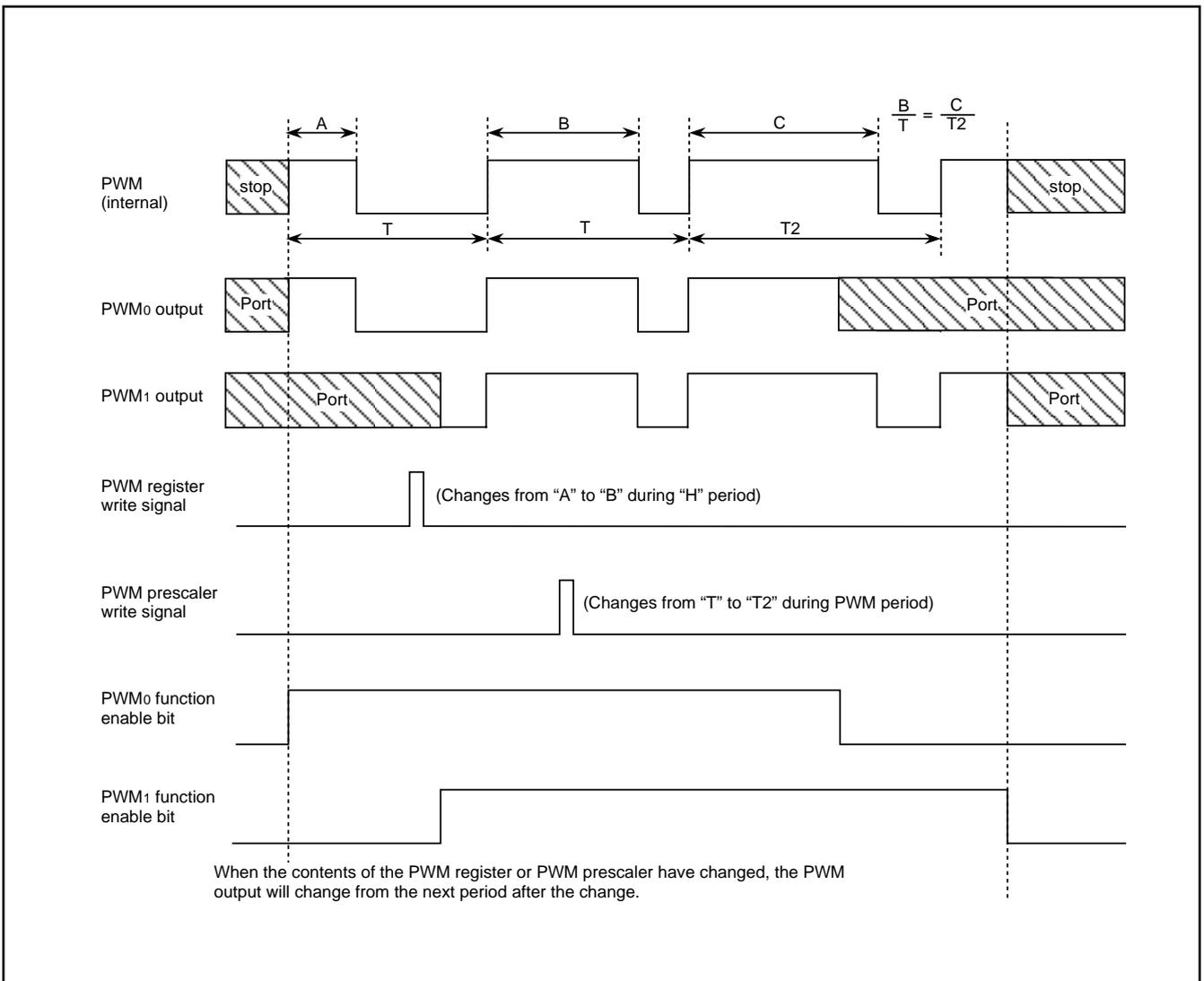


Fig. 34 PWM output timing when PWM register or PWM prescaler is changed

**A-D CONVERTER**

The functional blocks of the A-D converter are described below.

**[A-D Conversion Register (AD)] 003516**

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

**[A-D Control Register (ADCON)] 003416**

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. Bit 4 controls the transistor which breaks the through current of the resistor ladder. When bit 5, which is the AD external trigger valid bit, is set to "1", this bit enables A-D conversion even by a falling edge of an ADT input. Set ports which share with ADT pins to input when using an A-D external trigger.

**Comparison Voltage Generator**

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

**Channel Selector**

The channel selector selects one of the input ports P67/AN7-P60/AN0.

**Comparator and Control Circuit**

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set  $f(X_{IN})$  to at least 500kHz during A-D conversion.

Use the clock divided from the main clock XIN as the internal clock  $\phi$ .

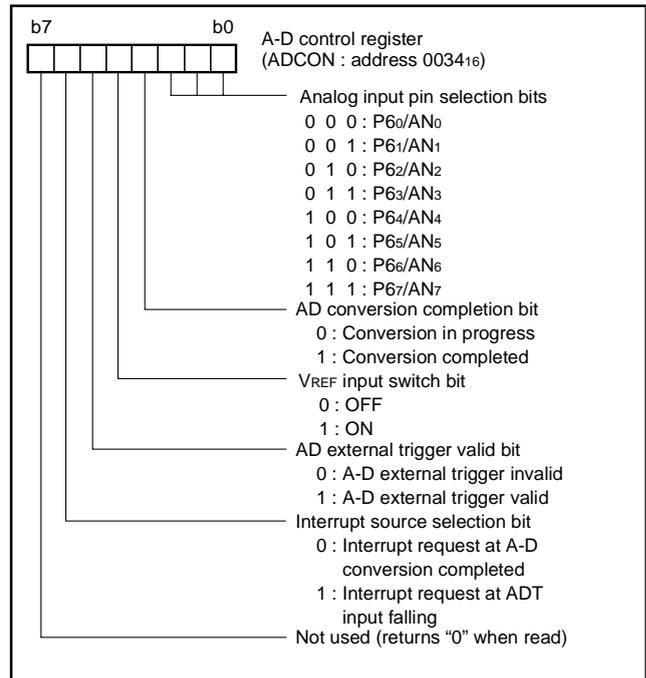


Fig. 35 Structure of A-D control register

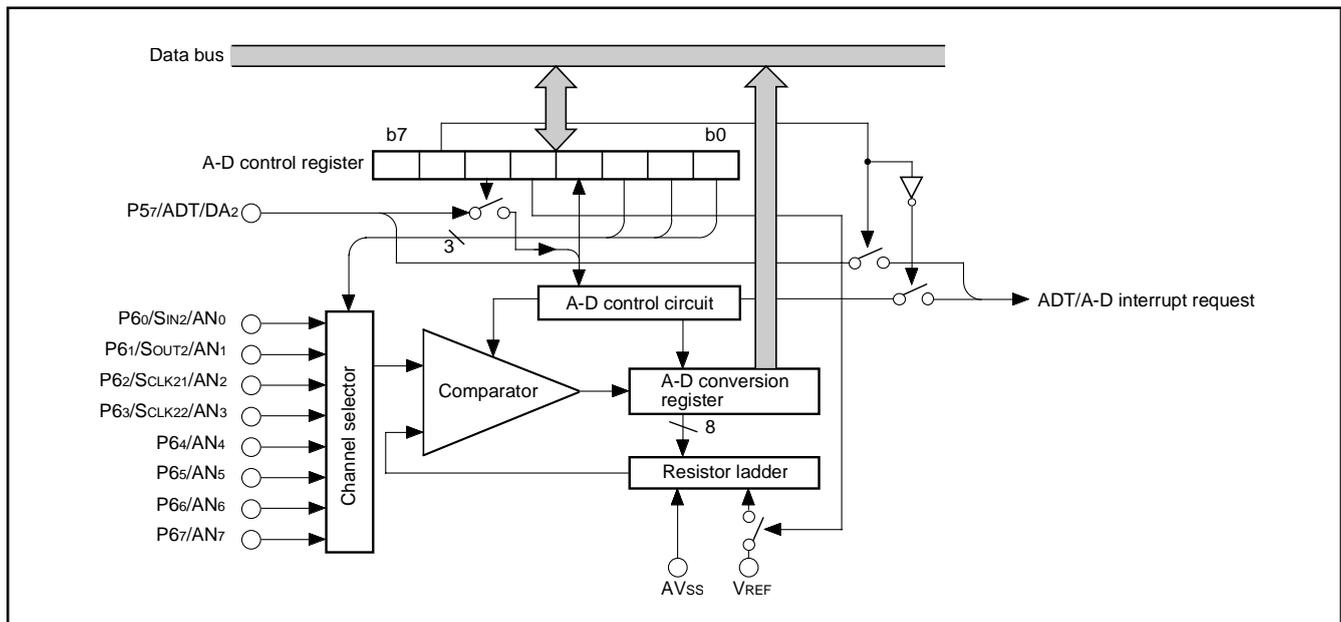


Fig. 36 A-D converter block diagram

**D-A Converter**

The 7560 group has an on-chip D-A converter with 8-bit resolution and 2 channels (DA<sub>i</sub> (i=1, 2)). After the DA<sub>1</sub> selection bit or DA<sub>2</sub> selection bit is set to "0", the D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from DA<sub>i</sub> pin. When using the D-A converter, the corresponding port direction register bit (P56/DA<sub>1</sub>, P57/DA<sub>2</sub>) should be set to "0" (input status) and the pull-up resistor should be in the OFF state.

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n=0 \text{ to } 255)$$

Where V<sub>REF</sub> is the reference voltage.

At reset, the D-A conversion registers are cleared to "0016", the DA<sub>i</sub> output enable bits are cleared to "0", and DA<sub>i</sub> pin goes to high impedance state. The DA output is not buffered, so connect an external buffer when driving a low-impedance load.

■ **Note on applied voltage to VREF pin**

When the P56/DA<sub>1</sub> pin and P57/DA<sub>2</sub> pin are used as I/O ports, be sure to apply V<sub>cc</sub> level to VREF pin.

When these pins are used as D-A conversion output pins, the V<sub>cc</sub> level is recommended for the applied voltage to VREF pin.

When the voltage below V<sub>cc</sub> level is applied, the D-A conversion accuracy may be worse.

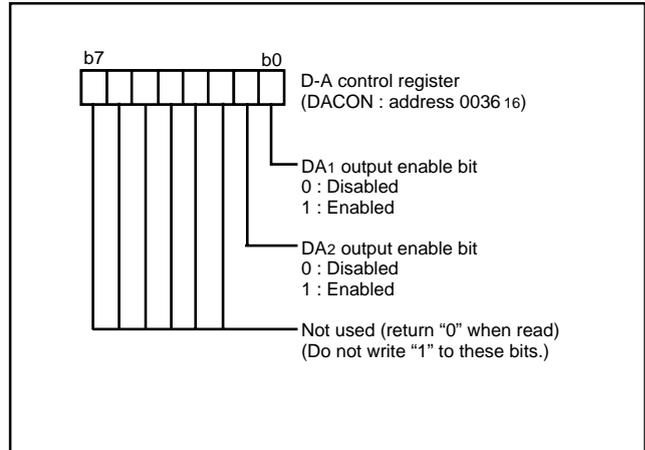


Fig. 37 Structure of D-A control register

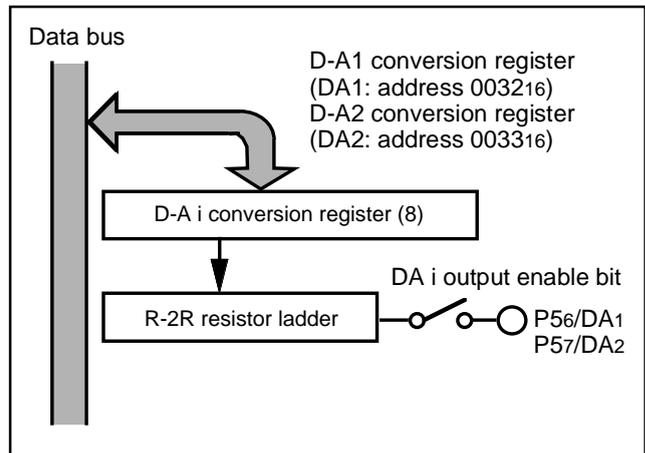


Fig. 38 Block diagram of D-A converter

**LCD DRIVE CONTROL CIRCUIT**

The 7560 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

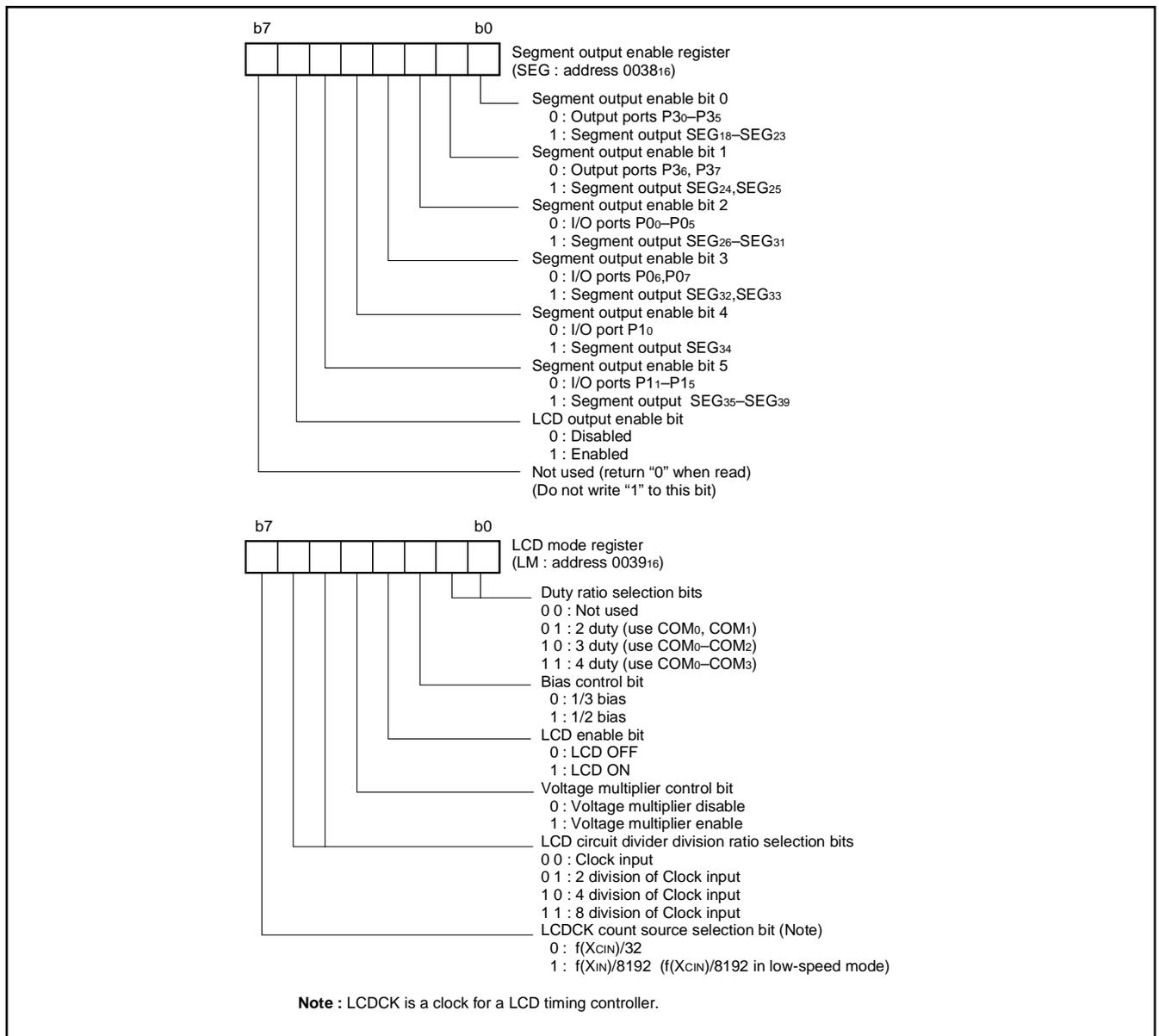
A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD

enable bit is set to "1" after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

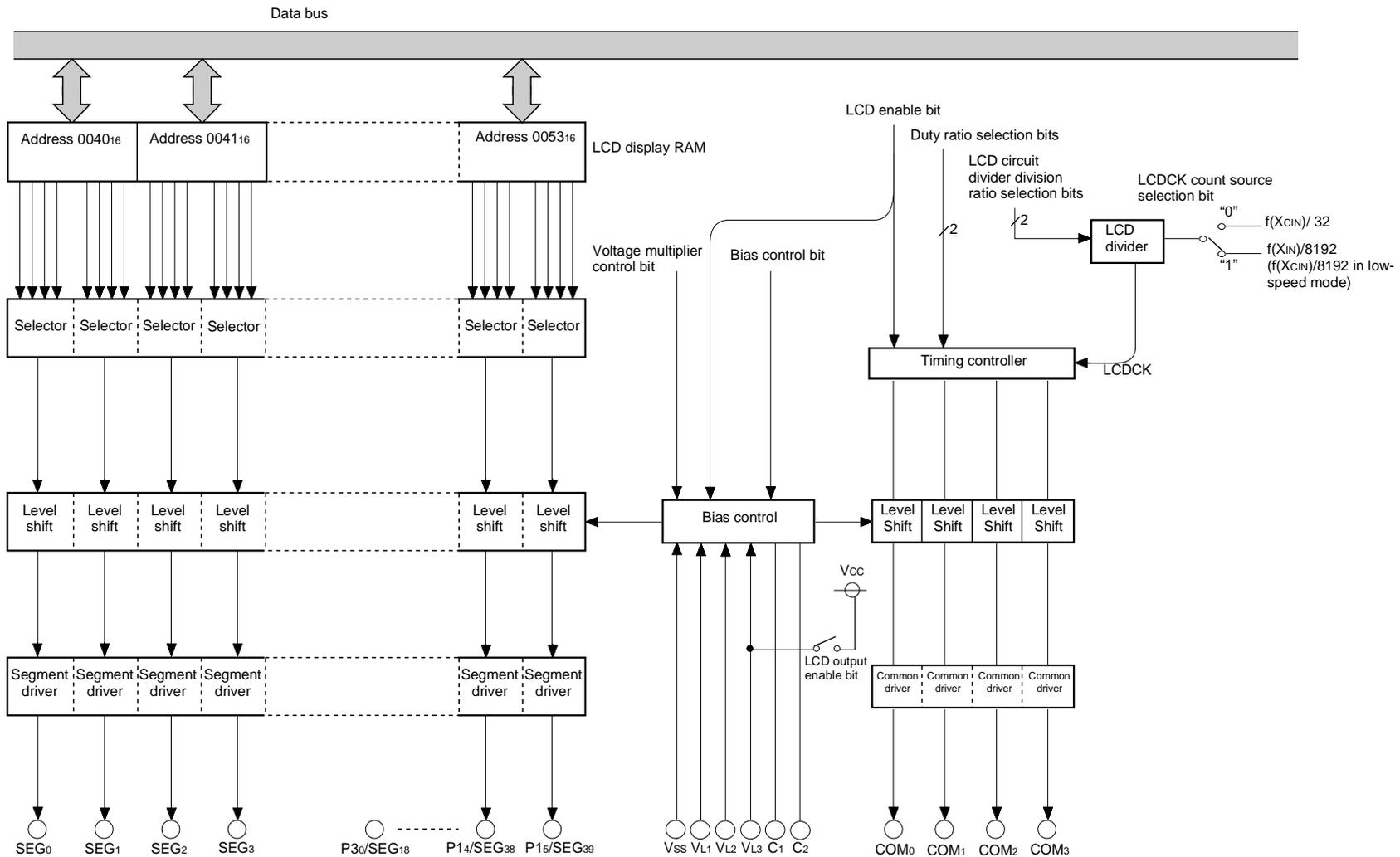
**Table 9. Maximum number of display pixels at each duty ratio**

Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits



**Fig. 39 Structure of segment output enable register and LCD mode register**

Fig. 40 Block diagram of LCD controller/driver



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS  
**7560 Group**

**Voltage Multiplier (3 Times)**

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin VL1. (However, when using a 1/2 bias, connect VL1 and VL2 and apply voltage by external resistor division.)

Set each bit of the segment output enable register and the LCD mode register in the following order for operating the voltage multiplier.

1. Set the segment output enable bits (bits 0 to 5) of the segment output enable register to "0" or "1."
2. Set the duty ratio selection bits (bits 0 and 1), the bias control bit (bit 2), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register to "0" or "1."
3. Set the LCD output enable bit (bit 6) of the segment output enable register to "1."
4. Set the voltage multiplier control bit (bit 4) of the LCD mode register to "1."

When voltage is input to the VL1 pin during operating the voltage multiplier, voltage that is twice as large as VL1 occurs at the VL2 pin, and voltage that is three times as large as VL1 occurs at the VL3 pin.

When using the voltage multiplier, apply  $1.3\text{ V} \leq \text{Voltage} \leq 2.1\text{ V}$  to the VL1 pin.

When not using the voltage multiplier, apply proper voltage to the LCD power input pins (VL1-VL3). Then set the LCD output enable bit to "1."

When the LCD output enable bit is set to "0," the VCC voltage is applied to the VL3 pin inside of this microcomputer.

The voltage multiplier control bit (bit 4 of the LCD mode register) controls the voltage multiplier.

**Bias Control and Applied Voltage to LCD Power Input Pins**

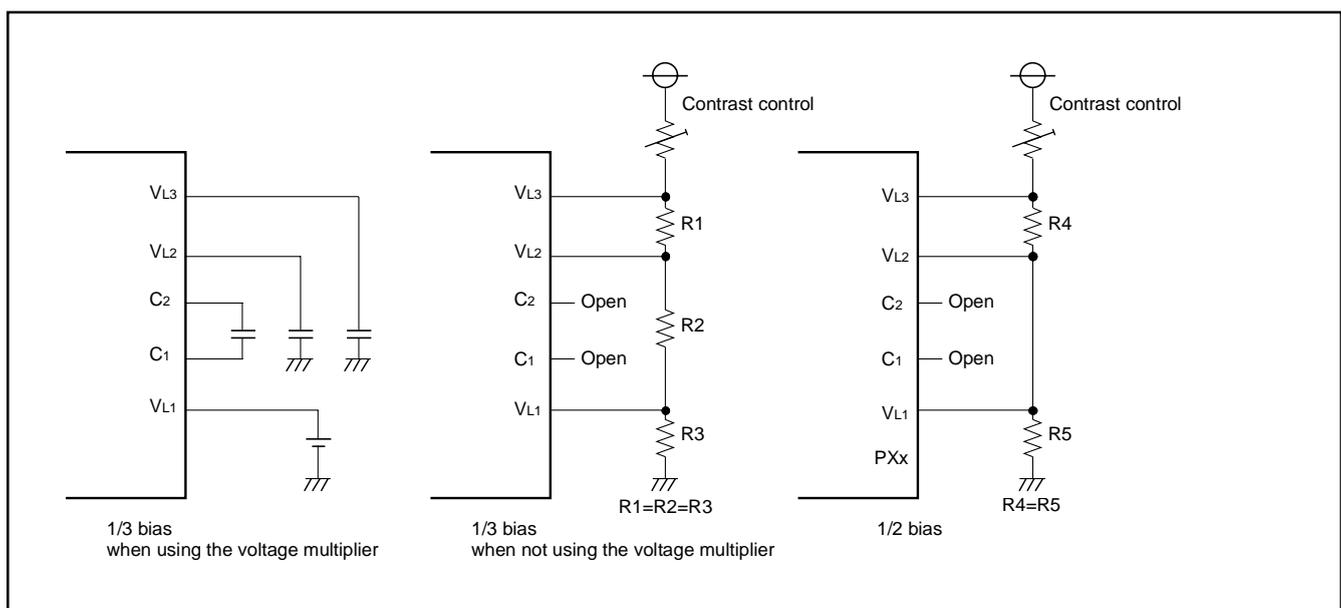
To the LCD power input pins (VL1-VL3), apply the voltage shown in Table 10 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

**Table 10. Bias control and applied voltage to VL1-VL3**

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD

**Note :** VLCD is the maximum value of supplied voltage for the LCD panel.



**Fig. 41 Example of circuit at each bias**

**Common Pin and Duty Ratio Control**

The common pins (COM0–COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

When releasing from reset, the VCC (VL3) voltage is output from the common pins.

**Table 11. Duty ratio control and common pins used**

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
2	0	1	COM0, COM1 (Note 1)
3	1	0	COM0–COM2 (Note 2)
4	1	1	COM0–COM3

**Notes 1:** COM2 and COM3 are open.  
**2:** COM3 is open.

**Segment Signal Output Pin**

Segment signal output pins are classified into the segment-only pins (SEG0–SEG17), the segment/output port pins (SEG18–SEG25), and the segment/I/O port pins (SEG26–SEG39).

Segment signals are output according to the bit data of the LCD RAM corresponding to the duty ratio. After reset release, a VCC (=VL3) voltage is output to the segment-only pins and the segment/output port pins are the high impedance condition and pulled up to VCC (=VL3) voltage.

Also, the segment/I/O port pins (SEG26–SEG39) are set to input ports, and VCC (=VL3) is applied to them by pull-up resistor.

**LCD Display RAM**

Address 0040<sub>16</sub> to 0053<sub>16</sub> is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

**LCD Drive Timing**

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

Address	Bit							
	7	6	5	4	3	2	1	0
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
0040 <sub>16</sub>			SEG1					SEG0
0041 <sub>16</sub>			SEG3					SEG2
0042 <sub>16</sub>			SEG5					SEG4
0043 <sub>16</sub>			SEG7					SEG6
0044 <sub>16</sub>			SEG9					SEG8
0045 <sub>16</sub>			SEG11					SEG10
0046 <sub>16</sub>			SEG13					SEG12
0047 <sub>16</sub>			SEG15					SEG14
0048 <sub>16</sub>			SEG17					SEG16
0049 <sub>16</sub>			SEG19					SEG18
004A <sub>16</sub>			SEG21					SEG20
004B <sub>16</sub>			SEG23					SEG22
004C <sub>16</sub>			SEG25					SEG24
004D <sub>16</sub>			SEG27					SEG26
004E <sub>16</sub>			SEG29					SEG28
004F <sub>16</sub>			SEG31					SEG30
0050 <sub>16</sub>			SEG33					SEG32
0051 <sub>16</sub>			SEG35					SEG34
0052 <sub>16</sub>			SEG37					SEG36
0053 <sub>16</sub>			SEG39					SEG38

**Fig. 42 LCD display RAM map**

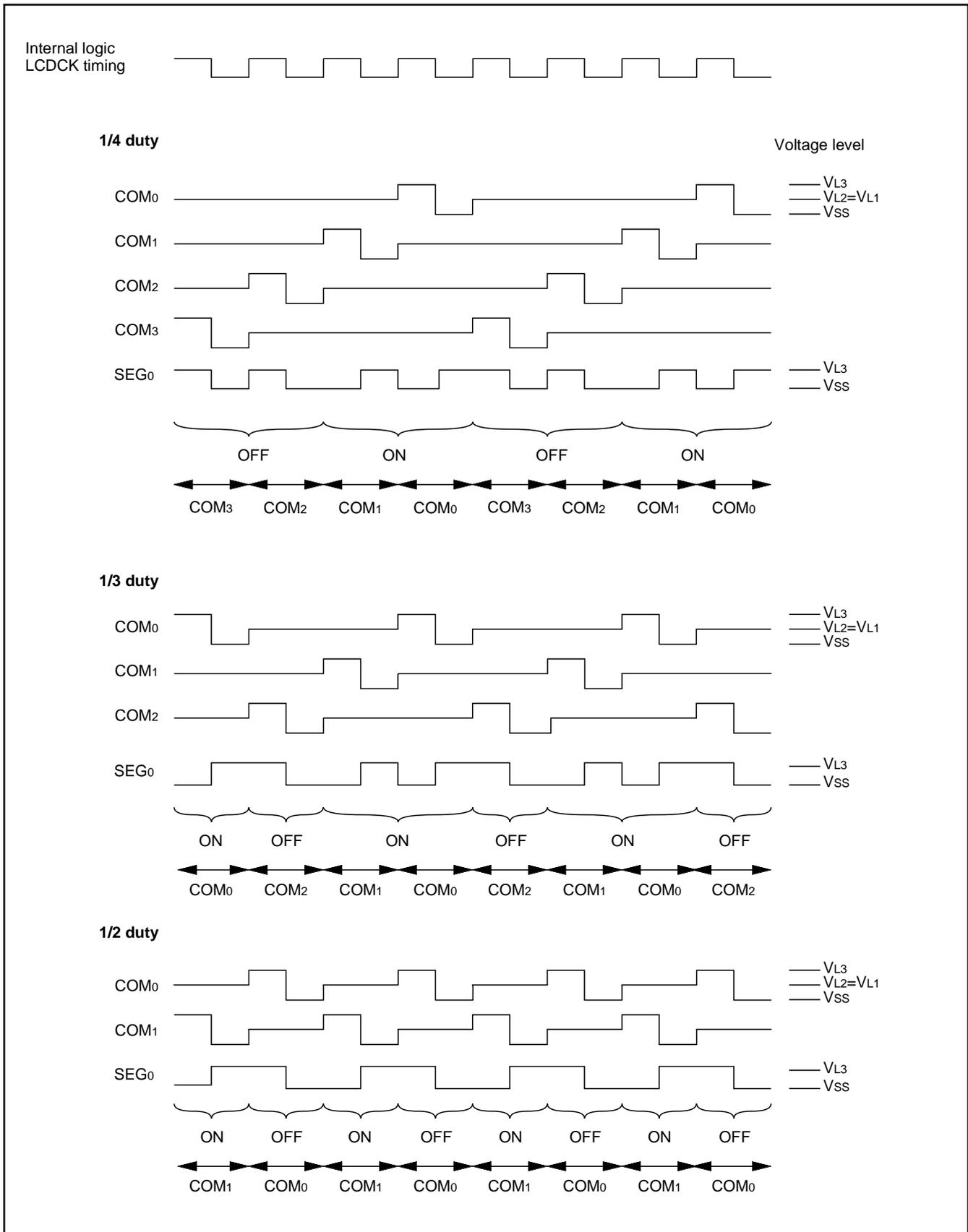


Fig. 43 LCD drive waveform (1/2 bias)

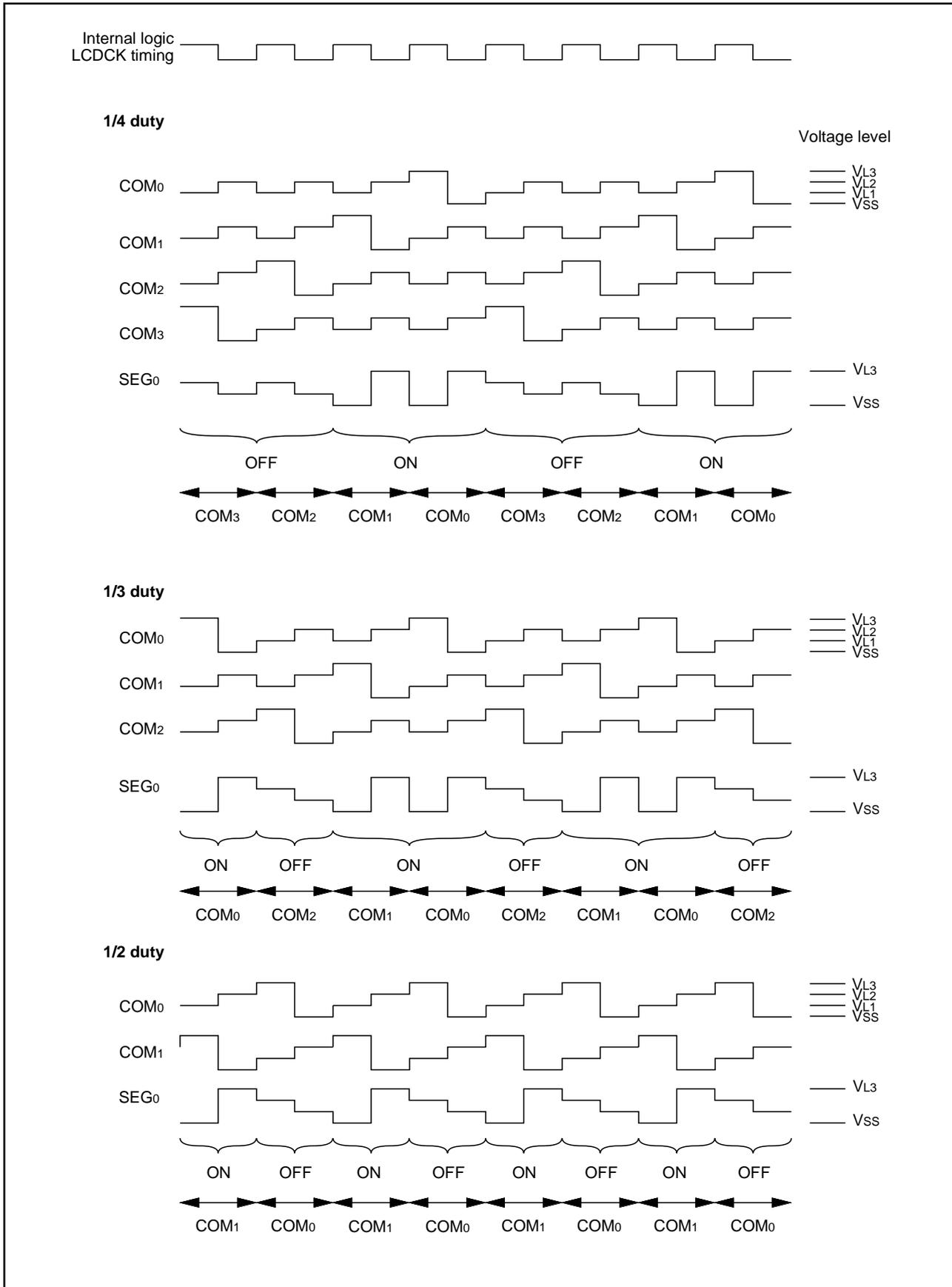


Fig. 44 LCD drive waveform (1/3 bias)

**Watchdog Timer**

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway).

The watchdog timer consists of an 8-bit watchdog timer L and a 6-bit watchdog timer H. At reset or writing to the watchdog timer control register (address 0037<sub>16</sub>), the watchdog timer is set to "3FFF<sub>16</sub>." When any data is not written to the watchdog timer control register (address 0037<sub>16</sub>) after reset, the watchdog timer is in stop state. The watchdog timer starts to count down from "3FFF<sub>16</sub>" by writing an optional value into the watchdog timer control register (address 0037<sub>16</sub>) and an internal reset occurs at an underflow. Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0037<sub>16</sub>) may be started before an underflow. The watchdog timer does not function when an optional value has not been written to the watchdog timer control register (address 0037<sub>16</sub>). When address 0037<sub>16</sub> is read, the following values are read:

- value of high-order 6-bit counter
- value of STP instruction disable bit
- value of count source selection bit.

When bit 6 of the watchdog timer control register (address 0037<sub>16</sub>) is set to "0," the STP instruction is valid. The STP instruction is disabled by rewriting this bit to "1." At this time, if the STP instruction is executed, it is processed as an undefined instruction, so that a reset occurs inside.

This bit cannot be rewritten to "0" by programming. This bit is "0" immediately after reset.

The count source of the watchdog timer becomes the system clock  $\phi$  divided by 8. The detection time in this case is set to 8.19 s at  $f(XCIN) = 32$  kHz and 32.768 ms at  $f(XIN) = 8$  MHz.

However, count source of high-order 6-bit timer can be connected to a signal divided system clock by 8 directly by writing the bit 7 of the watchdog timer control register (address 0037<sub>16</sub>) to "1." The detection time in this case is set to 32 ms at  $f(XCIN) = 32$  kHz and 128  $\mu$ s at  $f(XIN) = 8$  MHz. There is no difference in the detection time between the middle-speed mode and the high-speed mode.

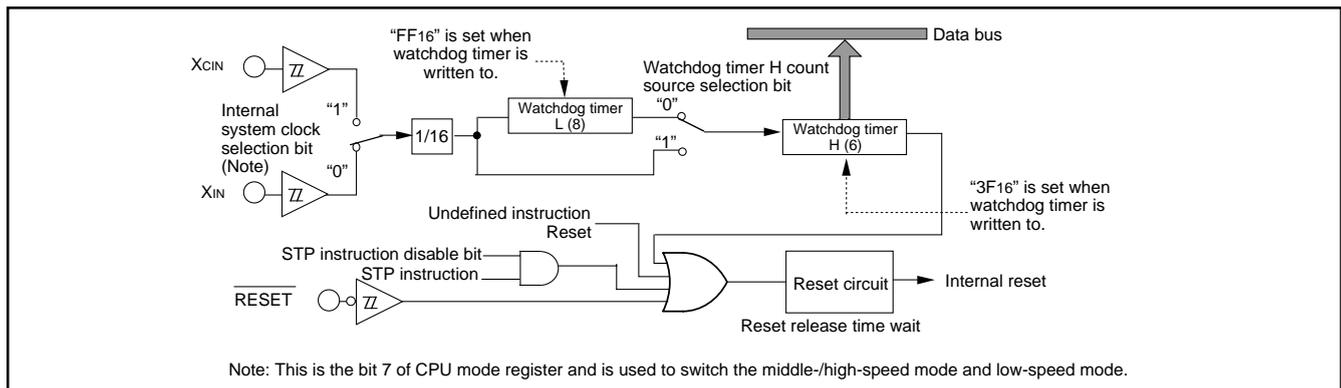


Fig. 45 Block diagram of watchdog timer

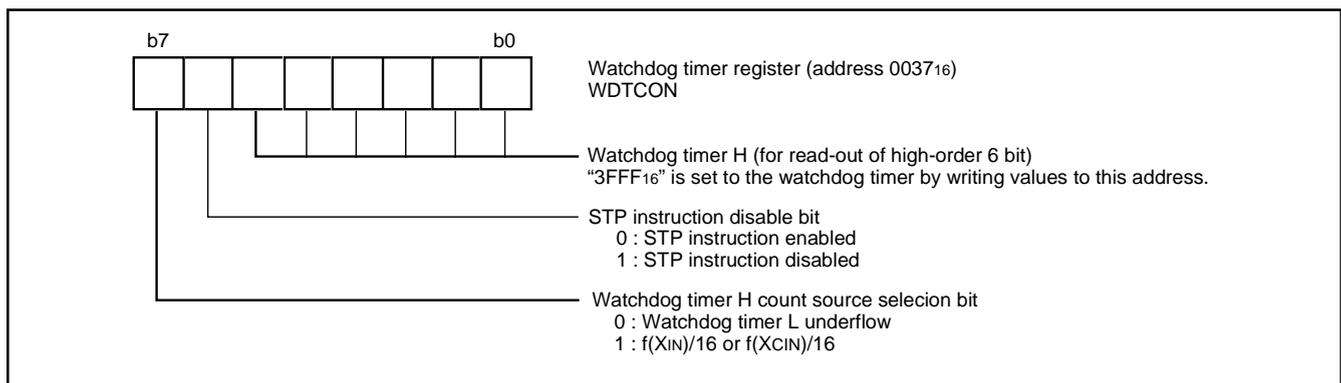


Fig. 46 Structure of watchdog timer control register

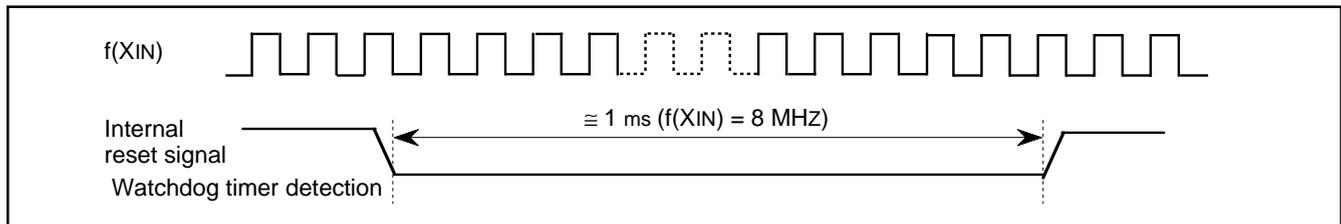


Fig. 47 Timing of reset output

**TOUT/ $\phi$  CLOCK OUTPUT FUNCTION**

The internal system clock  $\phi$  or timer 2 divided by 2 (TOUT output) can be output from port P4<sub>3</sub> by setting the TOUT/ $\phi$  output control bit (bit 1) of the timer 123 mode register and the TOUT/ $\phi$  output control register. Set bit 3 of the port P4 direction register to "1" when outputting the clock.

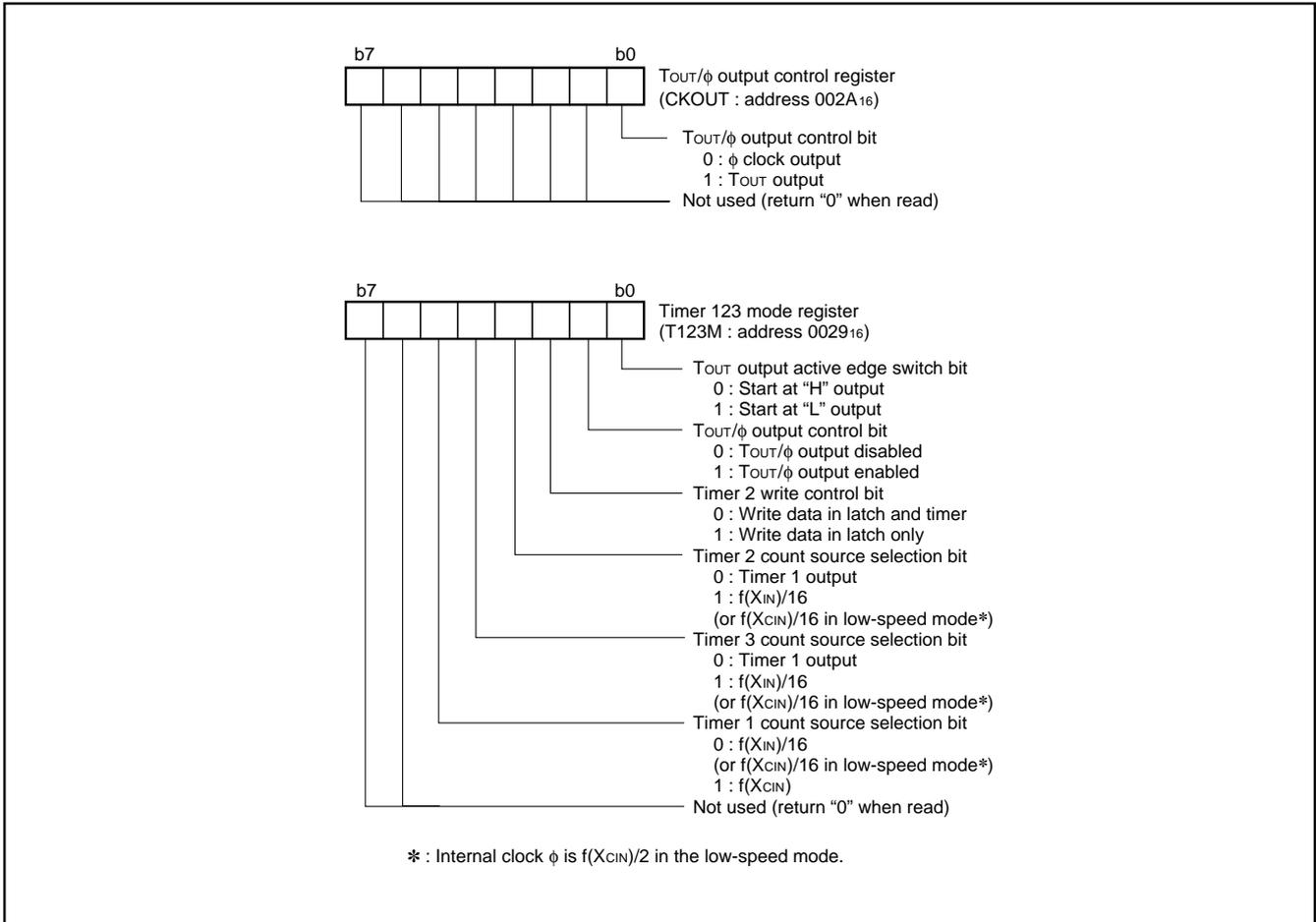


Fig. 48 Structure of TOUT/ $\phi$  output-related register

**RESET CIRCUIT**

To reset the microcomputer,  $\overline{\text{RESET}}$  pin should be held at an "L" level for 2  $\mu\text{s}$  or more. Then the  $\overline{\text{RESET}}$  pin is returned to an "H" level (the power source voltage should be between  $V_{CC}(\text{min.})$  and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (high-order byte) and address  $\text{FFFC}_{16}$  (low-order byte). Make sure that the reset input voltage is less than 0.2  $V_{CC}$  for  $V_{CC}$  of  $V_{CC}(\text{min.})$ .

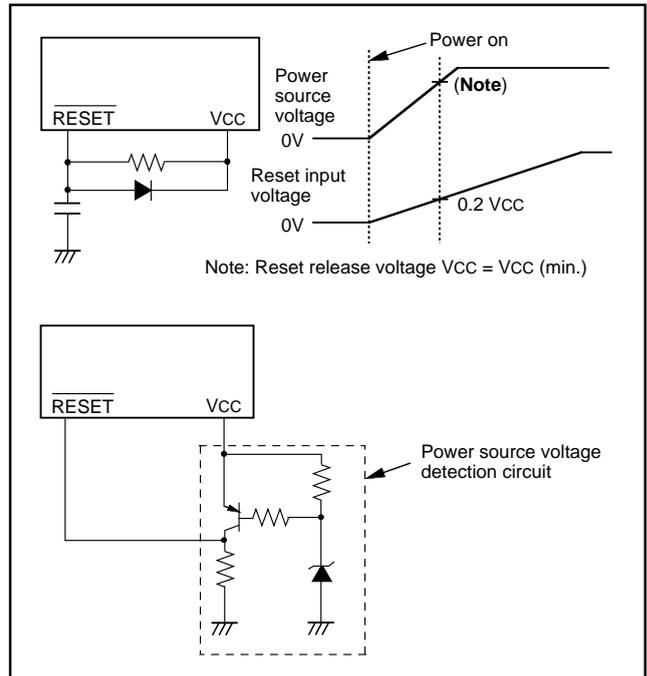


Fig. 49 Example of reset circuit

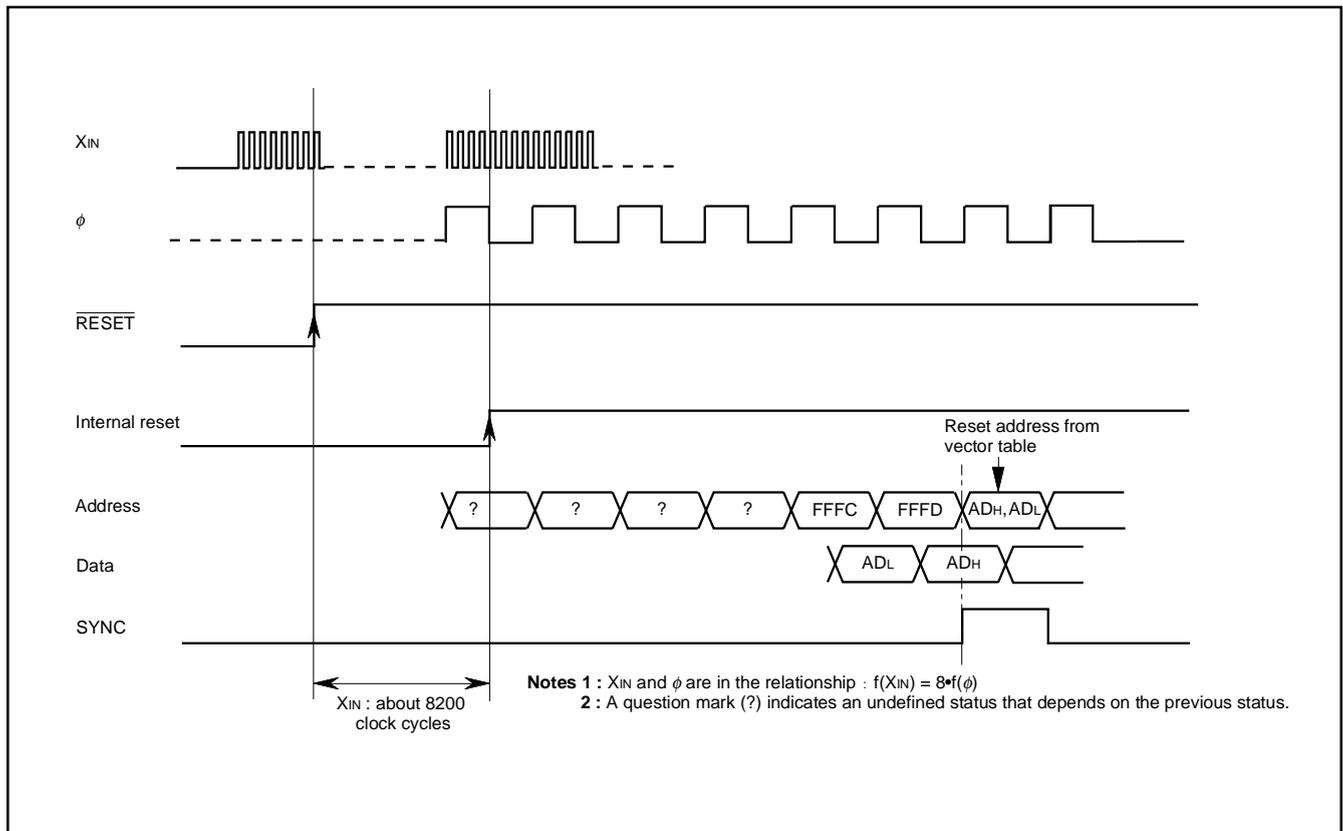


Fig. 50 Reset Sequence

	Address	Register contents
(1) Port P0 direction register	0001 <sub>16</sub>	00 <sub>16</sub>
(2) Port P1 direction register	0003 <sub>16</sub>	00 <sub>16</sub>
(3) Port P2 direction register	0005 <sub>16</sub>	00 <sub>16</sub>
(4) Port P3 output control register	0007 <sub>16</sub>	00 <sub>16</sub>
(5) Port P4 direction register	0009 <sub>16</sub>	00 <sub>16</sub>
(6) Port P5 direction register	000B <sub>16</sub>	00 <sub>16</sub>
(7) Port P6 direction register	000D <sub>16</sub>	00 <sub>16</sub>
(8) Port P7 direction register	000F <sub>16</sub>	00 <sub>16</sub>
(9) Key input control register	0015 <sub>16</sub>	00 <sub>16</sub>
(10) PULL register A	0016 <sub>16</sub>	3F <sub>16</sub>
(11) PULL register B	0017 <sub>16</sub>	00 <sub>16</sub>
(12) Serial I/O1 status register	0019 <sub>16</sub>	1 0 0 0 0 0 0 0
(13) Serial I/O1 control register	001A <sub>16</sub>	00 <sub>16</sub>
(14) UART control register	001B <sub>16</sub>	1 1 1 0 0 0 0 0
(15) Serial I/O2 control register	001D <sub>16</sub>	00 <sub>16</sub>
(16) Timer X (low)	0020 <sub>16</sub>	FF <sub>16</sub>
(17) Timer X (high)	0021 <sub>16</sub>	FF <sub>16</sub>
(18) Timer Y (low)	0022 <sub>16</sub>	FF <sub>16</sub>
(19) Timer Y (high)	0023 <sub>16</sub>	FF <sub>16</sub>
(20) Timer 1	0024 <sub>16</sub>	FF <sub>16</sub>
(21) Timer 2	0025 <sub>16</sub>	01 <sub>16</sub>
(22) Timer 3	0026 <sub>16</sub>	FF <sub>16</sub>
(23) Timer X mode register	0027 <sub>16</sub>	00 <sub>16</sub>
(24) Timer Y mode register	0028 <sub>16</sub>	00 <sub>16</sub>
(25) Timer 123 mode register	0029 <sub>16</sub>	00 <sub>16</sub>
(26) T <sub>OUT</sub> /φ output control register	002A <sub>16</sub>	00 <sub>16</sub>
(27) PWM control register	002B <sub>16</sub>	00 <sub>16</sub>
(28) D-A1 conversion register	0032 <sub>16</sub>	00 <sub>16</sub>
(29) D-A2 conversion register	0033 <sub>16</sub>	00 <sub>16</sub>
(30) A-D control register	0034 <sub>16</sub>	0 0 0 0 1 0 0 0
(31) D-A control register	0036 <sub>16</sub>	00 <sub>16</sub>
(32) Watchdog timer control register	0037 <sub>16</sub>	0 0 1 1 1 1 1 1
(33) Segment output enable register	0038 <sub>16</sub>	00 <sub>16</sub>
(34) LCD mode register	0039 <sub>16</sub>	00 <sub>16</sub>
(35) Interrupt edge selection register	003A <sub>16</sub>	00 <sub>16</sub>
(36) CPU mode register	003B <sub>16</sub>	0 1 0 0 1 0 0 0
(37) Interrupt request register 1	003C <sub>16</sub>	00 <sub>16</sub>
(38) Interrupt request register 2	003D <sub>16</sub>	00 <sub>16</sub>
(39) Interrupt control register 1	003E <sub>16</sub>	00 <sub>16</sub>
(40) Interrupt control register 2	003F <sub>16</sub>	00 <sub>16</sub>
(41) Processor status register	(PS)	X X X X 1 X X
(42) Program counter	(PC <sub>H</sub> )	Contents of address FFFD <sub>16</sub>
	(PC <sub>L</sub> )	Contents of address FFFC <sub>16</sub>
(43) Watchdog timer (high-order)		3F <sub>16</sub>
(44) Watchdog timer (low-order)		FF <sub>16</sub>

**Note:** The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.  
X : Undefined

Fig. 51 Internal state of microcomputer immediately after reset

**CLOCK GENERATING CIRCUIT**

The 7560 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins go to high-impedance state.

**Frequency Control**

**(1) Middle-speed mode**

The internal clock  $\phi$  is the frequency of XIN divided by 8. After reset, this mode is selected.

**(2) High-speed mode**

The internal clock  $\phi$  is half the frequency of XIN.

**(3) Low-speed mode**

- The internal clock  $\phi$  is half the frequency of XCIN.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1".

When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

**Note:** If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power-on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that  $f(XIN) > 3 \cdot f(XCIN)$ .

**Oscillation Control**

**(1) Stop mode**

If the STP instruction is executed, the internal clock  $\phi$  stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock  $\phi$  is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize when a ceramic resonator is used.

**(2) Wait mode**

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level. The states of XIN and XCIN are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

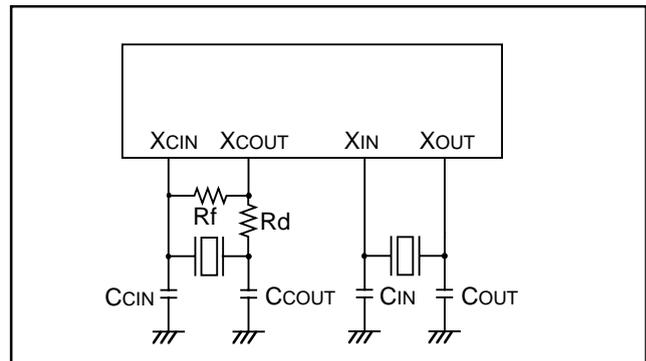


Fig. 52 Ceramic resonator circuit

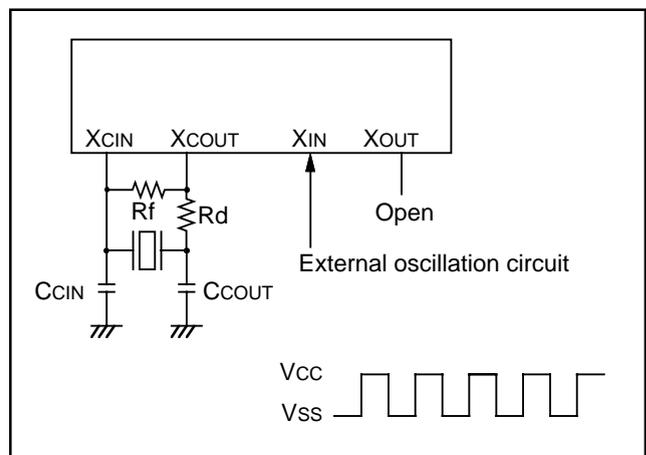


Fig. 53 External clock input circuit

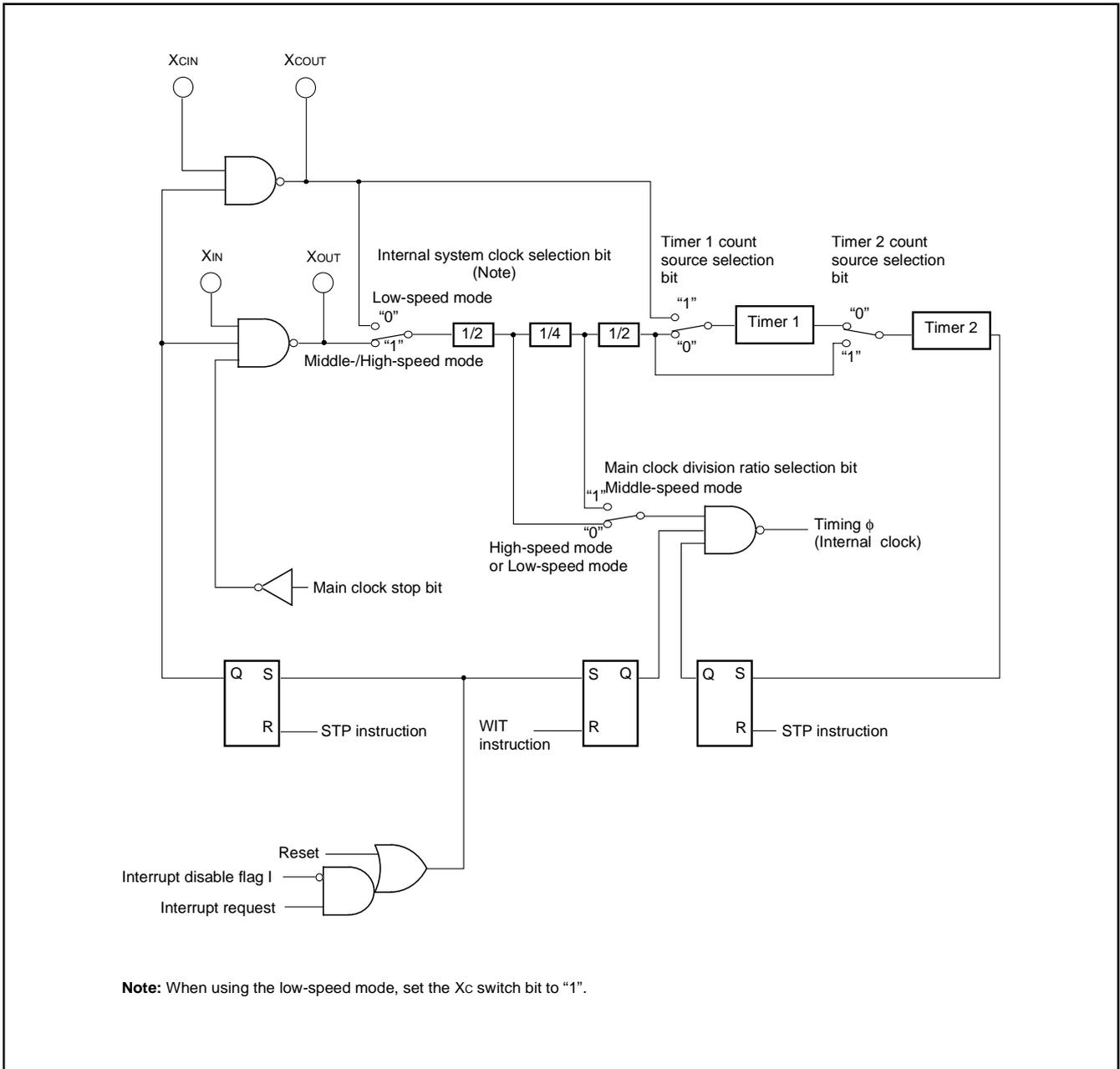


Fig. 54 Clock generating circuit block diagram

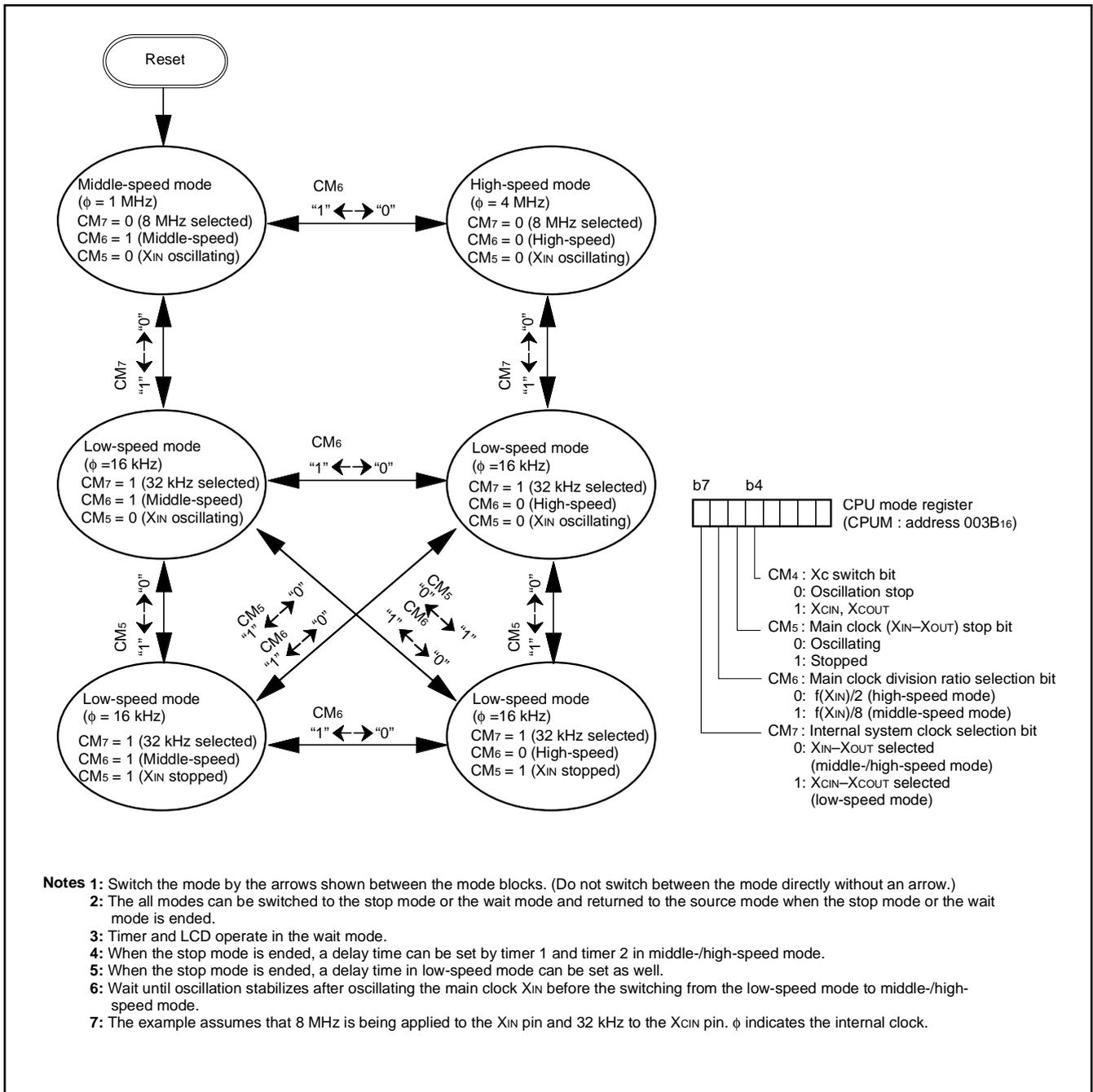


Fig. 55 State transitions of system clock

## NOTES ON PROGRAMMING

### Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.

In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

### Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

### Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

### Timers

If a value  $n$  (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n + 1)$ .

### Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

### Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

### Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the  $\overline{\text{SRDY}}$  signal, set the transmit enable bit, the receive enable bit, and the  $\overline{\text{SRDY}}$  output enable bit to "1".

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed.

In serial I/O2, the SOUT2 pin goes to high impedance state after transmission is completed.

### A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that  $f(\text{XIN})$  is at least 500kHz during an A-D conversion. Do not execute the STP or WIT instruction during an A-D conversion.

### Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock  $\phi$  is half of the XIN frequency.

### DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form\*
- 2.Mark Specification Form\*
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

\*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.mesc.co.jp/indexe.htm>).

**ELECTRICAL CHARACTERISTICS**  
**ABSOLUTE MAXIMUM RATINGS**

Table 12 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit	
VCC	Power source voltage		-0.3 to 6.5	V	
Vi	Input voltage P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67	All voltages are based on Vss. Output transistors are cut off.	-0.3 to Vcc +0.3	V	
Vi	Input voltage P70-P77		-0.3 to Vcc +0.3	V	
Vi	Input voltage VL1		-0.3 to VL2	V	
Vi	Input voltage VL2		VL1 to VL3	V	
Vi	Input voltage VL3		VL2 to 6.5	V	
Vi	Input voltage C1, C2		-0.3 to 6.5	V	
Vi	Input voltage RESET, XIN		-0.3 to Vcc +0.3	V	
Vo	Output voltage C1, C2		-0.3 to 6.5	V	
Vo	Output voltage P00-P07, P10-P15, P30-P37		At output port	-0.3 to VCC	V
			At segment output	-0.3 to VL3	V
Vo	Output voltage P16, P17, P20-P27, P40-P47, P50-P57, P60-P67, P71-P77		-0.3 to Vcc +0.3	V	
Vo	Output voltage VL3		-0.3 to 6.5	V	
Vo	Output voltage VL2, SEG0-SEG17		-0.3 to VL3	V	
Vo	Output voltage XOUT		-0.3 to Vcc +0.3	V	
Pd	Power dissipation	Ta = 25°C	300	mW	
Topr	Operating temperature		-20 to 85	°C	
Tstg	Storage temperature		-40 to 125	°C	

**RECOMMENDED OPERATING CONDITIONS**

Table 13 Recommended operating conditions (1) (Vcc = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min.	Typ.	Max.		
VCC	Power source voltage	High-speed mode f(XIN) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(XIN) = 8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
VSS	Power source voltage		0		V	
VREF	A-D, D-A conversion reference voltage	2.0		Vcc	V	
AVSS	Analog power source voltage		0		V	
VIA	Analog input voltage AN0-AN7	AVSS		Vcc	V	

**Table 14 Recommended operating conditions (2) ( $V_{CC} = 2.5$  to  $5.5$  V,  $T_a = -20$  to  $85^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$V_{IH}$	"H" input voltage	P00–P07, P10–P17, P40, P43, P45, P47, P50–P53, P56, P61, P64–P67, P71–P77	0.7 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	P20–P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70	0.8 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	RESET	0.8 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	XIN	0.8 $V_{CC}$		$V_{CC}$	V
$V_{IL}$	"L" input voltage	P00–P07, P10–P17, P40, P43, P45, P47, P50–P53, P56, P61, P64–P67, P71–P77	0		0.3 $V_{CC}$	V
$V_{IL}$	"L" input voltage	P20–P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70	0		0.2 $V_{CC}$	V
$V_{IL}$	"L" input voltage	RESET	0		0.2 $V_{CC}$	V
$V_{IL}$	"L" input voltage	XIN	0		0.2 $V_{CC}$	V

**Table 15 Recommended operating conditions (3) ( $V_{CC} = 2.2$  to  $2.5$  V,  $T_a = -20$  to  $85^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$V_{IH}$	"H" input voltage	P00–P07, P10–P17, P40, P43, P45, P47, P50–P53, P56, P61, P64–P67, P71–P77	0.8 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	P20–P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70	0.95 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	RESET	0.95 $V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage	XIN	0.95 $V_{CC}$		$V_{CC}$	V
$V_{IL}$	"L" input voltage	P00–P07, P10–P17, P40, P43, P45, P47, P50–P53, P56, P61, P64–P67, P71–P77	0		0.2 $V_{CC}$	V
$V_{IL}$	"L" input voltage	P20–P27, P41, P42, P44, P46, P54, P55, P57, P60, P62, P63, P70	0		0.05 $V_{CC}$	V
$V_{IL}$	"L" input voltage	RESET	0		0.05 $V_{CC}$	V
$V_{IL}$	"L" input voltage	XIN	0		0.05 $V_{CC}$	V

Table 16 Recommended operating conditions (4) (Vcc = 2.2 to 5.5 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-20	mA
ΣIOH(peak)	"H" total peak output current P41-P47, P50-P57, P60-P67 (Note 1)			-20	mA
ΣIOL(peak)	"L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P41-P47, P50-P57, P60-P67 (Note 1)			20	mA
ΣIOL(peak)	"L" total peak output current P40, P71-P77 (Note 1)			80	mA
ΣIOH(avg)	"H" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			-10	mA
ΣIOH(avg)	"H" total average output current P41-P47, P50-P57, P60-P67 (Note 1)			-10	mA
ΣIOL(avg)	"L" total average output current P00-P07, P10-P17, P20-P27, P30-P37 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P41-P47, P50-P57, P60-P67 (Note 1)			10	mA
ΣIOL(avg)	"L" total average output current P40, P71-P77 (Note 1)			40	mA
IOH(peak)	"H" peak output current P00-P07, P10-P15, P30-P37 (Note 2)			-1.0	mA
IOH(peak)	"H" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2)			-5.0	mA
IOL(peak)	"L" peak output current P00-P07, P10-P15, P30-P37 (Note 2)			5.0	mA
IOL(peak)	"L" peak output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 2)			10	mA
IOL(peak)	"L" peak output current P40, P71-P77 (Note 2)			20	mA
IOH(avg)	"H" average output current P00-P07, P10-P15, P30-P37 (Note 3)			-0.5	mA
IOH(avg)	"H" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67			-2.5	mA
IOL(avg)	"L" average output current P00-P07, P10-P15, P30-P37 (Note 3)			2.5	mA
IOL(avg)	"L" average output current P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 3)			5.0	mA
IOL(avg)	"L" average output current P40, P71-P77 (Note 3)			10	mA

**Notes1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.  
**2:** The peak output current is the peak current flowing in each port.  
**3:** The average output current is an average value measured over 100 ms.

Table 17 Recommended operating conditions (5) ( $V_{CC} = 2.2$  to  $5.5$  V,  $T_a = -20$  to  $85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	$(4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V})$			4.0	MHz
		$(V_{CC} \leq 4.0 \text{ V})$			$(10 \times V_{CC} - 4)/9$	MHz
f(XIN)	Main clock input oscillation frequency <b>(Note 1)</b>	High-speed mode $(4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V})$			8.0	MHz
		High-speed mode $(2.2 \text{ V} \leq V_{CC} \leq 4.0 \text{ V})$			$(20 \times V_{CC} - 8)/9$	MHz
		Middle-speed mode			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency <b>(Notes 1, 2)</b>			32.768	50	kHz

**Notes1:** When the oscillation frequency has a duty cycle of 50%.

**2:** When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that  $f(XCIN) < f(XIN)/3$ .

Table 18 Electrical characteristics (1) (V<sub>CC</sub> =4.0 to 5.5 V, T<sub>a</sub> = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P15, P30-P37	IOH = -1 mA	V <sub>CC</sub> -2.0			V
		IOH = -0.25 mA V <sub>CC</sub> = 2.2 V	V <sub>CC</sub> -0.8			V
VOH	"H" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67 (Note 1)	IOH = -5 mA	V <sub>CC</sub> -2.0			V
		IOH = -1.5 mA	V <sub>CC</sub> -0.5			V
		IOH = -1.25 mA V <sub>CC</sub> = 2.2 V	V <sub>CC</sub> -0.8			V
VOL	"L" output voltage P00-P07, P10-P15, P30-P37	IOL = 5 mA			2.0	V
		IOL = 1.5 mA			0.5	V
		IOL = 1.25 mA V <sub>CC</sub> = 2.2 V			0.8	V
VOL	"L" output voltage P16, P17, P20-P27, P41-P47, P50-P57, P60-P67	IOL = 10 mA			2.0	V
		IOL = 3.0 mA			0.5	V
		IOL = 2.5 mA V <sub>CC</sub> = 2.2 V			0.8	V
VOL	"L" output voltage P40, P71-P77	IOL = 10 mA			0.5	V
		IOL = 5 mA V <sub>CC</sub> = 2.2 V			0.3	V
VT+ - VT-	Hysteresis INT0-INT2, ADT, CNTR0, CNTR1, P20-P27			0.5		V
VT+ - VT-	Hysteresis SCLK, RXD, SIN2			0.5		V
VT+ - VT-	Hysteresis RESET			0.5		V
I <sub>IH</sub>	"H" input current P00-P07, P10-P17, P20-P27, P40-P47, P50-P57, P60-P67, P70-P77	V <sub>I</sub> = V <sub>CC</sub>			5.0	μA
I <sub>IH</sub>	"H" input current RESET	V <sub>I</sub> = V <sub>CC</sub>			5.0	μA
I <sub>IH</sub>	"H" input current XIN	V <sub>I</sub> = V <sub>CC</sub>		4.0		μA
I <sub>IL</sub>	"L" input current P00-P07, P10-P17, P20-P27, P41-P47, P50-P57, P60-P67	V <sub>I</sub> = V <sub>SS</sub> Pull-ups "off"			-5.0	μA
		V <sub>CC</sub> = 5 V, V <sub>I</sub> = V <sub>SS</sub> Pull-ups "on"	-60.0	-120.0	-240.0	μA
		V <sub>CC</sub> = 2.2 V, V <sub>I</sub> = V <sub>SS</sub> Pull-ups "on"	-5.0	-20.0	-40.0	μA
I <sub>IL</sub>	"L" input current P40, P70-P77				-5.0	μA
I <sub>IL</sub>	"L" input current RESET	V <sub>I</sub> = V <sub>SS</sub>			-5.0	μA
I <sub>IL</sub>	"L" input current XIN	V <sub>I</sub> = V <sub>SS</sub>		-4.0		μA
I <sub>LOAD</sub>	Output load current P30-P37	V <sub>CC</sub> = 5.0 V, V <sub>O</sub> = V <sub>CC</sub> , Pullup ON Output transistors "off"	-60.0	-120.0	-240.0	μA
		V <sub>CC</sub> = 2.2 V, V <sub>O</sub> = V <sub>CC</sub> , Pullup ON Output transistors "off"	-5.0	-20.0	-40.0	μA
I <sub>LEAK</sub>	Output leak current P30-P37	V <sub>O</sub> = V <sub>CC</sub> , Pullup OFF Output transistors "off"			5.0	μA
		V <sub>O</sub> = V <sub>SS</sub> , Pullup OFF Output transistors "off"			-5.0	μA

Table 19 Electrical characteristics (2) (V<sub>CC</sub> = 2.2 to 5.5 V, T<sub>a</sub> = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
I <sub>CC</sub>	Power source current	<ul style="list-style-type: none"> <li>High-speed mode, V<sub>CC</sub> = 5 V f(X<sub>IN</sub>) = 8 MHz f(X<sub>CIN</sub>) = 32.768 kHz Output transistors "off" A-D converter in operating</li> </ul>		8.0	15	mA
		<ul style="list-style-type: none"> <li>High-speed mode, V<sub>CC</sub> = 5 V f(X<sub>IN</sub>) = 8 MHz (in WIT state) f(X<sub>CIN</sub>) = 32.768 kHz Output transistors "off" A-D converter stop</li> </ul>		2.5	4.0	mA
		<ul style="list-style-type: none"> <li>Low-speed mode, V<sub>CC</sub> = 5 V, T<sub>a</sub> ≤ 55°C f(X<sub>IN</sub>) = stopped f(X<sub>CIN</sub>) = 32.768 kHz Output transistors "off"</li> </ul>		45	67	μA
		<ul style="list-style-type: none"> <li>Low-speed mode, V<sub>CC</sub> = 5 V, T<sub>a</sub> = 25°C f(X<sub>IN</sub>) = stopped f(X<sub>CIN</sub>) = 32.768 kHz (in WIT state) Output transistors "off"</li> </ul>		23	46	μA
		<ul style="list-style-type: none"> <li>Low-speed mode, V<sub>CC</sub> = 3 V, T<sub>a</sub> ≤ 55°C f(X<sub>IN</sub>) = stopped f(X<sub>CIN</sub>) = 32.768 kHz Output transistors "off"</li> </ul>		18	36	μA
		<ul style="list-style-type: none"> <li>Low-speed mode, V<sub>CC</sub> = 3 V, T<sub>a</sub> = 25°C f(X<sub>IN</sub>) = stopped f(X<sub>CIN</sub>) = 32.768 kHz (in WIT state) Output transistors "off"</li> </ul>		8	16	μA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C Ta = 85 °C		0.1	10
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.1	V
IL1	Power source current (VL1) <b>(Note)</b>	VL1 = 1.8 V		4.0		μA

**Note:** When the voltage multiplier control bit of the LCD mode register (bit 4 at address 0039<sub>16</sub>) is "1".

**Table 20 A-D converter characteristics**

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85°C, f(XIN) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	VCC = VREF = 5 V			±2	LSB
tCONV	Conversion time	f(XIN) = 8 MHz			12.5 (Note)	µs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference power source input current	VREF = 5 V	50	150	200	µA
IIA	Analog port input current				5.0	µA

**Note:** When an internal trigger is used in middle-speed mode, it is 14 µs.

**Table 21 D-A converter characteristics**

(VCC = 2.7 to 5.5 V, VCC = VREF, VSS = AVSS = 0 V, Ta = -20 to 85°C, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy	VCC = VREF = 5 V			1.0	%
		VCC = VREF = 2.7 V			2.0	%
tsu	Setting time			3		µs
RO	Output resistor		1	2.5	4	kΩ
IVREF	Reference power source input current	<b>(Note)</b>			3.2	mA

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

Table 22 Timing requirements 1 (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	250			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
twH(INT)	INT0 to INT2 input "H" pulse width	80			ns
twL(INT)	INT0 to INT2 input "L" pulse width	80			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	800			ns
twH(SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	370			ns
twL(SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	370			ns
tsu(RxD-SCLK1)	Serial I/O1 input set up time	220			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	100			ns
tc(SCLK2)	Serial I/O2 clock input cycle time (Note)	1000			ns
twH(SCLK2)	Serial I/O2 clock input "H" pulse width (Note)	400			ns
twL(SCLK2)	Serial I/O2 clock input "L" pulse width (Note)	400			ns
tsu(SIN2-SCLK2)	Serial I/O2 input set up time	200			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time	200			ns

Note: When bit 6 of address 001A16 is "1".  
Divide this value by four when bit 6 of address 001A16 is "0".

Table 23 Timing requirements 2 (Vcc = 2.2 to 4.0 V, Vss = 0 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	Main clock input cycle time (XIN input)	125			ns
twH(XIN)	Main clock input "H" pulse width	45			ns
twL(XIN)	Main clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	900/(Vcc+0.4)			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	tc(CNTR)/2-20			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	tc(CNTR)/2-20			ns
twH(INT)	INT0 to INT2 input "H" pulse width	230			ns
twL(INT)	INT0 to INT2 input "L" pulse width	230			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	2000			ns
twH(SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	950			ns
twL(SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	950			ns
tsu(RxD-SCLK1)	Serial I/O1 input set up time	400			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	200			ns
tc(SCLK2)	Serial I/O2 clock input cycle time (Note)	2000			ns
twH(SCLK2)	Serial I/O2 clock input "H" pulse width (Note)	950			ns
twL(SCLK2)	Serial I/O2 clock input "L" pulse width (Note)	950			ns
tsu(SIN2-SCLK2)	Serial I/O2 input set up time	400			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time	300			ns

Note: When bit 6 of address 001A16 is "1".  
Divide this value by four when bit 6 of address 001A16 is "0".

**Table 24 Switching characteristics 1 (V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85°C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>wH</sub> (SCLK1)	Serial I/O1 clock output "H" pulse width	t <sub>c</sub> (SCLK1)/2-30			ns
t <sub>wL</sub> (SCLK1)	Serial I/O1 clock output "L" pulse width	t <sub>c</sub> (SCLK1)/2-30			ns
t <sub>d</sub> (SCLK1-TxD)	Serial I/O1 output delay time ( <b>Note 1</b> )			140	ns
t <sub>v</sub> (SCLK1-TxD)	Serial I/O1 output valid time ( <b>Note 1</b> )	-30			ns
t <sub>r</sub> (SCLK1)	Serial I/O1 clock output rising time			30	ns
t <sub>f</sub> (SCLK1)	Serial I/O1 clock output falling time			30	ns
t <sub>wH</sub> (SCLK2)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK2)/2-160			ns
t <sub>wL</sub> (SCLK2)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK2)/2-160			ns
t <sub>d</sub> (SCLK2-SOUT2)	Serial I/O2 output delay time			0.2 X t <sub>c</sub> (SCLK2)	ns
t <sub>v</sub> (SCLK2-SOUT2)	Serial I/O2 output valid time	0			ns
t <sub>f</sub> (SCLK2)	Serial I/O2 clock output falling time			40	ns
t <sub>r</sub> (CMOS)	CMOS output rising time ( <b>Note 2</b> )		10	30	ns
t <sub>f</sub> (CMOS)	CMOS output falling time ( <b>Note 2</b> )		10	30	ns

**Notes1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** XOUT and XCOUNT pins are excluded.

**Table 25 Switching characteristics 2 (V<sub>CC</sub> = 2.2 to 4.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85°C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>wH</sub> (SCLK1)	Serial I/O1 clock output "H" pulse width	t <sub>c</sub> (SCLK1)/2-50			ns
t <sub>wL</sub> (SCLK1)	Serial I/O1 clock output "L" pulse width	t <sub>c</sub> (SCLK1)/2-50			ns
t <sub>d</sub> (SCLK1-TxD)	Serial I/O1 output delay time ( <b>Note 1</b> )			350	ns
t <sub>v</sub> (SCLK1-TxD)	Serial I/O1 output valid time ( <b>Note 1</b> )	-30			ns
t <sub>r</sub> (SCLK1)	Serial I/O1 clock output rising time			50	ns
t <sub>f</sub> (SCLK1)	Serial I/O1 clock output falling time			50	ns
t <sub>wH</sub> (SCLK2)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK2)/2-240			ns
t <sub>wL</sub> (SCLK2)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK2)/2-240			ns
t <sub>d</sub> (SCLK2-SOUT2)	Serial I/O2 output delay time			0.2 X t <sub>c</sub> (SCLK2)	ns
t <sub>v</sub> (SCLK2-SOUT2)	Serial I/O2 output valid time	0			ns
t <sub>f</sub> (SCLK2)	Serial I/O2 clock output falling time			50	ns
t <sub>r</sub> (CMOS)	CMOS output rising time ( <b>Note 2</b> )		20	50	ns
t <sub>f</sub> (CMOS)	CMOS output falling time ( <b>Note 2</b> )		20	50	ns

**Notes1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** XOUT and XCOUNT pins are excluded.

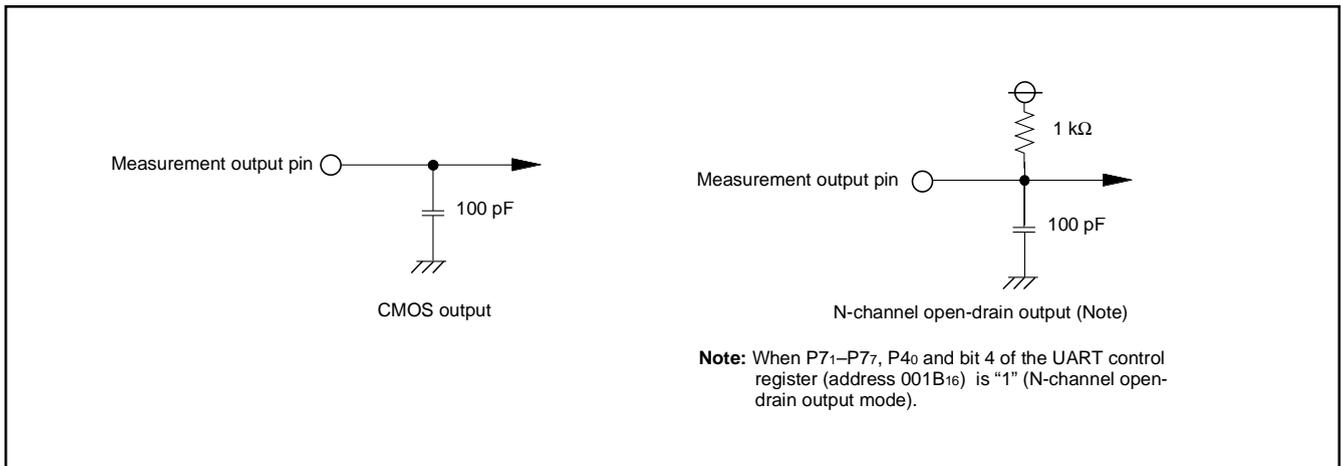


Fig. 56 Circuit for measuring output switching characteristics

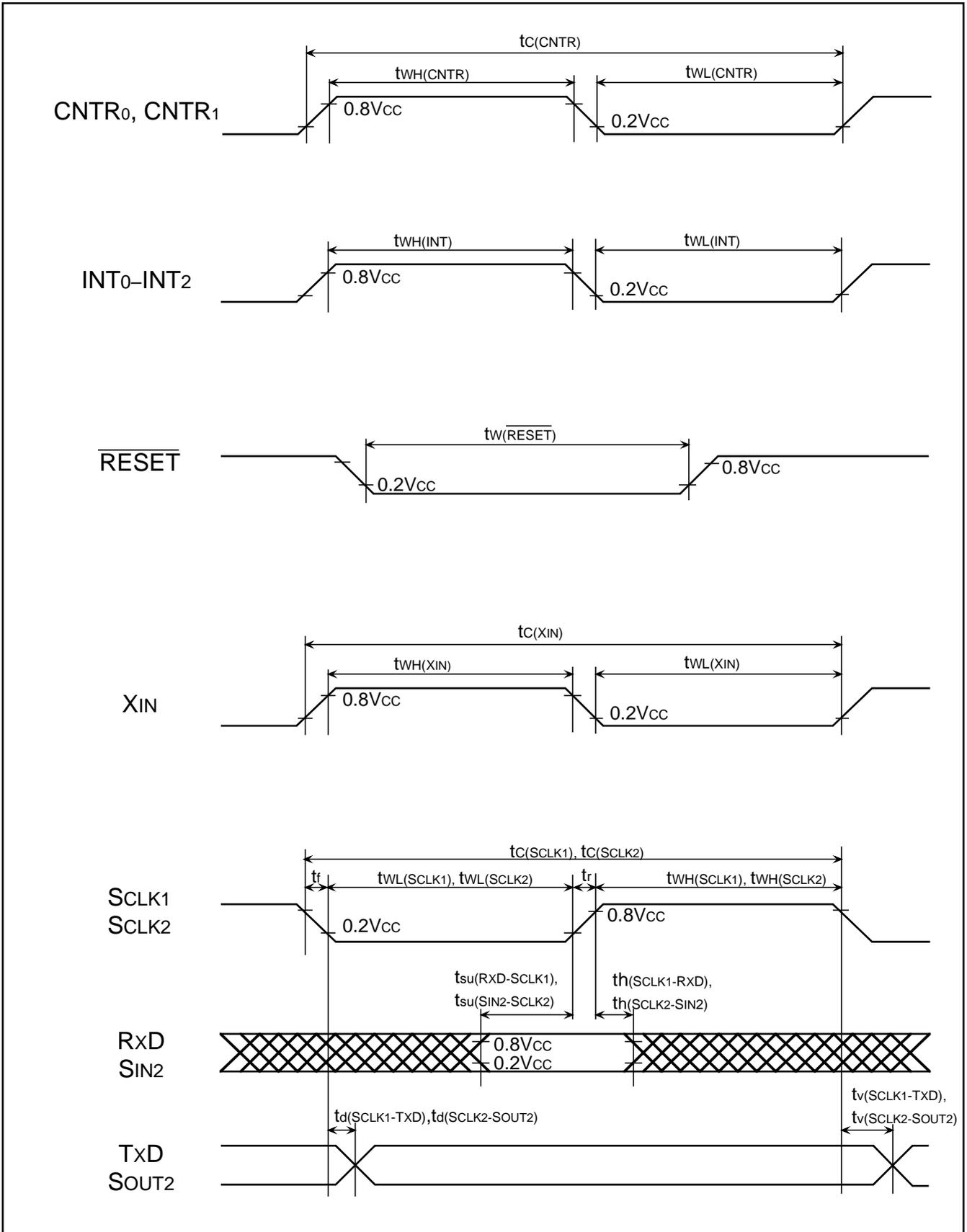
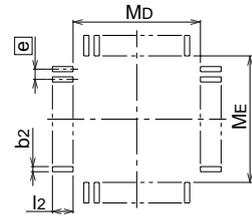
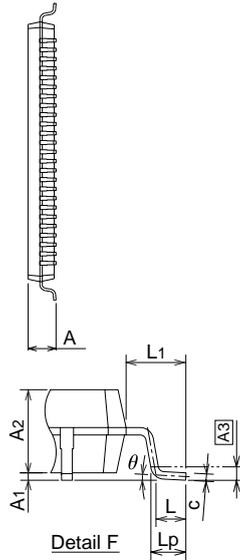
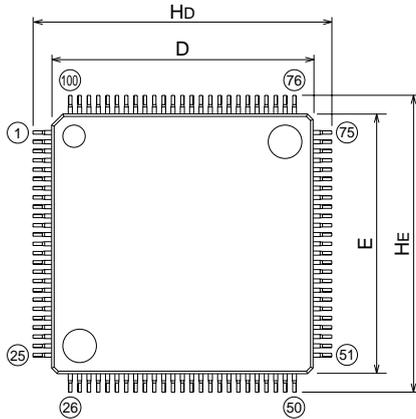


Fig. 57 Timing diagram

**PACKAGE OUTLINE**  
**100P6Q-A** (MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	-	0.63	Cu Alloy



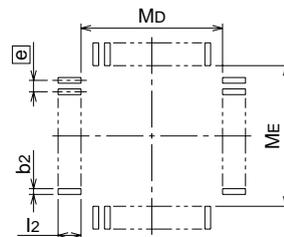
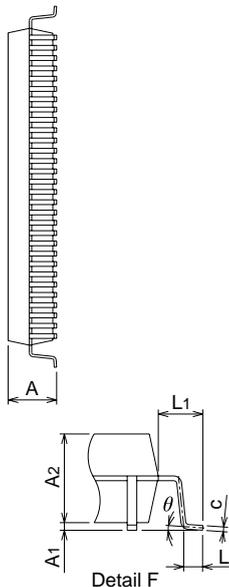
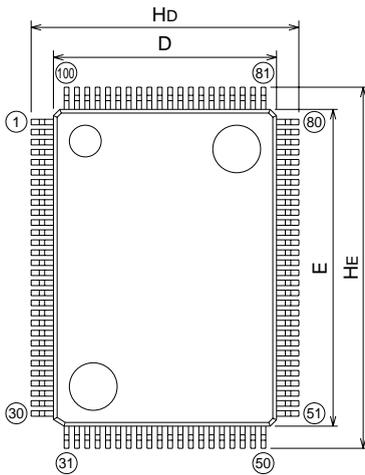
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	-	0.5	-
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	14.4	-
ME	-	14.4	-

**100P6S-A** (MMP)

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
theta	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-



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