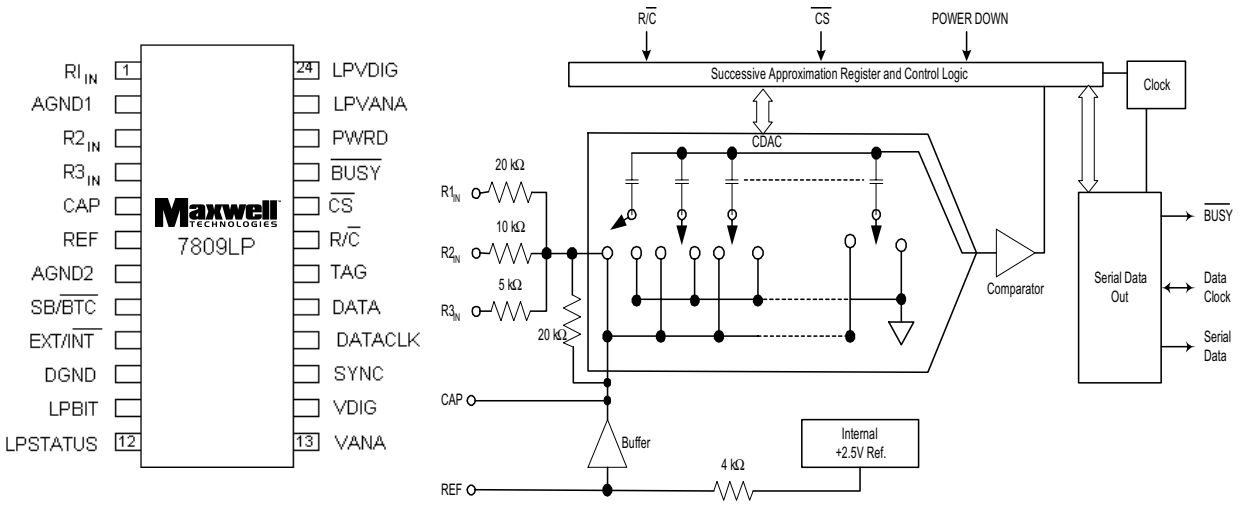
7809LP
16-Bit Latchup Protected Analog to Digital Converter



Logic Diagram

FEATURES:

- RAD-PAK® radiation-hardened against natural
- space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Latch-up Protection Technology (LPT™)
- SEL converted into a reset
  - Rate based on cross section and mission
- Same footprint as ADS7809
- Package: 24 pin RAD-PAK flat package
- 100 kHz min sampling rate
- ±10 V and 0 V to 5 V input range
- DNL: 15-bits "No Missing Codes"
- 83 dB min SINAD with 20 kHz input
- Single +5 V supply operation
- Utilizes internal or external reference
- Serial output
- Power dissipation: 132 mW max

DESCRIPTION:

Maxwell Technologies' 7809LP high-speed 16-bit analog to digital converter features a greater than 100 kilorad (Si) total dose tolerance depending upon space mission. Using Maxwell's radiation-hardened RAD-PAK® packaging technology, the 7809LP has the same footprint as ADS7809 and is latchup protected by Maxwell Technologies' Latchup Protection Technology (LPT™). It is a 24 pin, 16-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. The 7809LP contains a 16-bit capacitor based SAR A/D with S/H, reference, clock, interface for microprocessor use, and serial output drivers. The 7809LP is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges include ±10 V and 0 to 5 V, while the innovative design allows operation from a single +5 V supply, with power dissipation of under 132 mW.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 50 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defined Class K.

(858) 503-3300- Fax: (858) 503-3301 - www.maxwell.com

TABLE 1. 7809LP PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	R1IN	Analog Input.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	R2IN	Analog Input.
4	R3IN	Analog Input.
5	CAP	Reference Buffer Capacitor. 2.2 µF tantalum to ground.
6	REF	Reference Input/Output. 2.2 µF tantalum capacitor to ground.
7	AGND2	Analog Ground.
8	SB/$\overline{\text{BTC}}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/INT	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	LPBIT	Built In test function of the latchup protection. Drive LOW during normal operation.
12	LPSTATUS	Latchup Protection Status Output. LPSTATUS when HIGH indicates latchup protection is active and output data is invalid.
13	VANA	Analog Supply Input. Nominally 5V.
14	VDIG	Digital Supply Input. Nominally 5V.
15	SYNC	Sync Output. If EXT/INT is HIGH, either a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW or a falling edge on $\overline{\text{CS}}$ with R/$\overline{\text{C}}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
16	DATACLK	Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
17	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16-bits of data, the 7809LOPO will output the level input of TAG as long as $\overline{\text{CS}}$ is LOW and R/$\overline{\text{C}}$ is HIGH. If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
18	TAG	Tag input for use in external clock mode. If EXT/INT is HIGH, the digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{\text{CS}}$ is LOW and R/$\overline{\text{C}}$ is HIGH.
19	R/$\overline{\text{C}}$	Read/Convert Input. With $\overline{\text{CS}}$ LOW, a falling edge on R/$\overline{\text{C}}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW, or a falling edge on $\overline{\text{CS}}$ with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
20	$\overline{\text{CS}}$	Chip Select. Internally OR'ed with R/$\overline{\text{C}}$.

TABLE 1. 7809LP PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
21	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
22	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversions are maintained in the output shift register.
23	LPVANA	Latchup Protection Analog Supply.
24	LPVDIG	Latchup Protection Digital Supply.

TABLE 2. 7809LP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog Inputs	$R1_{IN}$ $R2_{IN}$ $R3_{IN}$ CAP REF [1]	-25 -25 -25 V_{ANA} + 0.3	25 25 25 AGND2 - 0.3	V V V V
Ground Voltage Differences: DGND, AGND2		-0.3	0.3	V
V_{ANA}		--	7	V
V_{DIG}			7	V
V_{DIG} to V_{ANA}		--	0.3	V
Specified Performance		-40	85	˚C
Digital Inputs		-0.3	V_{DIG} + 0.3	V
Storage Temperature	T_{STG}	-65	150	˚C

1. Indefinite short to AGND2, momentarily short to V_{ANA}.

TABLE 3. 7809LP DC ACCURACY SPECIFICATIONS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	MIN	TYP	MAX	UNIT
Integral Linearity Error -40 to 85°C	-- --	-- --	±3 ±5	LSB [1]
Differential Linearity Error -40 to 85°C	-- --	-- --	-2, 3 -1, 6	LSB LSB
No Missing Codes [2]	15	--	--	Bits
Transition Noise [3]	--	1.3	--	LSB
Full Scale Error [4,5]	--	--	±0.6	%
Full Scale Error [4,5] (using ext. 2.5000 V_{ref})	--		±0.6	%
Full Scale Error Drift	--	±7	--	ppm/˚C

TABLE 3. 7809LP DC ACCURACY SPECIFICATIONS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	MIN	TYP	MAX	UNIT
Full Scale Error Drift (using ext. 2.5000 V_{ref})	--	±2	--	ppm/°C
Bipolar Zero Error [4]	--	--	±10	mV
Bipolar Zero Error Drift	--	±2	--	ppm/°C
Unipolar Zero Error [4] -40 to 85°C	-- --	-- --	±3 ±16	mV mV
Unipolar Zero Error Drift	--	±2	--	ppm/°C
Recovery to Rated Accuracy after Power Down (1 uF Capacitor to CAP)	--	1	--	ms
Power Supply Sensitivity ($V_{DIG} = V_{ANA} = V_D$) 4.75 V $\geq V_D \leq$ 5.2 V -40 to 85°C	-- --	-- --	±8 ±32	LSB LSB

1. LSB stands for Least Significant Bit. One LSB is equal to 305 µV.
2. Not tested.
3. Typical rms noise at worst case transitions and temperatures.
4. Measured with various fixed resistors.
5. For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last scale code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

TABLE 4. DELTA LIMITS

PARAMETER	VARIATION
I_{CC}	+/- 10%

TABLE 5. 7809LP DIGITAL INPUTS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
V_{IL}	1, 2, 3	-0.3	--	0.8	V
V_{IH}		2.0	--	V_D + 0.3	V
I_{IL}, I_{IH}		--	--	±10	µA

TABLE 6. 7809LP ANALOG INPUT AND THROUGHPUT SPEED

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Voltage Ranges		10 V, 0 V to 5 V See Table 2.			
Impedance					
Capacitance[1]	1, 2, 3	--	35	--	pF
Conversion Time	9, 10, 11	--	7.6	8	µs
Complete Cycle (Acquire and Convert)	9, 10, 11	--	--	10	µs
Throughput Rate [2]	9, 10, 11	100	--	--	kHz

1. Guarenteed by design.
2. Tested by application of signal.

TABLE 7. 7809LP AC ACCURACY SPECIFICATIONS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, f_{IN} = 20 kHz [1]	4, 5, 6	90	100	--	dB [2]
Total Harmonic Distortion, f_{IN} = 20 kHz [1]	4, 5, 6	--	-100	-90	dB
Signal-to-Noise (Noise + Distortion) [1] f_{IN} = 20 kHz -60 dB Input	4, 5, 6	 83 --	 88 30	 -- --	dB
Signal-to-Noise [1], f_{IN} = 20 kHz		83	88	--	dB
Full-Power Bandwidth [1,3]	9, 10, 11	--	250	--	kHz

1. Guaranteed by design.
2. All specifications in dB are referred to a full-scale ±10 V input.
3. Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-Noise (Noise + Distortion) degrades to 60 dB.

TABLE 8. 7809LP SAMPLING DYNAMICS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	MIN	TYP	MAX	UNIT
Aperture Delay	9, 10, 11	--	40	--	ns
Aperture Jitter	9, 10, 11	Sufficient to meet AC specification			
Transient Response FS Step	9, 10, 11	--	2	--	us
Overvoltage Recovery [1]	9, 10, 11	--	150	--	ns

1. Recovers to specified performance after 2 X FS input overvoltage.

TABLE 9. 7809LP REFERENCE

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must be ext. buffer)		--	1	--	µA
External Reference Voltage Range for Specified Linearity [1]		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref	--	--	100	µA

1. Tested by application of signal.

TABLE 10. 7809LP DIGITAL OUTPUTS

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
Data Format Data Coding Pipeline Delay		Serial 16-bits Binary Two's Complement or Straight Binary Conversion results only available after completed conversion				
Data Clock	Selectable for internal or external data clock					
Internal (Output Only When Transmitting Data) External (Can Run Continually)	9, 10, 11	EXT/$\overline{INT}$ Low EXT/$\overline{INT}$ High	-- 0.1	2.3 --	-- 10	MHz
V_{OL} V_{OH}	1, 2, 3	I_{SINK} = 1.6 mA I_{SOURCE} = 500 µA	-- 4	-- --	0.4 --	V
Leakage Current [1]	1, 2, 3	High-Z State, V_{OUT} = 0V to V_{DIG}	--	--	±10	µA
Output Capacitance [1]	1, 2, 3	High-Z State	--	15	--	pF

1. Not tested.

TABLE 11. 7809LP POWER SUPPLIES

(SPECIFIED PERFORMANCE -40 TO +85°C)

PARAMETER	SUBGROUPS	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG}	1, 2, 3	Must be < V_{ANA}	4.75	5	5.25	V
V_{ANA}	1, 2, 3		4.75	5	5.25	V
I_{DIG}	1, 2, 3		--	0.3	--	mA
I_{ANA}	1, 2, 3		--	16	--	mA
Power Dissipation PWRD LOW PWRD HIGH	1, 2, 3	 V_{ANA} = V_{DIG} = 5V f_s = 100 kHz	 -- --	 -- --	 132 100	mW

TABLE 12. 7809LP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data using Internal Clock	1 > 0	0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n-1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK
	0	1 > 0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n-1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK
Initiate Conversion and Output Data using External Clock	1 > 0	0	1	1	Input	0	x	Initiates conversion “n”
	0	1 > 0	1	1	Input	0	x	Initiates conversion “n”
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion “n” clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pules on SYNC followed by data from conversion “n-1” clocked out synchronized to external DATACLK [1]. Conversion “n” in process.
	0	0 > 1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion “n-1” clocked out synchronized to external DATACLK [1]. Conversion “n” in process.
Incorrect Conversions	0	0	0 > 1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion will be initiated without time for acquisition
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers

TABLE 12. 7809LP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Selecting Output Format	x	x	x	x	x	x	0 3	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

1. See Figure 4 for constraints on previous data valid during conversion.

TABLE 13. 7809LP INPUT RANGE CONNECTION

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9 kΩ
±5V	AGND	V_{IN}	CAP	13.3 kΩ
±3.3V	V_{IN}	V_{IN}	CAP	10.7 kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0 kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7 kΩ

TABLE 14. 7809LP CONVERSION AND DATA TIMING

(T_A = -40 °C TO 85 °C UNLESS OTHERWISE SPECIFIED)

SYMBOL	DESCRIPTION	SUBGROUPS	MIN	TYP	MAX	UNIT
t1	Convert Pulse Width	9, 10, 11	40	--	6000	ns
t2	$\overline{BUSY}$ Delay	9, 10, 11	--	--	65	ns
t3	$\overline{BUSY}$ LOW	9, 10, 11	--	--	8	µs
t4	$\overline{BUSY}$ Delay after End of Conversion	9, 10, 11	--	220	--	ns
t5	Aperture Delay	9, 10, 11	--	40	--	ns
t6	Conversion Time	9, 10, 11	--	7.6	8	µs
t7	Acquisition Time	9, 10, 11	--	--	2	µs
t6 + t7	Throughput Time	9, 10, 11	--	9	10	µs
t8	R/$\overline{C}$ Low to DATACLK Delay	9, 10, 11	--	450	--	ns
t9	DATACLK Period	9, 10, 11	--	440	--	ns
t10	Data Valid to DATACLK HIGH Delay	9, 10, 11	20	75	--	ns
t11	Data Valid after DATACLK LOW Delay	9, 10, 11	100	125	--	ns
t12	External DATACLK	9, 10, 11	100	--	--	ns

TABLE 14. 7809LP CONVERSION AND DATA TIMING

(T_A = -40 °C TO 85 °C UNLESS OTHERWISE SPECIFIED)

SYMBOL	DESCRIPTION	SUBGROUPS	MIN	TYP	MAX	UNIT
t13	External DATACLK HIGH	9, 10, 11	20	--	--	ns
t14	External DATACLK LOW	9, 10, 11	30	--	--	ns
t15	DATACLK HIGH Setup Time	9, 10, 11	20	--	t12 + 5	ns
t16	R/$\overline{C}$ to $\overline{CS}$ Setup Time	9, 10, 11	10	--	--	ns
t17	SYNC Delay After DATACLK High	9, 10, 11	15	--	35	ns
t18	Data Valid Delay	9, 10, 11	25	--	55	ns
t19	$\overline{CS}$ to Rising Edge Delay	9, 10, 11	25	--	--	ns
t20	Data Available after $\overline{CS}$ LOW	9, 10, 11	6	--	--	µs

TABLE 15. 7809LP CONVERSION DATA TIMING

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305 µV	153 µV	102 µV	153 µV	76 µV	61 µV				
+ Full Scale (FS - 1 LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999938V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	-305 µV	-153 µV	-102 µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
-Full Scale	-10V	-5V	3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

FIGURE 1. CONVERSION TIMING

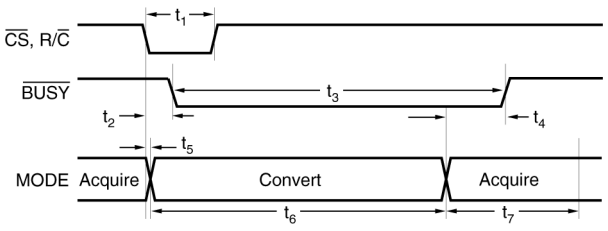


FIGURE 2. SERIAL DATA TIMING USING INTERNAL CLOCK ($\overline{CS}$, EXT/$\overline{INT}$ AND TAG TIED LOW)

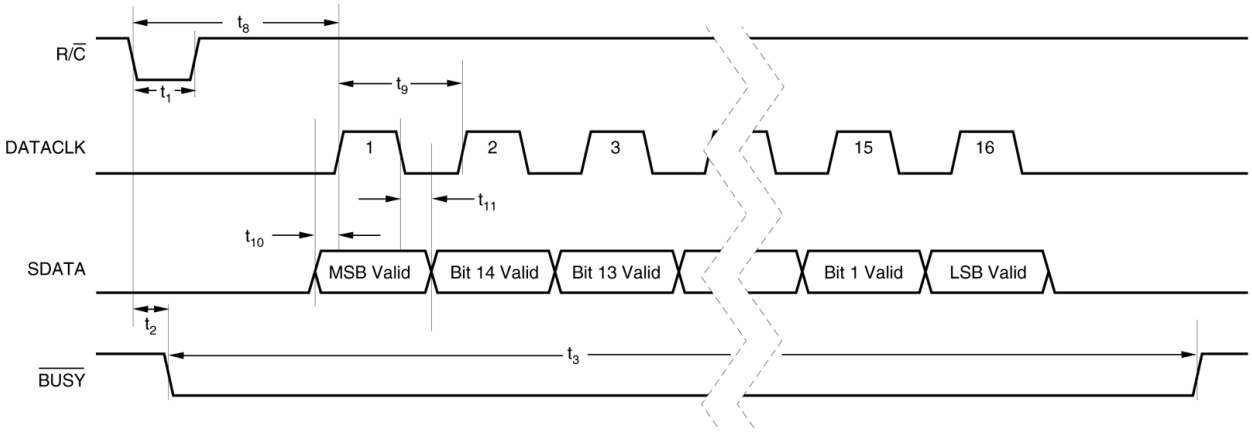


FIGURE 3. CONVERSION AND READ TIMING WITH EXTERNAL CLOCK (EXT/INT TIED HIGH). READ AFTER CONVERSION

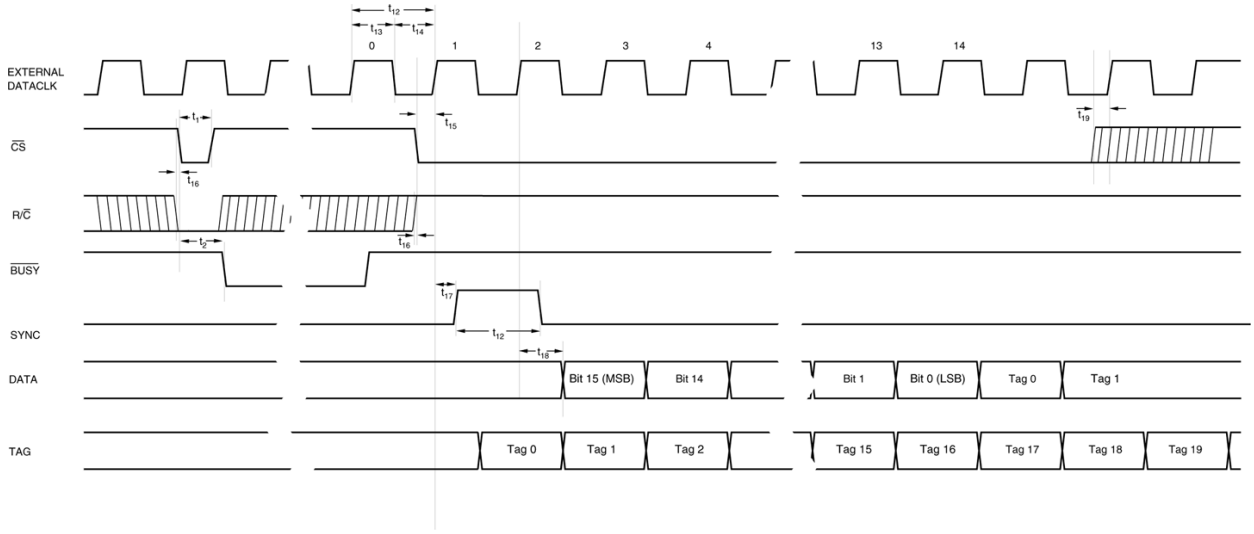


FIGURE 4. CONVERSION AND READ TIMING WITH EXTERNAL CLOCK (EXT/INT TIED HIGH). READ DURING CONVERSION

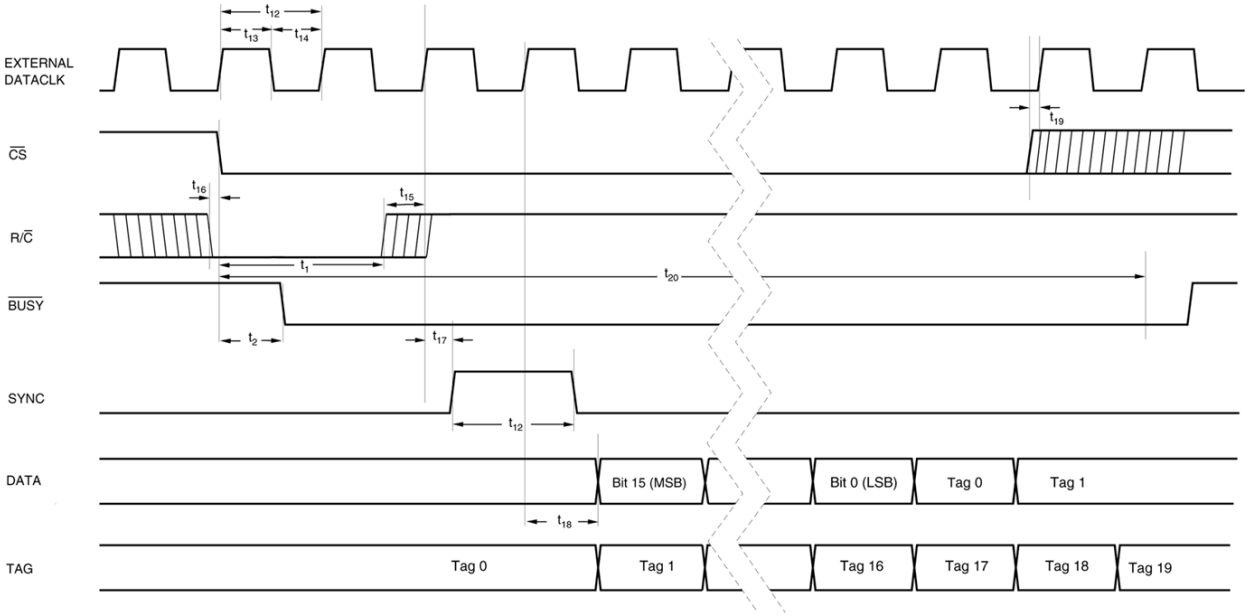


FIGURE 5. OFFSET/GAIN CIRCUITS FOR UNIPOLAR INPUT RANGES

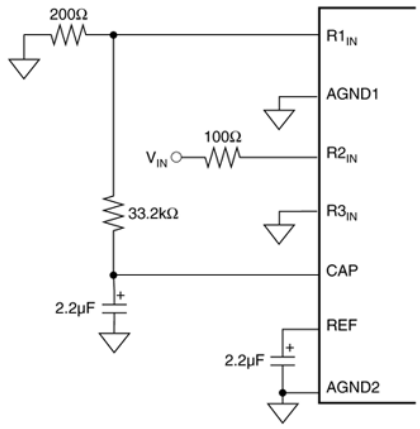
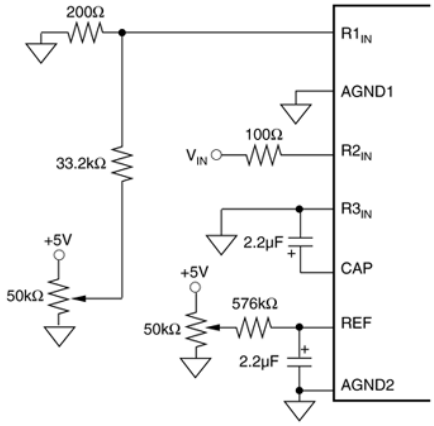
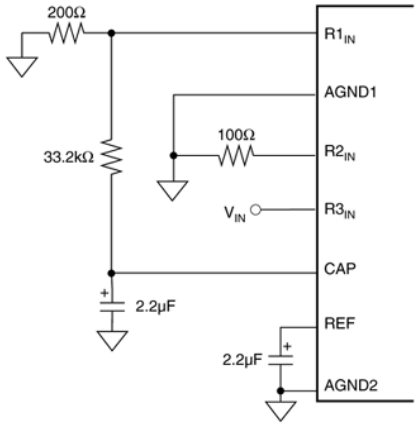
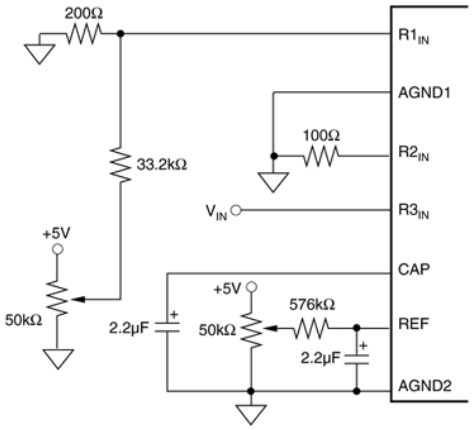
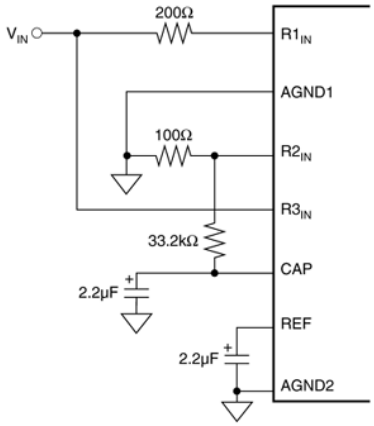
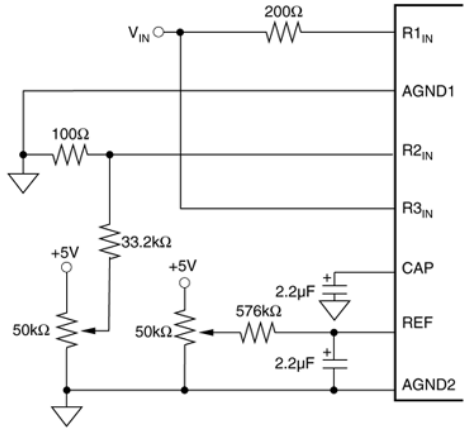
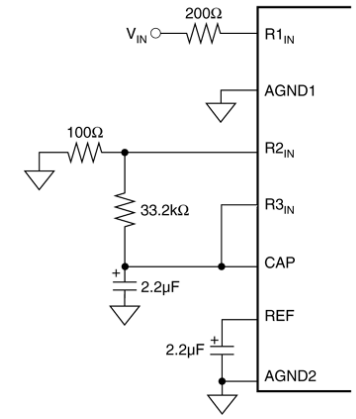
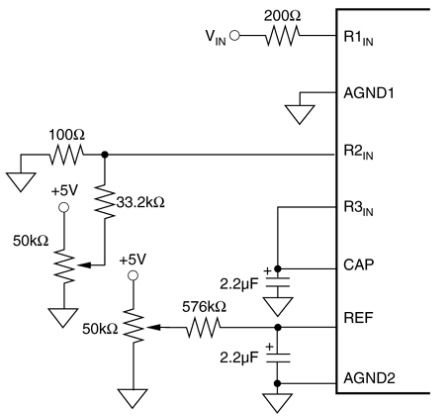
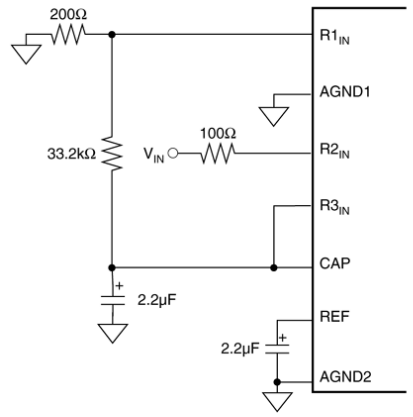
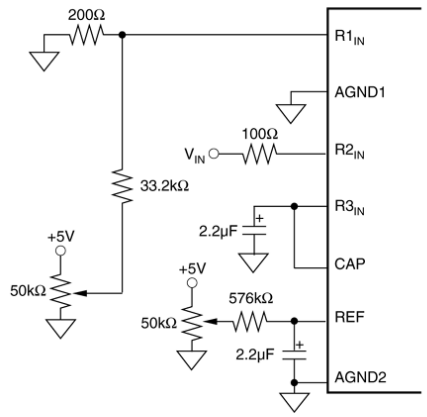
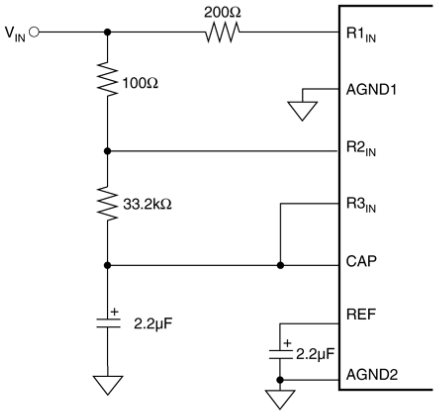
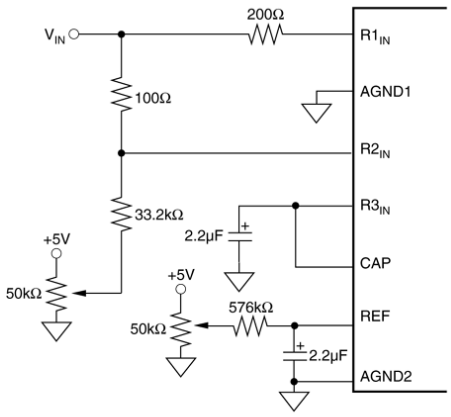
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

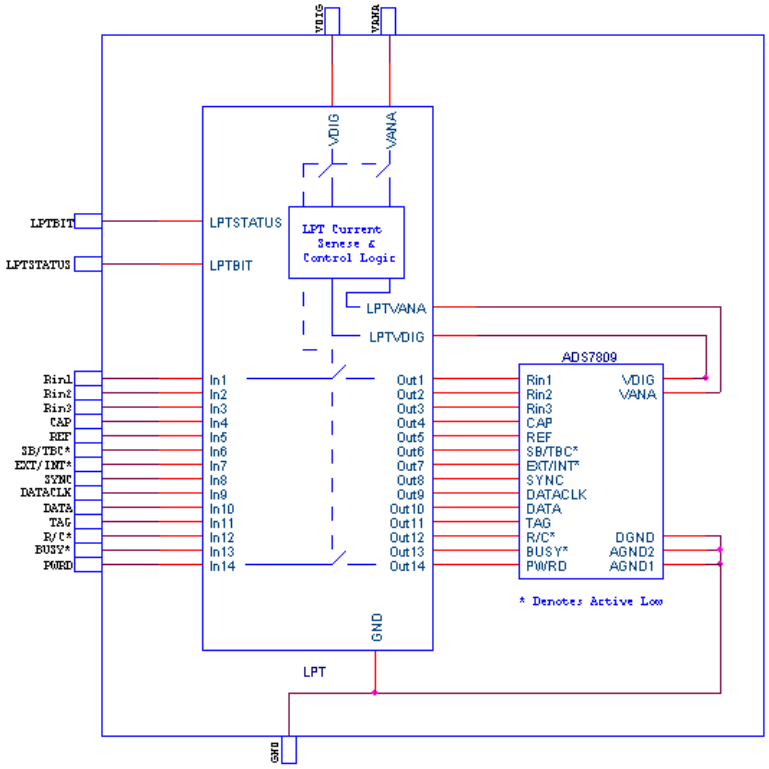
FIGURE 6. OFFSET/GAIN CIRCUITS FOR BIPOLAR INPUT RANGES

Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

LPT™ Operation

Latchup Protection Technology (LPT™) automatically detects an increase in the supply current of the 7809LP converter due to a single event effect and internally cycles the power to the converter off, then on, which restores the steady state operation of the device. A simplified block diagram of the 7809LP circuitry is shown in Figure 7. The LPT™ circuitry consists of two power switch and current sensor blocks, an LPT™ controller block, a BIT current load block, and an active input protection block.

Figure 7. 7809LP Simplified Block Diagram



The power switch/current sensor blocks sense the supply current drawn by the protected device on the analog and digital supply pins. When a threshold level is exceeded on either supply line, indicating single event induced latchup of the protected device, a signal is sent to the LPT™ controller block. The LPT™ controller then drives the power switches to an off state which removes the power supplies from the protected device. At the same time, a signal is sent to open the active input protection circuits and the LPSTATUS output pin is activated. After a period of time sufficient to clear the latchup, the LPT™ controller drives the power switches and input protection back to the on state restoring the operation of the protected device. The LPTBIT circuit is used during system test to electrically trigger the latchup function by drawing current through the power switch/current sensor blocks sufficient to trigger the LPT™ protection.

Differences Between the 7809LP and the ADS7809

Because the 7809LP uses the ADS7809 die to perform the analog to digital conversion function, its operation and performance is very similar to the ADS7809 packaged part from Burr-Brown. In general the operation and application will be the same for both parts. There are three primary differences: the operation of the supply pins, the operation of the additional LPBIT and LPSTATUS pins, and the operation of the I/O pins when a latchup is detected.

The ADS7809 provides separate analog and digital supply pins, VANA and VDIG. These same supply pins on the 7809LPRP should be connected to the analog and digital supplies. There is no limit to the capacitance that can be connected to these pins in the system application.

The 7809LP package also provides access to the ADS7809 die supply pins with the LPVANA and LPVDIG pins. The signal paths between the supply input pins and the respective die supply pins are low resistance during normal device operation. When an excessive supply current due to a single event latchup is sensed on either of the supply pins, the LPT™ circuit opens both paths to the die supply pins allowing the latchup condition to clear. The LPVANA and LPVDIG pins allow access to the current sense circuitry for electrical testing at the component level and provide optimal locations for attaching supply decoupling capacitors. **CAUTION:** The LPVANA and LPVDIG pins must not be connected to the respective power supplies since this will defeat the LPT™ power switch and could result in permanent latchup of the device during operation in a radiation environment. Electrolytic capacitors should not be connected to these decoupling pins because the large capacitance will increase the recovery time of the 7809LP. Low ESR ceramic capacitors should be used with a maximum of .2µF per pin.

The LPBIT input provides a means to electrically test the LPT™ circuit. A high level on the this pin causes a preset current to be drawn in addition to the normal device current through the analog and digital current sensors. If the high level is maintained for a sufficient duration, it will trigger the LPT™ circuit which will cycle the power to the protected device. If the LPBIT remains high, the LPT™ circuit will continuously cycle the supply voltages off then on. Driving this input with a 10 µs high level pulse is sufficient duration to assure the LPT™ circuit cycles the power off then on one time only.

A high level on the LPSTATUS output indicates that the LPT™ circuit has removed power from the protected device. The LPSTATUS returns low when the power is restored. LPSTATUS can be used to generate an input to the system data processor indicating that an LPT™ cycle has occurred and the protected device output accuracy may not be met until after the respective recovery time to the event.

During the time that power is removed from the protected device, it is critical that external circuitry driving the device I/O pins does not back-drive the device supply through input protection diodes or similar integrated structures. Back-driving of the supply through the device I/O pins could contribute to an extended or even a permanent latchup condition. For the ADS7809 testing has shown that for the normal signal range of operation on the analog input pins R1IN, R2IN, and R3IN, latchup will not be sustained.

In order to prevent back-driving the supply from the digital I/O pins DATA, SYNC, TAG, R/$\overline{C}$, $\overline{CS}$, and PWRD, the 7809LP incorporates active input protection circuits. These circuits act as transmission gates in series with the digital inputs. During normal operation, these gates are on and present low resistance connections between the package input pins and the respective die pins. When the LPT™ circuit detects a latchup, these gates are switched off and present a high resistance path between the package inputs and the die inputs. The protected I/O pins are crow barred during the latchup. The bidirectional signal, DATACLK, is also protected by a transmission gate.

Dedicated digital outputs are not similarly protected since in most applications there will be no appreciable drive signal on these outputs to back-drive the pins. Pull up resistors on these outputs should be 10 KΩ or greater to limit the back-drive current. Low on resistance, transmission gate circuits are also connected between the package pins and the die REF and CAP pins. These gates minimize the transient loading on the external filter capacitors required on these pins. This greatly reduces the single event recovery time of the 7809LP to full accuracy after an LPT™ cycle.

During an LPT™ cycle, all outputs of the 7809LP are invalid and unpredictable until after the functional recovery time. After the functional recovery time, data conversions occur with a degraded accuracy until the full accuracy recovery time.

A summary of the pin differences between the ADS7809 and the 7809LP is provided in the table below.

TABLE 15. ADS7809 AND 7809LP PIN DIFFERENCES

PIN NUMBER	ADS7809	7809LPRP	PIN DIFFERENCE DESCRIPTION
1-10	Various	Various	Equivalent function to ADS7809 pins 1-10 respectively. Timing specifications change slightly (0 - 10 ns) for the 7809LPRP due to the latchup protection circuitry on ADS7809 die inputs.
15-22	Various	Various	Equivalent function to ADS7809 pins 11-18 respectively. Timing specifications change slightly (0 - 10 ns) for the 7809LPRP due to the latchup protection circuitry on ADS7809 die inputs.
11	--	LPBIT	A built in test function of latchup protection. A TTL high level pulse for > 5 microseconds duration on this input will trigger latchup protection of the device. This input shall be low during normal operation.
12	--	LPSTATUS	Latchup protection status output. This TTL level output is low during normal operation and goes high during a 10 µs decision time period prior to power being removed. If the latch up current does not last at least 10 µs then LPTSTATUS will go low (inactive) after the 10 µs decision period without power being removed. When latchup protection is triggered, this output will go high for the duration of the time that power is removed from the protected device (50 µs). All output except LPSTATUS are invalid during the time that power is removed from the ADS7809 die. This output foes low within 1 us of the power being re-applied to the protected device. Functional operation of the device is within ~25 µs after the LPSTATUS output returns low with degraded accuracy due to the latchup filter circuitry. Full accuracy is restored ~5 ms later. This output can be used to inform the system processor of the latchup protection trigger and the subsequent degraded accuracy in the 7809LPRP output data. Output pull-up resistors should be 10kΩ or larger on outputs. I/O pins must not be driven high while this signal is active.
13	VANA	VANA	Equivalent function to ADS7809 pin 19. Analog Supply Input.
14	VDIG	VDIG	Equivalent function to ADS7809 pin 20. Digital Supply Input.
23	--	LPVANA	Latchup protected analog supply pin to the ADS7809 die. Decouple to analog ground with 0.1 µF ceramic capacitor. Do not exceed 0.2 µF. Do not connect to VDIG and/or VANA.
24	--	LPVDIG	Latchup protected digital supply pin to the ADS7809 die. Decouple to digital ground with 0.1 µF ceramic capacitor. Do not exceed 0.2 µF. Do not connect to VDIG and/or VANA.

Testing the 7809LPRP Latchup Protection Circuitry

The LPVANA and LPVDIG pins provide direct access to the 7809LP converter supply pins for attaching external decoupling capacitors to ground. These pins can also be used to test the LPT™ operation and threshold level by sinking a pulsed current load to ground as shown in the test circuit in Figure 8. The most accurate threshold current measurements are made with the ADS7809 in its lowest power state (PWRD = 5V).

The LPT™ operation and device recovery times are most easily measured using the LPBIT input to trigger protection and recovery. Applying a 10 µsec high duration TTL level to the LPBIT pin causes internal test currents sufficient to trigger the LPT™ circuit to be drawn through both the analog and digital supply sense circuits.

LPT™ operating characteristics are summarized in Table 16 according to the timing diagram shown in Figure 9. During the time that the power is cycled, output signals and data from the 7809LP are invalid. The LPSTATUS signal high indicates that power is removed from the ADS7809 die. When this signal is low, power is applied to the ADS7809 die. The LPSTATUS signal is used to measure the supply recovery time. The supply recovery time interval starts when the supply current rises (causing LPSTATUS to go high) and ends when the LPSTATUS signal stabilizes low again.

Within the functional recovery time interval (~25 µsec after the LPT™ circuit reapplies power), the normal functional operation of the converter is restored with less than 5% full scale error. Additional settling time is then required to return to full accuracy operation. Recovery time intervals are defined which indicate the time to recover first to within 8 bit accuracy, then to within 12 bit accuracy, and finally to full 16 bit accuracy. These recovery times are primarily due to the single event and power cycling effects on the reference circuits and the settling times of their respective filter capacitors.

TABLE 16. 7809LP LPT™ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
Supply Threshold Current	ITHR	PWRD = 5V	75	mA
Protection Time	TPT	LPBIT = 2.4V for 5 µs	10	µsec
Supply Recovery Time	TSR	LPBIT = 2.4V for 5 µs	50	µsec
Functional Recovery Time	TFR	LPBIT = 2.4V for 5 µs	TSR + 25	µsec
8-bit Accuracy Recovery Time	T8R	LPBIT = 2.4V for 5 µs	80	µsec
Full Accuracy Recovery Time	TFAR	LPBIT = 2.4V for 5 µs	5	msec

FIGURE 8. 7809LP LPT™ TEST CIRCUIT

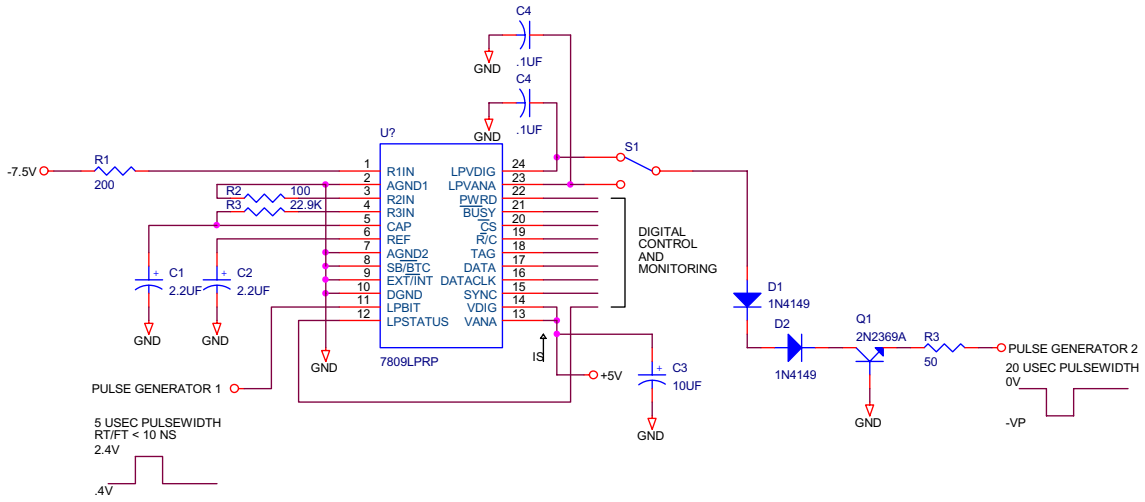


FIGURE 9. 7809LP LPT™ TIMING DIAGRAM

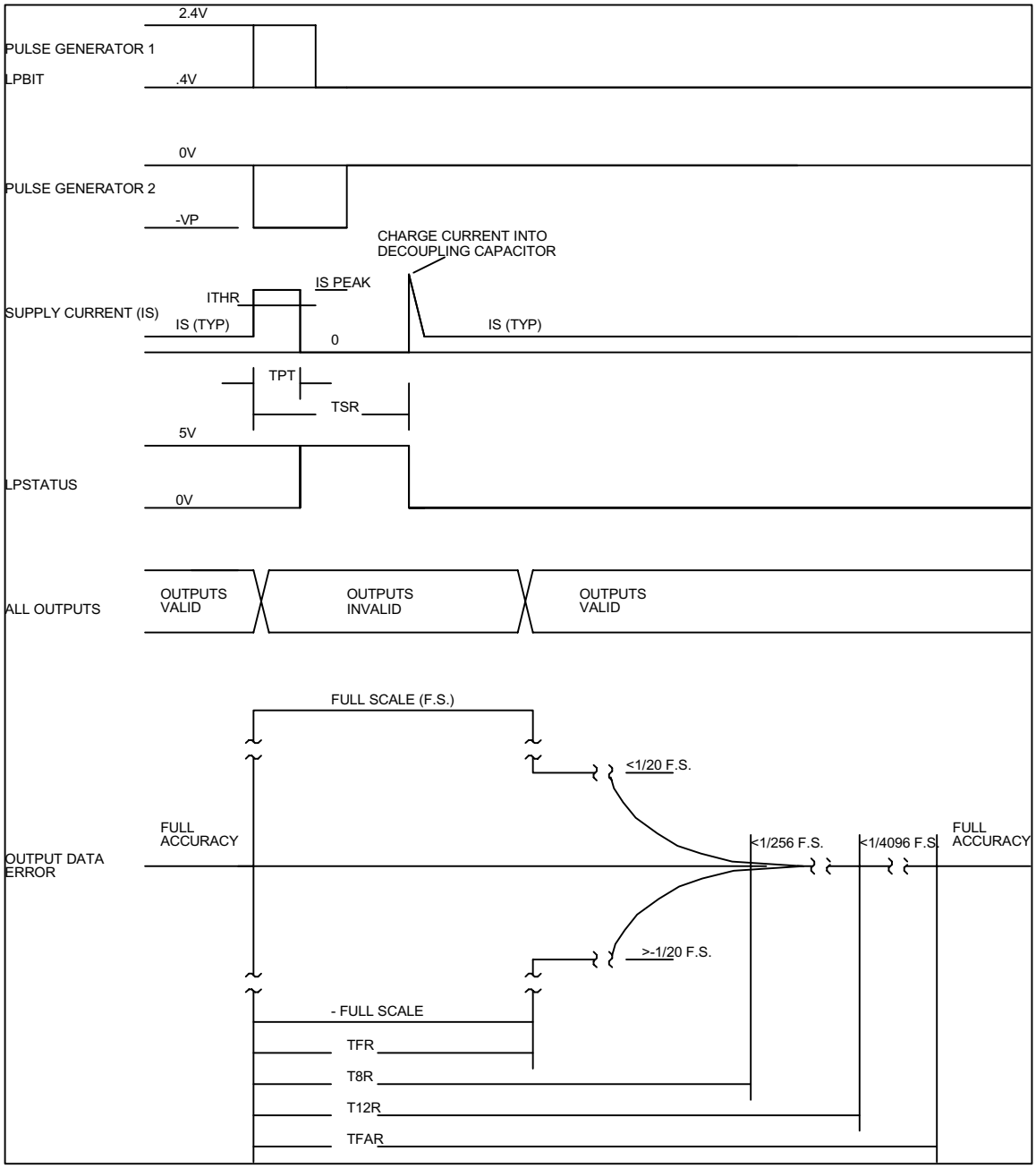


FIGURE 10. SEL CROSS SECTION

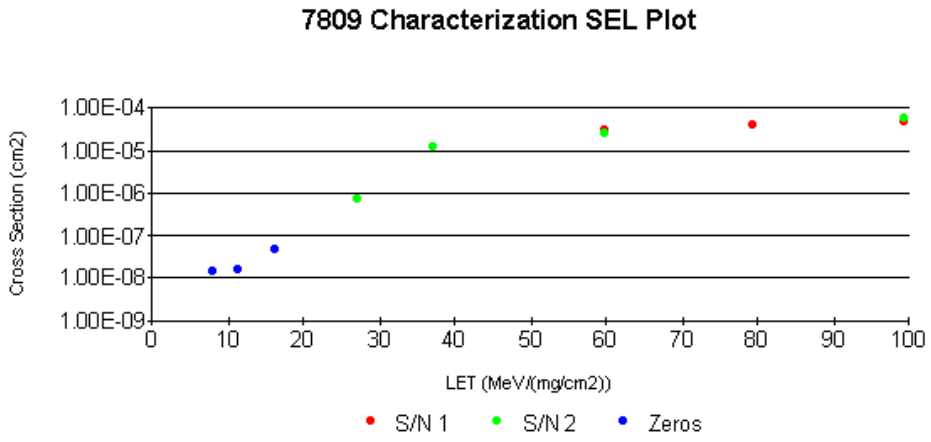
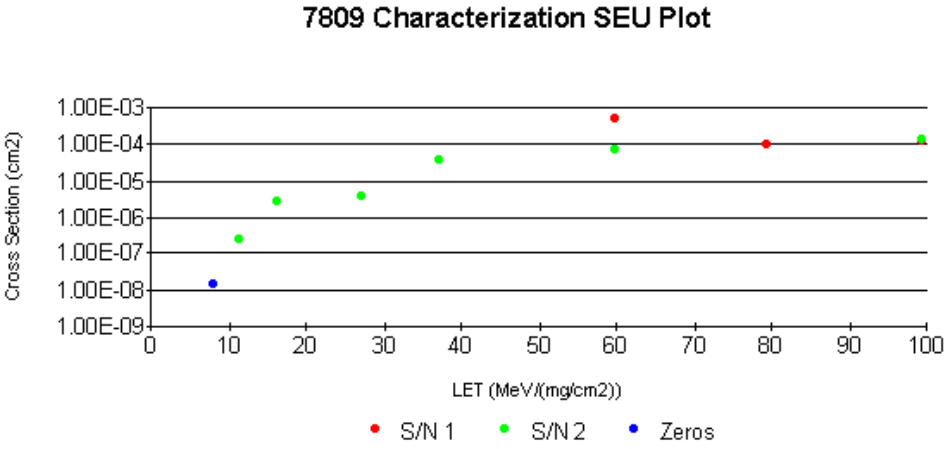
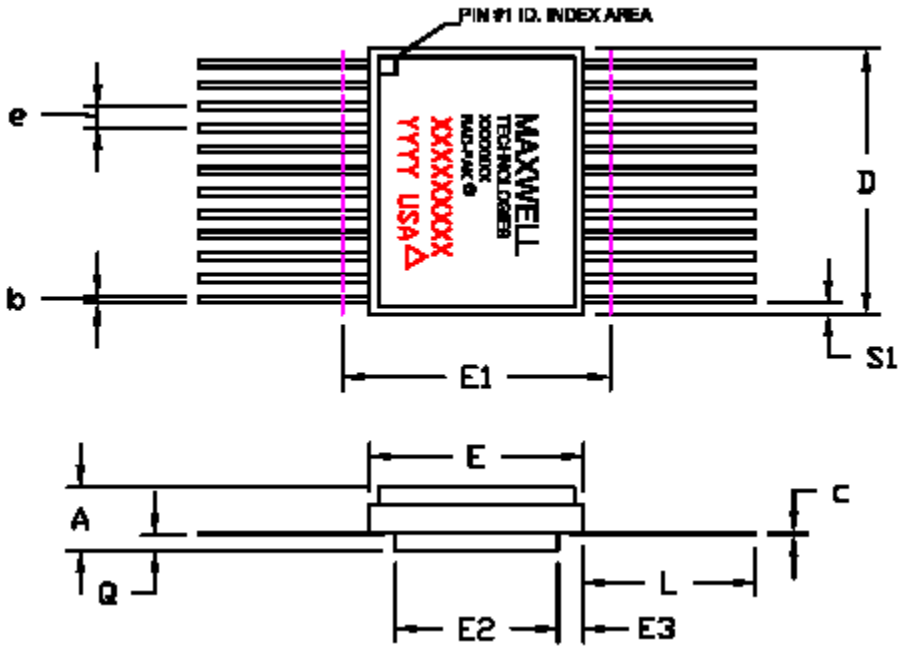


FIGURE 11. SEU CROSS SECTION





24-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.255	0.278	0.302
b	0.015	0.017	0.022
c	0.006	0.008	0.010
D	--	0.596	0.640
E	0.900	0.400	0.410
E1	--	--	0.440
E2	0.268	0.270	0.272
E3	0.055	0.065	--
e		0.050 BSC	
L	0.420	0.430	0.045
Q	0.040	0.045	0.006
S1	0.006	0.014	--
N		24	

Note: All dimensions in inches

Important Notice:

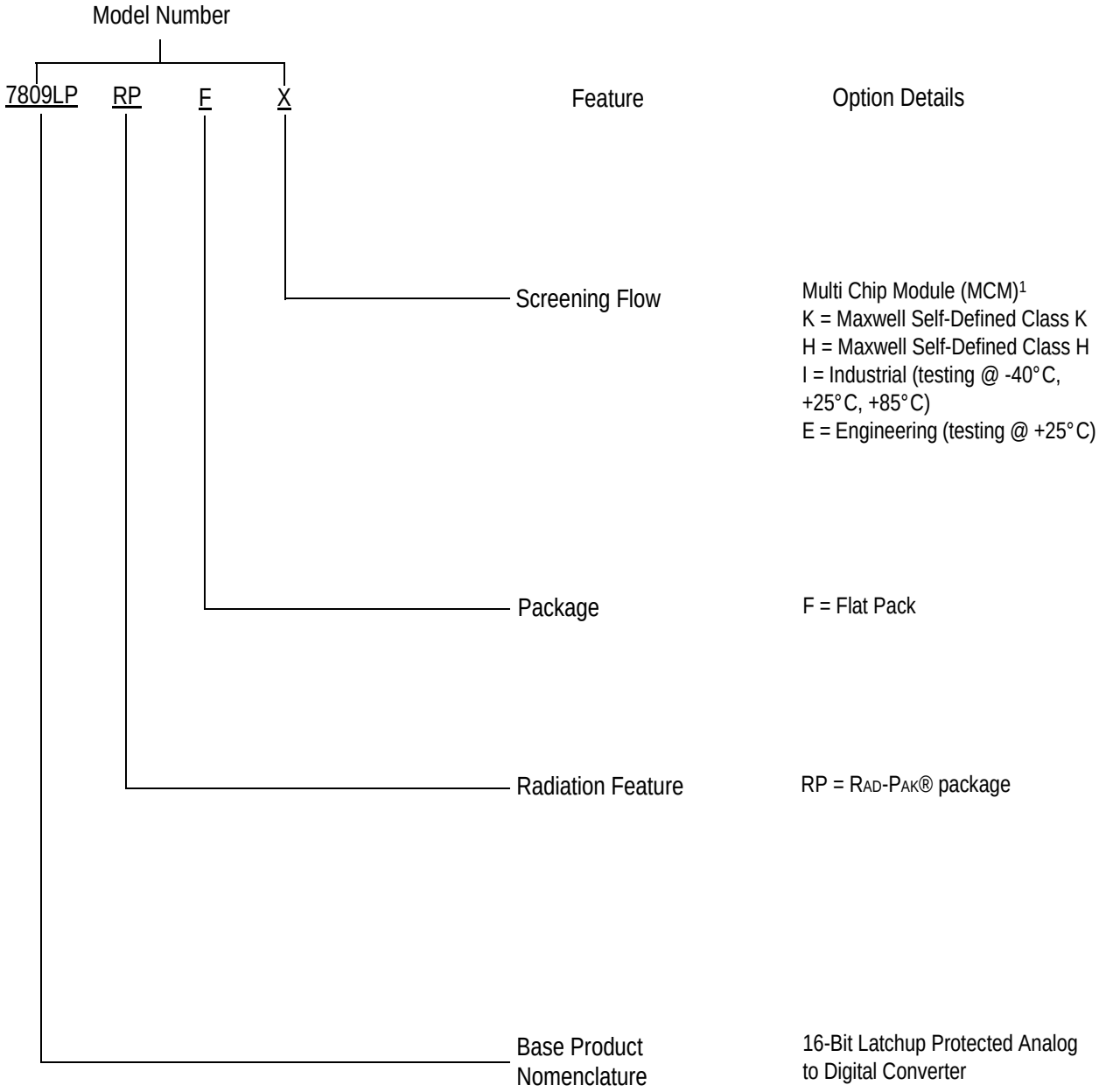
These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

Product Ordering Options



1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.