78M6618
Octal Power and Energy Measurement IC

DATA SHEET

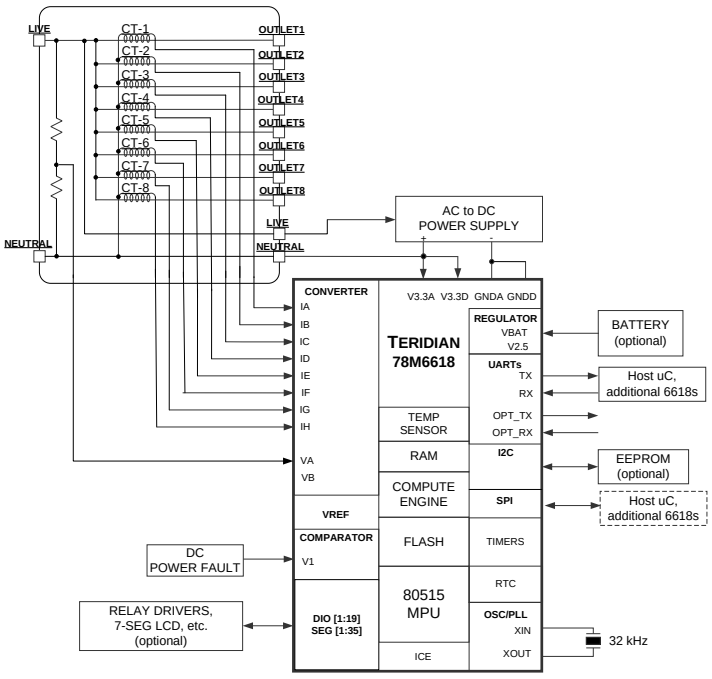
APRIL 2016

DESCRIPTION

The Teridian 78M6618 is a highly integrated IC for independent monitoring and measurement of up to eight single-phase AC outlets. With multiple host interface options, an integrated LCD driver, and configurable I/Os, the device is ideal for metered power distribution units (PDUs) and rack enclosures for the data center, as well as intelligent power strips and subpanels in the grid-friendly digital home.

At the measurement interface, the device provides 10 analog inputs for interfacing to voltage and current sensors. Scaled voltages from the sensors are fed to our Single Converter Technology® that uses a 21-bit delta-sigma ADC, independent 32-bit compute engine (CE), digital temperature compensation, and precision voltage references to provide better than 0.5% accuracy over a wide 2000:1 dynamic range.

The integrated MPU core and 128KB of flash memory provides a flexible means of configuration, post-processing, data formatting, interfacing to host processor through a UART or SPI™ interface, displaying output data to an LCD, or using DIO pins for intelligent relay control. Complete firmware for common applications is available from Teridian and can be loaded into the IC during manufacturing test. Alternatively, a complete array of ICE, development tools, and programming libraries are available to allow customization MPU code for each application.



FEATURES

- < 0.5% Wh Accuracy Over Wide 2000:1 Current Range and Over Temperature
- Exceeds IEC 62053/ANSI C12.20 Standards
- Voltage Reference < 40ppm/°C
- 10 Sensor Inputs—V3P3 Referenced
- 21-Bit Delta-Sigma ADC with Independent 32-Bit Compute Engine (CE)
- 8-Bit MPU (80515), One Clock Cycle per Instruction with 4KB MPU XRAM
- 128KB Flash with Security
- Integrated ICE for MPU Debug
- 32kHz Time Base with Hardware Watchdog Timer
- UART and High-Speed Slave SPI Host Interface Options
- Up to 19 General-Purpose 5V Tolerant I/O Pins
- LCD Driver (Up to 70 Pixels)
- Packaged in a Lead(Pb)-Free/RoHS-Compliant (6/6) 68-Pin QFN
- Robust Sub-Metering Application Firmware:
  - True RMS Calculations for Current, Voltage, Line Frequency, Real Power, Reactive Power, Apparent Power, and Power Factor
  - Accumulated Watt-Hours, Kilowatt-Hours, and Cost
  - Intelligent Switch Control at Zero Crossings
  - Digital Temperature Compensation
  - Phase Compensation (±15°)
  - Quick Calibration Routines
  - 46-64Hz Line Frequency Range with Same Calibration
  - Programmable Alarm Thresholds
  - High-Level UART Communication Protocols
  - High-Level SPI Communication Protocols

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1 Hardware Functional Description

1.1 Hardware Overview

The Teridian 78M6618 single-chip measurement and monitoring IC integrates all the primary AC measurement and control blocks required to implement an 8-outlet single-phase PDU with per outlet metering and intelligent relay control The 78M6618 includes:

- A ten-input analog front end (AFE)
- An independent digital computation engine (CE)
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference
- A temperature sensor
- RAM and Flash memory
- A variety of I/O pins
- LCD drivers

Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts and Rogowski coils.

In a sub-metering application, the 32-bit compute engine (CE) of the 78M6618 sequentially process the samples from the analog inputs on pins IA, IB, IC, ID, IE, IF, IG, IH, VA, VB and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h and V^2h for four-quadrant measurement. These measurements are then accessed by the MPU, processed further, and output via the peripheral devices available to the MPU.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of undesirable temperature effects on measurement accuracy. Temperature-dependent external components such as a crystal oscillator and current sensors can be characterized and their correction factors can be programmed to produce measurements with exceptional accuracy over the industrial temperature range.

A block diagram of the 78M6618 IC is shown in Figure 1. A detailed description of the various functional blocks follows.

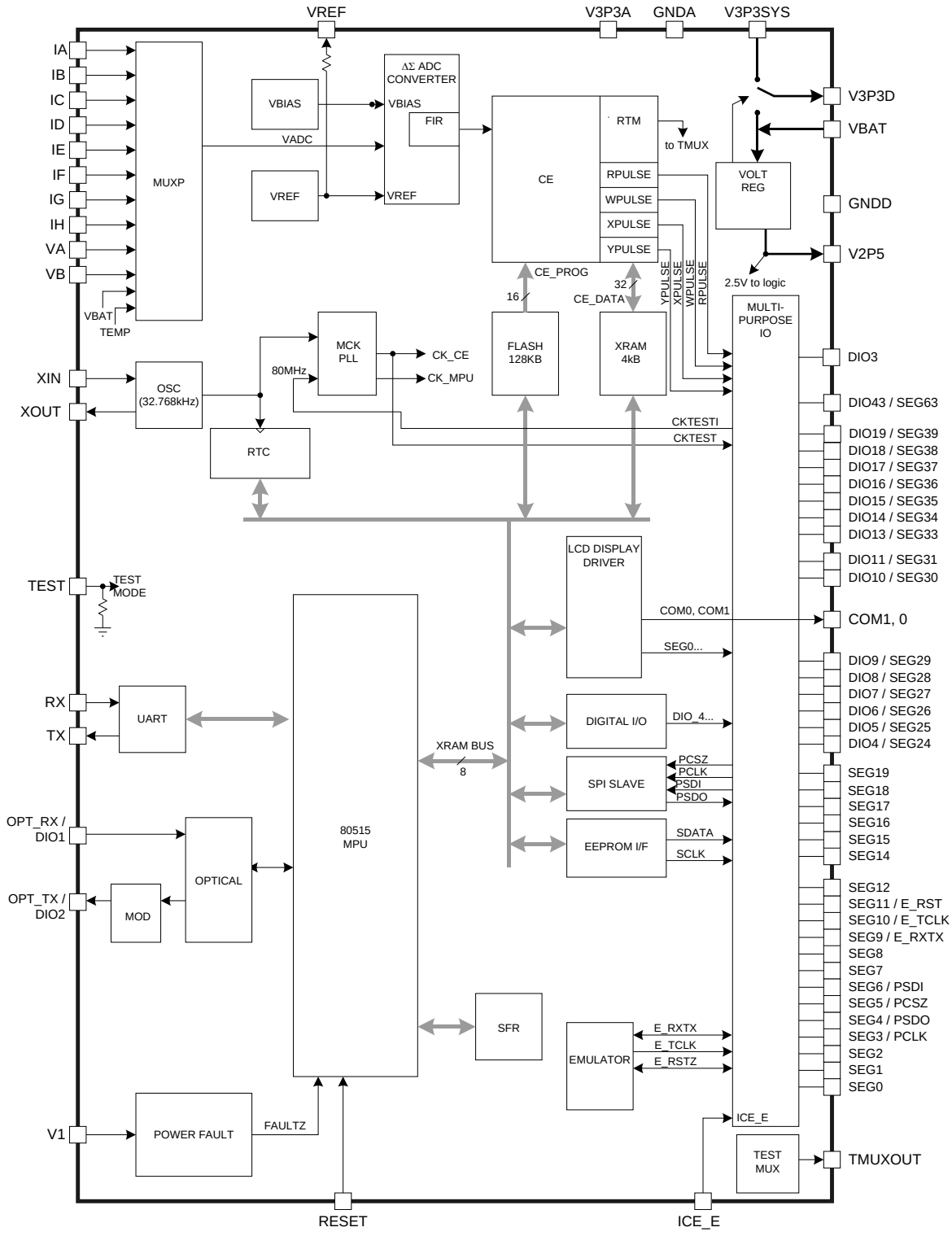


Figure 1: 78M6618 IC Functional Block Diagram

1.2 Device Reset

When the RESET pin is pulled high, all digital activity stops. Only the oscillator and RTC module continue to run. Additionally, all IORAM bits are set to their default states. As long as V1 (the input voltage at the power fault block) is greater than VBIAS, the internal 2.5 V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out. This will occur in 4096 cycles of the crystal clock after RESET goes low, at which time the MPU will begin executing its preboot and boot sequences from address 0x0000.

1.3 Power Management

1.3.1 Voltage Regulator

The 78M6618 provides an on chip voltage regulator to create a 2.5V supply for the digital logic. This regulator can be run off of the V3P3SYS or VBAT inputs depending upon power availability.

1.3.2 Power Fault Management

The 78M6618 includes both hardware and software controlled power fault management. V1 is connected to a comparator to monitor system power fault conditions. When the output of the comparator falls (V1<VBIAS) the device will enter BROWNOUT mode if there is sufficient voltage on VBAT. If there is not sufficient voltage on VBAT then the part will enter RESET mode.

1.3.3 BROWNOUT

In BROWNOUT mode the AFE, CE and other analog circuits are disabled leaving only the non-metering digital circuits running. The MPU is reduced to the crystal clock rate (32kHz). From BROWNOUT the 78M6618 SW may choose to voluntarily enter other power management modes. See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of the 78M6618 power management modes. If the overhead on VBAT is insufficient to maintain the BROWNOUT mode then the device will attempt to enter SLEEP mode. If power is restored the device will return to normal (mission mode) operation once the PLL has settled.

1.3.4 SLEEP Mode

SLEEP mode provides the savings in battery current as only the Oscillator, and RTC functions are active. As the CPU is disabled in SLEEP, the device can only wake up from SLEEP by the restoration of power or RTC autowake.

1.4 Analog Front End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. The main blocks in the AFE consist of an input multiplexer, a delta-sigma A/D converter, a FIR(Finite Impulse Response) filter and a voltage reference. The metrology input signals (IA→IH, VA, VB, VBAT and TEMP) are multiplexed before being sampled by the ADC. The ADC output is decimated by the FIR filter and the results are stored in XRAM where they can be accessed by the CE and the MPU. The AFE is programmable for various system requirements including but not limited to:

- Programmable Input Multiplexer settings
- Voltage reference, Battery and Temperature monitors inputs
- Programmable ADC sampling rate
- Programmable FIR length/resolution

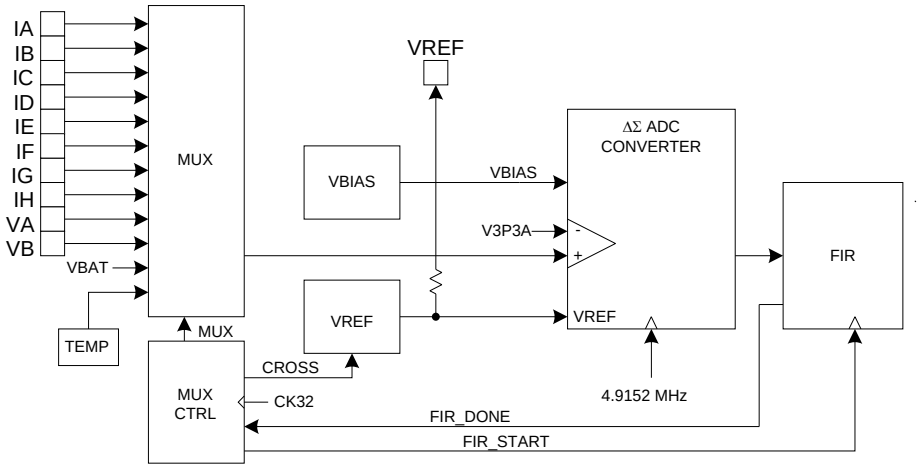


Figure 2: AFE Block Diagram

See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of the 78M6618 AFE.

1.4.1 Analog Current and Voltage Inputs

Pins *IA, IB, IC, ID, IE, IF, IG, IH, VA, VB* are analog inputs the AFE that provide support for measuring current and voltage in a variety of ways. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts and Rogowski coils.

1.5 Digital Computation Engine (CE)

The CE, a dedicated 32-bit digital signal processor, performs the precision computations necessary to accurately measure energy. Typically CE calculations and processes include:

- Scaling of the processed samples based on calibration coefficients.
- Frequency-insensitive delay cancellation on all channels
- 90° phase shifter (for narrowband VAR calculations).
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Multiplication of each voltage and current sample to obtain the energy per sample.
- RTM(Real Time Monitor) for debug purposes
- Pulse Generators used to output CE status indicators (e.g. SAG) directly to designated DIO pins.

Due to the custom nature and complexity of the CE, generally, pre-compiled CE code is provided by Teridian as a part of the available reference firmware and is not modified by the user. Please contact Teridian support for more information regarding CE code.

See the *78M6618 Programmer's Reference Manual* for more information on interfacing to and configuration of the 78M6618 CE.

1.6 80515 MPU Core

The 78M6618 includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally, a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the Intel® 8051 device running at the same clock frequency. See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of MPU Memory Organization, Special Function Registers, Interrupts, Counters, and other CPU controls.

1.6.1 SFR

Several custom Special Function Registers (SFR) registers are implemented in the 78M6618's 80515 MPU. See the *78M6618 Programmer's Reference Manual* for more information regarding the mapping of functionality to specific SFR and IORAM addresses.

1.7 XRAM

The CE and MPU share a single, general purpose 4 KB RAM (also referred to as XRAM) for data. The XRAM is natively accessible as 32bit words from the CE and on 8 bit boundaries from the CPU. The XRAM is accessed by the CPU through addresses 0x0000 to 0x0FFF.

1.8 IORAM

The MPU accesses most of its external input and output functionality as well as programmable functionality through memory mapped IO (IORAM). The IORAM is accessed by the CPU as data addresses 0x2000 to 0x20FF. See the *78M6618 Programmer's Reference Manual* for more information regarding the mapping of functionality to specific IORAM addresses.

1.9 FLASH

The 78M6618 includes 128 KB of on-chip Flash memory. For read/write access from the CPU, the flash is broken into four 32 KB banks that are managed by SFR settings. For erasing of the flash memory from the CPU the flash is segmented into individual 1024-byte pages and also controlled by SFR settings. See the *78M6618 Programmer's Reference Manual* for more information regarding the use of flash and the mapping of functionality to specific SFR settings.

1.9.1 Program Security

The 78M6618 has functionality to guarantee the security of the user's MPU and CE program code. When enabled, the security feature limits the ICE to global Flash erase operations only. All other ICE operations are blocked. Security is enabled by MPU code that is executed in a pre-boot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the Flash, followed by a chip reset.

1.10 Oscillator

The 78M6618 oscillator drives a standard 32.768 kHz watch crystal. These crystals are accurate and do not require a high-current oscillator circuit. The 78M6618 oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability.

The oscillator is powered directly and only from the VBAT pin, which therefore must be connected to a DC voltage source not to exceed 4 V. The oscillator requires approximately 100 nA, which is negligible compared to the internal leakage of a battery

Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

1.11 PLL and Internal Clock Generation

Timing for the device is derived from the 32.768 kHz crystal oscillator output. The PLL and on-chip timing functions provide several clocks which include:

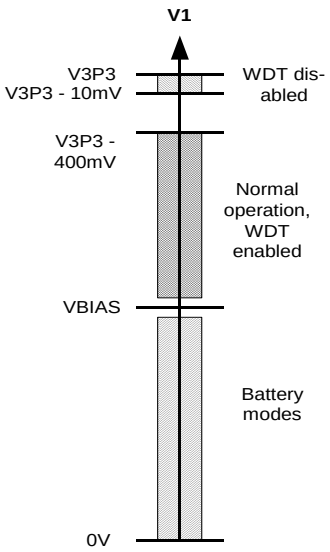
- The MPU clock (CKMPU)
- The emulator clock (2 x CKMPU)
- The clock for the CE (CKCE)
- The delta-sigma ADC and FIR clock(CKADC, CKFIR)

These internal clocks can be adjusted for various programmable rates which affect device functionality. See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of the 78M6618 PLL and internal clock generation modules.

1.12 Real-Time Clock (RTC)

The RTC circuit is driven directly by the crystal oscillator. The RTC consists of a counter chain and output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year (including leap years). See the *78M6618 Programmer's Reference Manual* for more information regarding the use of the 78M6618 RTC.

1.13 Hardware Watchdog Timer



In addition to the basic watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, watchdog timer (WDT) is included in the device. It uses the crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time the WDT overflows, and the part is reset as if the RESET pin were pulled high, except that the IORAM bits will be maintained. 4096 oscillator cycles (or 125 ms) after the WDT overflow, the MPU will be launched from program address 0x0000. Asserting ICE_E will deactivate the WDT.

The WDT can also be disabled by tying the V1 pin to V3P3. This also deactivates V1 power fault detection. Since there is no method in firmware to disable the crystal oscillator or the WDT, it is guaranteed that whatever state the part might find itself in, upon watchdog overflow, the part will be reset to a known state.

Figure 3: Functions Defined by V1

1.14 Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system. See the *78M6618 Programmer's Reference Manual* for more information regarding the use of the 78M6618 Temperature Sensor.

1.15 General Purpose Digital I/O

The 78M6618 includes up to 19 pins of general-purpose digital I/O. When configured as inputs, these pins are 5V compatible (no current-limiting resistors are needed). On reset or power-up, all DIO pins are inputs until they are configured for the desired direction under MPU control. The Digital I/O pins can be categorized as follows:

- DIO1/OPT_RX, DIO2/OPT_TX (2 pins) UART/DIO pin
- DIO3 (1 pin) Dedicated DIO pin
- DIO4/SEG24 -- DIO11/SEG31 (8 pins) LCD/DIO pins
- DIO13/SEG33 -- DIO19/SEG39 (7 pins) LCD/DIO pins
- DIO43/SEG63 (1 pin) LCD/DIO pin

1.16 LCD Drivers

The 78M6618 contains a total of 35 dedicated and multiplexed LCD drivers which are grouped as follows:

- 11 dedicated LCD segment drivers.
- 3 drivers multiplexed with the ICE interface (E_TCLK, E_RST, E_RXTX).
- 1 driver multiplexed with auxiliary signal CKTEST (SEG19).
- 4 drivers multiplexed with the SPI port (PCLK, PSDO, PCSZ, PSDI).
- 16 drivers multiplexed with general purpose DIO pins.
- 2 common drivers for multiplexing (50%, or 100% duty cycle) – always available.

With a minimum of 15 driver pins always available and a total of 35 driver pins in the maximum configuration, the device is capable of driving between 30 to 70 pixels of LCD display. At eight pixels per digit, this corresponds to 3 to 8 digits. The following dedicated and multi-use pins can be assigned as LCD segment pins for the 78M6618:

- 11 dedicated LCD segment pins: SEG0 to SEG2, SEG7, SEG8, SEG12, SEG14 to SEG18.
- 8 dual-function pins: SEG3/PCLK, SEG4/PSDO, SEG5/PCSZ, SEG6/PSDI, E_RXTX/SEG9, E_TCLK/SEG10, E_RST/SEG11, and SEG19/CKTEST.
- 16 combined DIO and segment pins: SEG24/DIO4 to SEG31/DIO11, SEG33/DIO13 to SEG39/DIO19, and SEG63/DIO43. Of which, DIO7/SEG27 through DIO15/SEG35 can be used for controlling relays.

See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of the 78M6618 LCD drivers. See the 78M6618 Hardware Design Guidelines for more information regarding connecting the 78M6618 LCD drivers to LCDs.

1.17 EEPROM Interface

The 78M6618 provides hardware support for an optional two-pin or a three-wire (µ-wire) EEPROM interface.

Two-Pin EEPROM Interface

The dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto the DIO4 (SCK) and DIO5 (SDA) pins.

Three-Wire (µ-Wire) EEPROM Interface

A 500 kHz three-wire interface, using SDATA, SCK and a DIO pin for CS is also available.

See the *78M6618 Programmer's Reference Manual* for more information regarding the programmability of the 78M6618 EEPROM interfaces. See the *78M6618 Hardware Design Guidelines* for more information regarding connecting the 78M6618 EEPROM interfaces to various EEPROM.

1.18 SPI Slave Port

The slave SPI port communicates directly with the MPU data bus and is able to directly read and write XRAM and IORAM locations. It is also able to send commands to the MPU. The interface to the slave port consists of the PCSZ, PCLK, PSDI and PSDO pins. These pins are multiplexed with the LCD segment driver pins SEG3 to SEG6.

A typical SPI transaction is as follows. While PCSZ is high, the port is held in an initialized/reset state. During this state, PSDO is held in HiZ state and all transitions on PCLK and PSDI are ignored. When PCSZ falls, the port will begin the transaction on the first rising edge of PCLK. A transaction consists of an 8-bit command, a 16-bit address and then one or more bytes of data. The transaction ends when PCSZ is raised. Some transactions may consist of a command only. The last SPI command and address (if part of the command) are available in the IORAM.

The SPI port supports data transfers at up to 1 Mb/s. The SPI commands are described in Table 1 and Figure 4 illustrates the SPI Interface read and write timing.

Table 1: SPI Command Description

Command	Description
`11xx xxxx ADDR D0 ... DN`	Output data on PSDO is read from RAM starting with byte at ADDR. ADDR will auto-increment until PCSZ is raised. MPU SPI interrupt is generated
`1100 0000 ADDR D0 ... DN`	Output data on PSDO is read from RAM starting with byte at ADDR. ADDR will auto-increment until PCSZ is raised. No MPU SPI interrupt is generated
`10xx xxxx ADDR D0 ... DN`	Input data on PSDI is written to RAM starting with byte at ADDR. ADDR will auto-increment until PCSZ is raised. MPU SPI interrupt is generated
`1000 0000 ADDR D0 ... DN`	Input data on PSDI is written to RAM starting with byte at ADDR. ADDR will auto-increment until PCSZ is raised. No MPU SPI interrupt is generated
`CMD ADDR D0 ... DN`	CMD and ADDR are available to the CPU in IORAM `D0 … DN` are ignored. MPU SPI interrupt is generated

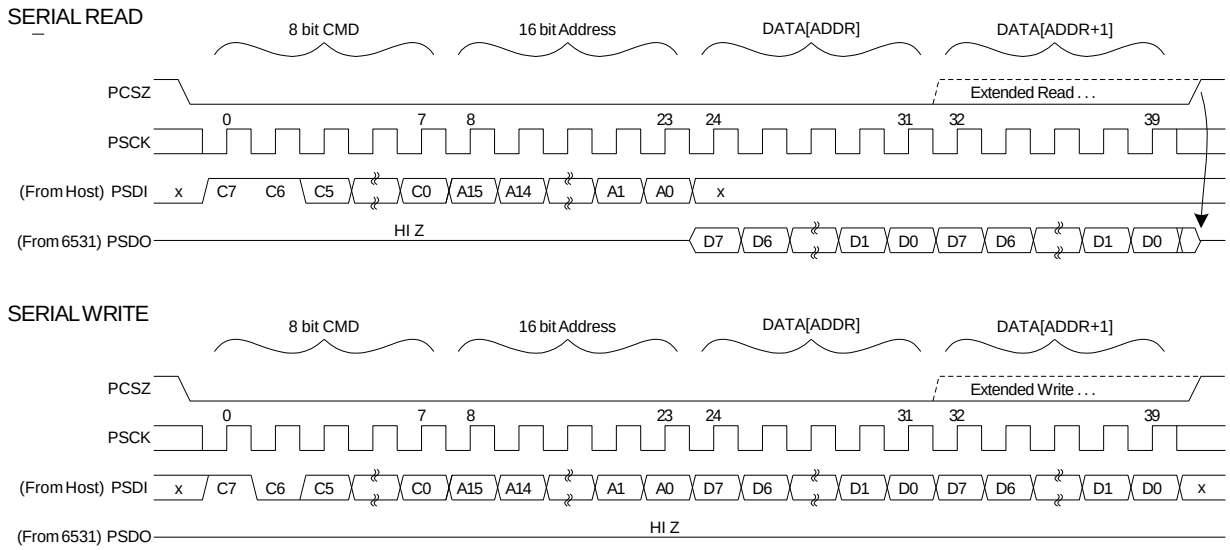


Figure 4: SPI Slave Port: Typical Read and Write Operations

Since the addresses are in 16-bit format, any type of XRAM data can be accessed: CE, MPU or IORAM but not SFRs or the 80515-internal register bank. See the *78M6618 Programmer's Reference Manual* for more information regarding the mapping and use of SPI functions.

1.19 Test Port

One out of 16 digital or 8 analog signals can be selected to be output on the TMUXOUT pin. See the *78M6618 Programmer's Reference Manual* for more information regarding the use of TMUXOUT.

1.20 UARTs

The 78M6618 includes two UARTs (UART0 and UART1) that can be programmed to communicate with a variety of external devices. The UARTs are dedicated 2-wire serial interfaces, which can communicate at rates up to 38,400 bits/s. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38,400 bps. See the *78M6618 Programmer's Reference Manual* for more information regarding the use of the UART resources.

1.20.1 UART1 (OPT_TX/OPT_RX)

The device includes an interface to implement an IR/optical port on UART1. The pin OPT_TX is designed to directly drive an external LED for transmitting data on an optical link. The pin OPT_RX has the same threshold as the RX(UART0) pin, but can also be used to sense the input from an external photo detector used as the receiver for the optical link. Alternately, the UART1 may be interfaced with a standard level UART transceiver. Contact Teridian support for more information.

1.21 In Circuit Emulator (ICE) Port

The 78M6618 implements an In Circuit Emulator(ICE) port for debug and programming of the device. To enable the use of the port the ICE_E pin must be pulled high. In this mode the SEG11,SEG10 and SEG9 pins are repurposed and the E_RST, E_TCLK and E_RXTX pins respectively. Please contact Teridian support for more information regarding the use of the ICE interface for device programming and debug.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2 shows the absolute maximum ranges for the device. Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under recommended operating conditions (Section 4.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

Table 2: Absolute Maximum Ratings

Voltage and Current	
Supplies and Ground Pins	
V3P3SYS, V3P3A	-0.5 V to 4.6 V
VBAT	-0.5 V to 4.6 V
GNDD	-0.5 V to +0.5 V
Analog Output Pins	
V3P3D	-10 mA to 10 mA, -0.5 V to 4.6 V
VREF	-10 mA to +10 mA, -0.5 V to V3P3A+0.5 V
V2P5	-10 mA to +10 mA, -0.5 V to 3.0 V
Analog Input Pins	
IA, IB, IC, ID, IE, IF, IG, IH, VA, VB, V1	-10 mA to +10 mA -0.5 V to V3P3A+0.5 V
XIN, XOUT	-10 mA to +10 mA -0.5 V to 3.0 V
All Other Pins	
Configured as SEG or COM drivers	-1 mA to +1 mA, -0.5 to V3P3D+0.5
Configured as Digital Inputs	-10 mA to +10 mA, -0.5 to 6 V
Configured as Digital Outputs	-15 mA to +15 mA, -0.5 V to V3P3D+0.5 V
All other pins	-0.5 V to V3P3D+0.5 V
Temperature and ESD Stress	
Operating Junction Temperature (peak, 100ms)	+140°C
Operating Junction Temperature (continuous)	+125°C
Storage Temperature Range	-45°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C
ESD Stress on All Pins	±4kV

2.2 Recommended External Components

Table 3: Recommended External Components

Name	From	To	Function	Value	Unit
C1	V3P3A	AGND	Bypass capacitor for 3.3 V supply	≥0.1 ±20%	µF
C2	V3P3D	DGND	Bypass capacitor for 3.3 V output	0.1 ±20%	µF
CSYS	V3P3SYS	DGND	Bypass capacitor for V3P3SYS	≥1.0 ±30%	µF
C2P5	V2P5	DGND	Bypass capacitor for V2P5	0.1 ±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF.	32.768	kHz
CXS	XIN	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	33 ±10%	pF
CXL	XOUT	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	15 ±10%	pF

Notes:

1. AGND and DGND should be connected together.
2. V3P3SYS and V3P3A should be connected together.

2.3 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS, V3P3A**:** 3.3 V Supply Voltage V3P3A and V3P3SYS must be at the same voltage	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.6	V
VBAT	No Battery	Externally Connect to V3P3SYS			
	Battery Backup: BRN and LCD modes SLEEP mode	 3.0 2.0		 3.8 3.8	 V V
Operating Temperature		-40		+85	ºC

2.4 Performance Specifications

2.4.1 Input Logic Levels

Table 5: Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage[a], V_{IH}		2			V
Digital low-level input voltage[a], V_{IL}				0.8	V
Input pull-up current, I_{IL} E_RXTX, E_RST, CKTEST Other digital inputs	VIN=0 V, ICE_E=1	 10 10 -1	 0	 100 100 1	 µA µA µA
Input pull down current, I_{IH} ICE_E RESET Other digital inputs	VIN = V3P3D	 10 10 -1	 0	 100 100 1	 µA µA µA

[a] In battery powered modes, digital inputs should be below 0.3 V or above 2.5 V to minimize battery current.

2.4.2 Output Logic Levels

Table 6: Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V3P3D–0.4			V
	I_{LOAD} = 15 mA	V3P3D-0.6			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0		0.4	V
	I_{LOAD} = 15 mA			0.8	V
OPT_TX V_{OH} (V3P3D-OPT_TX)	I_{SOURCE}=1 mA			0.4	V
OPT_TX V_{OL}	I_{SINK}=20 mA			0.7	V

2.4.3 Power-Fault Comparator

Table 7: Power-Fault Comparator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Offset Voltage: V1-VBIAS		-20		+15	mV
Hysteresis Current: V1	Vin = VBIAS – 100 mV	0.8		1.2	µA
Response Time: V1	±100 mV overdrive Voltage at V1 rising Voltage at V1 falling	 10	 8 37	 100 100	 µs µs
WDT Disable Threshold: V1-V3P3A		-400		-10	mV

2.4.4 Battery Monitor

Table 8: Battery Monitor Performance Specifications (*BME*= 1)

Parameter		Condition	Min	Typ	Max	Unit
Load Resistor			27	45	63	kΩ
LSB Value	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	*FIR_LEN*=0(L=138) *FIR_LEN*=1(L=288)	(-10%)	-48.7 -5.35	(+10%)	µV µV
	[*M40MHZ*, *M26MHZ*] = [01]	*FIR_LEN*=0(L=186) *FIR_LEN*=1(L=384)	(-10%)	-19.8 -2.26	(+10%)	µV µV
Offset Error			-200	0	+100	mV

2.4.5 Supply Current

Table 9: Supply Current Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS current (CE off)	Normal Operation, V3P3A = V3P3SYS = 3.3 V CKMPU = 614 kHz No Flash Memory write *RTM_E*=0, *ECK_DIS*=1, *ADC_E*=1, *ICE_E*=0		4.2	6.35	mA
V3P3SYS current (CE on)			8.4	9.6	mA
V3P3A current			3.3	3.8	mA
VBAT current		-400		+400	nA
V3P3SYS current, Write Flash	Normal Operation as above, except write Flash at maximum rate, *CE_E* = 0, *ADC_ E* = 0		9.1	12	mA
VBAT current	VBAT=3.6 V BROWNOUT mode LCD Mode, LCD DAC off <25°C over temperature LCD Mode, LCD DAC on <25°C over temperature SLEEP Mode, 25°C SLEEP Mode, over temperature		 52 11 15 16 21 0.5 0.7	 250 20 30 25 35 1 1.5	 µA µA µA µA µA µA µA

2.4.6 V3P3D Switch

Table 10: V3P3D Switch Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
On resistance – V3P3SYS to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA		9	15	Ω
On resistance – VBAT to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA		32	50	Ω

2.4.7 2.5 V Voltage Regulator

Table 11: 2.5 V Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	Iload = 0	2.3	2.5	2.7	V
V2P5 load regulation	Iload = 0 mA to 5 mA			40	mV
Voltage overhead V3P3-V2P5	Iload = 5 mA, reduce V3P3 until V2P5 drops 200 mV			470	mV
PSSR ΔV2P5/ΔV3P3	RESET=0, iload=0	-2		+2	mV/V

2.4.8 Low-Power Voltage Regulator

Unless otherwise specified, V3P3SYS = V3P3A = 0.

Table 12: Low-Power Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	I_{LOAD} = 0	2.3	2.5	2.7	V
V2P5 load regulation	I_{LOAD} = 0 mA to 1 mA			30	mV
VBAT voltage requirement	I_{LOAD} = 1 mA, reduce VBAT until REG_LP_OK = 0			3.0	V
PSRR ΔV2P5/ΔVBAT	I_{LOAD} = 0	-50		50	mV/V

2.4.9 Crystal Oscillator

Table 13: Crystal Oscillator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power to Crystal [4]	Crystal connected			1	µW
XIN to XOUT Capacitance [1]				3	pF
Capacitance to DGND [1] XIN XOUT	RTCA_ADJ = 0			 5 5	 pF pF

2.4.10 LCD DAC

Table 14: LCD DAC Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VLCD Voltage $V_{LCD} = V3P3 \cdot (1 - 0.059 \cdot LCD_DAC) - 0.019V$	$1 \le LCD_DAC \le 7$	-10		+10	%

2.4.11 LCD Drivers

The information in Table 15 applies to all COM and SEG pins with *LCD_DAC*[2:0] = 000.

Table 15: LCD Driver Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VLC2 Voltage	With respect to VLCD[1]	-0.1		+0.1	V
VLC0 Voltage, ½ bias	With respect to VLC2/2	-4		+1	%
VLC0 Impedance	ΔILOAD = 100 µA (Isink)		9	15	kΩ
	ΔILOAD = -100 µA (Isource)		9	15	

[1]VLCD is V3P3SYS in MISSION mode and VBAT in BROWNOUT and LCD modes.

2.4.12 Optical Interface

Table 16: Optical Interface Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
OPT_TX VOH (V3P3D-OPT_TX)	ISOURCE = 1 mA			0.4	V
OPT_TX VOL	ISINK = 20 mA			0.7	V

2.4.13 Temperature Sensor

Table 17 shows the performance for the temperature sensor. The LSB values do not include the 8-bit left shift at CE input.

Table 17: Temperature Sensor Performance Specifications

Parameter		Condition	Min	Typ	Max	Unit
Nominal relationship: $N(T) = S_n*(T-T_n) + N_n$, T_n = 25ºC						
Nominal Sensitivity (S_n) $S_n = -0.00107 \cdot \left(\frac{L}{3}\right)^3$	[*M26MHZ, M40MH*] = [00], [01], or [11]	*FIR_LEN*=0 (L=138) *FIR_LEN*=1 (L=288)		-104 -947		LSB/ºC
	[*M26MHZ, M40MHZ*] = [10]	*FIR_LEN*=0 (L=186)		-255		
Nominal Offset (N_n) [4] $N_n = 0.510 \cdot \left(\frac{L}{3}\right)^3$	[*M26MHZ, M40MH*] = [00], [01], or [11]	*FIR_LEN*=0 (L=138) *FIR_LEN*=1 (L=288)		49641 451200		LSB
	[*M26MHZ, M40MHZ*] = [10]	*FIR_LEN*=0 (L=186)		121500		
Temperature Error [2] $ERR = T - \left\{\frac{(N(T) - N_n)}{S_n} + T_n\right\}$		T_n = 25°C, T = -40ºC to +85ºC	-10[1]		10[1]	ºC

[1] Guaranteed by design; not production tested.

[2] N_n is measured at T_n during measurement calibration and is stored in MPU or CE for use in temperature calculations.

2.4.14 VREF

Table 18 shows the performance specifications for VREF. Unless otherwise specified, $VREF_DIS$ = 0.

Table 18: VREF Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VREF output voltage, VREF(22)	Ta = 22ºC	1.193	1.195	1.197	V
VREF chop step				40	mV
VREF power supply sensitivity ΔVREF / ΔV3P3A	V3P3A = 3.0 to 3.6 V	-1.5		1.5	mV/V
VREF input impedance	$VREF_DIS$ = 1, VREF = 1.3 to 1.7 V	100			kΩ
VREF output impedance	CAL =1, I_{LOAD} = 10 μA, -10 μA			2.5	kΩ
VNOM definition[2]	$VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^2 TC2$				V
VNOM temperature coefficients: TC1 TC2		3.18·(52.46-$TRIMT$) -0.444			 μV/ºC μV/°C[2]
VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM(T)}\frac{10^6}{\max(\lvert T-22\rvert,40)}$		-40[1]		+40[1]	PPM/ºC
VREF aging			±25		PPM/ year

[1] Guaranteed by design; not production tested.

[2] This relationship describes the nominal behavior of VREF at different temperatures.

2.4.15 ADC Converter, V3P3A Referenced

Table 19 shows the performance specifications for the ADC converter, V3P3A referenced. For this data, *FIR_LEN*=0, *VREF_DIS*=0 and LSB values do not include the 9-bit left shift at the CE input.

Table 19: ADC Converter Performance Specifications

Parameter		Condition	Min	Typ	Max	Unit
Recommended Input Range (Vin-V3P3A)			-250		250	mV peak
Voltage to Current Crosstalk $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$		Vin = 200 mV peak, 65 Hz, on VA. Vcrosstalk = largest measurement on IA or IB	-10[1]		10[1]	µV/V
THD (First 10 harmonics) [1]: 250 mV-pk 20 mV-pk		Vin=65 Hz, 64 kpts FFT, Blackman-Harris window CKCE = 5 MHz			 -75 -90	 dB dB
Input Impedance		Vin = 65 Hz	40		90	kΩ
Temperature coefficient of Input Impedance		Vin = 65 Hz		1.7		Ω/°C
LSB size $V_{LSB} = V_{REF} \cdot \frac{1.25}{4.75} \cdot \left(\frac{3}{L}\right)^3$ *L* = FIR length	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	*FIR_LEN*=0 *FIR_LEN*=1		3231 355		nV/ LSB
	[*M40MHZ*, *M26MHZ*] = [01]	*FIR_LEN*=0		1319		nV/ LSB
Digital Full Scale $\left(\frac{L}{3}\right)^3$ *L* = FIR length	[*M40MHZ*, *M26MHZ*] = [00], [10], or [11]	*FIR_LEN*=0 *FIR_LEN*=1		±97336 ±884736		LSB
	[M40MHZ, M26MHZ] = [01]	*FIR_LEN*=0		±238328		LSB
ADC Gain Error versus %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$		Vin=200 mV pk, 65 Hz V3P3A=3.0 V, 3.6 V			50	ppm/%
Input Offset (Vin-V3P3A)			-10		10	mV

[1] Guaranteed by design; not production tested.

2.5 Timing Specifications

2.5.1 Flash Memory

Table 20: Flash Memory Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
Flash write cycles	-40°C to +85°C	20,000			Cycles
Flash data retention	25°C	100			Years
Flash data retention	85°C	10			Years
Flash byte write operations between page or mass erase operations				2	Cycles
Write Time per Byte				42	µs
Page Erase (1024 bytes)				20	ms
Mass Erase				200	ms

2.5.2 EEPROM Interface

Table 21: EEPROM Interface Timing

Parameter	Condition	Min	Typ	Max	Unit
Write Clock frequency (I^2C)	CKMPU = 4.9152 MHz, Using interrupts		78		kHz
	CKMPU = 4.9152 MHz, bit-banging DIO4/5		150		kHz
Write Clock frequency (3-wire)	CKMPU = 4.9152 MHz		500		kHz

2.5.3 RESET

Table 22: RESET Timing

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse width		5			µs
Reset pulse fall time				1[1]	µs

[1] Guaranteed by design; not production tested.

2.5.4 RTC

Table 23: RTC Range

Parameter	Condition	Min	Typ	Max	Unit
Range for date		2000		2255	year

2.5.5 SPI Slave Port (MISSION Mode)

Table 24: SPI Slave Port (MISSION Mode) Timing

Parameter	Condition	Min	Typ	Max	Unit
t_{SPIcyc} PCLK cycle time		1			µs
$t_{SPILead}$ Enable lead time		15			ns
t_{SPILag} Enable lag time		0			ns
t_{SPIW} PCLK pulse width: High Low		 40 40			 ns ns
t_{SPISCK} PCSZ to first PCLK fall	Ignore if PCLK is low when PCSZ falls.	2			ns
t_{SPIDIS} Disable time		0			ns
t_{SPIEV} PCLK to Data Out				15	ns
t_{SPISU} Data input setup time		10			ns
t_{SPIH} Data input hold time		5			ns

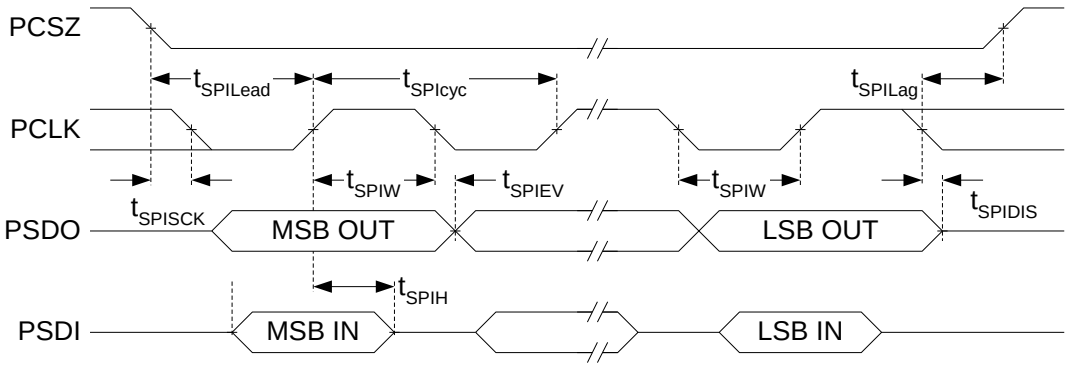


Figure 5: SPI Slave Port (MISSION Mode) Timing

3 Packaging

3.1 68-Pin QFN Package

3.1.1 Pinout

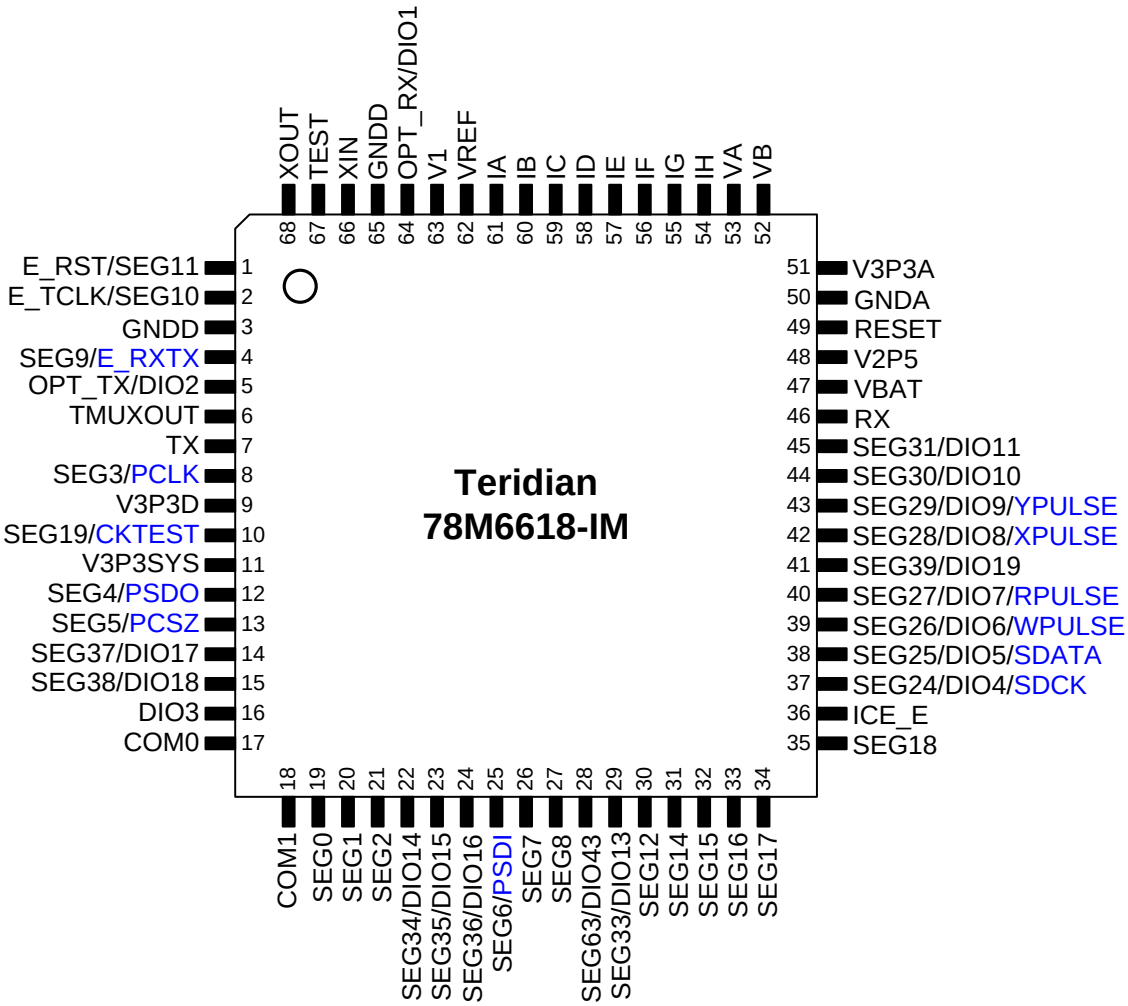


Figure 6: Pinout for QFN-68 Package

3.1.2 68-Pin QFN Package Outline

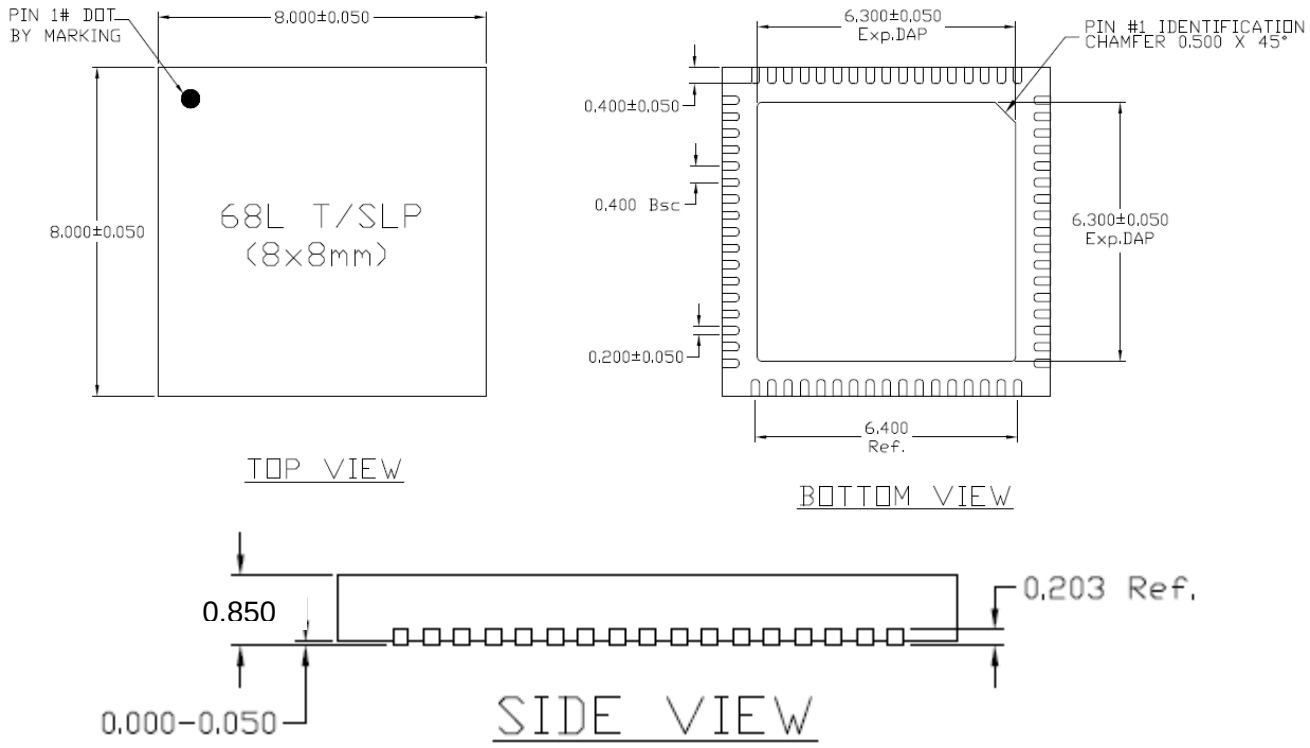


Figure 7: QFN-68 Package Outline (Top, Bottom, and Side View)

NOTE:
Controlling dimensions are in mm
Pin length is nominally 0.4mm (min. 0.3 mm, max 0.4 mm).

3.1.3 Recommended PCB Land Pattern for the QFN-68 Package

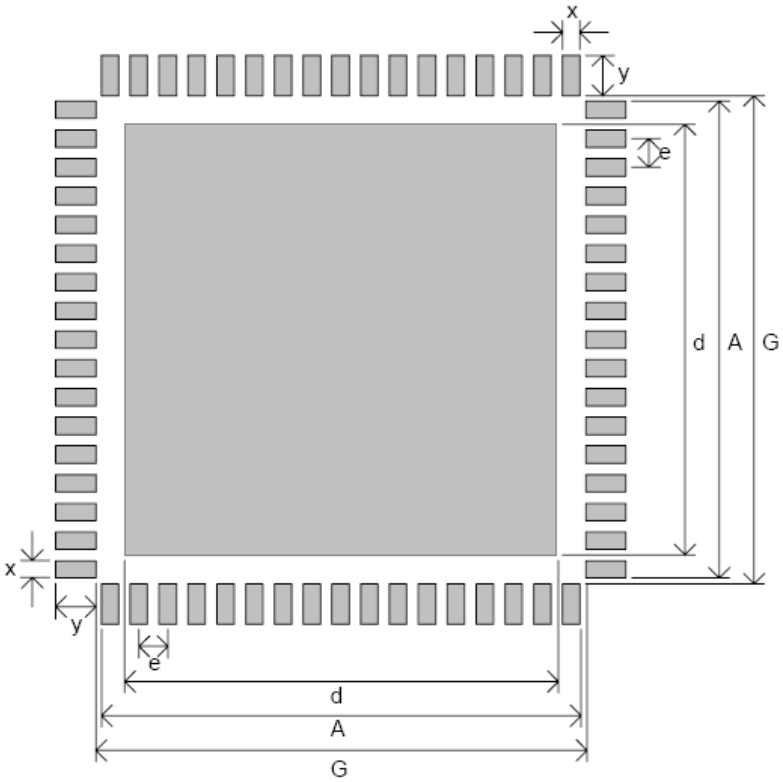


Figure 8: PCB Land Pattern for QFN 68 Package

Table 25: Recommended PCB Land Pattern Dimensions

Symbol	Description	Typical Dimension
e	Lead pitch	0.4 mm
x	Pad width	0.23 mm
y	Pad length. Nee Note 3.	0.8 mm
d	See Note 1	6.3 mm
A		6.63 mm
G		7.2 mm

Notes:

1. Do not place unmasked vias in the region denoted by dimension d.
2. Soldering of bottom internal pad is not required for proper operation.
3. The y dimension has been elongated to allow for hand soldering and reworking. Production assembly may allow this dimension to be reduced as long as the G dimension is maintained.

4 Pin Descriptions

4.1 Power and Ground Pins

Table 26: Power and Ground Pins

Name	Type	Circuit	Description
GNDA	P	–	Analog ground: This pin should be connected directly to the ground plane.
GNDD	P	–	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	P	–	Analog power supply: A 3.3 V power supply should be connected to this pin, must be the same voltage as V3P3SYS.
V3P3SYS	P	–	System 3.3 V supply. This pin should be connected to a 3.3 V power supply.
V3P3D	O	13	Auxiliary voltage output of the chip, controlled by the internal 3.3 V selection switch. In mission mode, this pin is internally connected to V3P3SYS. In BROWNOUT mode, it is internally connected to VBAT. This pin is left unconnected in LCD and sleep mode. A bypass capacitor to ground should not exceed 0.1 μF.
VBAT	P	12	Battery backup and oscillator power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS.
V2P5	O	10	Output of the internal 2.5 V regulator. Leave this pin open.

4.2 Analog Pins

Table 27: Analog Pins

Name	Type	Circuit	Description
IA, IB, IC, ID, IE, IF, IG, IH	I	6	Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be tied to V3P3A**.
VA, VB	I	6	Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be tied to V3P3A.**
V1	I	7	Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to the internal BIAS voltage (1.6 V). If the input voltage is above VBIAS, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. A series 5 kΩ resistor should be connected from V1 to the resistor divider.
VREF	O	9	Voltage Reference for the ADC. Normally disabled and left unconnected. If enabled, a 0.1 μF capacitor to V3P3A should be connected to this pin.
XIN XOUT	I	8	Crystal Inputs: A 32 kHz crystal should be connected across these pins. Typically, a 33 pF capacitor is also connected from XIN to GNDA and a 15 pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details. If an external clock is used, a 150 mV (p-p) clock signal should be applied to XIN, and XOUT should be left unconnected.

[1)] Pin types: P = Power, O = Output, I = Input, I/O = Input/Output

The circuit number denotes the equivalent circuit, as specified under Section 5, I/O Equivalent Circuits.

4.3 Digital Pins

Table 28: Digital Pins

Name	Type	Circuit	Description
COM1,COM0	O	5	LCD Common Outputs: These 2 pins provide the select signals for an LCD display.
DIO3	I/O	3,4	Dedicated DIO pin.
SEG0…SEG2, SEG7, SEG8 SEG12, SEG14…SEG18	O	5	Dedicated LCD Segment Output pins.
SEG24/DIO4… SEG31/DIO11, SEG33/DIO13… SEG39/DIO19, SEG63/DIO43	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface; WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **If unused, these pins must be configured as DIOs and set to outputs by the firmware.**
SEG3/PCLK SEG4/PSDO SEG5/PCSZ SEG6/PSDI	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or SPI PORT.
E_RXTX/SEG9	I/O	1, 4, 5	Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E tied to GND).
E_RST/SEG11	I/O	1, 4, 5	
E_TCLK/SEG10	O	4, 5	
ICE_E	I	2	ICE enable. When zero, E_RST, E_TCLK and E_RXTX become SEG32, SEG33 and SEG38 respectively. For production units, this pin should be pulled to GND to disable the emulator port.
CKTEST/SEG19, MUXSYNC/SEG7	O	4, 5	Multi-use pins, configurable as either multiplexer/clock output or LCD segment driver using the I/O RAM registers *CKOUT_E* or *MUX_SYNC_E*.
TMUXOUT	O	4	Digital output test multiplexer. Controlled by *TMUX[3:0]*.
OPT_RX/DIO1	I/O	3, 4, 7	Multi-use pin, configurable as Optical Receive Input or general DIO. When configured as OPT_RX, this pin receives a signal from an external photo-detector used in an IR serial interface. **If unused, this pin must be terminated to V3P3D or GNDD, or configured as a DIO and set to an output by the firmware.**
OPT_TX/DIO2	I/O	3, 4	Multi-use pin, configurable as either optical LED transmit output, WPULSE, RPULSE, or general DIO. When configured as OPT_TX, this pin is capable of directly driving an LED for transmitting data in an IR serial interface. **If unused, this pin must be left open, or configured as a DIO and set to an output by the firmware.**
RESET	I	2	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30 μA (nominal) current source pull-down. No external reset circuitry is necessary.
RX	I	3	UART input. **If this pin is unused, it must be terminated to V3P3D or GNDD.**
TX	O	4	UART output.
TEST	I	7	Enables Production Test. **This pin must be grounded in normal operation.**

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output.
The circuit number denotes the equivalent circuit, as specified in Section 5 I/O Equivalent Circuits.

5 I/O Equivalent Circuits

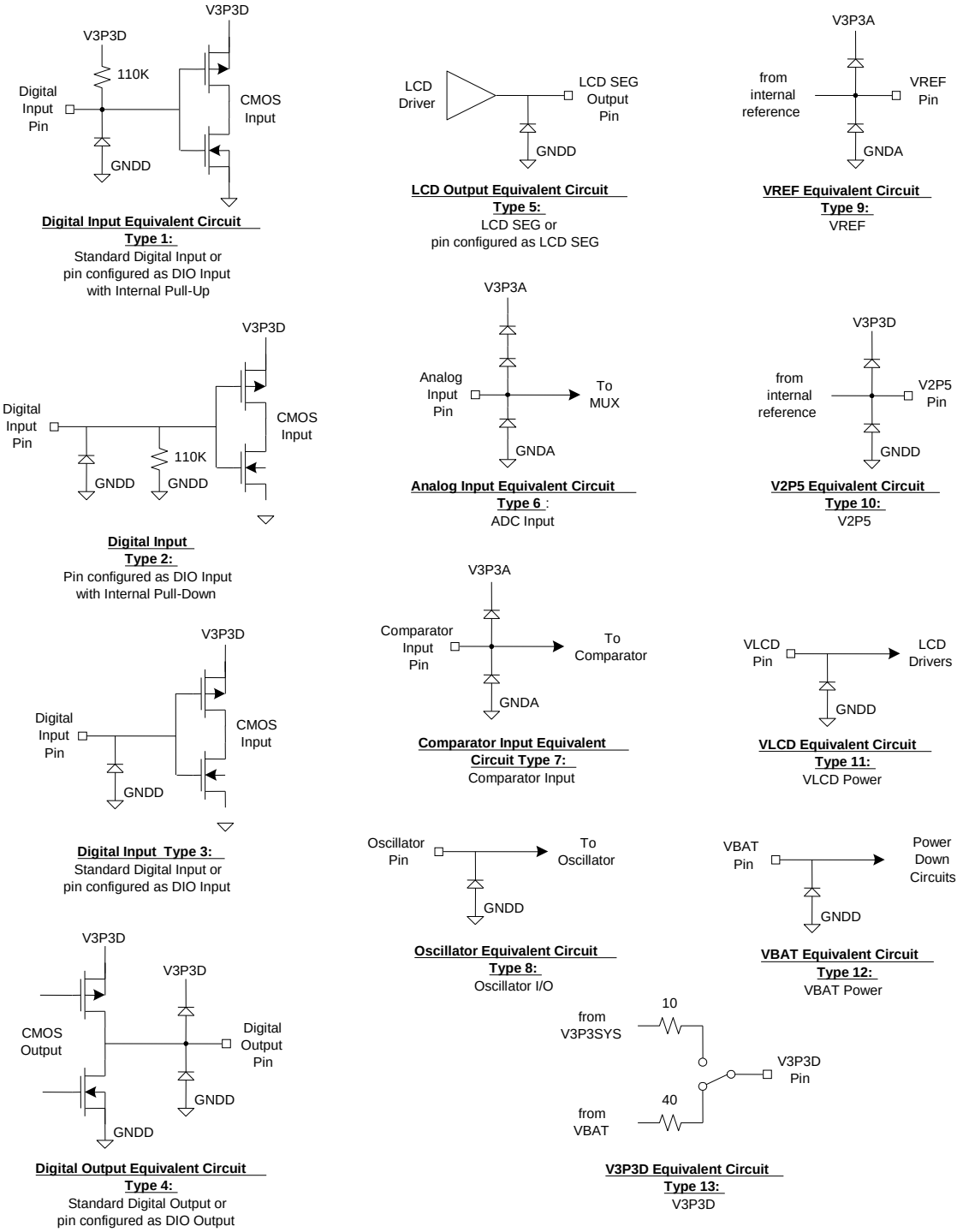


Figure 9: I/O Equivalent Circuits

6 Ordering Information

Table 29: Ordering Information

Part	Part Description (Package)	Flash Size	Packaging	Order Number	Package Marking
78M6618	68-pin QFN (Lead(Pb)- Free)	128 KB	Bulk	78M6618-IM/F	78M6618-IM
78M6618		128 KB	Bulk, *Programmed	78M6618-IM/F/Pxx	78M6618-IM
78M6618		128 KB	Tape and Reel	78M6618-IMR/F	78M6618-IM
78M6618		128 KB	Tape and Reel, *Programmed	78M6618-IMR/F/Pxx	78M6618-IM

* Contact Silergy for more information on programmed part options.

7 Contact Information

For more information about Silergy products or to check the availability of the 78M6618, contact support.em@silergy.com

8 Appendix A: Acronyms

ANSI	American National Standards Institute
CE	Compute Engine
DIO	Digital I /O
ICE	In-Circuit Emulator
IEC	International Electrotechnical Commission
MPU	Microprocessor Unit (CPU)
PLL	Phase-Locked Loop
RMS	Root Mean Square
SFR	Special Function Register
SOC	System on Chip
UART	Universal Asynchronous Receiver/Transmitter

9 Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	5/6/2009	First publication.	—
1.4	3/11	In Section 1.13, added text changes and Figure 3.	10
		In Section 2, Electrical Specifications, added Guaranteed By Design information.	19–23
		In Section 7, added the new contact information.	30
2	4/16	Rebranding only	

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