



Integrated Device Technology, Inc.

32K x 32  
128K x 32  
CMOS STATIC RAM MODULES

IDT7M4003  
IDT7M4013

**FEATURES**

- High-density 1Mb/4Mb CMOS Static RAM modules
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - 7M4003 — 30ns (max.) commercial
  - 7M4003 — 30ns (max.) military
  - 7M4013 — 15ns (max.) commercial
  - 7M4013 — 25ns (max.) military
- Low-power CMOS operation
- Surface mounted LCC or SOJ components on a multi-layered fired ceramic substrate
- Offered in a 66-pin "PGA-type" HIP (Hex In-line Package)
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

**DESCRIPTION**

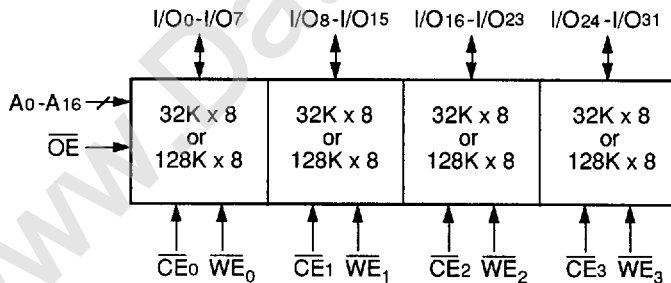
The IDT7M4003/4013 are high-speed, high-density 1Mb/4Mb CMOS Static RAM modules constructed on a multilayer fired ceramic substrate using either 32K x 8 or 128K x 8 SRAM components.

The IDT7M4003/4013 is available with access times as fast as 15ns over the commercial temperature range and 25ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit 1Mb/4Mb of memory into a minimum amount of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

**FUNCTIONAL BLOCK DIAGRAM**



2711 drw 01

The IDT logo is a registered trademark and Flex-Pak is a trademark of Integrated Device Technology, Inc.

**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

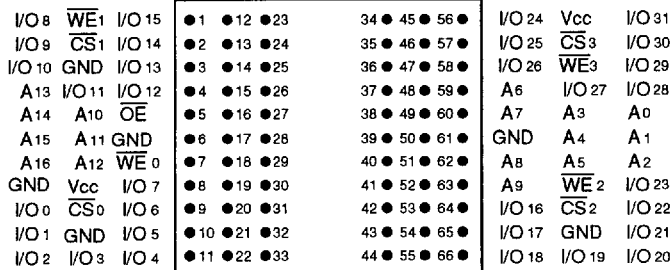
**SEPTEMBER 1993**

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DSC-7069/4

INTEGRATED DEVICE

PIN CONFIGURATION<sup>(1)</sup>



HIP  
TOP VIEW

2711 drw 02

NOTE:

1. For the IDT7M4003 (32K x 32) version, pins 6 and 7 are no connects

PIN NAMES

Name	Description
I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE0-3	Write Enables
CS0-3	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground

2711 tbl 01

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2711 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE<sup>(1)</sup> (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN <sup>(1)</sup>	Input Capacitance (DATA, CS, WE)	VIN = 0V	12	pF
CIN <sup>(2)</sup>	Input Capacitance (ADDRESS, OE)	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

2711 tbl 02

NOTE:

1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DATAOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DATAIN	Active

2711 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	6.0	V
VIL	Input LOW Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

NOTE:

2711 tbl 05

1. VIL = -3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2711 tbl 06

**DC ELECTRICAL CHARACTERISTICS**

**INTEGRATED DEVICE**

(VCC = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max. <sup>(1)</sup>	Max. <sup>(2)</sup>	Unit
ILI	Input Leakage Current (Address, OE)	VCC = Max., VIN = GND to VCC	—	20	40	μA
ILI	Input Leakage Current (Data, CS, WE)	VCC = Max., VIN = GND to VCC	—	5	10	μA
ILO	Output Leakage Current	VCC = Max CS = VIH, VOUT = GND to VCC	—	5	10	μA
ICC	Dynamic Operating Current	VCC = Max., CS ≤ VIL f = fMAX, Output Open	—	720	800	mA
ISB	Standby Supply Current	VCC = Max., CS ≥ VIH f = fMAX, Output Open	—	160	240	mA
ISB1	Full Standby Supply Current	CS ≥ VCC - 0.2V VIN > VCC - 0.2V or < 0.2V	—	60	80	mA
VOL	Output LOW Voltage	VCC = Min., IOL = 8mA	—	0.4	0.4	V
VOH	Output HIGH Voltage	VCC = Min., IOH = -4mA	2.4	—	—	V

**NOTES:**

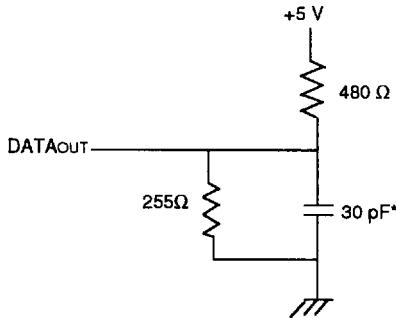
- 1 For TA = 0°C to +70°C versions only
- 2 For TA = -55°C to +125°C versions only

2711 tbi 07

**AC TEST CONDITIONS**

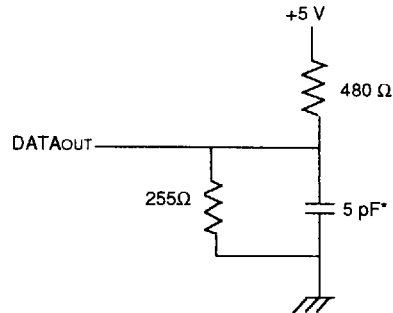
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2711 tbi 07



2711 drw 03

\*Including scope and jig  
**Figure 1. Output Load**



2711 drw 04

\*Including scope and jig  
**Figure 2. Output Load**  
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

**AC ELECTRICAL CHARACTERISTICS**

**INTEGRATED DEVICE**

(V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15 <sup>(2)</sup>		-17 <sup>(2)</sup>		-20 <sup>(2)</sup>		-25		-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
t <sub>RC</sub>	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
t <sub>AA</sub>	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
t <sub>ACS</sub>	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	2	—	2	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	6	—	7	—	8	—	12	—	15	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	—	6	—	7	—	7	—	12	—	13	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
<b>WRITE CYCLE</b>												
t <sub>WC</sub>	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	12	—	13	—	15	—	20	—	25	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	12	—	13	—	15	—	20	—	25	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	—	6	—	8	—	9	—	12	—	13	ns
t <sub>DW</sub>	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	5	—	5	—	ns

**NOTES:**

1. This parameter is guaranteed by design, but not tested
2. Preliminary specification only.

2711 tbl 09

**AC ELECTRICAL CHARACTERISTICS**

**INTEGRATED DEVICE**

(V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-35		-40		-50		-60		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	35	—	40	—	50	—	60	—	ns
t <sub>AA</sub>	Address Access Time	—	35	—	40	—	50	—	60	ns
t <sub>ACS</sub>	Chip Select Access Time	—	35	—	40	—	50	—	60	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	20	—	25	—	30	—	30	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	2	—	5	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	—	17	—	20	—	20	—	25	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	—	15	—	20	—	20	—	25	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
<b>WRITE CYCLE</b>										
t <sub>WC</sub>	Write Cycle Time	35	—	40	—	50	—	60	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	30	—	35	—	45	—	55	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	30	—	35	—	45	—	55	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	2	—	2	—	5	—	ns
t <sub>WP</sub>	Write Pulse Width	25	—	30	—	40	—	50	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	—	17	—	20	—	20	—	25	ns
t <sub>DW</sub>	Data to Write Time Overlap	16	—	16	—	25	—	30	—	ns
t <sub>DH</sub>	Data Hold from Write Time	3	—	3	—	5	—	5	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

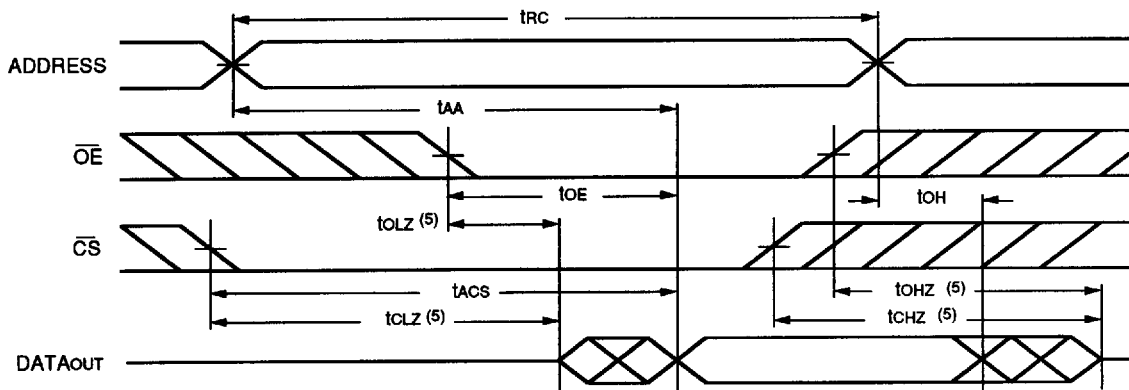
**NOTE:**

1 This parameter is guaranteed by design, but not tested

2711 tbl 10

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**

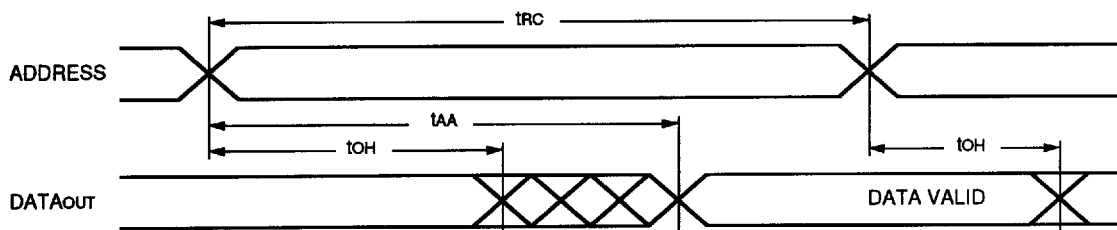
**INTEGRATED DEVICE**



2711 drw 05

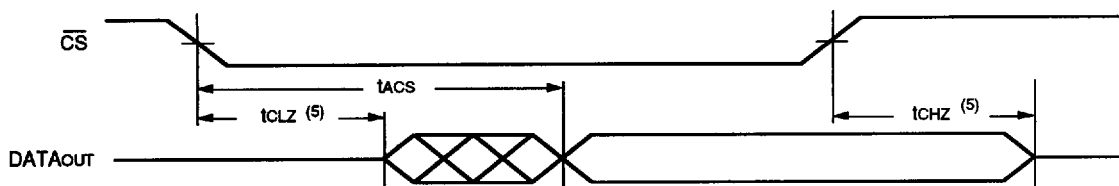
**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**

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2711 drw 06

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**

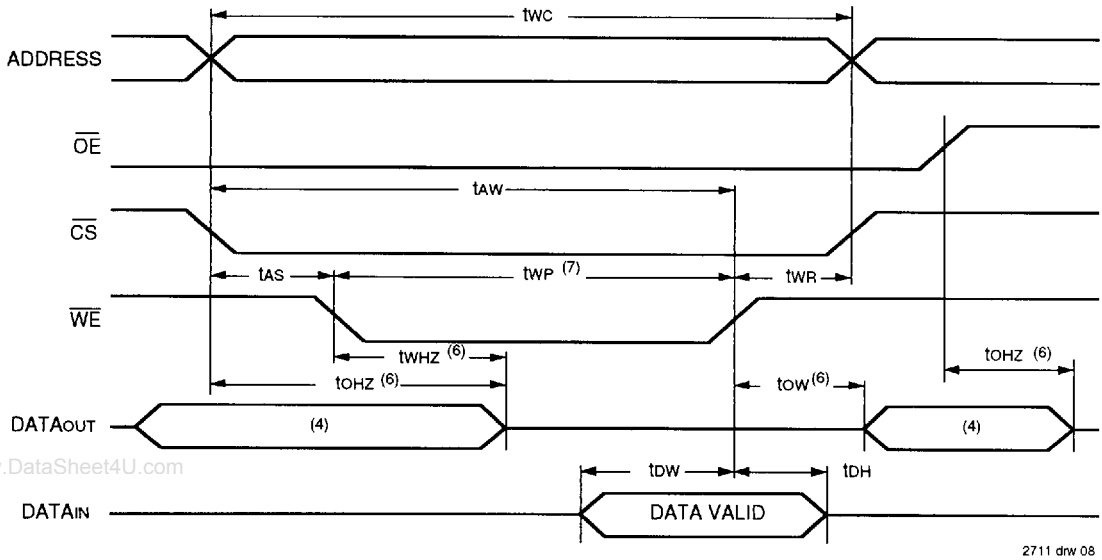


2711 drw 07

**NOTES:**

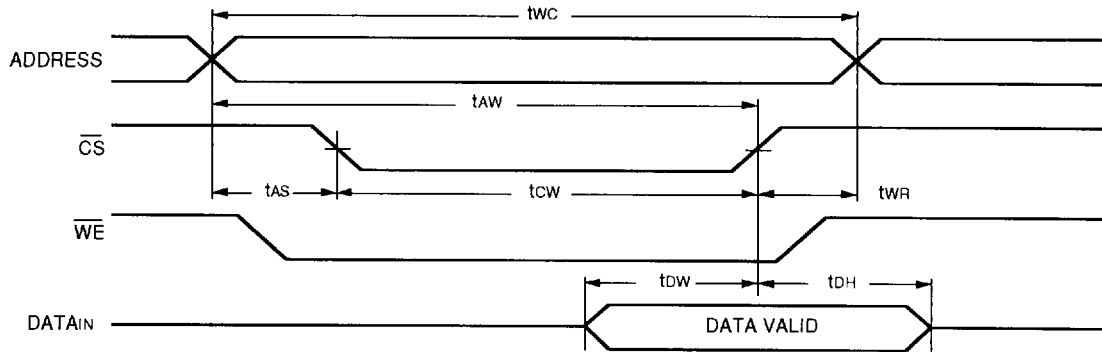
1. WE is HIGH for Read Cycle.
2. Device is continuously selected, CS = V<sub>IL</sub>.
3. Address valid prior to or coincident with CS transition LOW.
4. OE = V<sub>IL</sub>.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED)**(1, 2, 3, 7)



2711 drw 08

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED)**(1, 2, 3, 5)



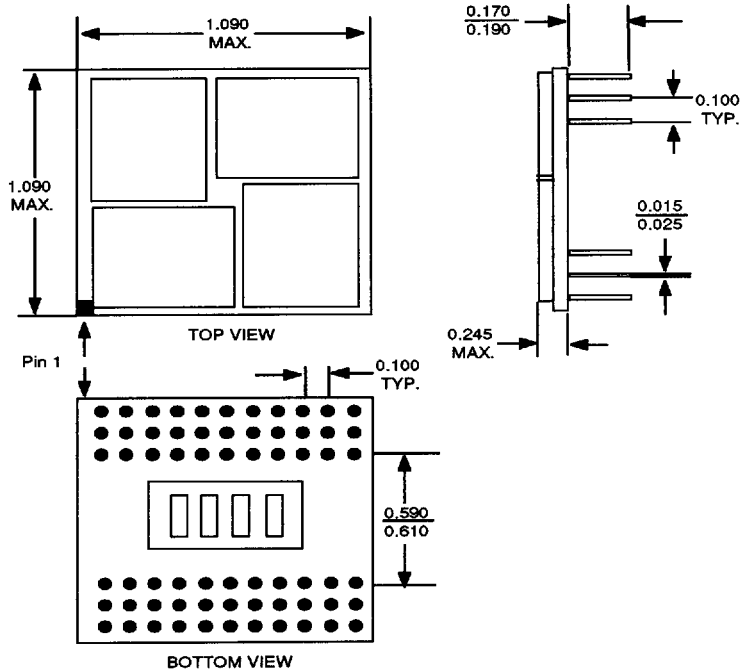
2711 drw 09

- NOTES:**
- 1  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions
  - 2 A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$
  - 3  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle
  - 4 During this period, I/O pins are in the output state, input signals must not be applied
  - 5 If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state
  - 6 Transition is measured  $\pm 200mV$  from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested
  - 7 If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{WHZ} + t_{OW}$ ) to allow the I/O drivers to turn off data and to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

68E D ■ 4825771 0014463 344 ■ IDT

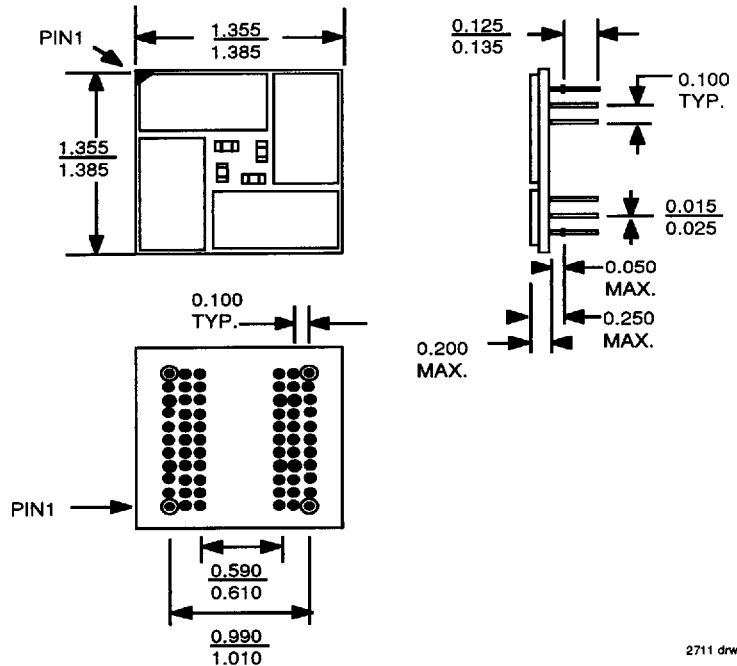
**PACKAGE DIMENSIONS**  
**7M4003SxxCHx**

**INTEGRATED DEVICE**



2711 drw 10

**7M4013SxxCHx**

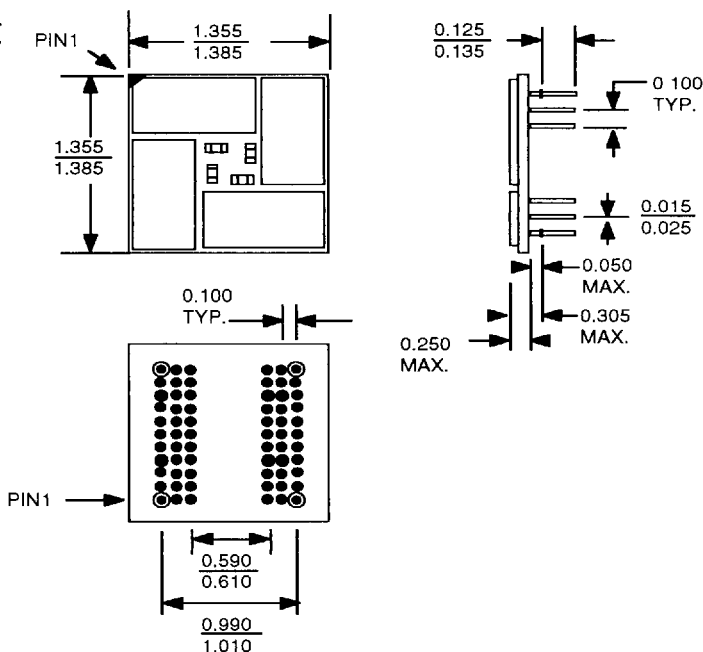


2711 drw 11



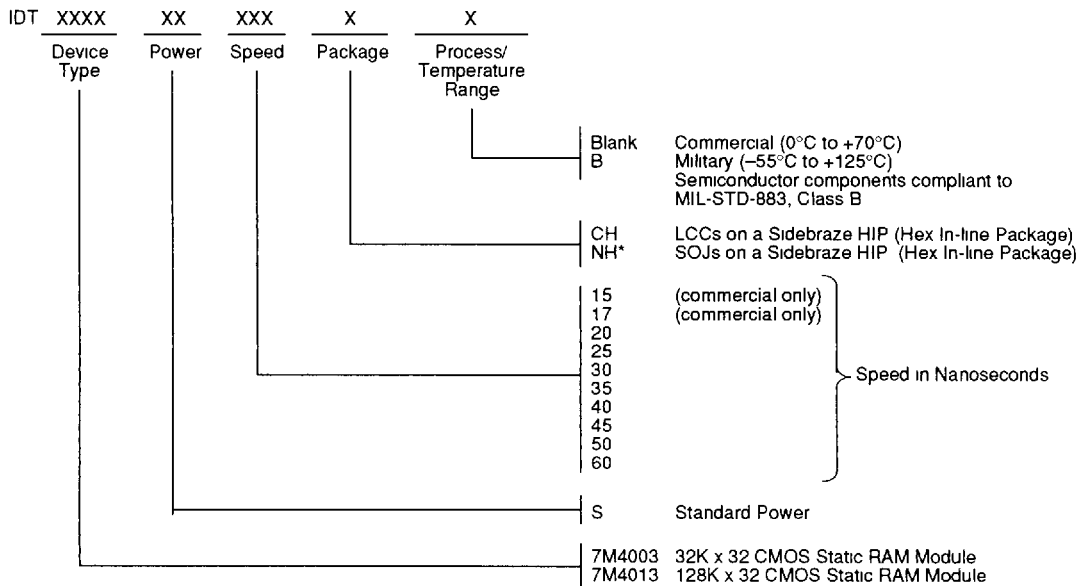
68E D ■ 4825771 0014464 280 ■ IDT

**7M4013SxxNH**  
INTEGRATED DEVICE



2711 drw 12

**ORDERING INFORMATION**



\* NH - This package option is only available on the IDT7M4013 version

2711 drw 13

7