



## 7A, 650V N-CHANNEL MOSFET

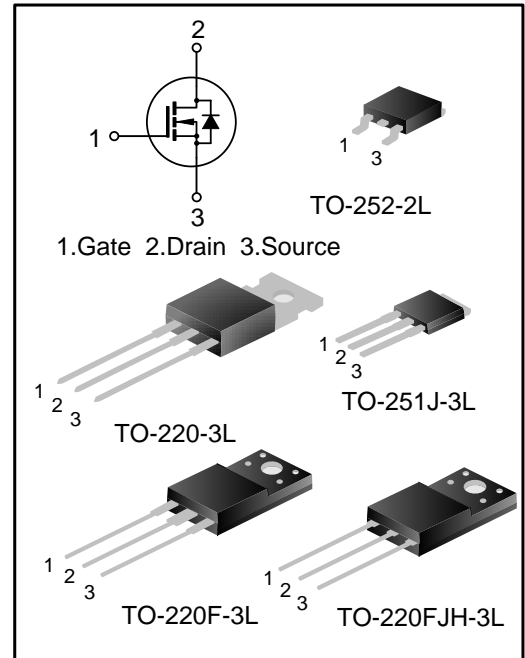
### GENERAL DESCRIPTION

SVF7N65RD(MJ)(FJH)(F)(T) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- ◆ 7A, 650V,  $R_{DS(on)(typ.)}=1.2\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low  $C_{rss}$
- ◆ Fast switching
- ◆ Improved dv/dt capability



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF7N65RMJ	TO-251J-3L	7N65RMJ	Halogen free	Tube
SVF7N65RDTR	TO-252-2L	7N65RD	Halogen free	Tape&Reel
SVF7N65RFJH	TO-220FJH-3L	7N65RFJH	Halogen free	Tube
SVF7N65RF	TO-220F-3L	SVF7N65RF	Halogen free	Tube
SVF7N65RT	TO-220-3L	SVF7N65RT	Halogen free	Tube



**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C UNLESS OTHERWISE NOTED)**

Characteristics	Symbol	Ratings			Unit
		SVF7N65 RD/MJ	SVF7N65 RFJH/F	SVF7N65 RT	
Drain-Source Voltage	V <sub>DS</sub>	650			V
Gate-Source Voltage	V <sub>GS</sub>	±30			V
Drain Current	I <sub>D</sub>	T <sub>C</sub> = 25°C			A
		T <sub>C</sub> = 100°C			
Drain Current Pulsed	I <sub>DM</sub>	28			A
Power Dissipation(T <sub>C</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	90	46	145	W
		0.72	0.31	1.16	W/°C
Single Pulsed Avalanche Energy (Note 1)	E <sub>AS</sub>	317			mJ
Reverse diode dv/dt (Note 2)	dv/dt	4.5			V/ns
MOSFET dv/dt ruggedness (Note 3)	dv/dt	50			V/ns
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150			°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150			°C

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings			Unit
		SVF7N65 RD/MJ	SVF7N65 RFJH/F	SVF7N65 RT	
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.39	2.7	0.86	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.0	62.5	62.5	°C/W



**ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C UNLESS OTHERWISE NOTED)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	--	--	1.0	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Gate resistance	R <sub>g</sub>	f=1.0MHz	--	3.2	--	Ω
Static Drain- Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A	--	1.2	1.4	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	--	895	--	pF
Output Capacitance	C <sub>oss</sub>		--	88	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	7.5	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =325V, R <sub>G</sub> =25Ω, I <sub>D</sub> =7.0A (注 4, 5)	--	14	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	33	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	58	--	
Turn-off Fall Time	t <sub>f</sub>		--	36	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =520V, I <sub>D</sub> =7.0A, V <sub>GS</sub> =10V (注 4, 5)	--	24	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	6.0	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	11	--	

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I <sub>S</sub>	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I <sub>SM</sub>		--	--	28	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =7.0A, V <sub>GS</sub> =0V	--	--	1.4	V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>S</sub> =7.0A, V <sub>GS</sub> =0V, dIF/dt=100A/μS (Note 4)	--	566	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	3.2	--	μC

**Notes:**

1. L=30mH, I<sub>AS</sub>=4.3A, V<sub>DD</sub>=100V, R<sub>G</sub>=25Ω, starting T<sub>J</sub>=25°C;
2. V<sub>DS</sub>=0~400V, I<sub>SD</sub>≤7A, T<sub>J</sub>=25°C;
3. V<sub>DS</sub>=0~480V;
4. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
5. Essentially independent of operating temperature.



## TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

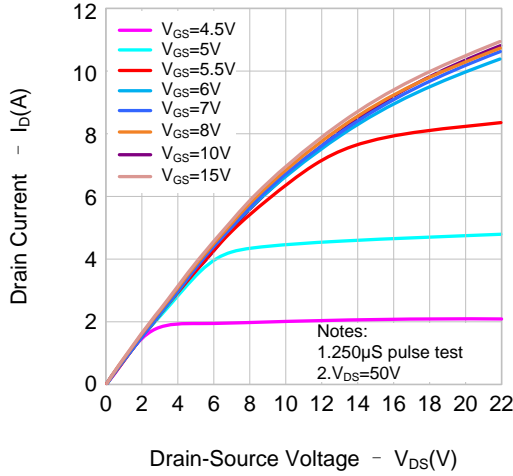


Figure 2. Transfer Characteristics

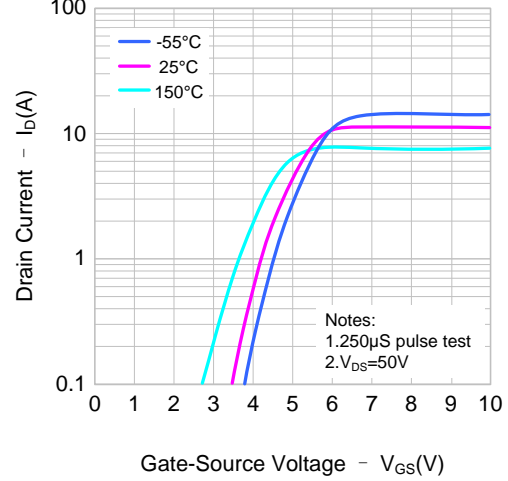


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

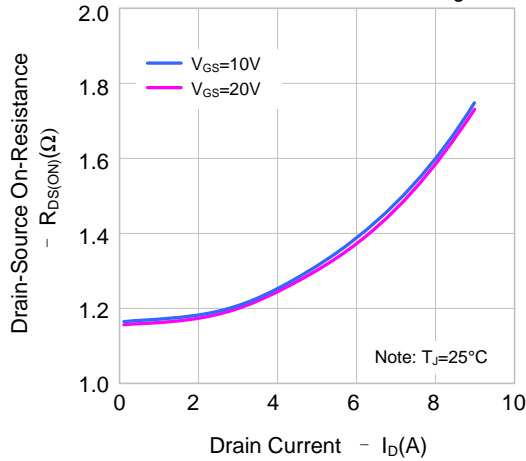


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

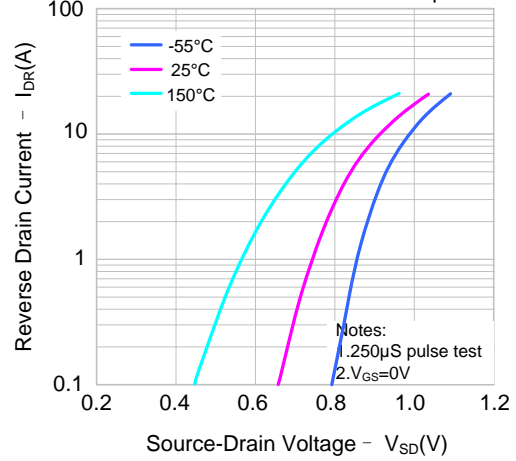


Figure 5. Capacitance Characteristics

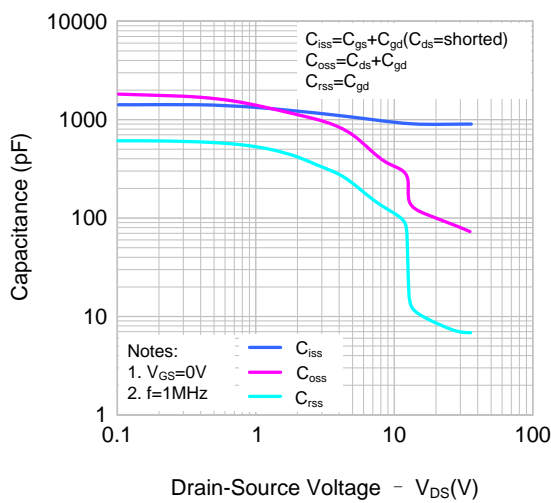
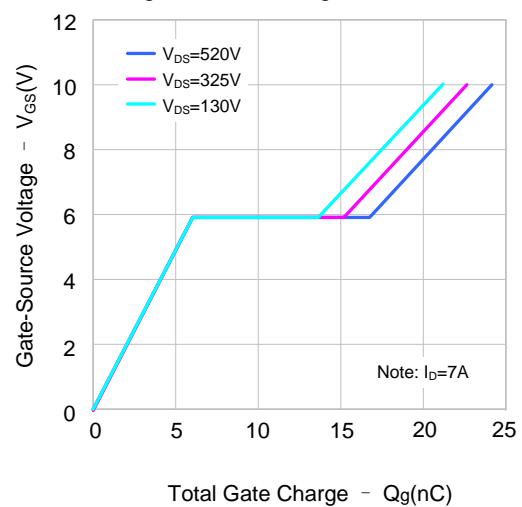


Figure 6. Gate Charge Characteristics





## TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage vs. Temperature

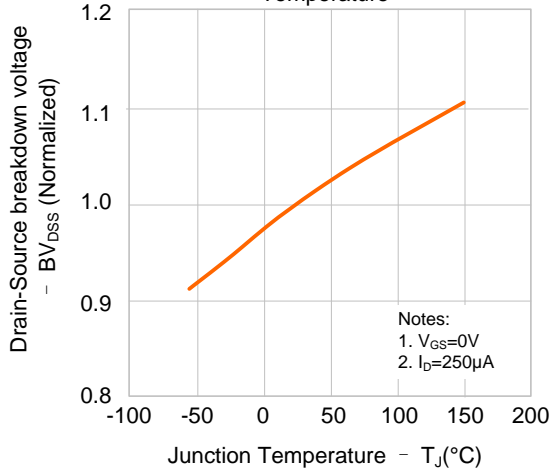


Figure 8. On-resistance Variation vs. Temperature

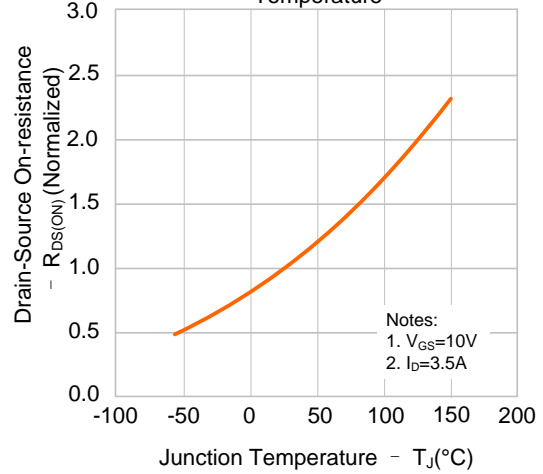


Figure 9-1. Max. Safe Operating Area SVF7N65RD(MJ)

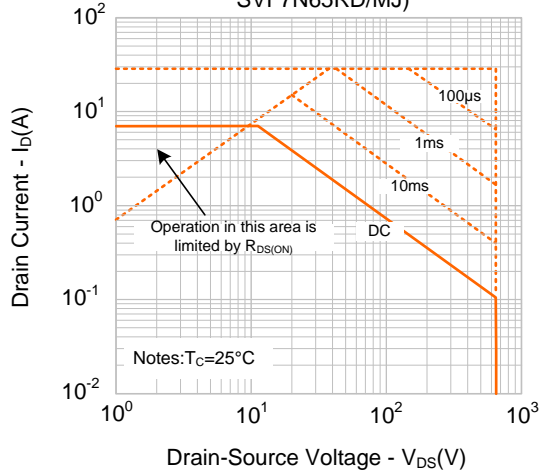


Figure 9-2. Max. Safe Operating Area (SVF7N65RFJH/F)

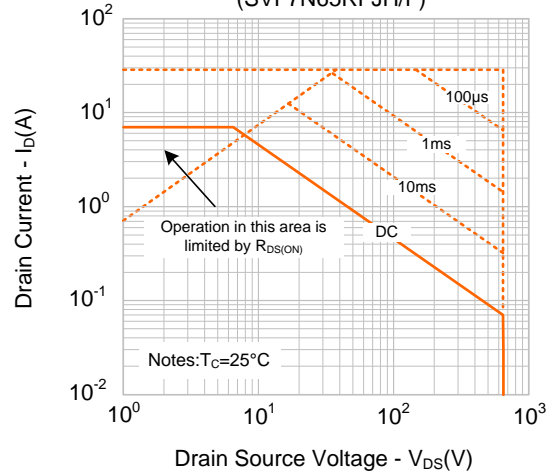
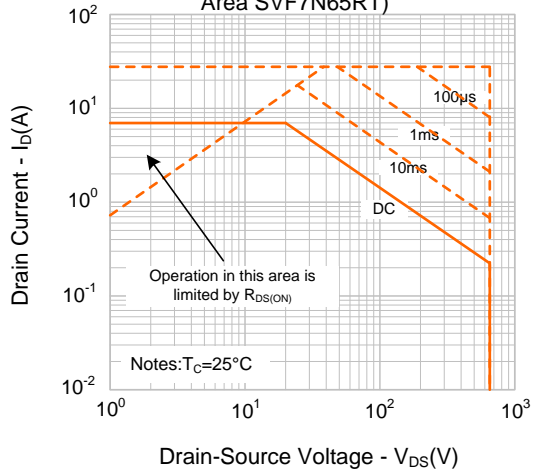


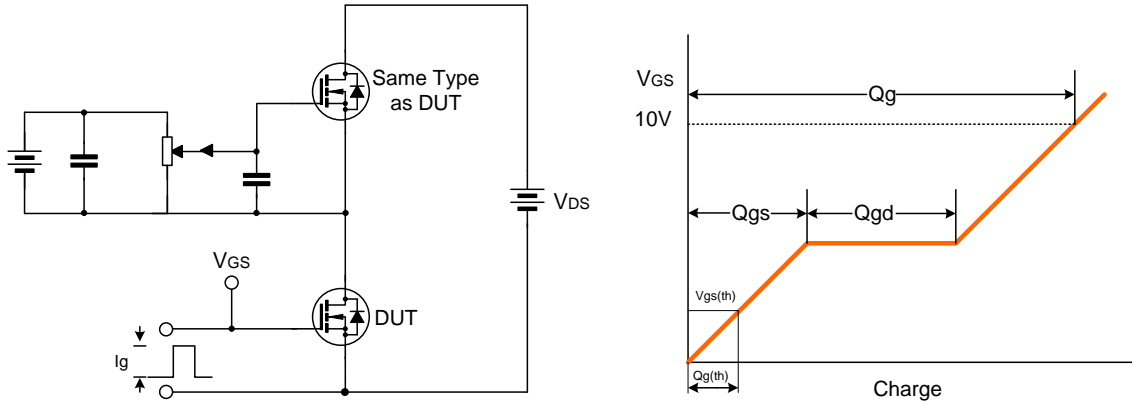
Figure 9-3. Max. Safe Operating Area SVF7N65RT)



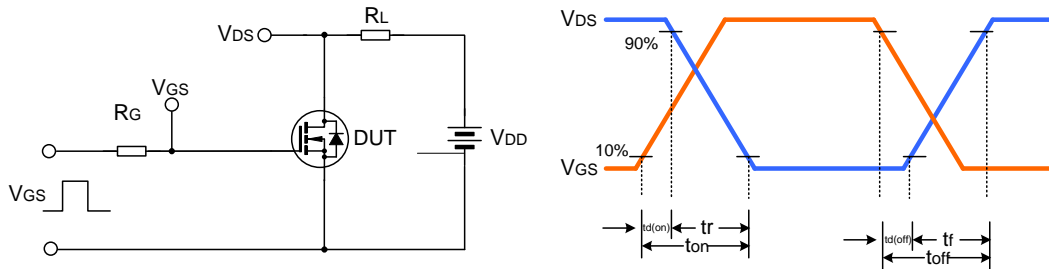


## TYPICAL TEST CIRCUIT

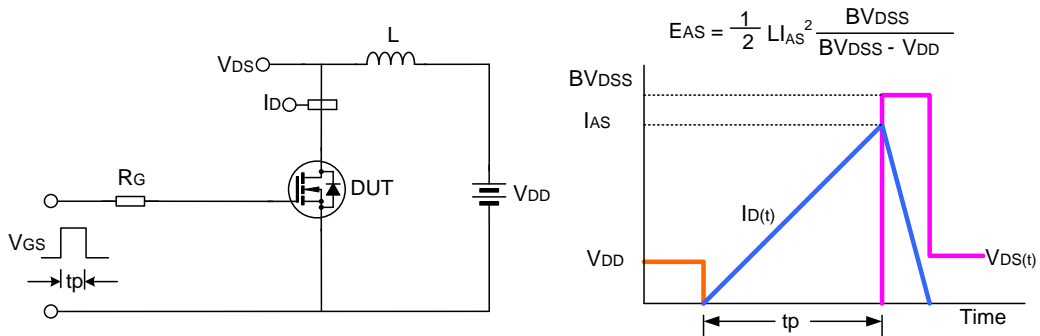
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



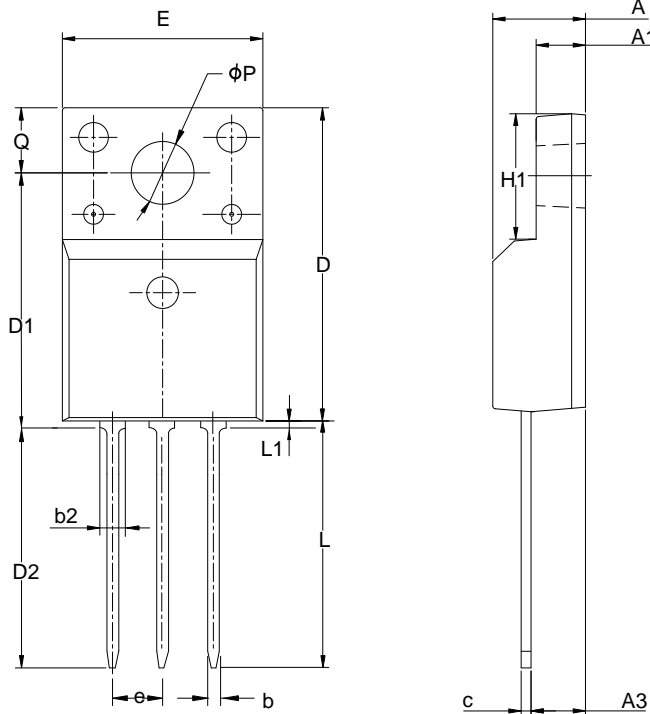
Unclamped Inductive Switching Test Circuit & Waveform





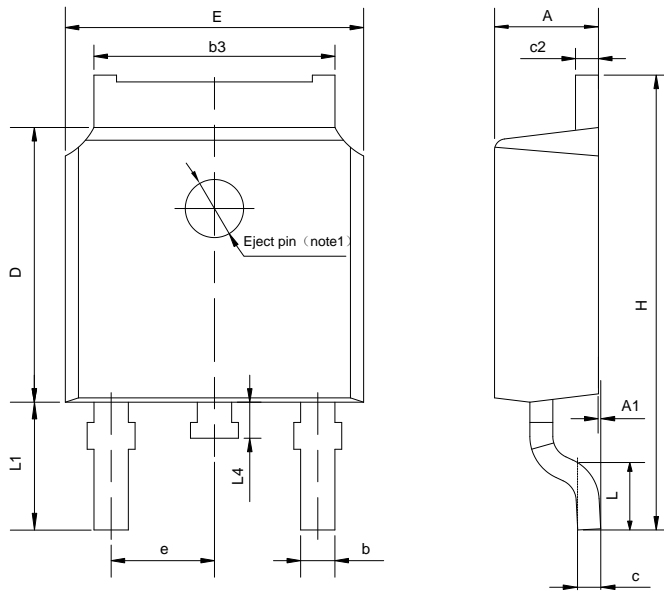
PACKAGE OUTLINE

TO-220FJH-3L 单位: 毫米



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	<b>0.80</b>
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	12.87	13.07	13.27
D2	12.28	12.48	12.68
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	0.85
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-252-2L 单位: 毫米



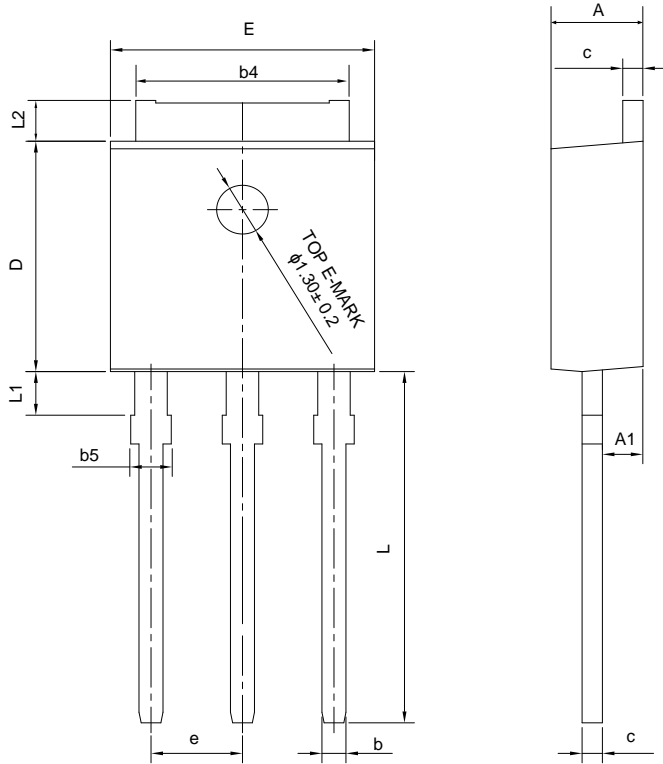
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.



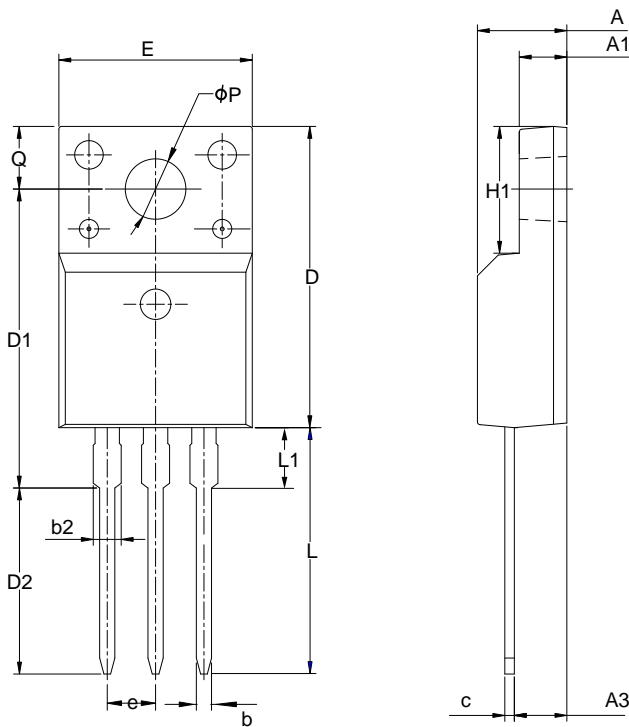
**PACKAGE OUTLINE(continued)**

**TO-251J-3L UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	—	0.89
b4	4.95	5.33	5.46
b5	—	—	1.05
c	0.46	—	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	—	1.50
L2	0.89	—	1.27

**TO-220F-3L UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	3.50
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

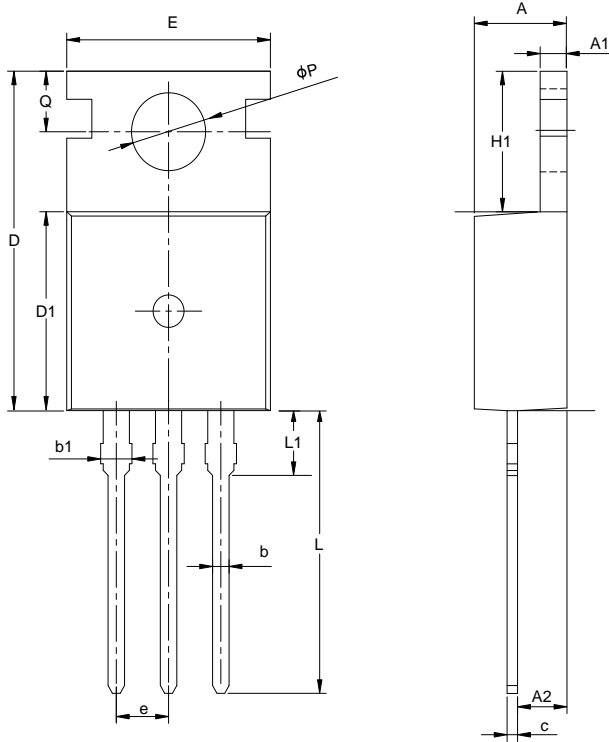




PACKAGE OUTLINE(continued)

TO-220-3L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
$\phi P$	3.40	3.70	3.90
Q	2.60	—	3.20

**Important notice :**

- The instructions are subject to change without notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- Our products are consumer electronic products, and / or civil electronic products.
- When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.
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- Product promotion is endless, our company will wholeheartedly provide customers with better products!
- Website: <http://www.silan.com.cn>



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Rev.: 1.3

Revision History:

1. Deleted NOMENCLATURE
  2. Modify Important notice
- 

Rev.: 1.2

Revision History:

1. Add SVF7N65RT
  2. Update Important Notice
- 

Rev.: 1.1

Revision History:

1. Delete SVF7N65RFJ
  2. Add SVF7N65RFJH
  3. Add SVF7N65RF
- 

Rev.: 1.0

Revision History:

1. Preliminary
- 
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