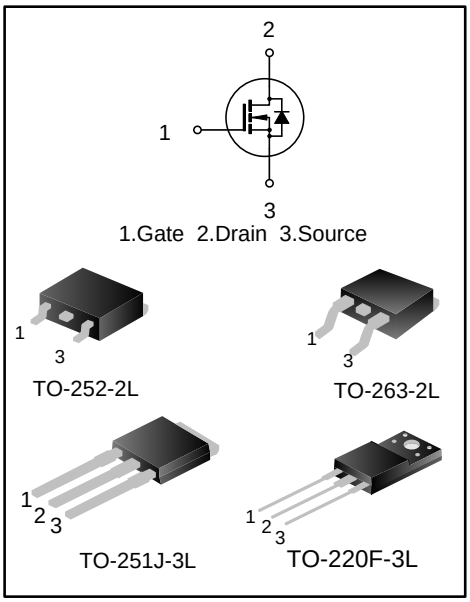
7A, 700V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVS7N70F(D)(MJ)(S)D2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 7A, 700V, $R_{DS(on)(typ.)}$=0.52Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVS7N70FD2	TO-220F-3L	7N70FD2	Halogen free	Tube
SVS7N70DD2TR	TO-252-2L	7N70DD2	Halogen free	Tape&reel
SVS7N70MJD2	TO-251J-3L	7N70MJD2	Halogen free	Tube
SVS7N70SD2	TO-263-2L	7N70SD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_A=25°C)

Characteristics		Symbol	Ratings			Unit
			SVS7N70FD2	SVS7N70DD2/ MJD2	SVS7N70SD2	
Drain-Source Voltage		V_{DS}	700			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	7.0			A
	T_C=100°C		4.4			
Drain Current Pulsed		I_{DM}	28			A
Power Dissipation (T_C=25°C)		P_D	35	125	89	W
- Derate above 25°C			0.3	1.0	0.7	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	400			mJ
Body diode (Note 2)		dv/dt	15			V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50			V/ns
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVS7N70FD2	SVS7N70DD2/ MJD2	SVS7N70SD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.7	1.0	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_j=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	700	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=700V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	0.52	0.6	Ω
Gate Resistance	R_g	f=1.0MHz	--	4.9	--	Ω
Input Capacitance	C_{iss}	V_{DS}=100V，V_{GS}=0V，f=1.0MHz	--	494	--	pF
Output Capacitance	C_{oss}		--	27	--	
Reverse Transfer Capacitance	C_{rss}		--	1.7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=350V, I_D=7.0A, V_{GS}=10V, R_G=24Ω (Note 4,5)	--	10	--	ns
Turn-on Rise Time	t_r		--	28	--	
Turn-off Delay Time	$t_{d(off)}$		--	53	--	
Turn-off Fall Time	t_f		--	26	--	
Total Gate Charge	Q_g	V_{DS}=560V, I_D=7.0A, V_{GS}=10V (Note 4,5)	--	18	--	nC
Gate-Source Charge	Q_{gs}		--	3.9	--	
Gate-Drain Charge	Q_{gd}		--	9.3	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	317	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.8	--	μC

Notes:

1. L=79mH,I_{AS}=2.5A,V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=7.0A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

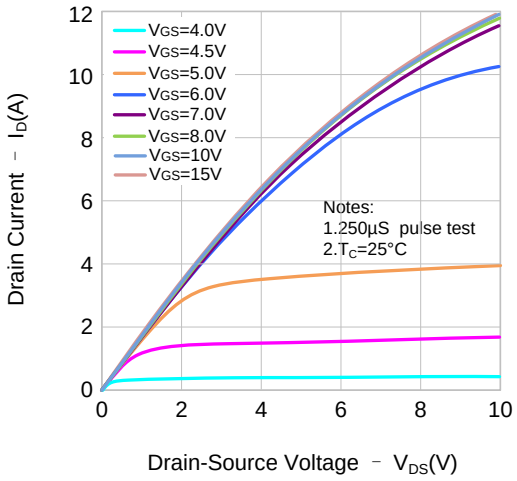


Figure 2. Transfer Characteristics

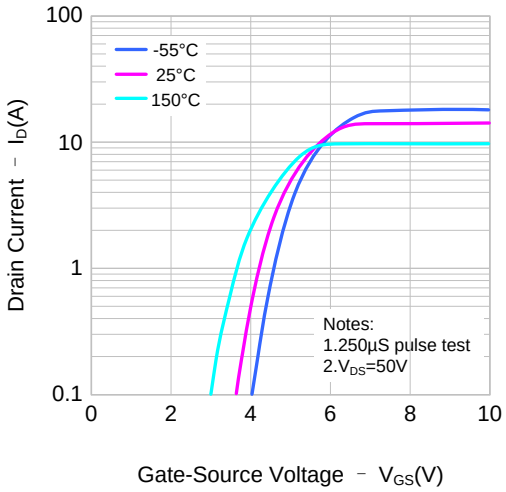


Figure 3. On-Resistance vs. Drain Current

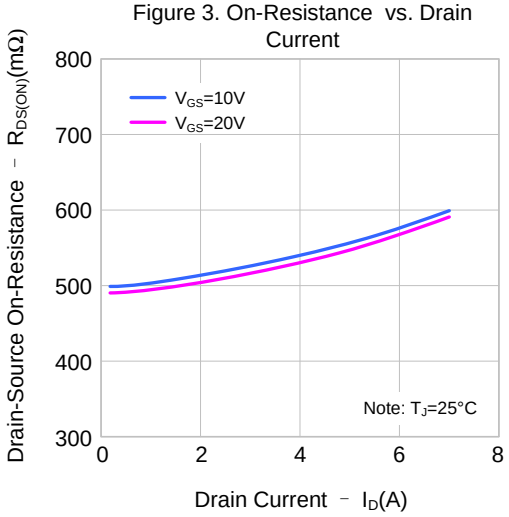


Figure 4. Body Diode Forward Voltage vs. Source Current and Temperature

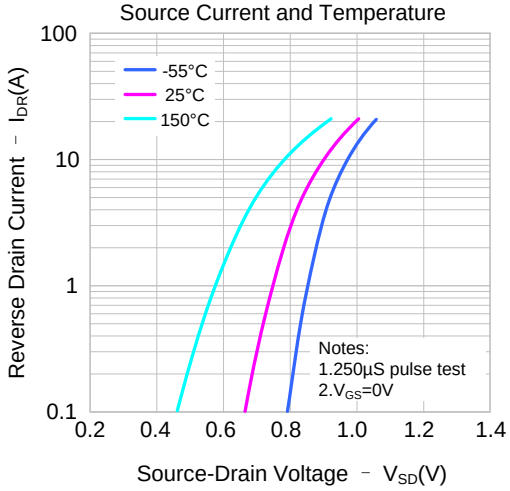


Figure 5. Capacitance Characteristics

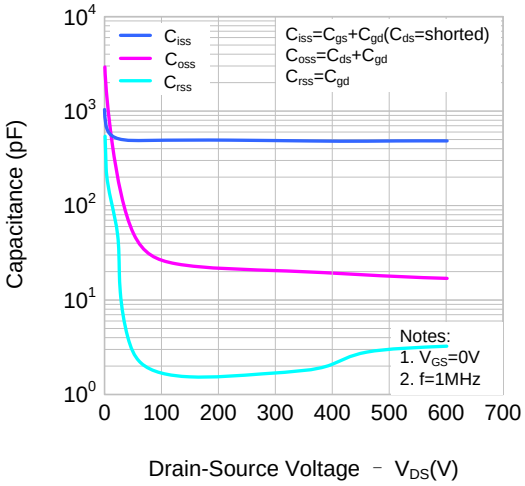
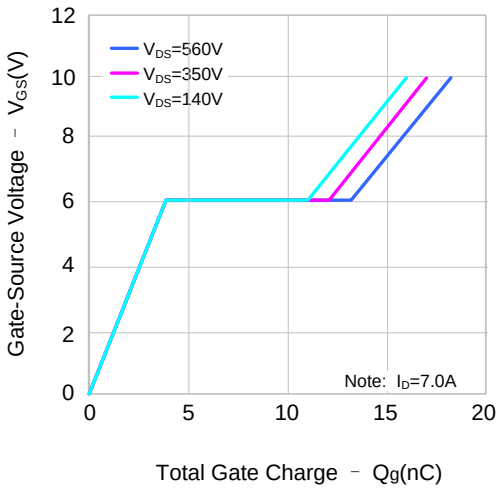


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage vs. Temperature

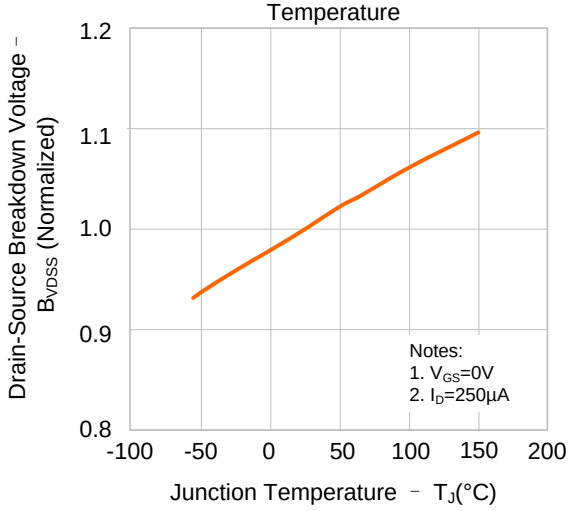


Figure 8. On-Resistance vs. Temperature

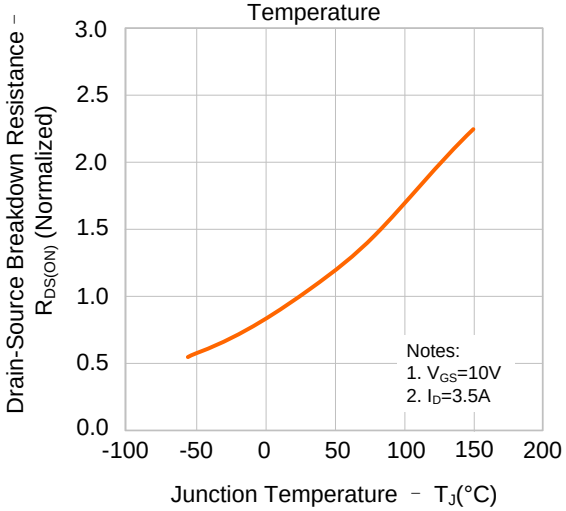


Figure 9-1. Max. Safe Operating Area(SVS7N70FD2)

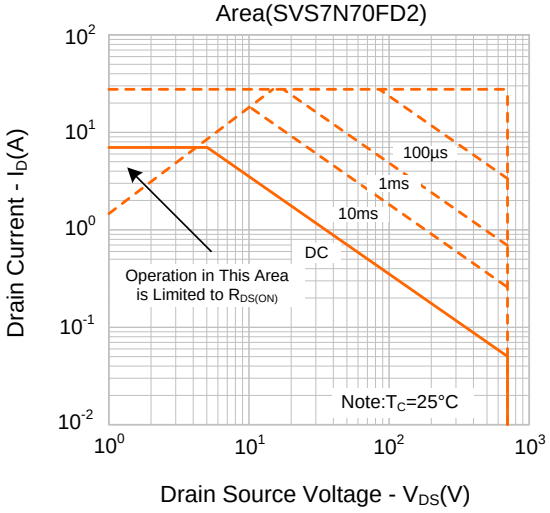


Figure 9-2. Max. Safe Operating Area(SVS7N70DD2/MJD2)

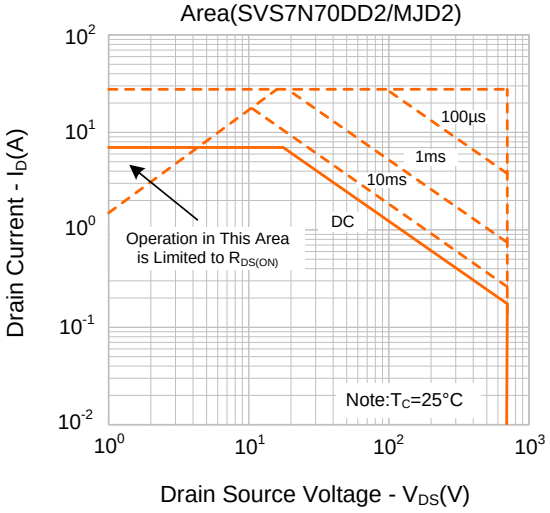
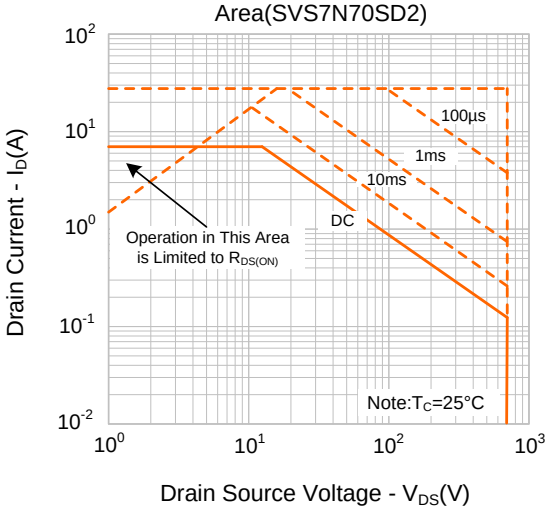
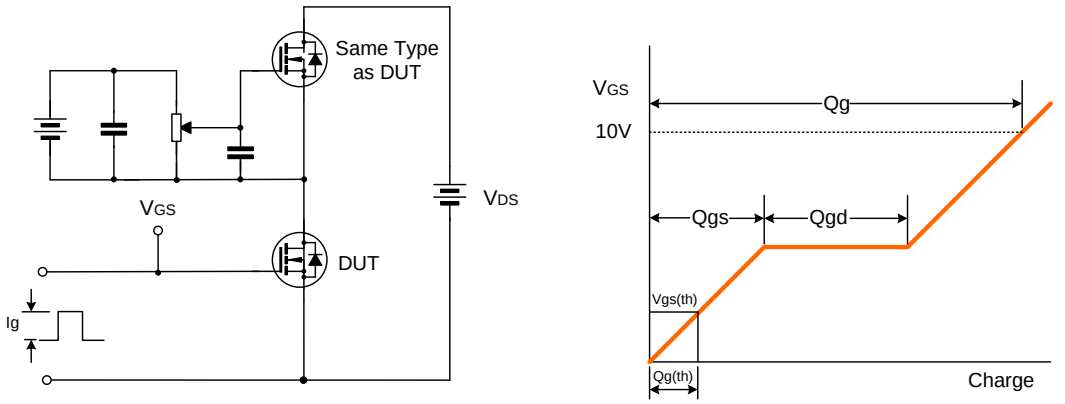


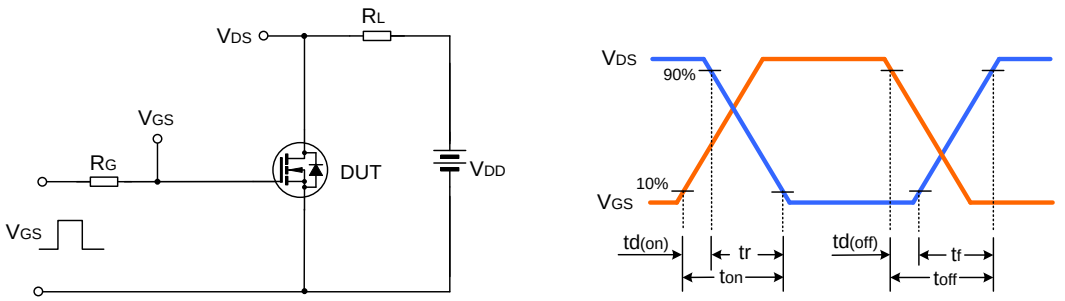
Figure 9-3. Max. Safe Operating Area(SVS7N70SD2)



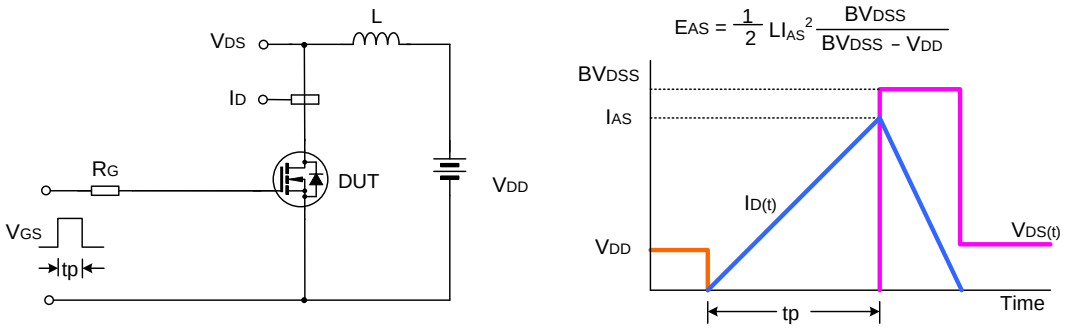
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

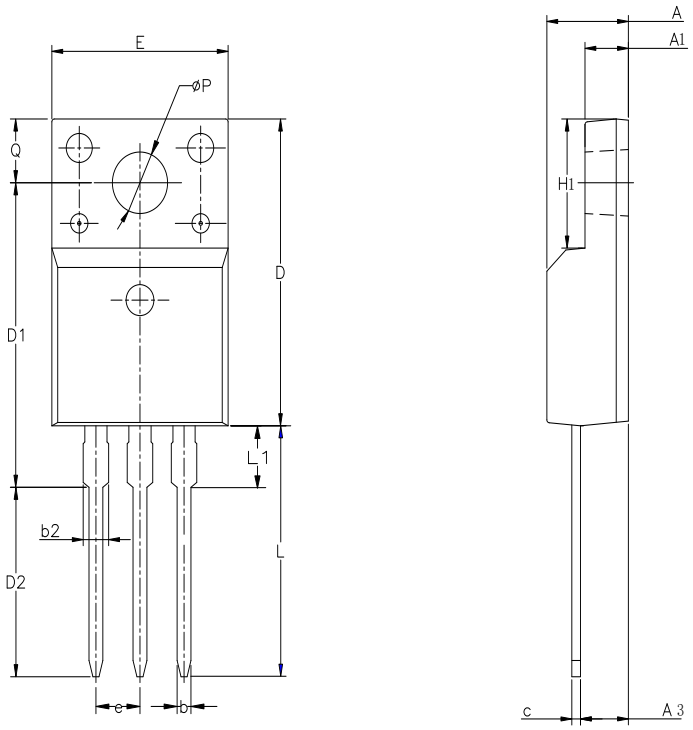


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220F-3L

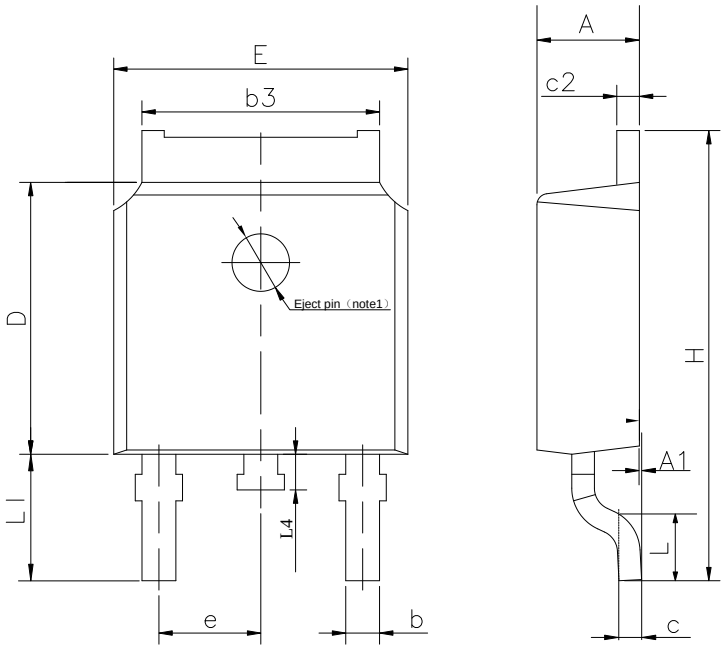
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-252-2L

UNIT: mm



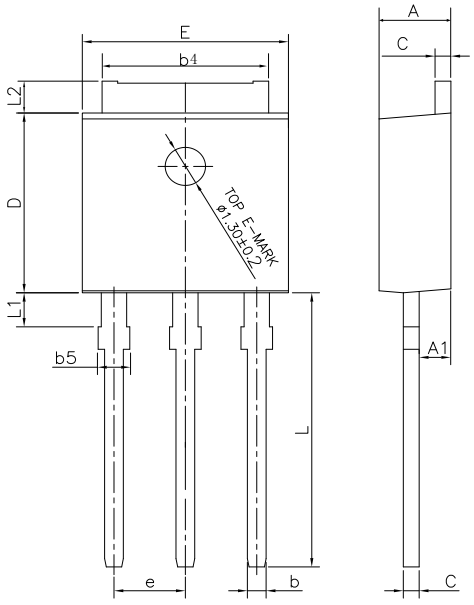
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE

TO-251J-3L

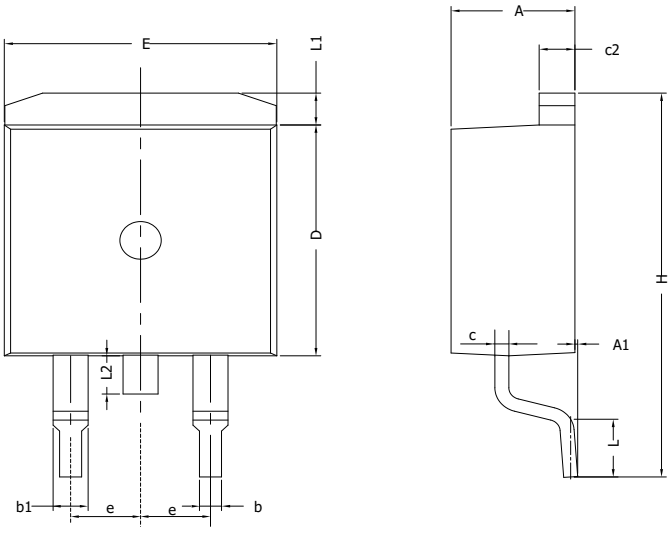
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

TO-263-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

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Rev.: 1.2

Revision History:

1. Update Electrical schematic and typical test circuit

Rev.: 1.1

Revision History:

1. Add TO-263-2L

Rev.: 1.0

Revision History:

1. First release