



7NM65Z

Preliminary

Power MOSFET

7.0A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

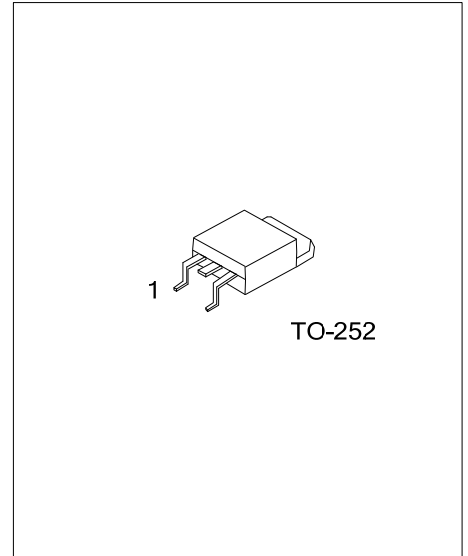
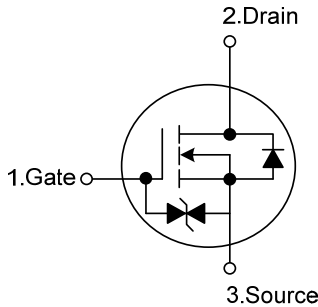
DESCRIPTION

The UTC **7NM65Z** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used in high speed switching applications at power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} \leq 1.4 \Omega @ V_{GS}=10V, I_D=3.5A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



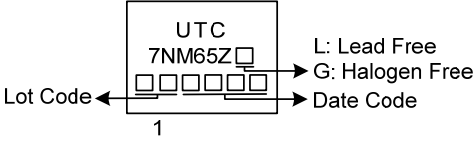
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7NM65ZL-TN3-R	7NM65ZG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

7NM65ZG-TN3-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) TN3: TO-252
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	7	A
	Pulsed (Note 2)	I_{DM}	14	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	159	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3	V/ns
Power Dissipation		P_D	49	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L = 144\text{mH}$, $I_{AS} = 1.48\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.55	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

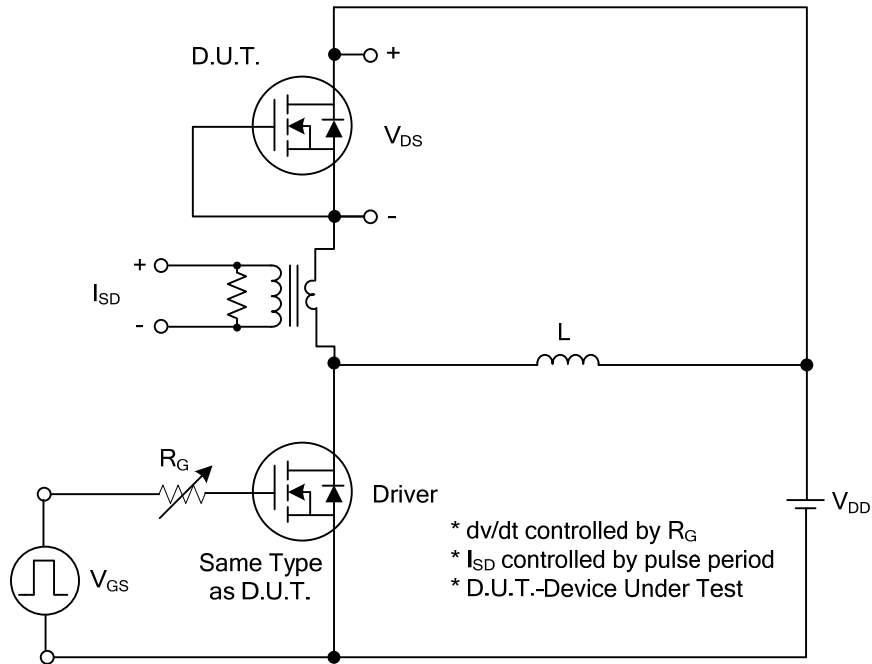
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	650			V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$			10	μA	
Gate-Source Leakage Current	Forward	$V_{GS}=20V, V_{DS}=0V$			10	μA	
	Reverse		$V_{GS}=-20V, V_{DS}=0V$				-10
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5		5.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=3.5A$			1.4	Ω	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$		610		pF	
Output Capacitance	C_{OSS}				75		pF
Reverse Transfer Capacitance	C_{RSS}				16		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)	Q_G	$V_{DS}=520V, V_{GS}=10V, I_D=3.0A, I_G=1mA$ (Note 1, 2)		18		nC	
Gate to Source Charge	Q_{GS}				8.5		nC
Gate to Drain Charge	Q_{GD}				4		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=100V, V_{GS}=10V, I_D=7.0A, R_G=25\Omega$ (Note 1, 2)		12		ns	
Rise Time	t_R				18		ns
Turn-OFF Delay Time	$t_{D(OFF)}$				27		ns
Fall-Time	t_F				28		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current	I_S				7	A	
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				14	A	
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=7.0A, V_{GS}=0V$			1.4	V	
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=7.0A, V_{GS}=0V, dI_F/dt=100A/\mu s$		320		ns	
Body Diode Reverse Recovery Charge	Q_{rr}				4		μC

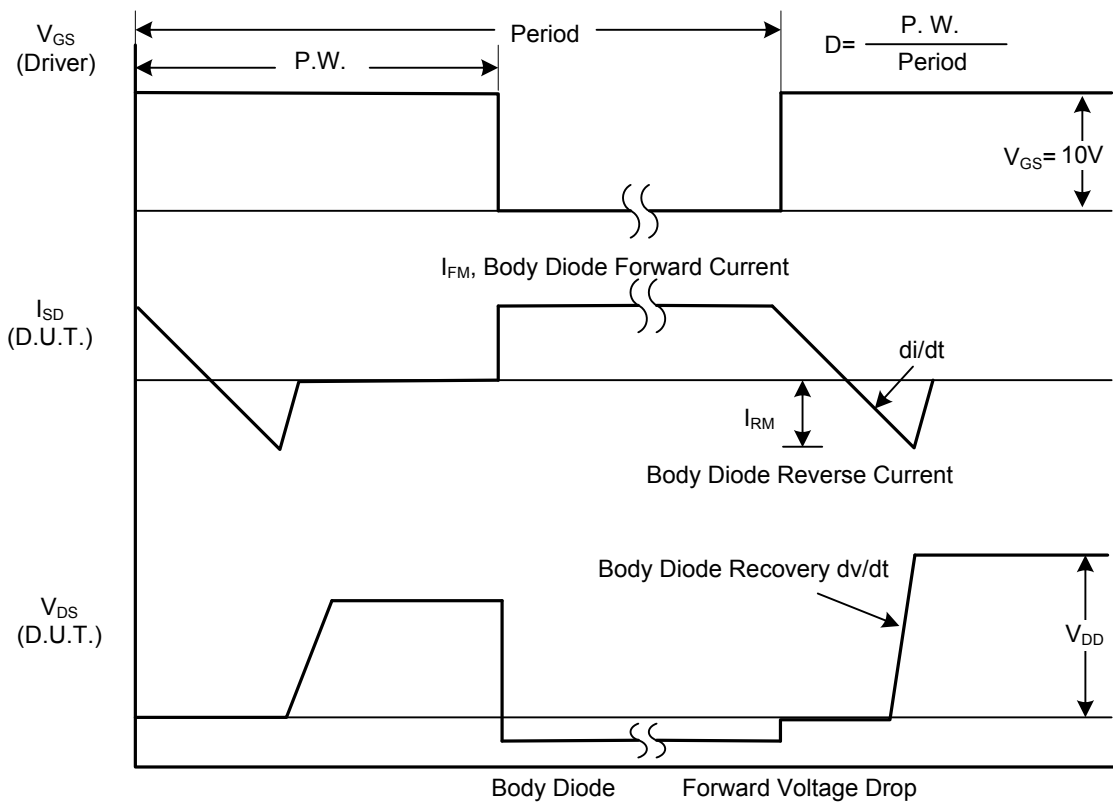
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

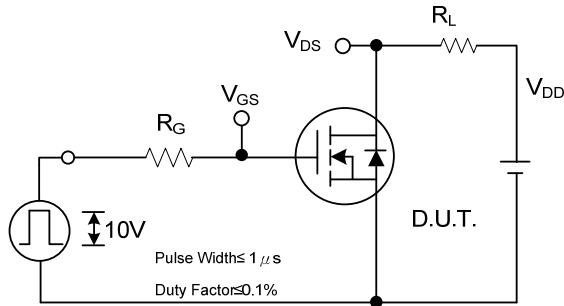


Peak Diode Recovery dv/dt Test Circuit

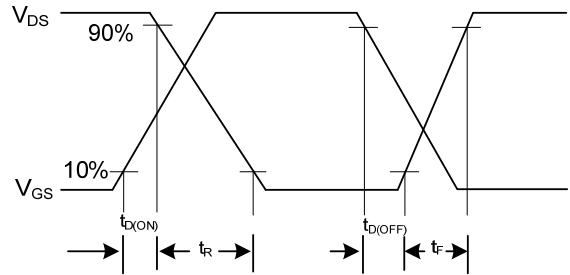


Peak Diode Recovery dv/dt Waveforms

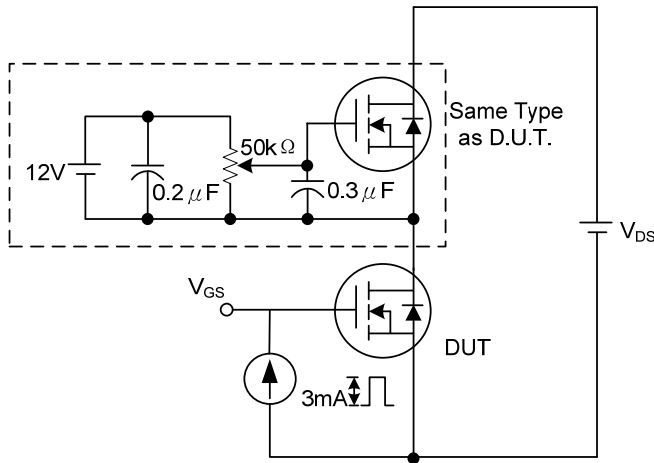
■ TEST CIRCUITS AND WAVEFORMS



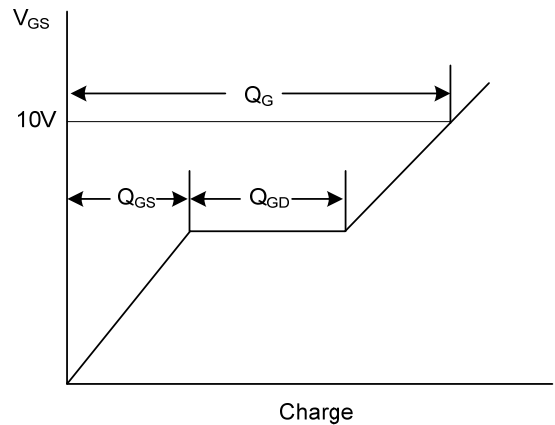
Switching Test Circuit



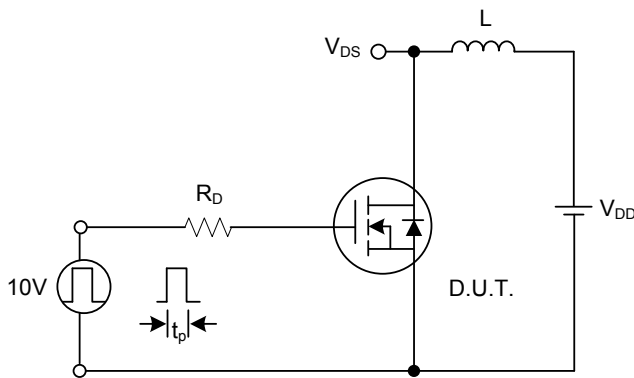
Switching Waveforms



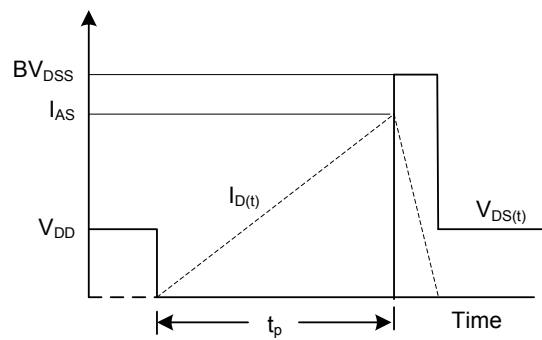
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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