Intel® 80303 I/O Processor

Design Guide

April 2002

Order Number: 273308-006

Contents

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Revision History

Rev	Date	Description of Changes
006	**4/3/02**	Modified 13.1 Thermal Recommendations. Modified case temperature in Table 14.
005	**12/04/00**	Revised PWRDELAY text on Pages 25 and 31. Revised Schematic text on page 37.
004	**10/15/00**	Table 8, changed pullup value of 2.7K on S_SERR# and S_TRDY# to 8.2K.
003	**09/2000**	Updated BOM.
002	**08/2000**	Updated Schematics.
001	**06/2000**	Original Document.

1.0 Introduction

This design guide addresses design considerations for designing with the Intel® 80303 I/O processor.

The 80303 I/O processor supports both 64-bit and 32-bit PCI running at 66 MHz. The 80303 I/O processor also supports 100 MHz SDRAM interface.

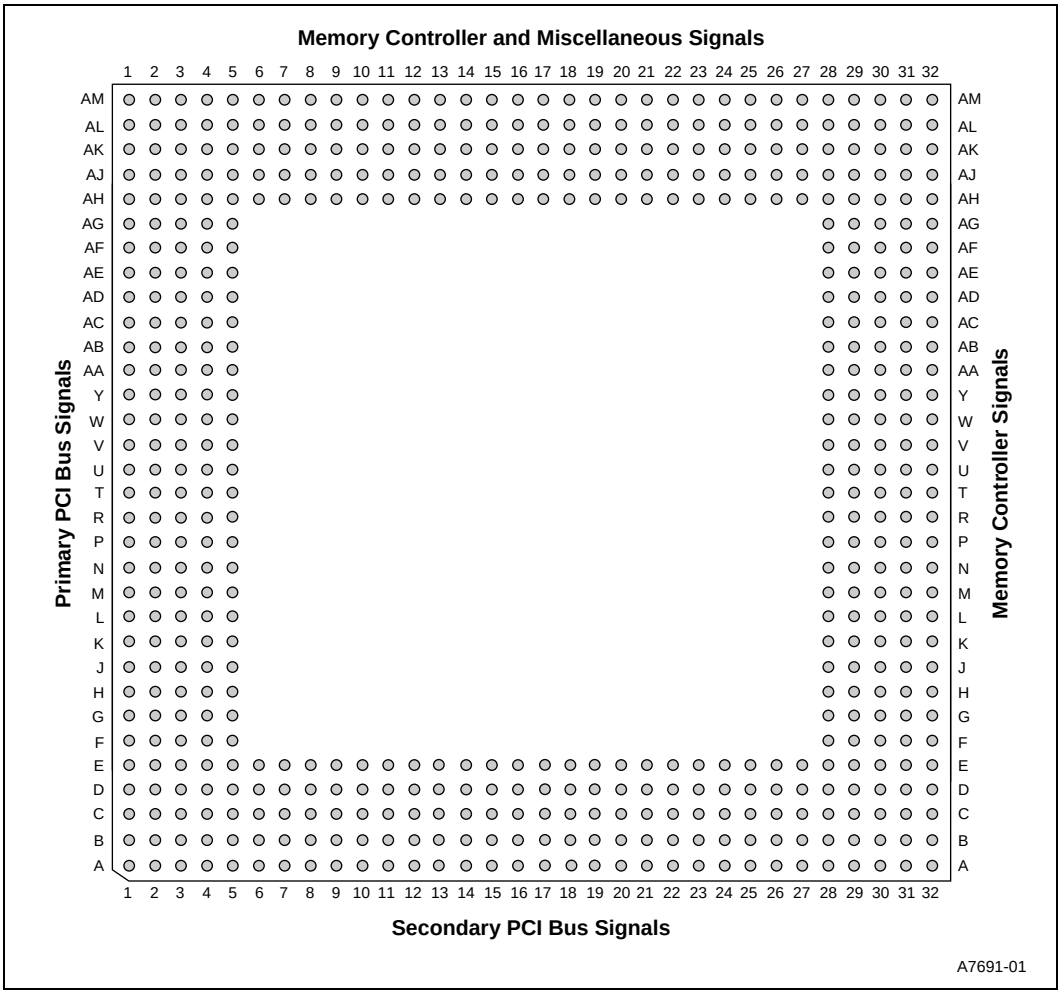
This design guide is intended to provide system designers valuable design information to be used while designing PCB boards with the 80303 I/O processor. Designers should note that this guide focuses upon specific design considerations for 80303 I/O processor and is not intended to be an all-inclusive list of all good design practices. Intel recommends employing best known design practices with signal integrity testing and validation to ensure a robust design. Use this guide as a starting point and use empirical data to optimize your particular design.

2.0 Intel® 80303 I/O Processor Ball Map

The 80303 I/O processor signals, by design, are located on the PBGA package to simplify signal routing and system implementation. Figure 1 shows the 80303 I/O processor major signal sections. To simplify routing and minimize the number of cross traces, keep this layout in mind when placing components in your system. Individual signals within the respective groups have also been laid out to minimize signal crossings.

For detailed signal descriptions refer to the *Intel® 80303 I/O Processor Datasheet* (273358) document. Contact your Intel sales representative to obtain a copy of the document.

Figure 1. 540L H-PBGA Diagram (Bottom View)



2.1 Intel® 80303 I/O Processor H-PBGA Signal Ball Map

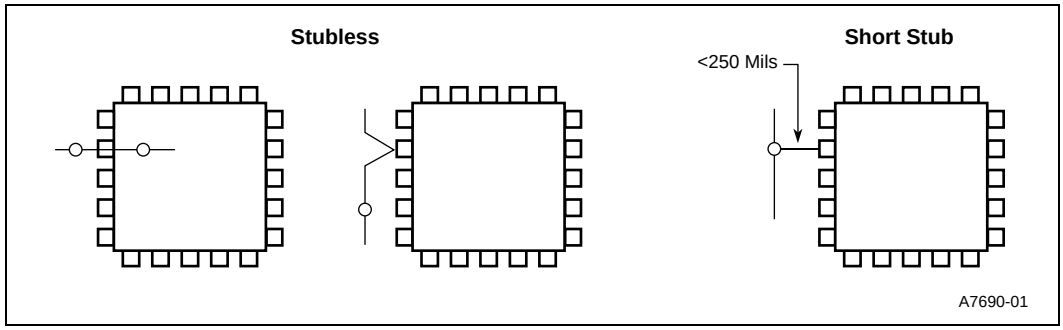
Table 23 details the ballout for the 80303 I/O Processor. See Appendix C.

3.0 Routing Guidelines

The order in which signals are routed first and last varies from designer to designer. Some prefer to route all clock signals first, while others prefer to route all high speed bus signals first. Either order can be used, provided the guidelines listed here are followed.

Route the 80303 I/O processor address/data and control signals using a “daisy chain” topology. This topology assumes that no stubs are used to connect any devices on the net. Figure 2 shows two possible techniques to achieve a stubless trace. When it is not possible to apply one of these two techniques due to congestion, a very short stub is allowed — preferably not to exceed 250 mils.

Figure 2. Examples of Stubless and Short Stub Traces



3.1 Trace Length Limits

For add-in cards, trace lengths from the top of the card edge connector to the 80303 I/O processor are as follows:

- The maximum trace length for all 32-bit interface signals should not exceed 1.5 inches for 32-bit and 64-bit cards. This includes all signals except those listed as ‘Signal Pins’, ‘Interrupt Pins’, and ‘JTAG Pins’ as per *PCI Local Bus Specification* Revision 2.2.
- The trace length of the additional signals used in the 64-bit extension are limited to 2 inches on all 64-bit cards.
- The trace length for the PCI CLK signal is 2.5 inches ± 0.1 inch for 32-bit and 64-bit cards and should be routed to only a single load.

4.0 Intel® 80303 I/O Processor Memory Subsystem

The 80303 I/O processor integrates a memory controller to provide a direct interface between the 80303 I/O processor and its local memory subsystem. The memory controller supports:

- Up to 16 Mbytes of 8-bit Flash, ROM, or SRAM
- Between 32 and 512 Mbytes of 64-bit synchronous DRAM (SDRAM)
- Single-bit error correction, double-bit and nibble detection support (ECC)

The Flash interface provides an 8-bit data bus, 23-bit address bus, and control to support up to two 64 Mbit Bulk-Erase or Boot-Block Flash devices. The Flash devices provide storage for the 80303 I/O processor initialization code.

The memory controller provides a separate SDRAM interface from the Flash interface. The SDRAM interface consists of a 100 MHz, 64-bit wide data path to support 800 Mbytes/sec throughput. An 8-bit Error Correction Code (ECC) across each 64-bit word improves system reliability.

- The memory controller supports two banks of SDRAM in the form of a single two-bank dual inline memory module (DIMM) or two single-bank DIMMs.
- The memory controller responds to internal bus memory accesses within its programmed address range and issues the memory request to either the Flash or SDRAM interface.

The memory controller provides four chip enables to the memory subsystem. Two chip enables service the SDRAM subsystem (one per bank) and two service the Flash devices.

Note: If the design does not follow the listed guidelines, then it is very important that the design be simulated. Even if the guidelines are followed it is still recommended that the design be simulated for proper signal integrity, flight time, and cross talk.

4.1 ROM, SRAM, or Flash Guidelines

The 80303 I/O processor memory controller provides an interface to two banks of static memory ranging from 64 Kbytes to 16 Mbytes. This memory may be SRAM, ROM, or Flash. Optionally, one of the banks may be dedicated to a UART device. Table 1 defines all Flash interface signals.

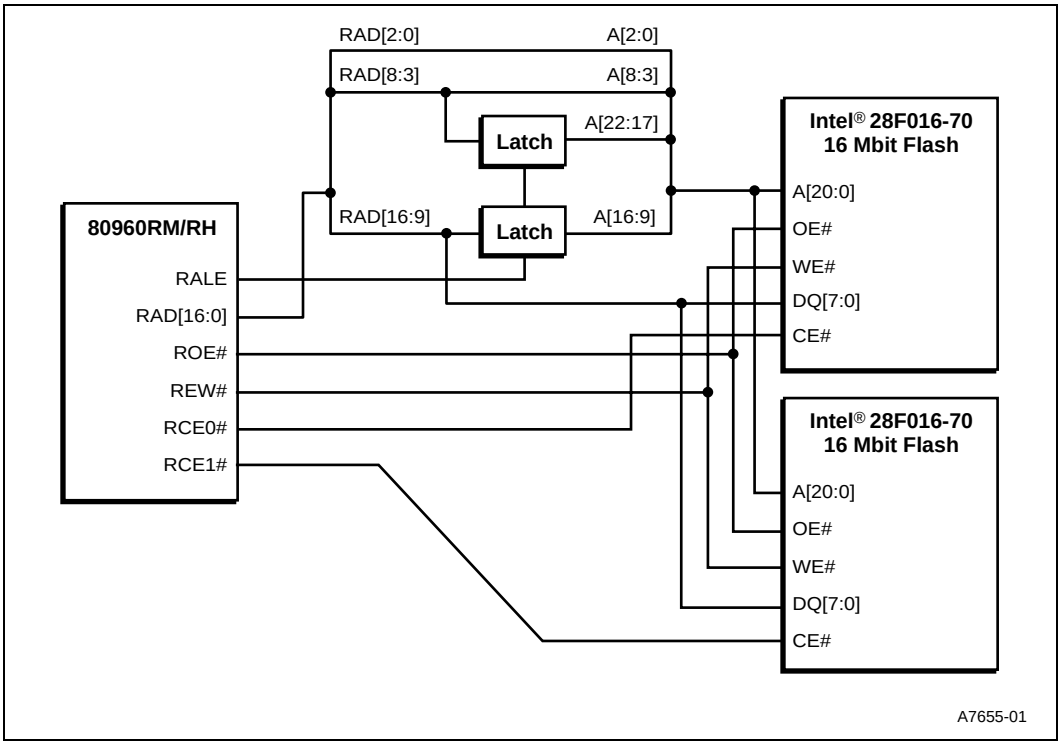
Table 1. Flash Interface Signals

Pin Name	Description
RCE[1:0]#	*Chip Enable* - Asserted for all transactions to the Flash device.
RWE#	*Write Enable* - Controls the Flash input data buffers.
ROE#	*Output Enable* - Asserted for reads, deasserted for writes. Controls the Flash output data buffers for write transactions.
RAD[16:0]	*Address/Data bus* - Capable of supporting 16 Mbit of Flash (2Mx8). The data bus is multiplexed on **RAD[16:9]**.
RALE	*Address Latch Enable* - Indicates the transfer of a physical address. **RALE** is asserted during a Flash address cycle and deasserted before the beginning of the data cycle.

4.1.1 Layout Guidelines

Figure 3 illustrates how two Flash devices would interface to the 80303 I/O processor with the memory controller. The Flash subsystem requires an external latch for address and data demultiplexing on **RAD[16:3]**. The data is multiplexed on **RAD[16:9]**.

Figure 3. 4 Mbyte Flash Memory System



Flash signal loading should not exceed 50 pF. If the system conforms to I_2O specification, then a minimum 16 Mbit Flash such as Intel's 28F016SA is suggested.

All traces between the 80303 I/O processor and Flash/SRAM should not exceed 8 inches.

4.1.2 Wait State Profiles

Table 2 summarizes various wait state profiles of SRAM and writable non-volatile memory devices.

Table 2. ROM, SRAM, or Flash Wait State Profile Programming

Device Speed	Address-to-Data Wait States	Recovery Wait States
≤ 55 ns	8	4
≤ 115 ns	12	4
≤ 175 ns	20	4

4.2 SDRAM Guidelines

The 80303 I/O processor memory controller supports up to two banks of 100 MHz, 72-bit SDRAM. The memory controller supports 64Mbit, 128Mbit or 256Mbit SDRAM technology offering up to 512Mbytes of ECC protected memory. The 80303 I/O processor only supports 64-bit wide unbuffered SDRAM with ECC. 32-bit wide SDRAM is not supported.

Table 3 shows the SDRAM interface signals.

Table 3. SDRAM Interface Signals

Pin Name	Description
DCLK[3:0]	*SDRAM Clock Out* - These are the four output clocks driven to the Unbuffered DIMMs supported by the Intel® 80303 I/O processor**.**
DCLKOUT	*SDRAM Clock Out* - This clock is driven in to the memory subsystem so that **DCLK[3:0]** may be skewed back to accommodate for the clocks' flight time and be compatible with 100/133 MHz SDRAM technologies.
DCLKIN	*SDRAM Clock In* - This is the **DCLKOUT** clock returning from the memory subsystem.
SCKE[1:0]	*Clock enables* - One clock after **SCKE[1:0]** is deasserted, the data is latched on **DQ[63:0]** and **SCB[7:0]**. The burst counters within the SDRAM device are not incremented. Deasserting this signal places the SDRAM in self-refresh mode. For normal operation, **SCKE[1:0]** must be asserted.
SDQM[7:0]	*Data Mask* - On a write, these signals disable the data on a byte-by-byte basis, thus preventing certain bytes from being written. On a read, two clocks after asserting **SDQM[7:0]** the output data bytes from the SDRAM device are disabled.
SCE[1:0]#	*Chip Select* - Must be asserted for all transactions to the SDRAM device. One per bank.
SWE#	*Write Enable* - Controls the SDRAM data input buffers. Asserting **SWE#** causes the data on **DQ[63:0]** and **SCB[7:0]** to be written into the SDRAM devices.
SBA[1:0]	*SDRAM Bank Selects* - Controls which of the internal SDRAM banks to read or write. For 16 Mbit devices (2 banks), only **SBA[0]** is used while 64 Mbit devices use **SBA[1:0]**.
SA[10]	*Address bit 10* - If high during a read or write command, then auto-precharge occurs after the command. During a **row-activate** command, this bit is part of the address.
SA[13:0]	*Address bits 13 through 0* - Indicates the row or column to access depending on the state of **SRAS#** and **SCAS#**.
SRAS#	*Row Address Strobe* - Indicates that the current address on **SA[13:0]** is the row.
SCAS#	*Column Address Strobe* - Indicates that the current address on **SA[13:0]** is the column.
DQ[63:0]	*Data Bus* - 64-bit wide data bus.
SCB[7:0]	*ECC Bus* - 8-bit error correction code which accompanies the data on **DQ[63:0].**

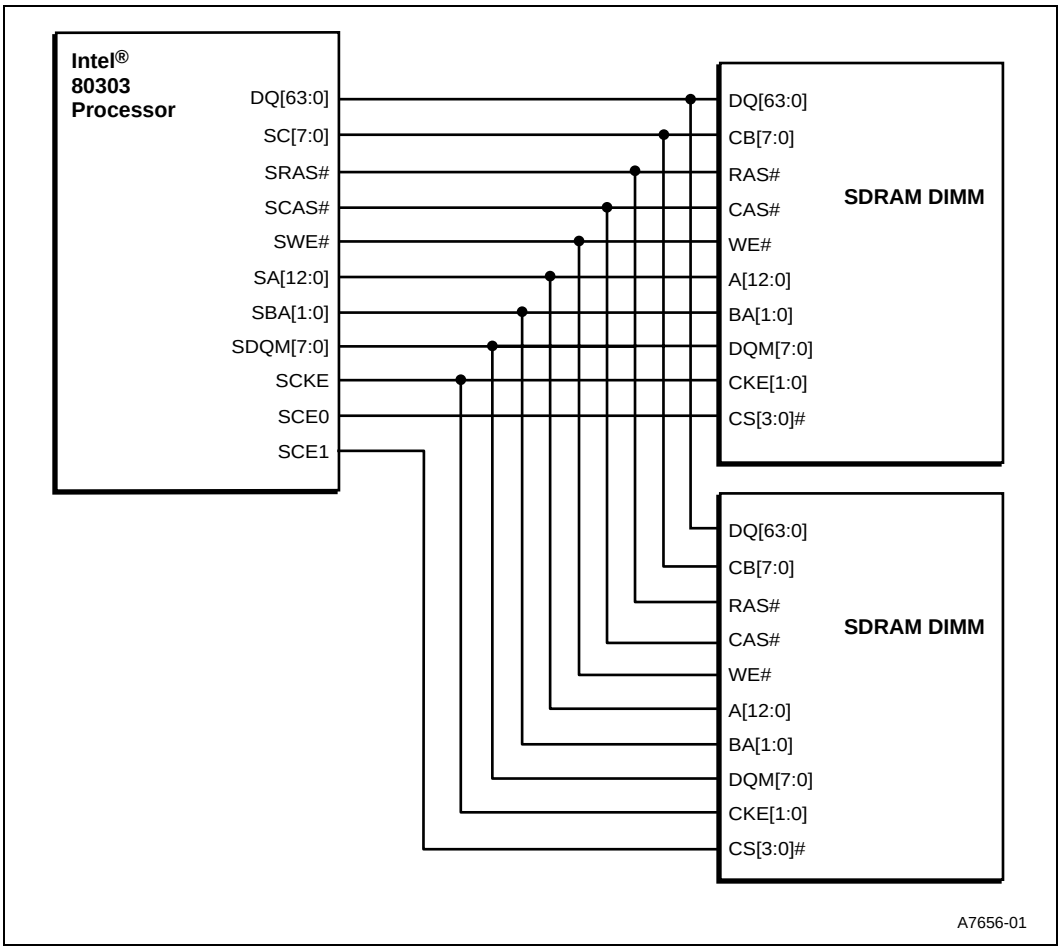
4.2.1 Layout Guidelines

The SDRAM subsystem may be implemented with:

- up to two banks directly connected on the printed circuit board (72 bits wide)
- up to two 168-pin DIMM sockets (72 bits wide)

The memory controller supports either one dual-bank DIMM or two single-bank DIMMs. The *72-bit ECC Unbuffered SDRAM DIMM Specification* requires four clock inputs. Figure 4 illustrates how two banks of SDRAM interfaces with the 80303 I/O processor memory controller. For the clock routing, refer to Figure 16.

Figure 4. Dual-Bank SDRAM Memory Subsystem



The drive strengths for the SDRAM signals are independently programmable using the SDCR register. Table 4 lists some example SDRAM configurations and how the SDCR should be programmed. The 80303 I/O processor determines the SDRAM configuration with the Serial Presence Detect EEROM (SPD) located on the DIMM. The I^2C bus interfaces the 80303 I/O processor with the SPD.

Table 4. Drive Strength Programmability Options

Bus Width	Form Factor	Bank 0	Bank 1	SDCR[4:3] (SDQ)	SDCR[6:5] (SCE0#, SCKE0)	SDCR[8:7] (SCE1#, SCKE1)	SDCR[10:9] (SDQM)	SDCR[12:11] (SA[12:0], Controls)
72	1 single-sided DIMM	9[x8]	None	00	01	10	10	10
	2 single-sided DIMMs	9[x8]	9[x8]	01	10	10	10	10
	1 double-sided DIMM	9[x8]	9[x8]	01	10	10	10	10
	1 single-sided DIMM	5[x16]	None	00	01	01	01	01
	2 single-sided DIMMs	5[x16]	5[x16]	01	10	01	01	10
	1 double-sided DIMM	5[x16]	5[x16]	01	10	01	01	10

NOTES:
1. 8-bit SDRAM are available in 64Mbit, 128Mbit, and 256Mbit SDRAM technologies.
2. 16-bit SDRAM are available in 64Mbit and 128Mbit SDRAM technologies.

Specific SDRAM signal topologies have been validated for 66 and 100 MHz operations. The following figures illustrate the proven topologies and are recommended. Proper signal integrity analysis should verify any other signal topologies.

To minimize crosstalk, SDRAM signal routing should use a minimum of 5 mils spacing and 5 mils trace width. SDRAM clocks should use a minimum of 12 mils spacing and 6 mils trace width.

Figure 5. Single DIMM Address, Data and Control Signals

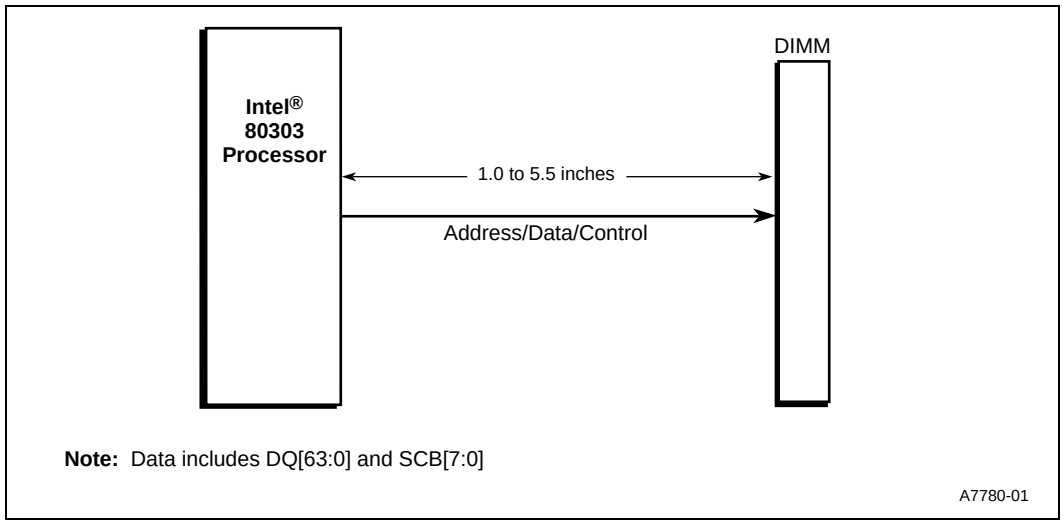


Figure 6. Dual DIMM Address, Data and Control Signals

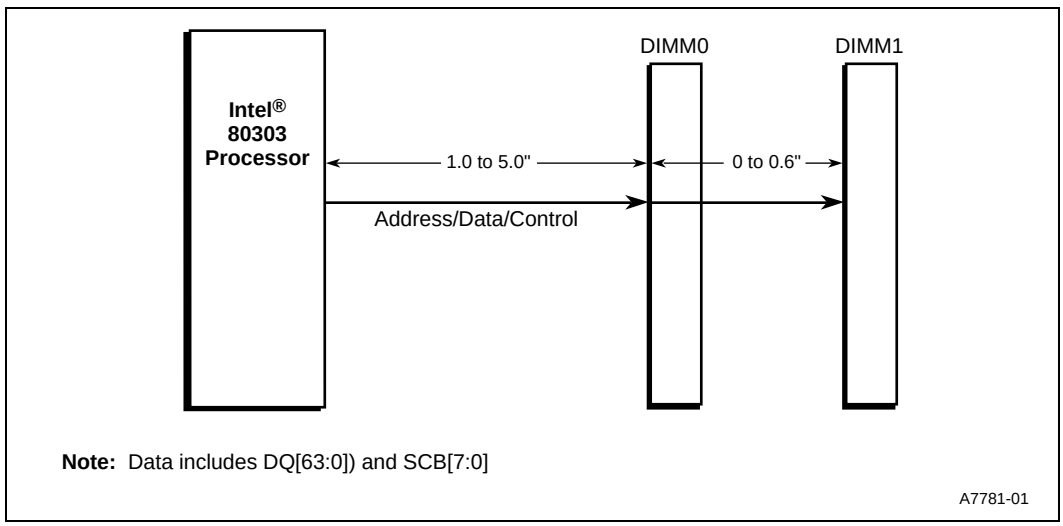


Figure 7. Single DIMM SCE[1:0] Signals

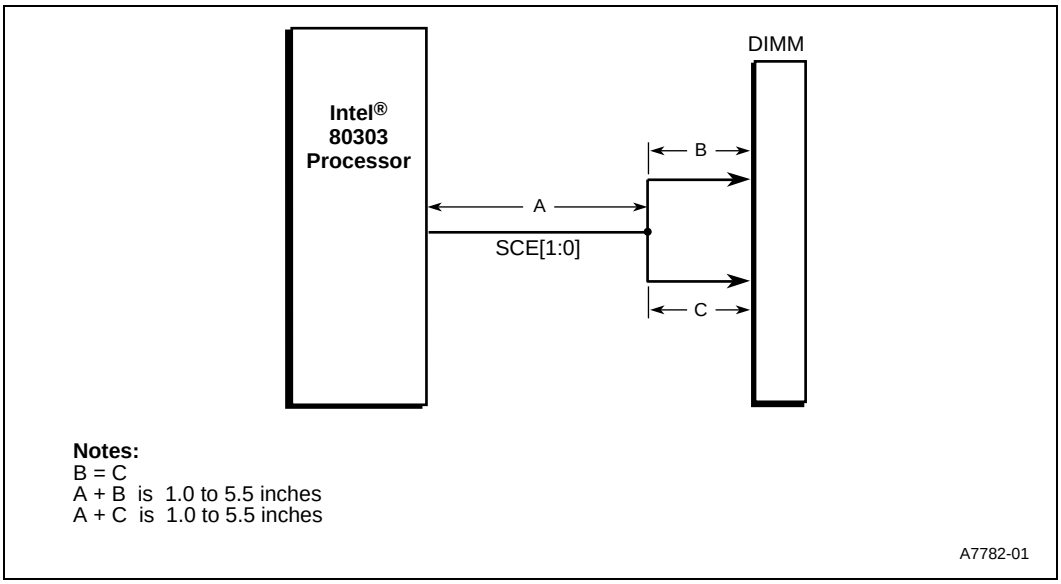


Figure 8. Dual DIMM SCE[1:0] Signals

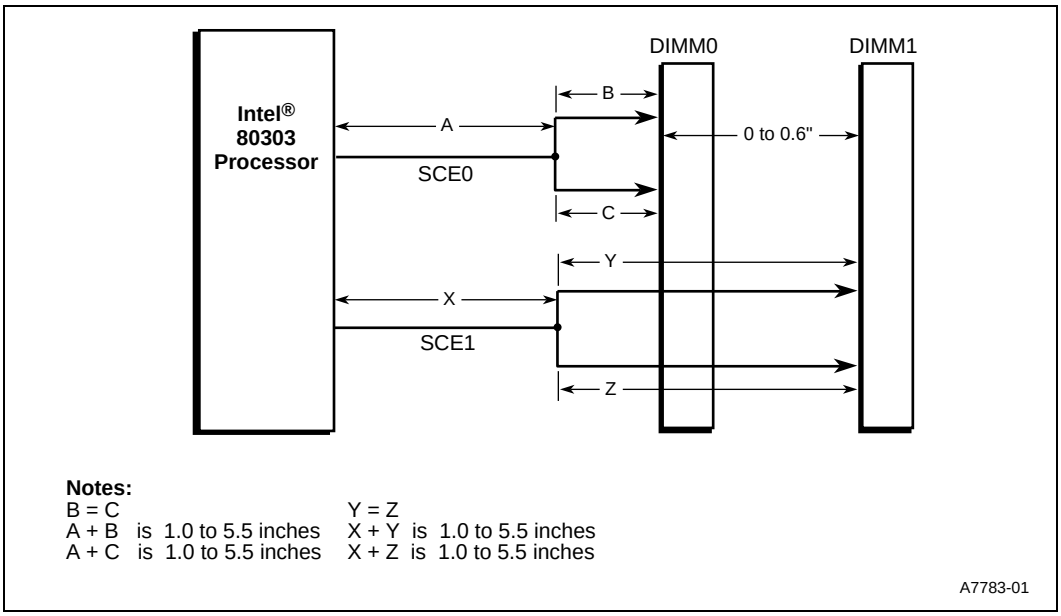


Figure 9. Single DIMM SCKE[1:0] Signals

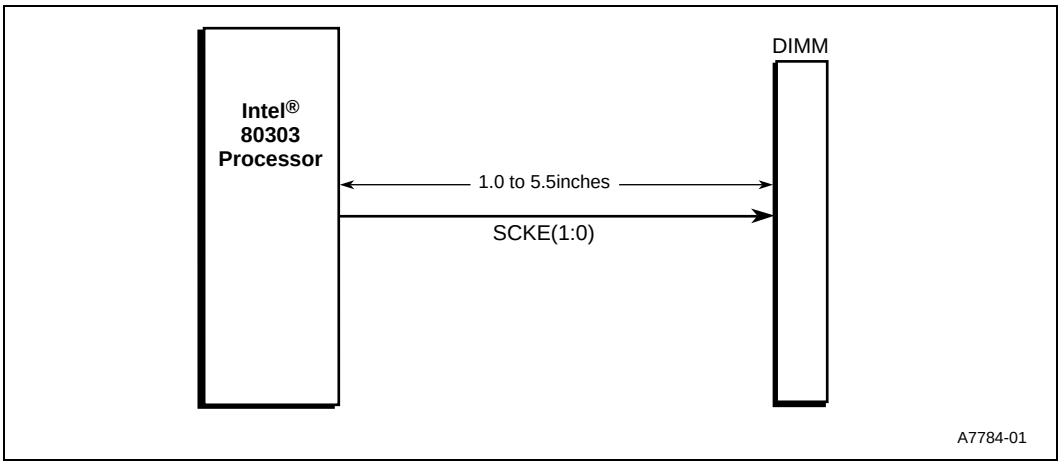


Figure 10. Dual DIMM SCKE[1:0] Signals

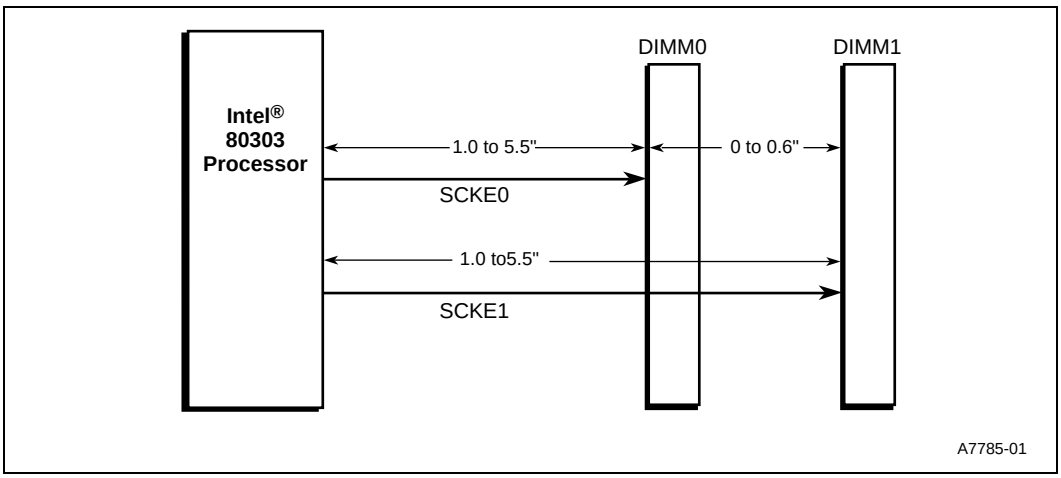


Figure 11. Single DIMM SDQM[7:0] Signals

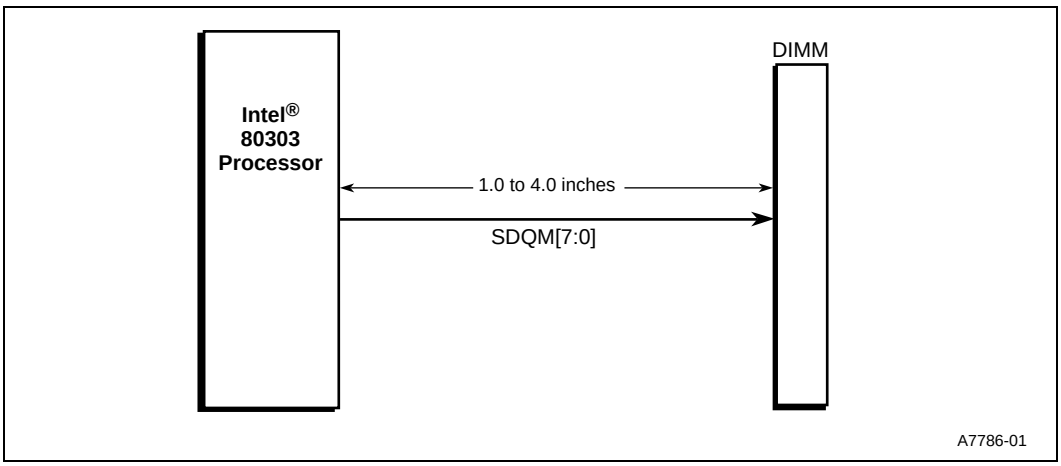


Figure 12. Dual DIMM SDQM[7:0] Signals

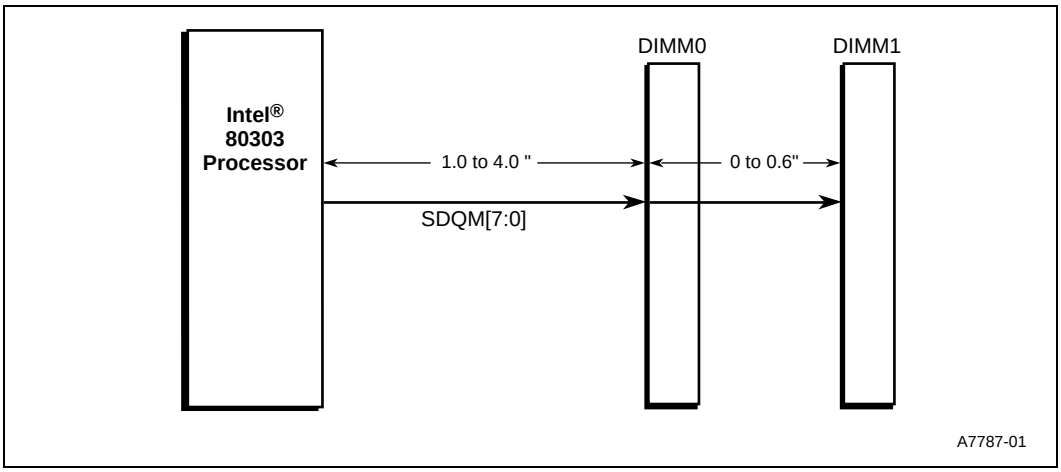


Figure 13. Discrete SDRAM Address and Control Signals

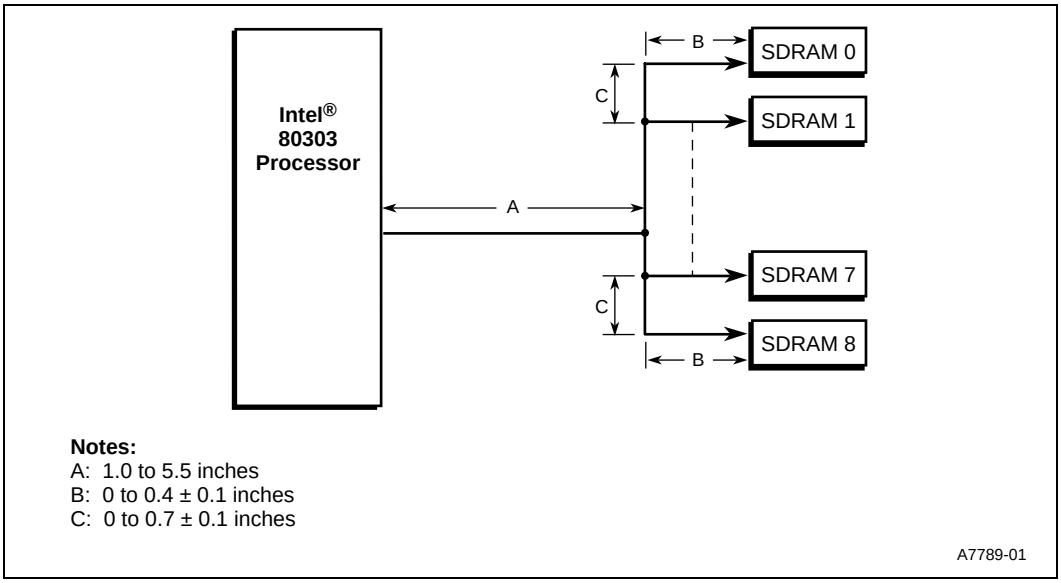


Figure 14. Discrete SDRAMs Data Signals

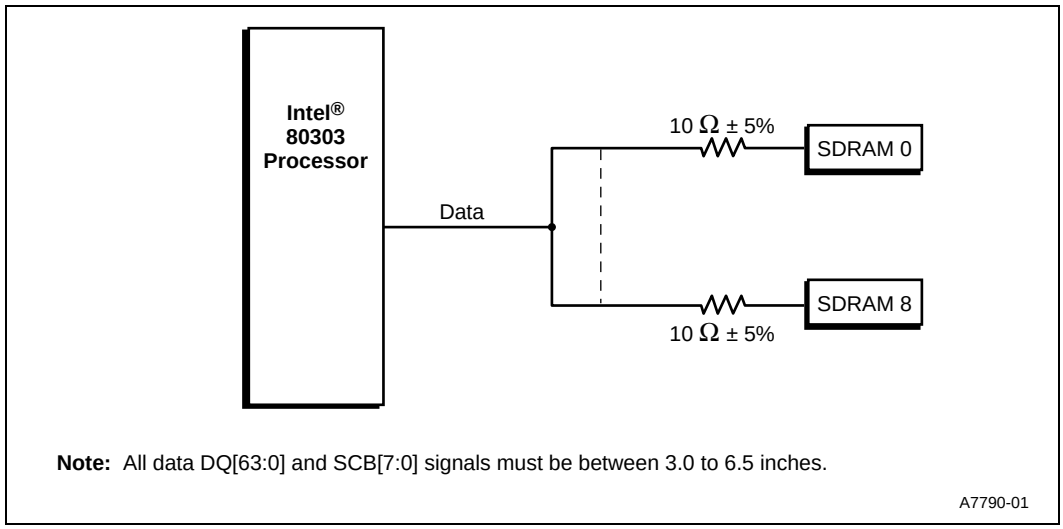
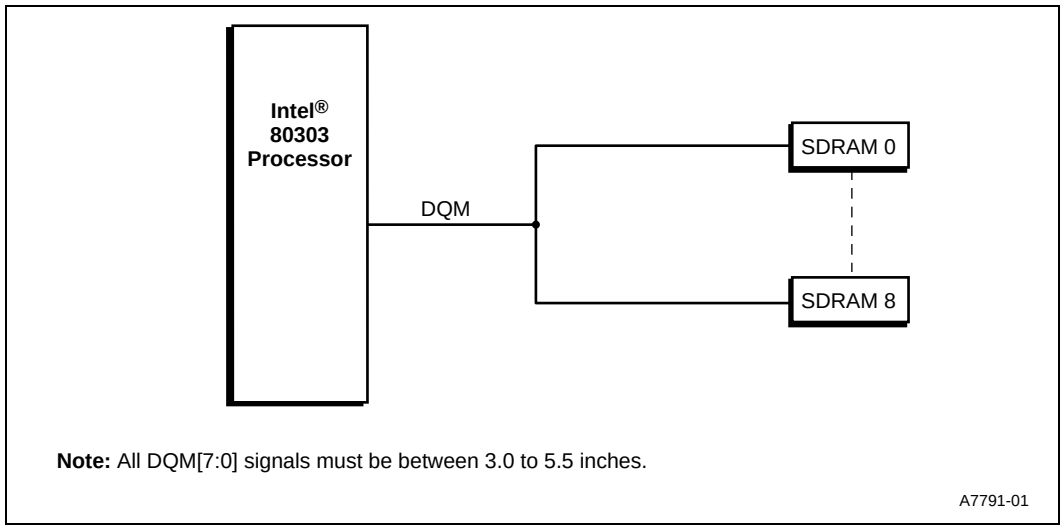


Figure 15. Discrete SDRAMs DQM[7:0] Signals

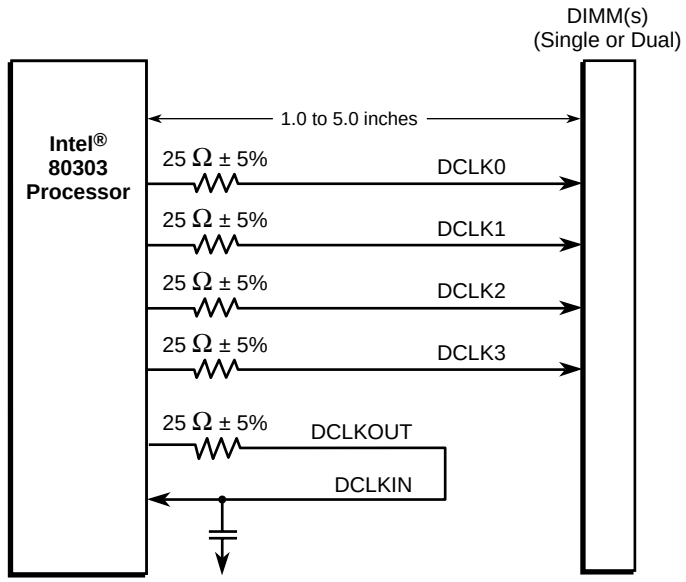


The address and control signals for the SDRAM subsystem include **SA[13:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SRAS#**, and **SWE#**. The SDRAM data signals include **DQ[63:0]**, and **SCB[7:0]**.

4.2.2 SDRAM Clocking

The MCU provides five clock signals (**DCLKOUT** and **DCLK[3:0]**) to the SDRAM memory subsystem with a 100MHz frequency. The 72-bit, 2-bank SDRAM DIMM specification requires four clocks to distribute the loading across eighteen x8 SDRAM components. Refer to Figure 16 for the clock routing diagram. External resistors and capacitors are required for proper signal integrity and clock skew management.

Figure 16. Clocking for a Dual-Bank SDRAM DIMM



Notes:
1. Single bank DIMM uses only two clocks. Therefore, in a dual DIMM design, each DIMM gets two clocks.
2. All the DCLK[3:0] should be equal in length. This also applies for dual DIMM designs.
3. DCLKIN/DCLKOUT trace length should be equal to DCLK[3:0] plus 4.0 ± 0.1 inches.
4. Use a 20 pF load on DCLKIN. Keep the load within 0.5 inches from the Intel 80303 DCLKIN ball.
5. Use 25 Ohms series resistors on DCLK[3:0] and DCLKOUT. Keep the series resistors within 0.5 inches of the Intel 80303 respective balls.
6. These guidelines also apply to discrete SDRAMS.

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Note: Any single SDRAM bank will use *two* clock outputs. Four clock outputs are used only when two SDRAM banks are populated.

The clock outputs may be between 1 and 5.0 inches. Each of the four clock outputs (**DCLK[3:0]**) must be equal in length. **DCLKIN** must be 4 inches longer then the output clocks and requires an external capacitor (20 pF) to match the loading seen on the other clock outputs. *Traces from the processor to the capacitor must be within 0.5 inches.*

Note: The *100 MHz Unbuffered 168-Pin SDRAM DIMM* requires four clock inputs. The lumped capacitance value required on DCLKIN is 20 pF in this reference design.

4.2.3 SDRAM Power Failure Guidelines

SDRAM technology provides a simple way of enabling data preservation through the **self-refresh** command. When the memory controller issues this command, the SDRAM refreshes itself autonomously with internal logic and timers.

The SDRAM device remains in self-refresh mode as long as:

- The device continues to be powered.
- **SCKE** is held low until the memory controller is ready to control the SDRAM once again.

The board design should ensure power to the SDRAM subsystem with an adequate battery backup and a reliable method for switching between system power and battery power. The memory controller is responsible for deasserting **SCKE[1:0]** when issuing the **self-refresh** command however, while power gradually drops, **SCKE[1:0]** must remain deasserted regardless of the state of V_{cc} powering the 80303 I/O processor.

4.2.4 System Assumptions

Reliable power must be present for at least 1 ms so that the 80303 I/O processor memory controller can execute its power-fail sequence. According to the PCI specification, P_RST# can be asserted when power has reached as low as 2.5 volts, which is too low for the 80303 I/O processor to operate. To overcome this problem, an external voltage detection circuit that will trigger just below 3.0 volts must be used.

The 80303 I/O processor power-fail state machine can not be initialized by the P_RST# pin like the rest of the device's state machines since the power-fail state machine is operational during P_RST# assertion.

The 80303 I/O processor provides a dedicated input pin, PWRDELAY that is used to initialize the memory controller's power-fail state machine when deasserted. This signal must be deasserted during the assertion of P_RST# and then gets asserted following the deassertion of P_RST#. PWRDELAY will not be deasserted again until power has truly failed. The IQ80303 schematics in Appendix A provides an example circuit to generate PWRDELAY.

4.2.5 External Logic Required for Power Failure

4.2.5.1 SCKE Logic

Figure 17 shows the state machine of the external logic required to control the SCKE[1:0] signals. Actual implementations may vary.

Figure 17. External Power Failure State Machine

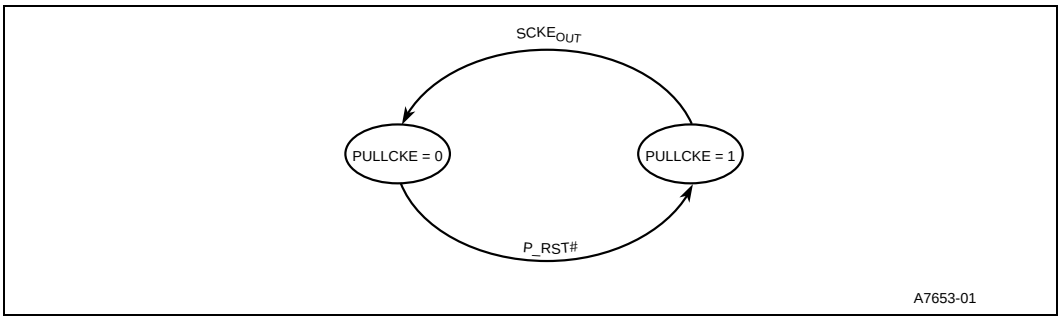
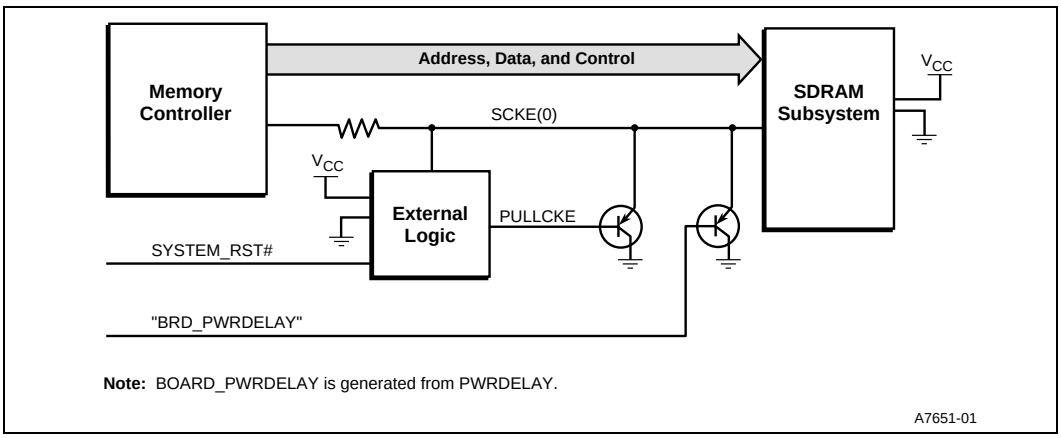


Figure 18. External Power Failure Logic in the System



The implementation illustrated in Figure 18 requires all external logic powered by V_{batt}. The edge detect state machine activates the pull-down when the MCU deasserts **SCKE[1:0]**. As long as V_{batt} is active, **SCKE[1:0]** is held low. Once the memory controller is reset, the rising edge of P_RST# deactivates the pull-down. The memory controller reliably controls **SCKE[1:0]** at this point, driving it low. Refer to IQ80303 schematics in Appendix A for an implementation example.

Note: Figure 18 shows logic for one **SCKE** signal. The loading of this signal is large enough that two signals are required (one per SDRAM bank) and the above logic should be replicated for each **SCKE[1:0]**.

The block diagram in Figure 19 show how SYSTEM_RST# and PWRDELAY can be generated. SYSTEM_RST# drives the 80303 I/O processor P_RST# signal and PWRDELAY drives the 80303 I/O processor PWRDELAY signal. SYSTEM_RST# is asserted when either PCI_RST# or the output of the comparator is asserted (low). When SYSTEM_RST# is asserted, the power-fail state machine on 80303 I/O processor is triggered. The output of the comparator is asserted when Vcc drops just below 3.0 Volts. PWRDELAY logically looks like PCI_RST# as shown in Figure 20, only that PWRDELAY transitions with a delay based on capacitor (C1). Since PWRDELAY is used to reset the power-fail state machine when low, the delay circuit allows ample time for the power-fail state machine to execute the power-fail sequence.

Note: P_RST# signal on 80303 I/O processor (driven by SYSTEM_RST#) triggers a power-fail sequence when transitioning from high to low. PWRDELAY is used to reset the power-fail state machine. The delay circuit in Figure 19 allows the power-fail state machine to execute the power-fail sequence before resetting.

Figure 19. Logic Generating PWRDELAY and SYSTEM_RST#

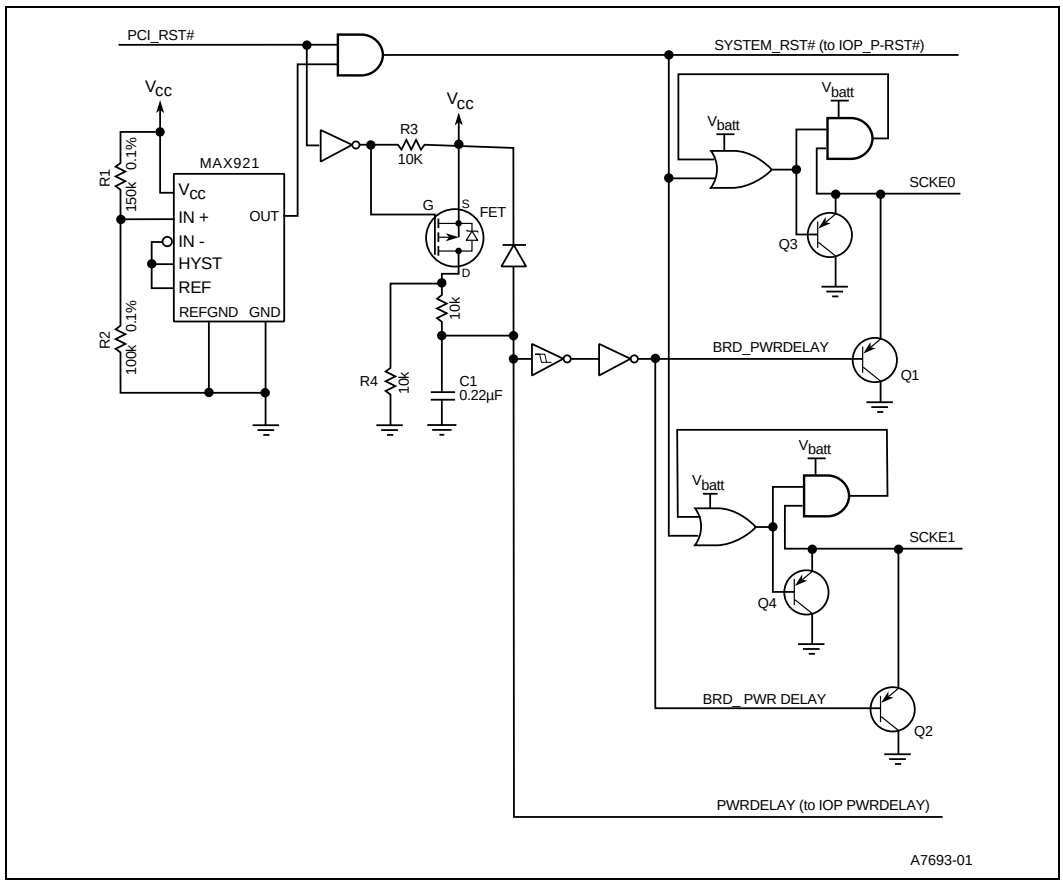
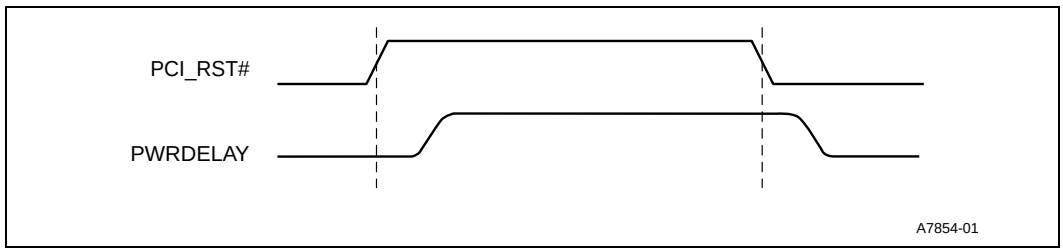


Figure 20. PWRDELAY Timings



In addition to the edge detect state machine described above, a second pull-down is used to force the SCKE[1:0] signals low during power-up. This is necessary if V_{batt} is not present during power-up. During power-up the 80303 I/O processor may erroneously toggle the SCKE[1:0] signals during. If the SCKE[1:0] signals toggle, they may cause the SDRAM to lock up.

Note: PWRDELAY can be permanently pulled low with a 1.5K pull-down resistor when the battery back-up circuit is not implemented.

5.0 Interrupt Routing

As stated in the *PCI Local Bus Specification* Revision 2.2 and the *PCI-to-PCI Bridge Architecture Specification* Revision 1.1, interrupt routing is system-specific. In general, the BIOS maps the device's interrupt line to the 80303 I/O processor's secondary bus INTx line. The IDSEL address originates from the 80303 I/O processor's secondary address bus and connects to the device's IDSEL pin or PCI connector slots.

Table 5 provides interrupt routing for devices with a single interrupt pin. Multifunction devices, which have more than one interrupt pin, would follow the interrupt routing guidelines shown in Figure 21. In this case, replace the connector with the multifunction device.

Table 5. Intel® 80303 I/O Processor Interrupt Routing Signals

Device's IDSEL Signal Pin	Device Interrupt Signal
S_AD16, 20, 24, 28	INTA#
S_AD17, 21, 25, 29	INTB#
S_AD18, 22, 26, 30	INTC#
S_AD19, 23, 27, 31	INTD#

Secondary Address lines **S_AD[25:16]** can be configured for public devices or private devices depending on the Secondary ID Select Register (SISR). **S_AD[31:26]** are for public devices only. When PCI connectors are present on the 80303 I/O processor's secondary bus, the interrupts rotate on the subsequent PCI connectors as shown in Figure 21.

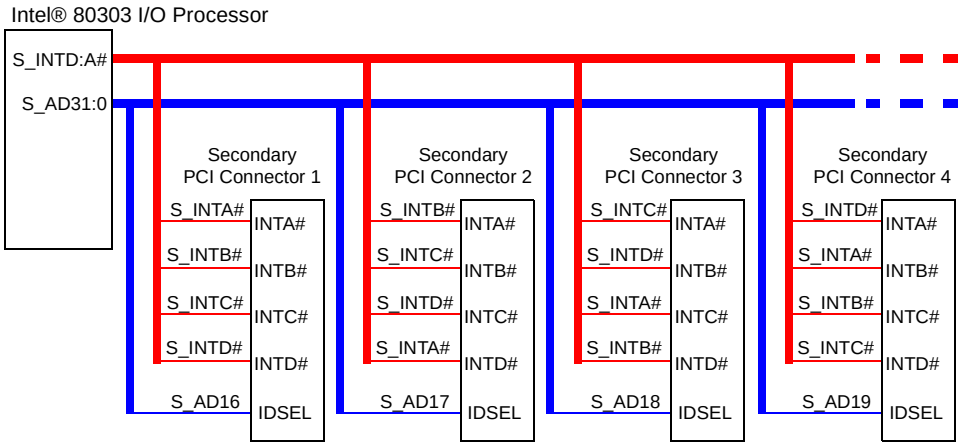
5.1 Intel® 80303 I/O Processor Implementation on a MotherBoard

When implementing the 80303 I/O processor onto a motherboard, you must adhere to the Device ID address and interrupt routing scheme used on the primary side of the PCI bus which is dependent on the individual motherboard implementation.

5.2 Intel® 80303 I/O Processor Implementation on an Add-in Card

When designing the 80303 I/O processor into an add-in card, refer to Figure 21 for Device ID address and interrupt routing.

Figure 21. Example Secondary PCI Connector Interrupt Routing



NOTE: Secondary PCI Bus interrupt signals “rotate” on subsequent PCI connectors.

6.0 Clocking Guidelines

The 80303 I/O processor uses **P_CLK** (synchronous clock) input for clocking. All AC timings on the primary PCI bus are referenced to the **P_CLK** input. The 80303 I/O processor provides six output clocks (**S_CLK[5:0]**) for devices on the secondary PCI bus. All AC timings on the secondary PCI bus are referenced to **S_CLK[5:0]**.

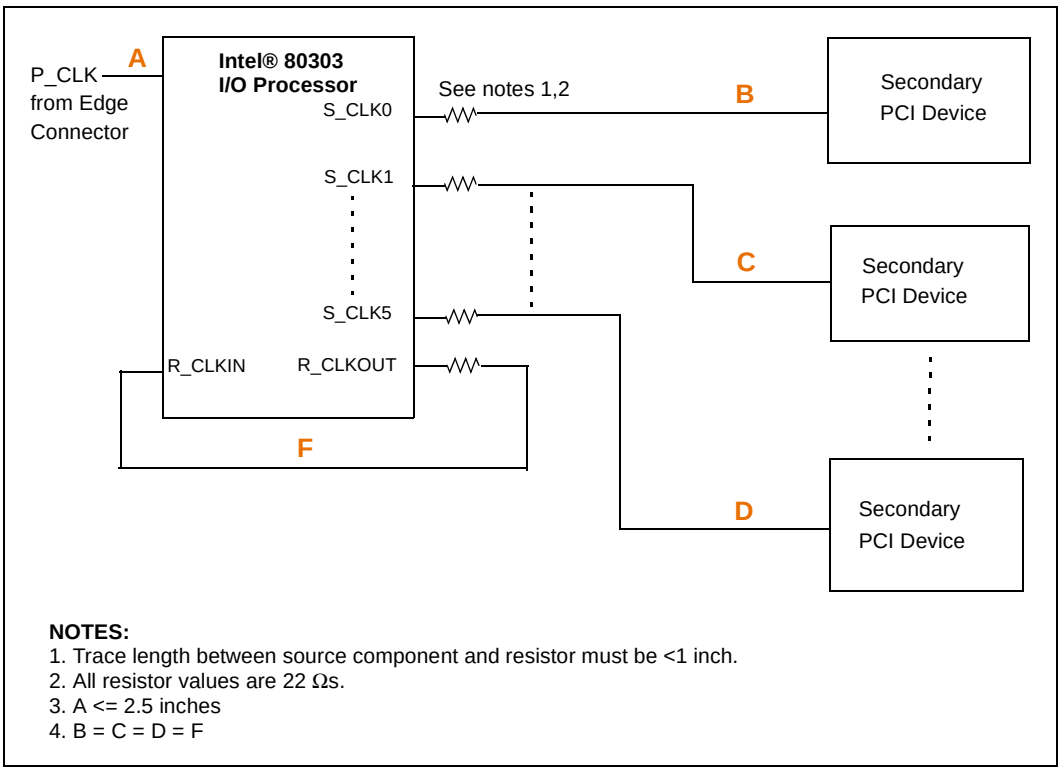
6.1 Layout Guidelines for Add-in Cards

A PCI edge connector provides a singular PCI clock which must only be connected to *one load* on the add-in card. Add-in cards which contain the 80303 I/O processor can use the output clocks (**S_CLK[5:0]**) for devices on the secondary PCI bus.

The PCI bus specification allows a maximum PCI clock skew of 2 ns between any two devices connected on the PCI bus (allowable clock skew for 66 MHz is 1 ns). To minimize skew on the primary PCI bus, place the 80303 I/O processor as close as possible to the PCI edge connector. Trace length from the PCI edge connector to the 80303 I/O processor P_CLK input ("A" in Figure 22) must be as short as physically possible (max length 2.5 inches).

For the secondary PCI bus, allowable skew is 2 ns between any device on the secondary PCI bus (allowable clock skew for 66 MHz is 1 ns). In general, keep these secondary clock routes shorter than eight inches to provide a skew of less than 2 ns.

Figure 22. PCI Add-in Card Example Configuration



6.2 Layout Guidelines for Motherboards

For motherboard implementations, the designer has much more flexibility with PCI clocking, primarily related to controlling the central clock resources. Skew requirements for the motherboard are more stringent due to the uncertainty of having PCI edge connectors on the secondary bus.

For motherboard implementation designs, it is best to choose a central clocking resource with enough PCI clock outputs to drive all PCI devices, including the 80303 I/O processor I/O processor P_CLK. All trace lengths should be equalized to minimize clock skew. The 80303 I/O processor I/O processor provides secondary PCI clocks (**S_CLK[5:0]**, R_CLKIN and R_CLKOUT) for secondary devices connected to its secondary PCI bus. All trace lengths should be equalized to minimize clock skew. R_CLKIN should be directly connected to R_CLKOUT and the trace length should match **S_CLK[5:0]**. Keep the secondary clock routes between 1.0 to 8.0 inches to maintain a 1 ns skew. Refer to Figure 23 for clock configuration example.

To minimize skew for these designs, use the following equation for trace length (see Figure 23):

Equation 1. A = B - 2.5 Inches

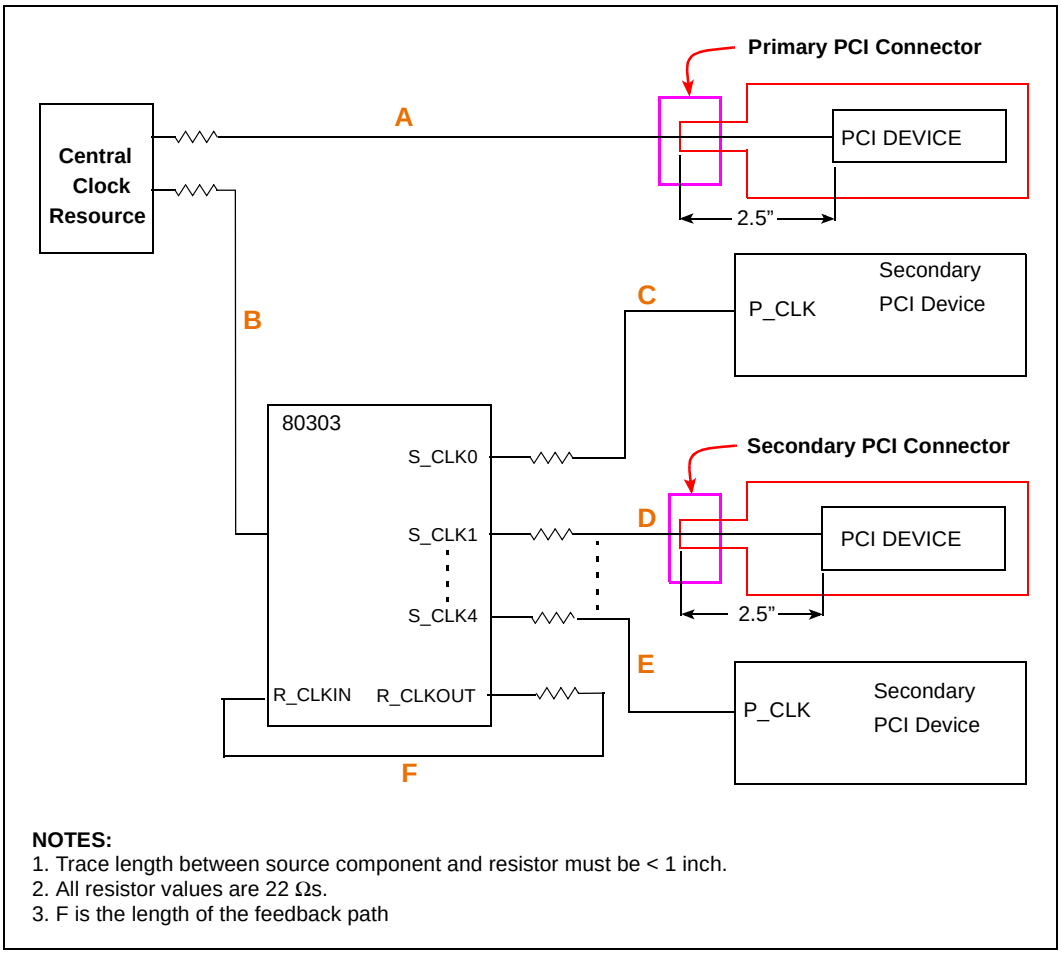
Equation 2. C = E

Equation 3. D = C - 2.5 Inches

Equation 4. C = E = F

S_CLK[5:0] and R_CLKOUT should be kept within 1 to 8 inches. Also, since implementations can be varied, each design must be simulated to meet specifications as per *PCI Local Bus Specification* Revision 2.2. To minimize skew, clocks to connectors should be 2.5 inches shorter than traces routed to motherboard devices.

Figure 23. Motherboard Example Configuration



NOTES:
1. Trace length between source component and resistor must be < 1 inch.
2. All resistor values are 22 Ωs.
3. F is the length of the feedback path

7.0 Intel® 80303 I/O Processor Signals Requiring Pull-Up/Down Resistors

Table 6 through Table 8 identify the signals that require pull-up and/or pull-down resistors and the recommended resistor values.

Table 6. Memory Controller, Core and JTAG Signals

Signal	Resistor Value (in Ω)	Pull-up or Pull-down	Comments
RAD[6]/RST_MODE#	1.5K	pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[4]/STEST	2.7K	pull-up or pull-down	Pull-up to enable RAD[4]/STEST, pull-down to disable.
RAD[3]/RETRY	1.5K	pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[2]/SPMEM#	1.5K	pull-down[2]	Pull-down for 32-bit SDRAM protocol. This signal has an internal pull-up.
RAD[1]/32BITPCI_EN#	1.5K	pull-down[3]	Pull-down for 32-bit SPCI bus protocol. This signal has an internal pull-up.
NMI#	2.7K	pull-up	
TRST#	1.5K	pull-down	Alternatively this signal may be tied to P_RST#.
GPIO[7:0]	1.5K	pull-down[4]	These pins have internal pull-ups which by default make them input pins after reset.
PWRDELAY	1.5K	pull-down	When not implementing the battery back-up circuit for the SDRAM, this pin can be permanently pulled low. There is no internal pull-up on this pin.

NOTES:
1. Pull-down only if other than default Reset Mode is required.
2. Pull-down only if a special downstream memory window is required to support an external Hot-Plug controller.
3. Pull-down only if the secondary PCI bus is required to function as a 32-bit bus.
4. Pull-down only if required to be output after reset.

Table 7. I²C Bus Signals

Signal	Resistor value (in Ω)	Pull-up or Pull-down	Comments
SCL	2.7K	pull-up	This signal must have a pull-up to allow reading the SDRAM size.
SDA	2.7K	pull-up	This signal must have a pull-up to allow reading the SDRAM size.

Table 8. PCI Signals

Signal	Resistor value (in Ω)	Pull-up or Pull-down	Comments
S_SERR#	8.2K	pull-up	On Secondary Bus
S_TRDY#	8.2K	pull-up	On Secondary Bus
S_LOCK#	8.2K	pull-up	On Secondary Bus
S_PERR#	8.2K	pull-up	On Secondary Bus
S_DEVSEL#	8.2K	pull-up	On Secondary Bus
S_ FRAME#	8.2K	pull-up	On Secondary Bus
S_ STOP#	8.2K	pull-up	On Secondary Bus
S_ IRDY#	8.2K	pull-up	On Secondary Bus
S_ INTA#	8.2K	pull-up	On Secondary Bus
S_ INTB#	8.2K	pull-up	On Secondary Bus
S_ INTC#	8.2K	pull-up	On Secondary Bus
S_ INTD#	8.2K	pull-up	On Secondary Bus
XINT4#	8.2K	pull-up	On Secondary Bus
XINT5#	8.2K	pull-up	On Secondary Bus
S_ REQ0#	8.2K	pull-up	On Secondary Bus
S_ REQ1#	8.2K	pull-up	On Secondary Bus
S_ REQ2#	8.2K	pull-up	On Secondary Bus
S_ REQ3#	8.2K	pull-up	On Secondary Bus
S_ REQ4#	8.2K	pull-up	On Secondary Bus
S_ REQ5#	8.2K	pull-up	On Secondary Bus
S_AD[63:32]	8.2K	pull-up	On Secondary Bus
S_C/BE[7:4]#	8.2K	pull-up	On Secondary Bus
S_PAR64	8.2K	pull-up	On Secondary Bus
S_REQ64#	8.2K	pull-up	On Secondary Bus
S_ACK64#	8.2K	pull-up	On Secondary Bus
S_M66EN	8.2K	pull-up[1]	On Secondary Bus, a pull-up will make the secondary PCI bus operate at 66 MHz.
S_HOLD#	8.2K	pull-up	On Secondary Bus

NOTES:
1. Pull-up only if secondary PCI bus is to operate at 66 MHz. A pull-down is required for 33 MHz operation.

8.0 Intel® 80303 I/O Processor 5 V and 3.3 V Design Considerations

8.1 V_{CC5REF} Pin Requirement (V_{DIFF})

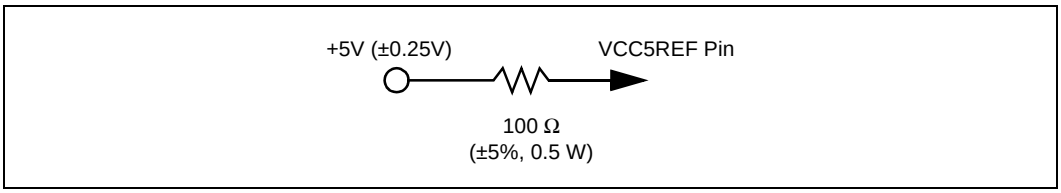
In mixed voltage systems that drive 80303 I/O processor inputs in excess of 3.3 V, the **V_{CC5REF}** pin must be connected to the system 5 V supply. To limit current flow into the **V_{CC5REF}** pin, there is a limit to the voltage differential between the **V_{CC5REF}** pin and the other V_{CC} pins. The voltage differential between the **V_{CC5REF}** pin and its 3.3V V_{CC} pins should never exceed 2.25V. Meeting this requirement ensures proper operation and guarantees component reliability. This limit applies to power-up, power-down, and steady-state operation. Table 9 outlines this requirement.

Table 9. V_{DIFF} Specification for Dual-Power Supply Requirements (3.3 V, 5 V)

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	**V_{CC5REF}** input should not exceed V_{CC} by more than 2.25V during power-up and power-down, or during steady-state operation.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 24, a 100 Ω 0.5W series resistor may be used to limit the current into the **V_{CC5REF}** pin. This resistor ensures that current drawn by the **V_{CC5REF}** pin does not exceed the maximum rating for this pin.

Figure 24. V_{CC5REF} Current-Limiting Resistor



This resistor is not necessary in systems that can guarantee the V_{DIFF} specification. Also, in 3.3V-only systems and systems that drive pins from 3.3V logic, connect the **V_{CC5REF}** pin directly to the 3.3V V_{CC} plane.

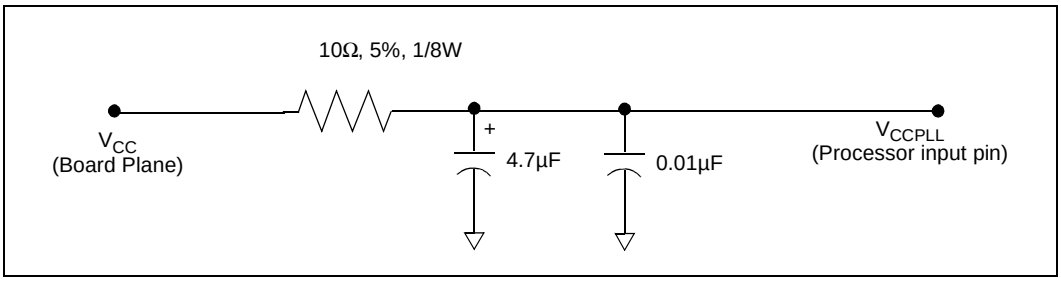
Note: This requirement also applies to the VREF_P and VREF_S pins.

8.2 V_{CCPLL} Pins Requirement

To reduce clock skew on the processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, shown in Figure 25, reduces noise induced clock jitter and its effects on timing relationships in system designs. The trace lengths between the 4.7 µF capacitor, the 0.01 µF capacitor, and V_{CCPLL} must be as short as possible.

There are three V_{CCPLL} pins on the 80303 I/O processor: V_{CCPLL1}, V_{CCPLL2} and V_{CCPLL3}. Each pin requires a lowpass filter. Providing just one lowpass filter and tying it to all three V_{CCPLL} inputs is not recommended.

Figure 25. V_{CCPLL} Lowpass Filter



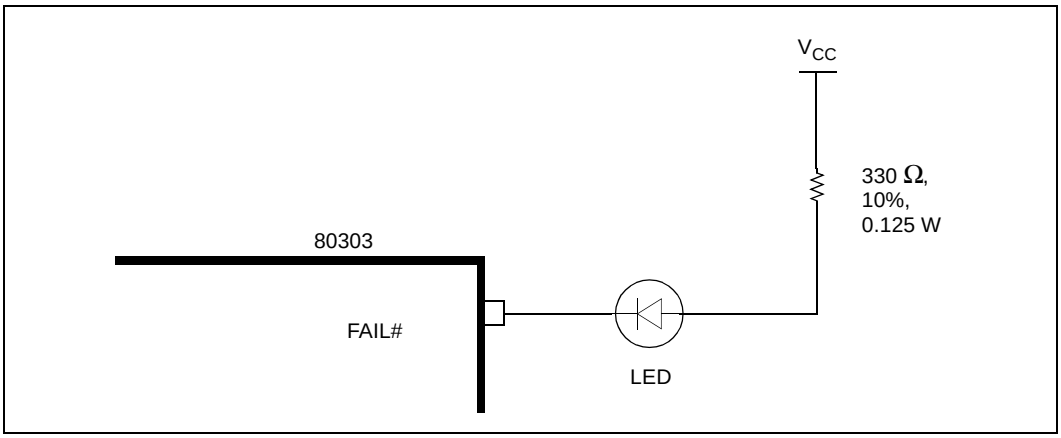
8.3 Pull-ups and Pull-down Resistors

80303 I/O processor inputs which require a pull-up should have the pull-up resistor tied to the appropriate supply voltage. In a 3.3V only design, the resistor should be tied to the 3.3V supply. In a design where the 80303 I/O processor interface to components operating at 5V, the resistors can be tied to either the 3.3V power island or the 5V supply.

8.4 FAIL# Pin Implementation

Many applications use a light emitting diode (LED) to indicate when the FAIL# pin is low (active). Intel recommends the circuit shown in Figure 26. Power the LED from the 3.3V supply of the 80303 I/O processor.

Figure 26. Recommended FAIL# Circuit



9.0 Processor Power Supply Decoupling

Processor power supply decoupling is critical for reliable operation. With the 3.3 V ready system, two areas of concern are described in Section 9.1:

- High frequency decoupling, necessitated by the processor's high speed operation
- Low frequency decoupling, necessitated by the processor's power saving features

9.1 High Frequency Decoupling

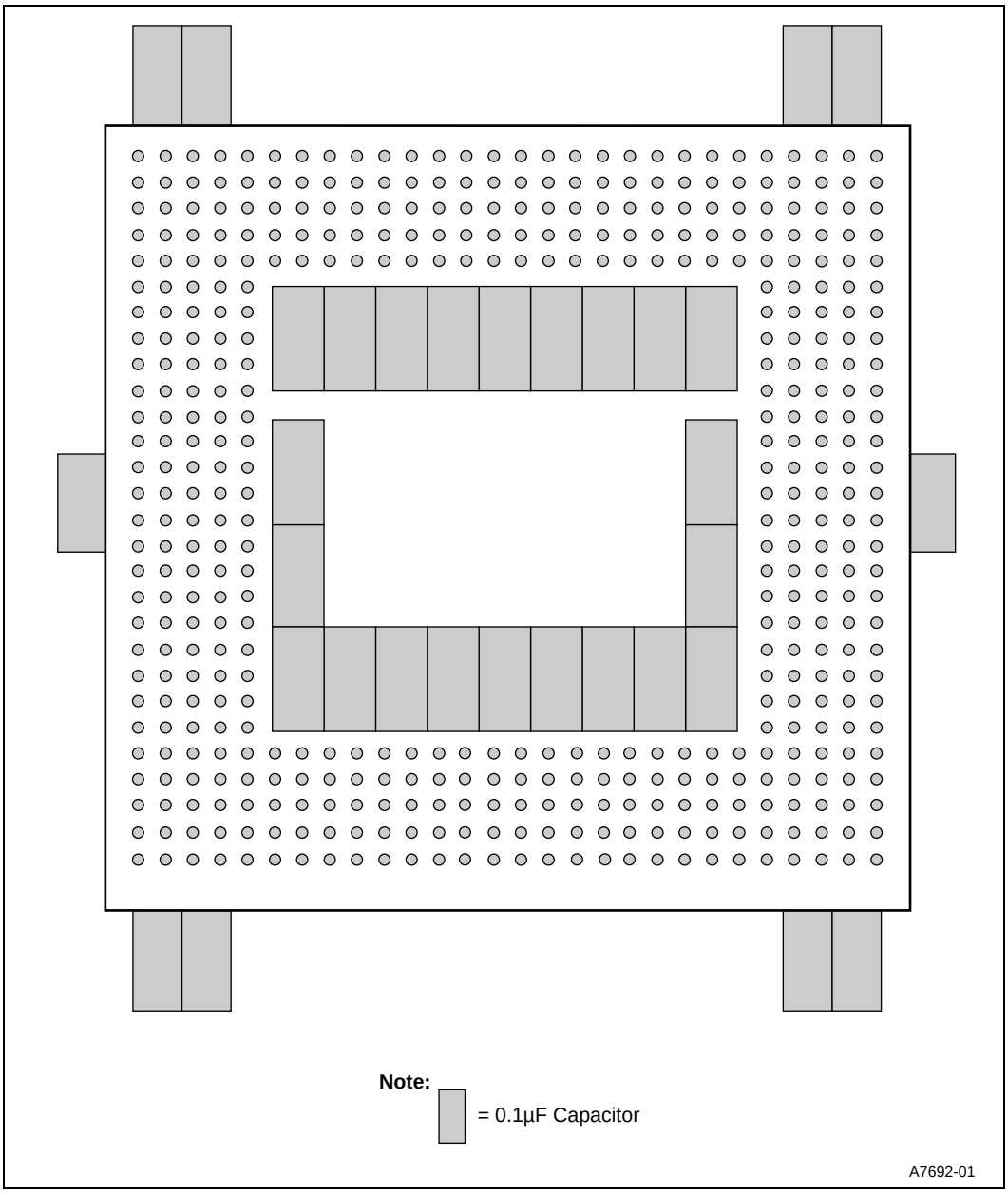
Decoupling capacitors reduce voltage spikes by supplying the extra current needed during switching. Decoupling is especially critical on the 80303 I/O processor because of its 100 MHz internal operation.

A reliable design will include a minimum of thirty-two 0.1 µF surface mount ceramic chip capacitors between power and ground, evenly distributed, around the processor. The capacitors must be placed as close to the processor as possible, attached directly to the power and ground planes, otherwise circuit board inductance will significantly reduce their effectiveness.

Figure 27 is an example of how to place high frequency capacitors on the back (solder) side of the motherboard or add-in card. The BGA package in Figure 27 is shown for reference only; normally it is not be visible from the back side. When the design does not permit components on the back side of the PCB, place the decoupling capacitors around the perimeter on the component side of the PCB.

Inadequate high frequency decoupling results in unreliable or inconsistent program behavior. These failures are often intermittent, and are difficult to diagnose and debug.

Figure 27. High-Frequency Capacitor Values and Layout



10.0 Intel® 80303 I/O Processor Based Reference Design

See Appendix A for schematics and Appendix B for bill of material. Schematic files for the evaluation board are available and can be supplied upon request.

11.0 Debug Connector Recommendations

This section describes debug hardware and connectors developed for the 80303 I/O processor. This includes sockets, headers, logic analyzer interposer, Mictor* signal cross reference lists and JTAG emulator debug connector/pin assignments.

11.1 PBGA Sockets and Headers

Figure 28 and Figure 29 illustrate surface mount sockets and headers available for the 80303 I/O processor. See Table 16 for socket and header vendor information.

Figure 28. 540L PBGA Header

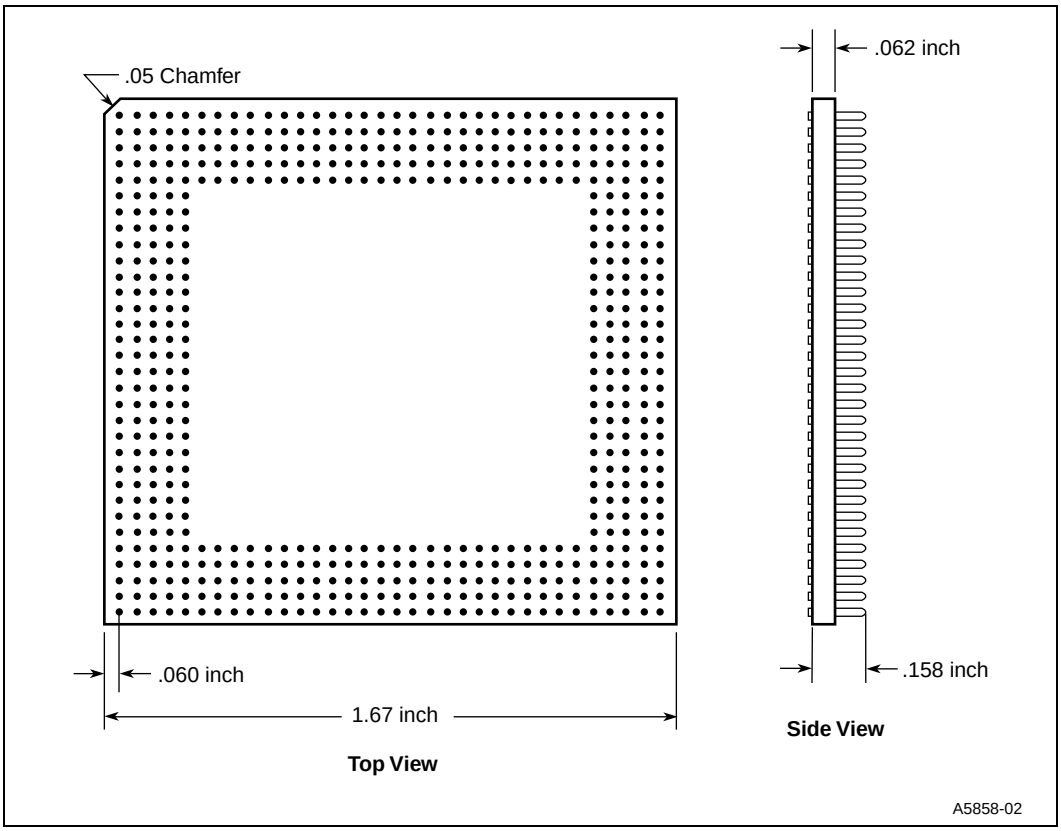
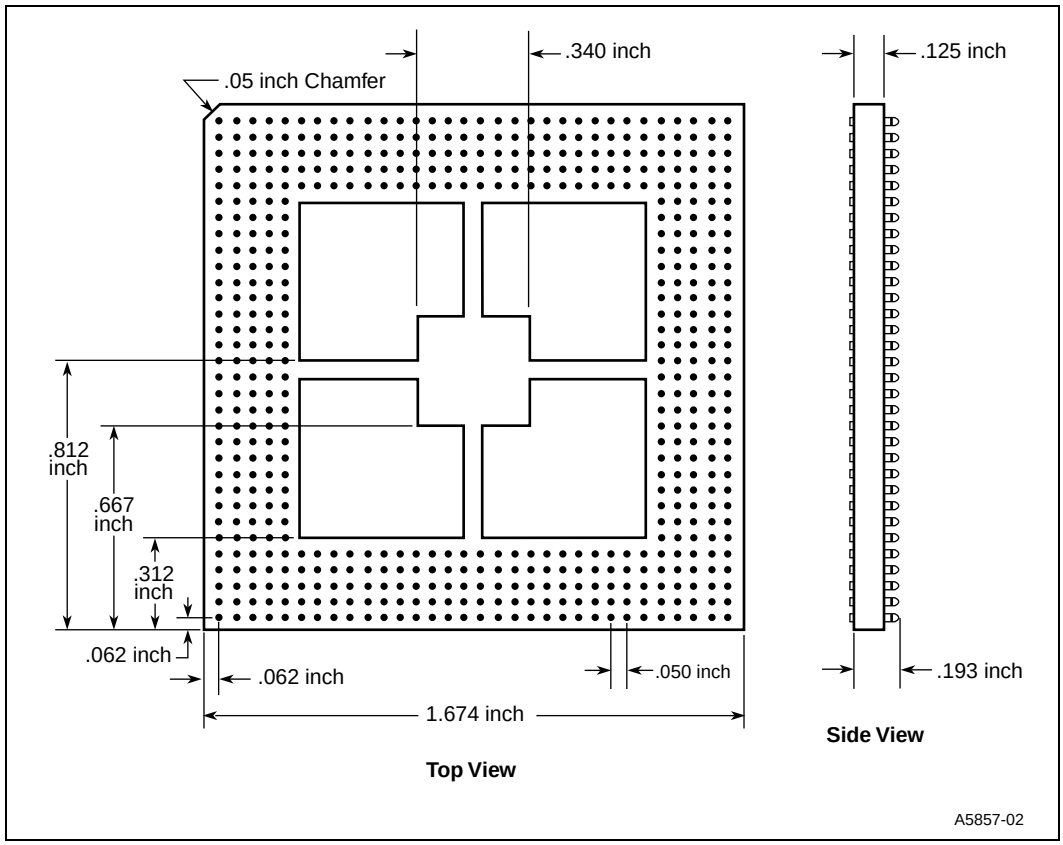


Figure 29. 540L PBGA Socket



11.2 Logic Analyzer Connectivity

The Mictor connector is the common connector used by the 80303 I/O processor for logic analysis connectivity. The Cyclone evaluation board developed for the Intel® 80960RM/RN I/O processor, integrates five Mictor connectors to route appropriate signals for logic analysis and probing (Table 10).

A removable interposer is also available for designs that may not have the available board space for Mictor connectors. See Figure 30, Figure 31 and Figure 32. Refer to Table 19 for logic analyzer interposer vendor information.

Table 10 is the signal cross-reference list for the 80303 I/O processor and associated Mictor connectors for the Cyclone board and flex tape interposer. Pins1,2,37 and 38 are not used.

Table 10. Logic Analyzer Header Definitions (Mictor)

PIN	Cyclone J12	Cyclone J11	Cyclone J10	Cyclone J9	Cyclone J13
3	N/C	N/C	N/C	N/C	N/C
4	DQ15	SDQM7	DQ31	SHOLD#	RAD15
5	DQ14	SDQM6	DQ30	SHOLDA#	RAD14
6	DQ13	SDQM5	DQ29	N/C	RAD13
7	DQ12	SDQM4	DQ28	N/C	RAD12
8	DQ11	SDQM3	DQ27	N/C	RAD11
9	DQ10	SDQM2	DQ26	N/C	RAD10
10	DQ9	SDQM1	DQ25	N/C	RAD9
11	DQ8	SDQM0	DQ24	N/C	RAD8
12	DQ7	SCB7	DQ23	N/C	RAD7
13	DQ6	SCB6	DQ22	N/C	RAD6
14	DQ5	SCB5	DQ21	N/C	RAD5
15	DQ4	SCB4	DQ20	N/C	RAD4
16	DQ3	SCB3	DQ19	SCE0#	RAD3
17	DQ2	SCB2	DQ18	SCE1#	RAD2
18	DQ1	SCB1	DQ17	SBA1	RAD1
19	DQ0	SCB0	DQ16	SBA0	RAD0
20	DQ32	SA0	DQ48	SREQ0#	RAD16
21	DQ33	SA1	DQ49	SREQ1#	N/C
22	DQ34	SA2	DQ50	SREQ2#	N/C
23	DQ35	SA3	DQ51	SREQ3#	RALE
24	DQ36	SA4	DQ52	SREQ4#	RCE0#
25	DQ37	SA5	DQ53	SREQ5#	RCE1#
26	DQ38	SA6	DQ54	SGNT0#	ROE#
27	DQ39	SA7	DQ55	SGNT1#	RWE#
28	DQ40	SA8	DQ56	SGNT2#	N/C
29	DQ41	SA9	DQ57	SGNT3#	I_RST#
30	DQ42	SA10	DQ58	SGNT4#	N/C
31	DQ43	SA11	DQ59	SGNT5#	N/C
32	DQ44	SA12	DQ60	N/C	N/C
33	DQ45	SRAS#	DQ61	N/C	N/C
34	DQ46	SCAS#	DQ62	N/C	N/C
35	DQ47	SWE#	DQ63	N/C	N/C
36	N/C	N/C	DCLK2	LOGIC_CLK	RALE

11.3 JTAG Connector and Test Interface

11.3.1 Intel® 80303 I/O Processor JTAG Emulator

The JTAG emulator for the 80303 I/O Processor is designed to provide a convenient and non-intrusive means of debugging. The JTAG emulator is connected to the processor by means of a simple 16-pin connector. The hardware provided with the JTAG emulator can also be used (with additional software) to test opens and shorts on the processor without the necessity for any additional circuitry, other than a single 16-pin connector once it has been installed onto the PCB. A JTAG emulator provides a designer the ability to download code, read data from registers, single-step the processor, insert breakpoints (both hardware and software) and perform full source level debugging without the need of an intrusive monitor program or a bulky hardware pod.

11.3.2 Intel® 80303 I/O Processor Target Debug Interface Connector

The i960 microprocessor target should have a 16-pin, two row header connector. Use AMP part number 103308-3 or equivalent. The header is made from a keyed plastic shroud with two rows of eight pins and the spacing between adjacent pins and between the two rows is 0.100”. The header pin assignment is illustrated in Figure 30.

Figure 30. JTAG Emulator Connector (Top View)

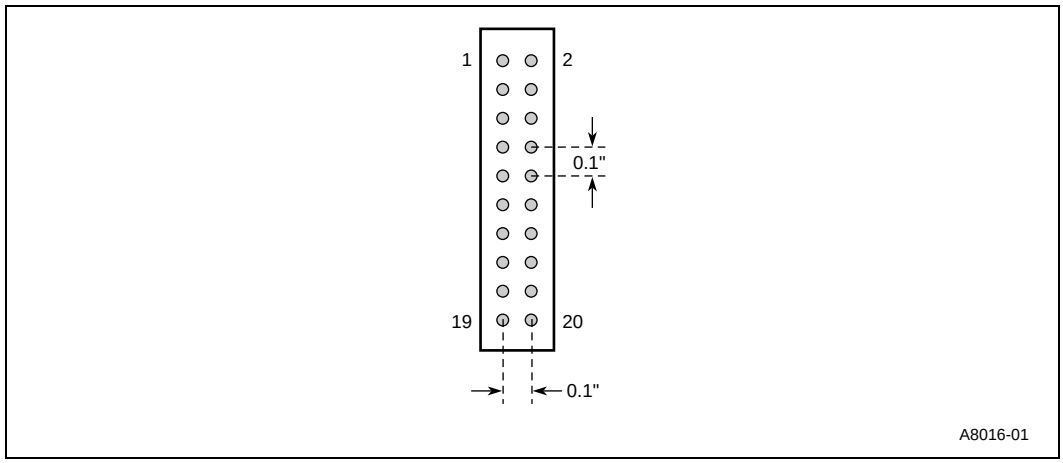


Table 11 describes the interconnections required between the target debug interface connector and the pins/balls of the 80303 I/O Processor family.

Table 11. Intel® 80303 I/O Processor Debug Connector Wiring

Header Pin	Intel® 80303 I/O Processor Ball/Direction	Signal Name	Recommended Target Resistor
1	AH30	TRST#	1.5 KΩ pull-down
2		SDA	2.7 KΩ pull-up
3	AJ32	TDI	
4		SCL	2.7 KΩ pull-up
5	AH32	TDO	
6		GND	
7	AH31	TMS	
8		GND	
9	AK32	TCK	
10		GND	
11	P32	LCDINIT#	2.7 KΩ pull-up
12		GND	
13	T28	I_RST#	
14		GND	
15		PWRVLD	Connected to V_{CC} through 2.7 KΩ series resistor
16		GND	

11.3.3 Connecting The Emulator To The Target

The emulation software uses the first Test Access Port (TAP) on the PC-1149.1/100F boundary-scan controller card to control the 80303 I/O Processor. A cable should be connected from the boundary-scan controller to the 80303 I/O Processor target debug interface connector as shown in the following tables. A cable built to one of the following specifications is supplied with the corresponding emulator.

Table 12. Intel® 80303 I/O Processor with PC-1149.1/100F (cable P/N AS01090025-Ax)

PC-1149.1/100F Signal Name	PC-1149.1/100F Pin	Target Signal Name	Target Debug Header Pin
TRST#	1	TRST#	1
GND	2	GND	2
TDO12	3	TDI	3
GND	4	GND	4
TDI12	5	TDO	5
GND	6	GND	6
TMS1	7	TMS	7
GND	8	GND	8
TCK12 (see note)	9	TCK	9
GND	10	GND	10
TMS3	25	LCDINIT#/ RSTIN#	11
GND	12	GND	12
SENSE#	13	I_RST/ RSTOUT#	13
GND	14	GND	14
T_OFF# (see note)	11	PWRVLD	15
GND	16	GND	16

NOTE: Connected to target through 33Ω series resistor.

Table 13. Intel® 80303 I/O Processor with PCMCIA-1149.1 (cable P/N AS01090025-Bx)

PCMCIA-1149.1 Signal Name	PCMCIA-1149.1 Pin	Target Signal Name	Target Debug Header Pin
TRST#	8	TRST#	1
GND	9	GND	2
TDO1	7	TDI	3
GND	5	GND	4
TDI1	6	TDO	5
GND	3	GND	6
TMS1	4	TMS	7
GND	1	GND	8
TCK1 (see note)	2	TCK	9
GND	11	GND	10
PIO_0	17	LCDINIT#/ RSTIN#	11
GND	13	GND	12
PIO_1	18	I_RST/ RSTOUT#	13
GND	25	GND	14
PIO_2 (see note)	19	PWRVLD	15
-	No Connection	GND	16

NOTE: Connected to target through 33Ω series resistor.

11.3.4 Other Tools

Other tools are available that are designed to complement the i960 family of JTAG emulators. These include a full complement of boundary-scan hardware and software for testing the 80303 I/O Processor for opens, shorts, and other manufacturing defects once it has been installed onto the target board.

12.0 Design for Manufacturability

The 80303 I/O processor is offered in a high-thermal BGA (H-PBGA) package. PBGA packaging is explained extensively in the *Intel® Packaging Databook* (240800).

13.0 Thermal Solutions

In general, three factors affect the thermal performance of the BGA: package and board materials, package geometry and use environment. The H-PBGA package utilizes a heat spreader or slug across the top of the package to dissipate heat efficiently.

Environmental conditions play a critical role in the thermal performance of PBGAs. Ambient conditions, junction and case temperatures, the device's placement and orientation on a board, in conjunction with the volume and temperature of air flowing past the unit present a broad range of possible thermal solutions. The profiles of the H-PBGA package are characterized in Table 14.

Table 14. H-PBGA Package Characteristics

Description	Criteria
Die Junction temperature	110° C
Case Temperature (optimal)	90° C
Ambient temperature	up to 55° C
Airflow (on motherboard) from system fan	up to 50 LFM (worst case)
Airflow (on add-in card)	0 LFM (worst case)
Passive heatsink dimensions Acceptable flange adds 5 mm per side on hole direction of fan	Clip = 45 mm x 45 mm < 11 mm (thickness) Flange type =55 mm x 45 mm <11 mm (thickness) with pins.
Maximum heatsink thickness	<11 mm
Clip Hole Pattern	4 holes (3.175 mm diameter), 48.4632 x 34.798 mm rectangular (see Figure 32 and Figure 33)
Heatsink Flatness	From center of heatsink to 1/2 inch in x and y directions, 2 mils maximum

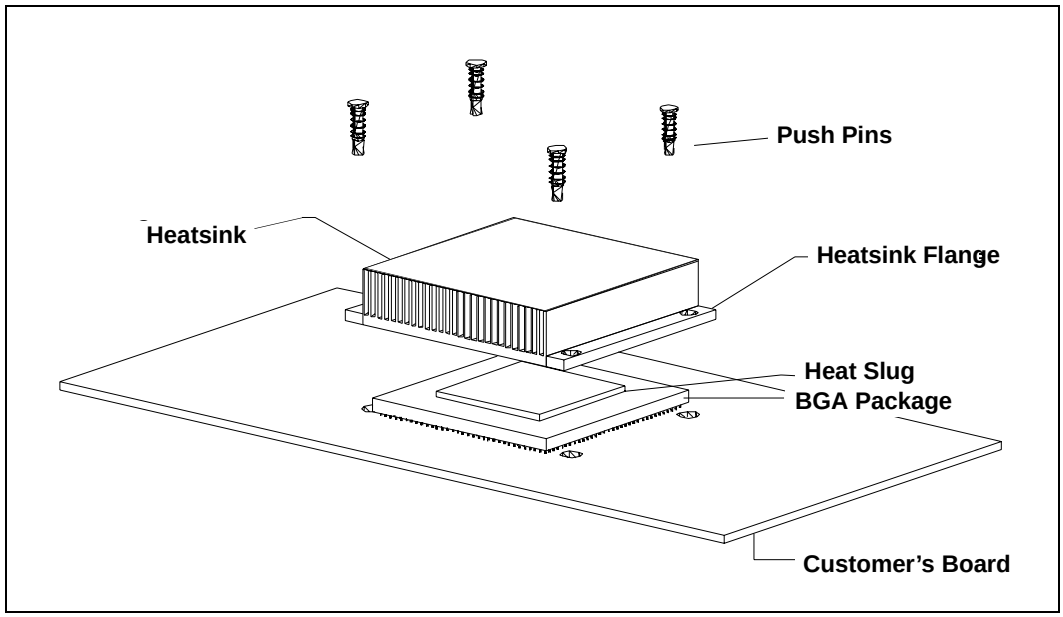
13.1 Thermal Recommendations

Refer to the thermal sections of the *Intel® 80303 I/O Processor Datasheet* (273358) and to the thermal section of the *Thermal Data for the 540-Lead PBGA Package Application Note* (273390).

13.2 3-Dimensional View: Processor With Heat Sink Attached

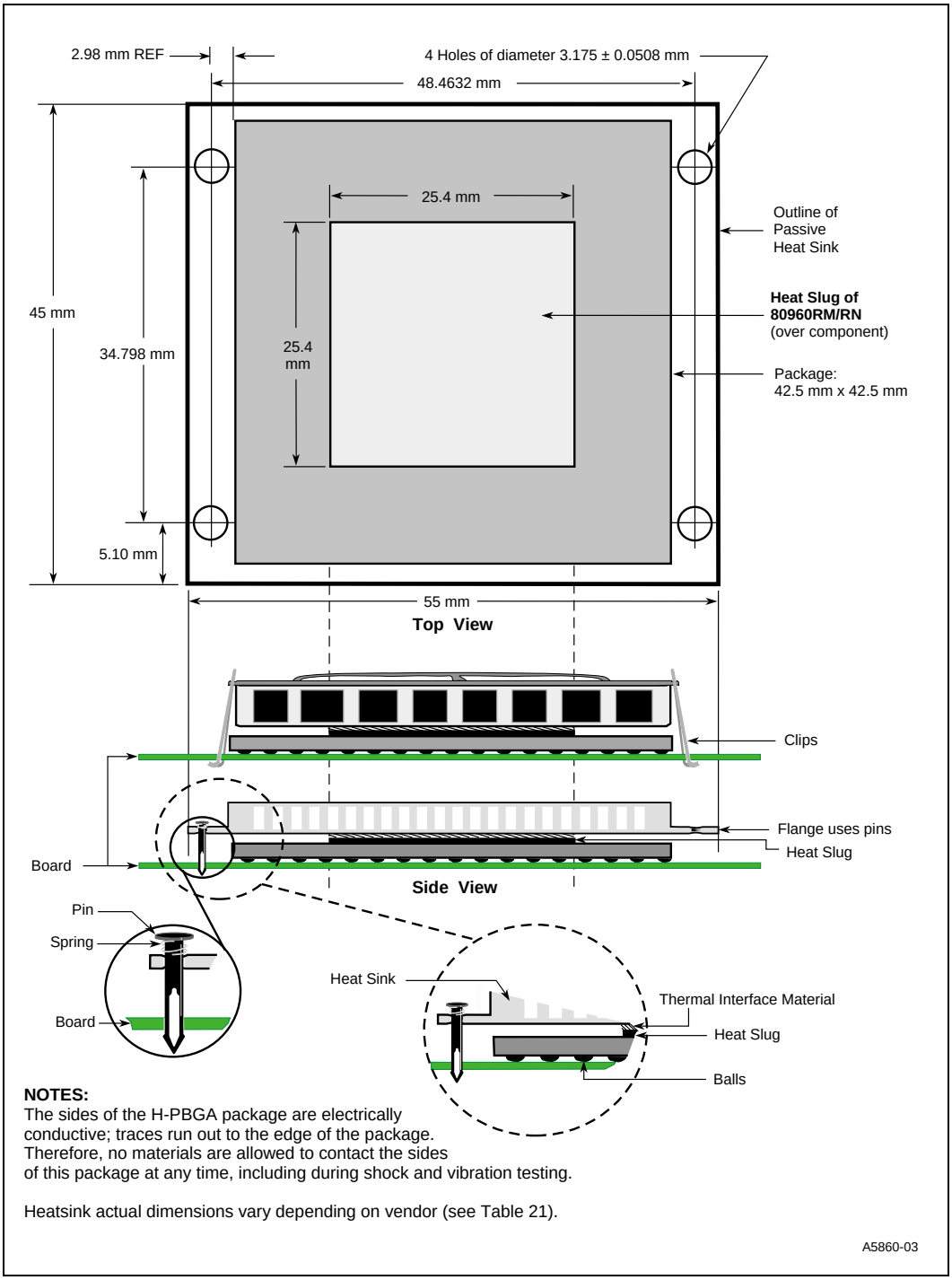
To assist the board designer in component placement, hole placement and dimensions, Figure 32 and Figure 33 detail specifics. Figure 32 details dimensions for board designs requiring a Passive Heat Sink.

Figure 31. Conceptual 3-D View of Processor with a Heat Sink



13.3 PCB Heatsink Hole Dimensions

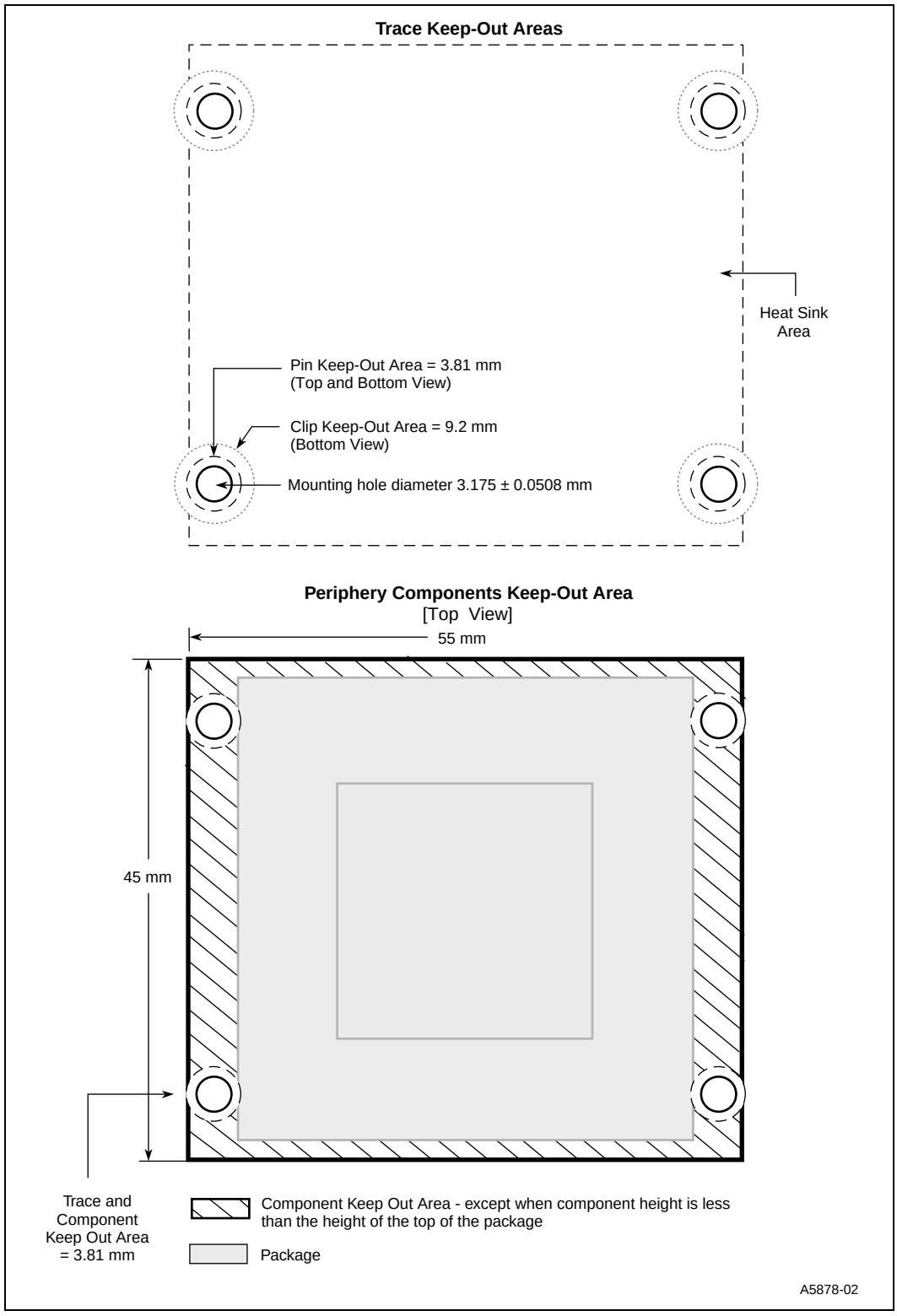
Figure 32. Hole Dimensions for Passive Heatsink



NOTES:
The sides of the H-PBGA package are electrically conductive; traces run out to the edge of the package. Therefore, no materials are allowed to contact the sides of this package at any time, including during shock and vibration testing.

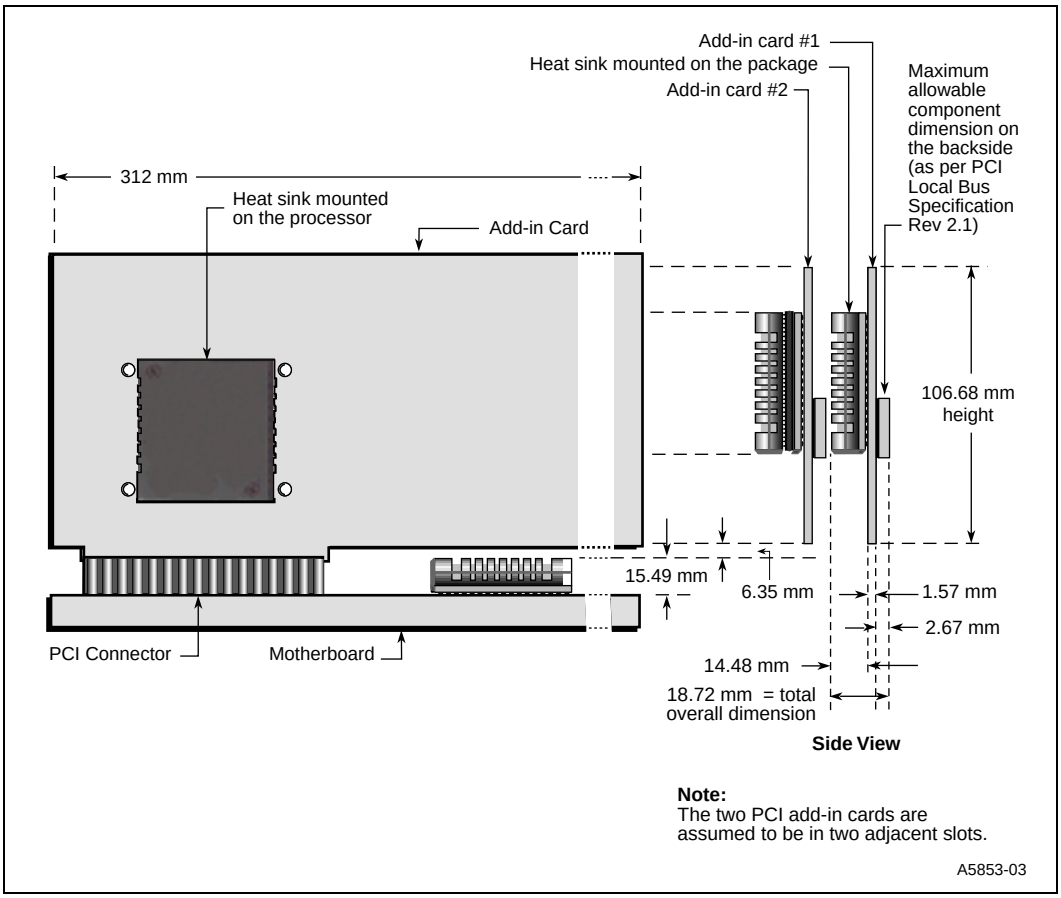
Heatsink actual dimensions vary depending on vendor (see Table 21).

Figure 33. Board Level Keep Out Areas



13.4 Clearances of PCI Board and Components

Figure 34. Clearances of PCI Board and Components



13.5 Heat Sink Information

Table 15 provides a list of suggested sources for heat sinks. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Table 15. Heat Sink Vendors and Contacts

Company	Factory Rep.	Phone #	Fax #	Heatsink Part #
				Passive
THERMALLOY, INC 2021 W. Valley View Lane Dallas Texas 75234-8993 Email:sales@thermalloyusa.com Outside of USA, refer to web page for contact information: http://www.thermalloy.com	Attn: Sales	(972) 243-4321	(972) 241-4656	21933 w/o thermal grease (uses pins) 21935 with Easy Ply (thermal grease (uses pins)

13.5.1 Socket Information

Table 16 and Table 17 provide vendor details for socket-headers and burn-in sockets for the 80303 I/O processor. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

13.5.2 Socket-Header Vendor

Table 16. Socket-Header Vendor

Company	Factory Represen-tative	Phone/Fax #	Part #	
			BGA 540 Pin Header	BGA 540 Pin Socket Carrier
Adapter Technologies, Inc. 214-218 South 4th St. Perkasie, PA 18944 www.adapter-tech.com	Attn: Sales	215-258-5750/ 215-258-5760	BGAH-540-0-01-320 1-0277-1	BGA-540-0-02-3201 -0275P-130

13.5.3 Burn-in Socket Vendor

Table 17. Burn-in Socket Vendor

Company	Factory Representative	Phone #	Burn-in Socket Part #
Texas Instruments 111 Forbes Blvd. Mansfield, MA 02048	Attn: Sales	508-236-5375	ULGA540-005

13.5.4 Shipping Tray Vendor

Table 18. Shipping Tray Vendor

Company	Factory Rep.	Phone #	Shipping Tray Part #
3M	Attention Sales	602-465-5381	7-0000-21001-184-167

13.5.5 JTAG Emulator Vendor

Table 19. JTAG Emulator Vendor

Company	Factory Rep.	Phone/Fax #	Part #
Spectrum Digital	Attention Sales	281-494-4500	SP1610

14.0 References

14.1 Related Documents

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

To obtain Intel literature write to or call:

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808

1-800-548-4725

or visit the Intel website at http://www.intel.com

Table 20. Related Documentation

Document Title	Intel Order #
Intel Packaging Databook	240800
PCI Local Bus Specification Revision 2.2	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
72-bit ECC Unbuffered SDRAM DIMM Specification	http://developer.intel.com/technology/memory/pcsdram/spec
PCI-to-PCI Bridge Architecture Specification Revision 1.1	PCI Special Interest Group 1-800-433-5177 www.pcisig.com

14.2 Electronic Information

Table 21. Electronic Information

Intel's World-Wide Web (WWW) Location:	http://www.intel.com
Customer Support (US and Canada):	800-628-8686

IQ80303 Schematics A

Figure 35 through Figure 47 contain the IQ80303 schematics.

Figure 35. Decoupling Schematic

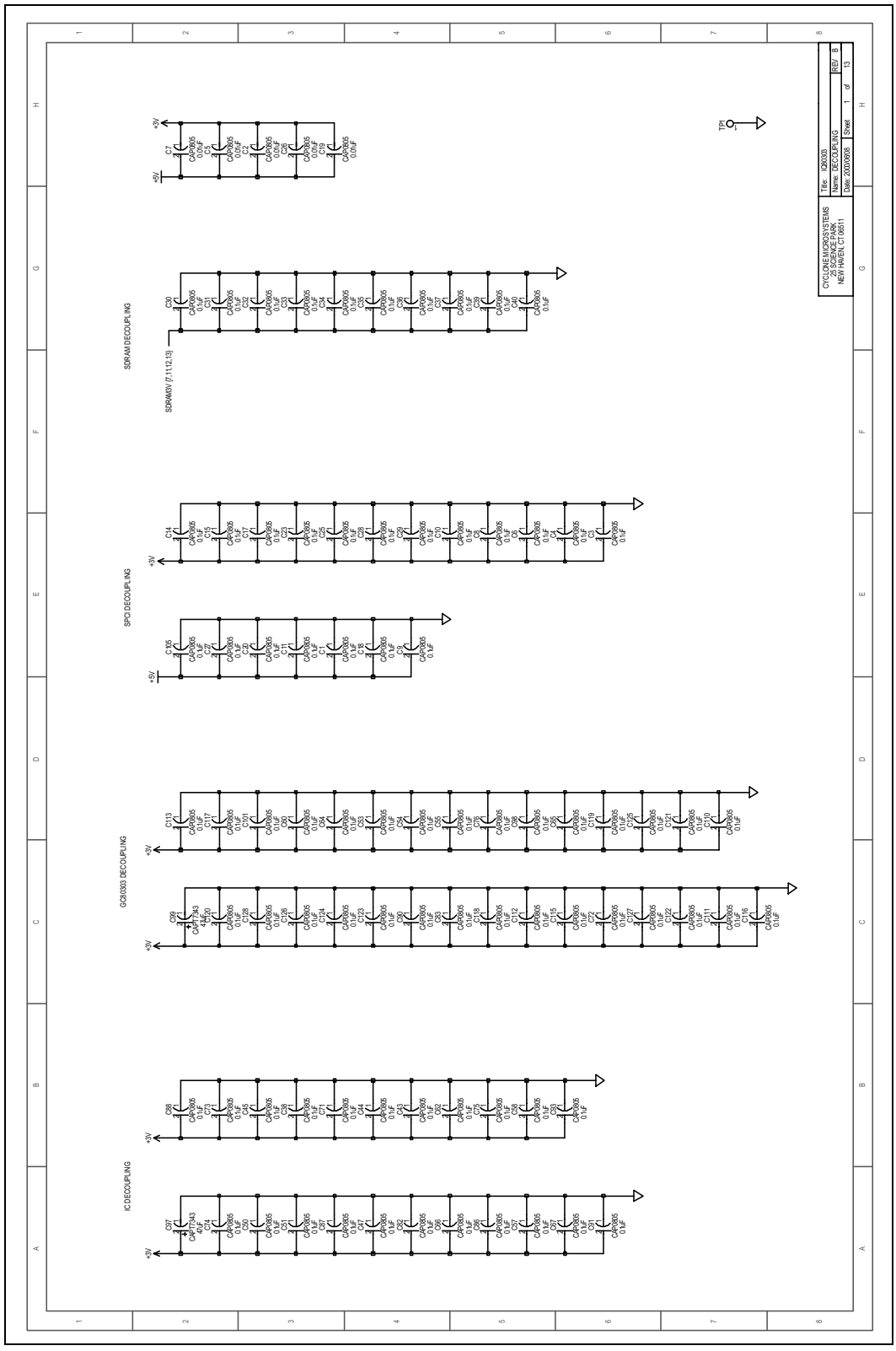


Figure 36. Primary PCI Interfacel Schematic

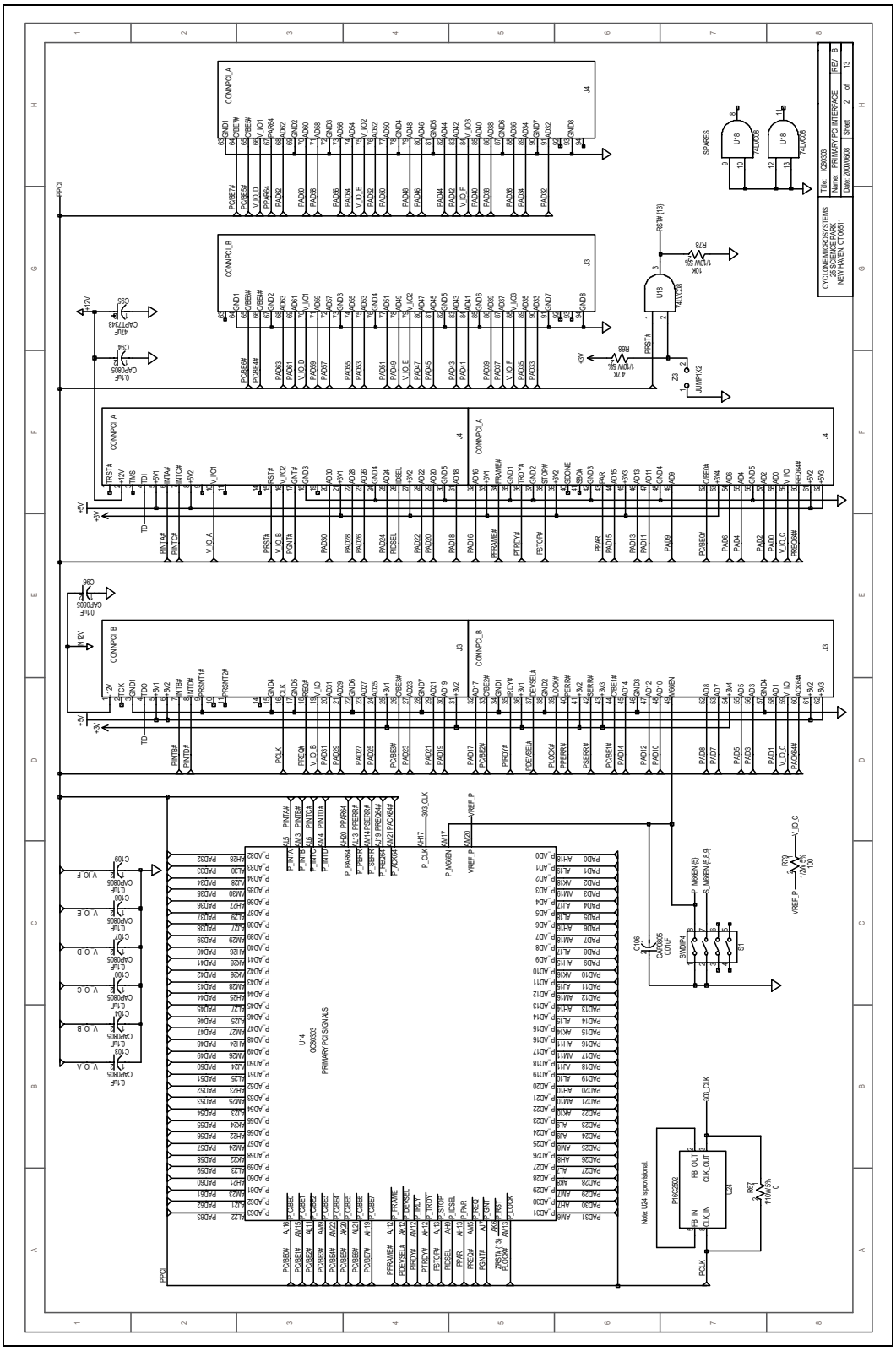


Figure 37. Memory Controllerl Schematic

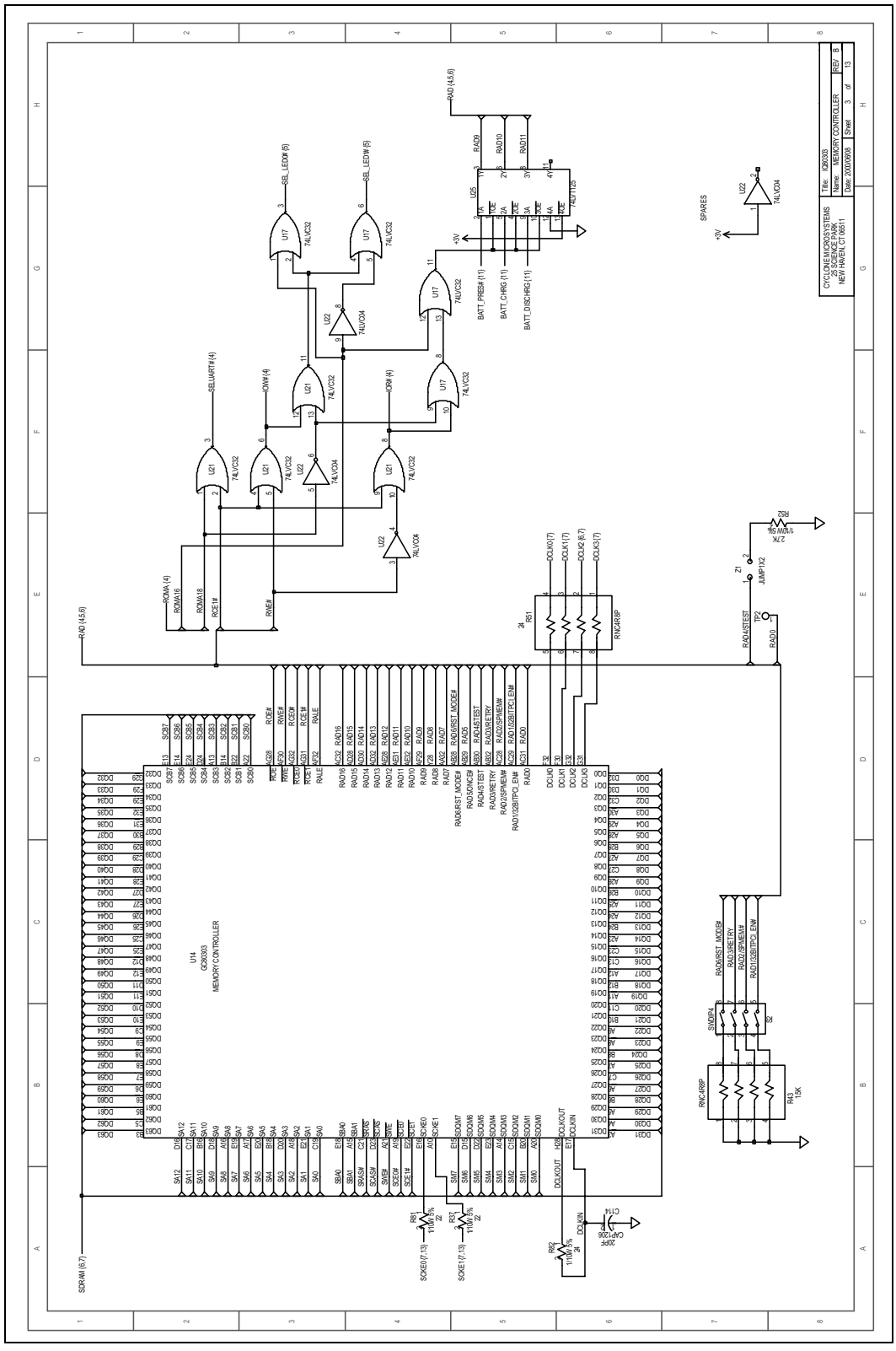


Figure 38. Flash ROM and UARTl Schematic

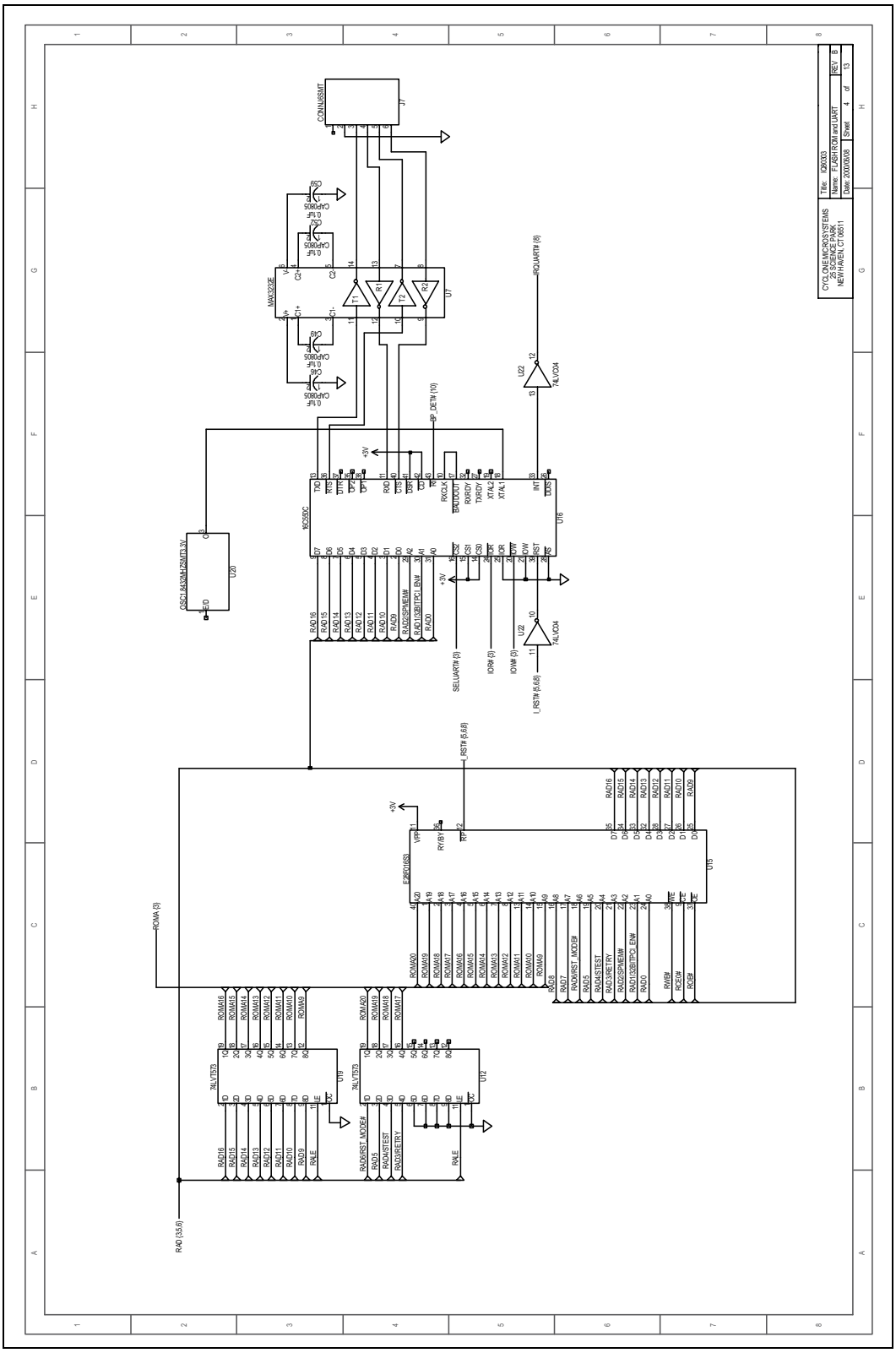


Figure 39. LEDs Schematic

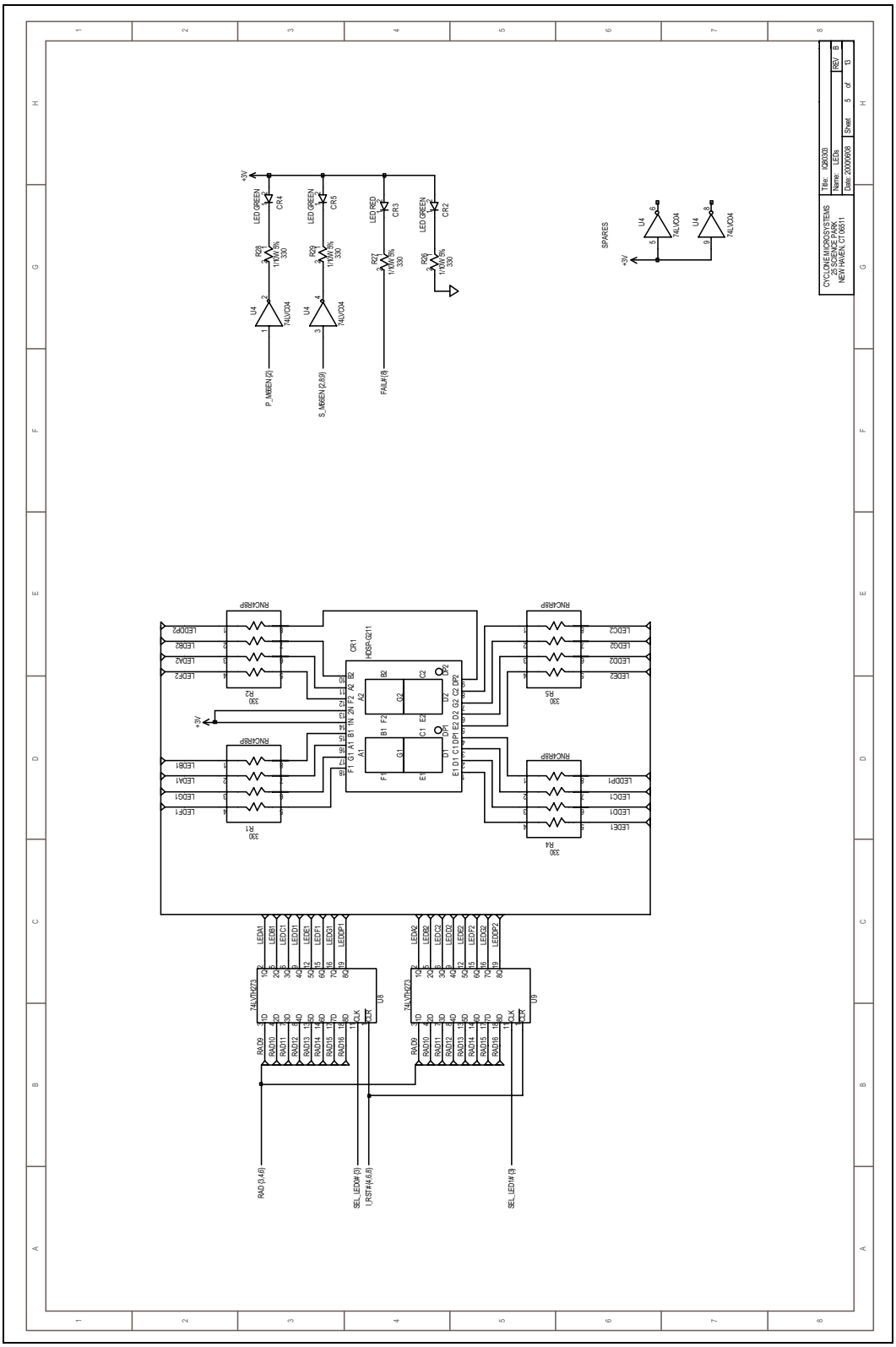


Figure 40. Logic Analyzer I/Fl Schematic

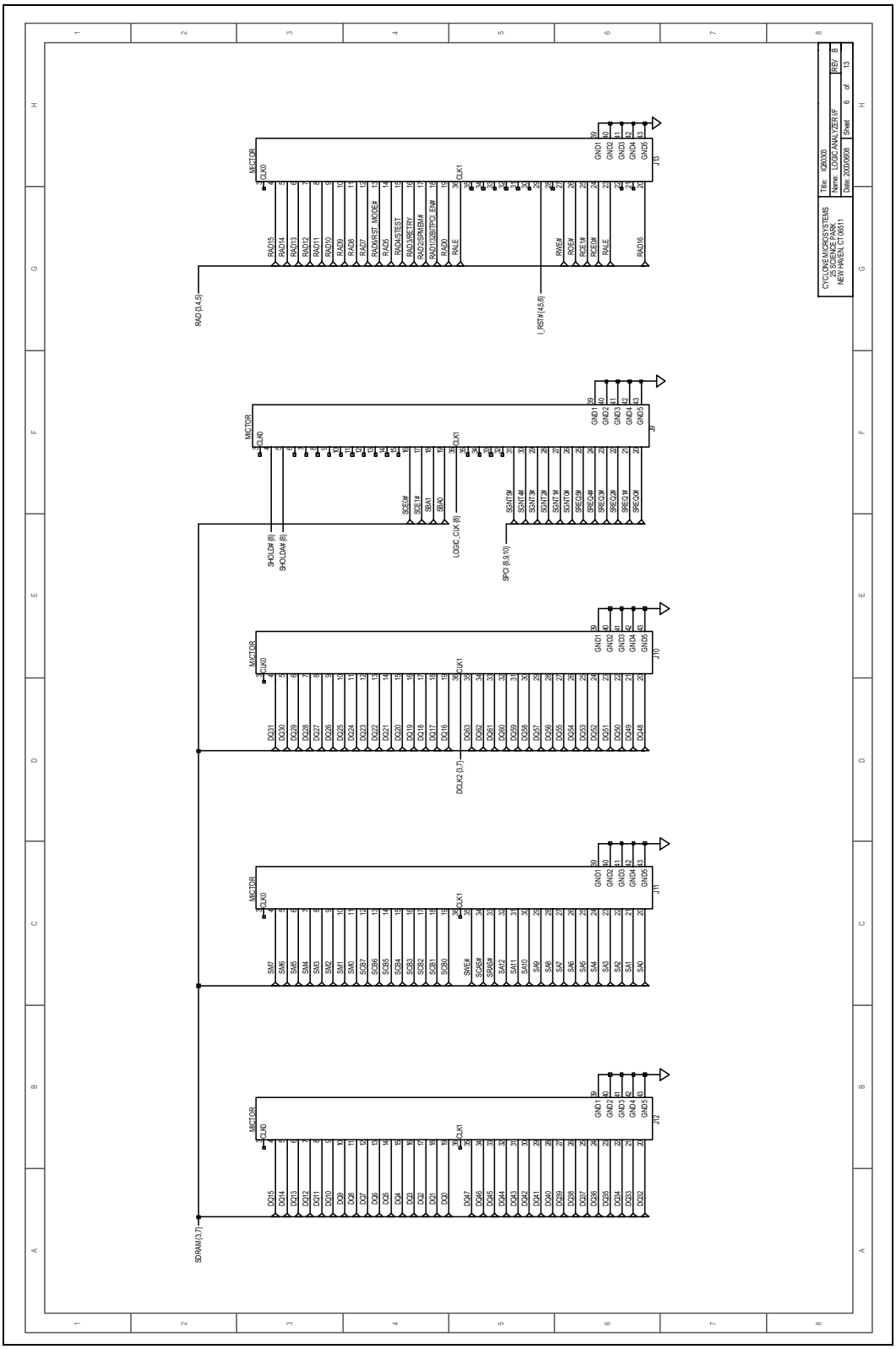


Figure 41. SDRAM 168-Pin DIMMl Schematic

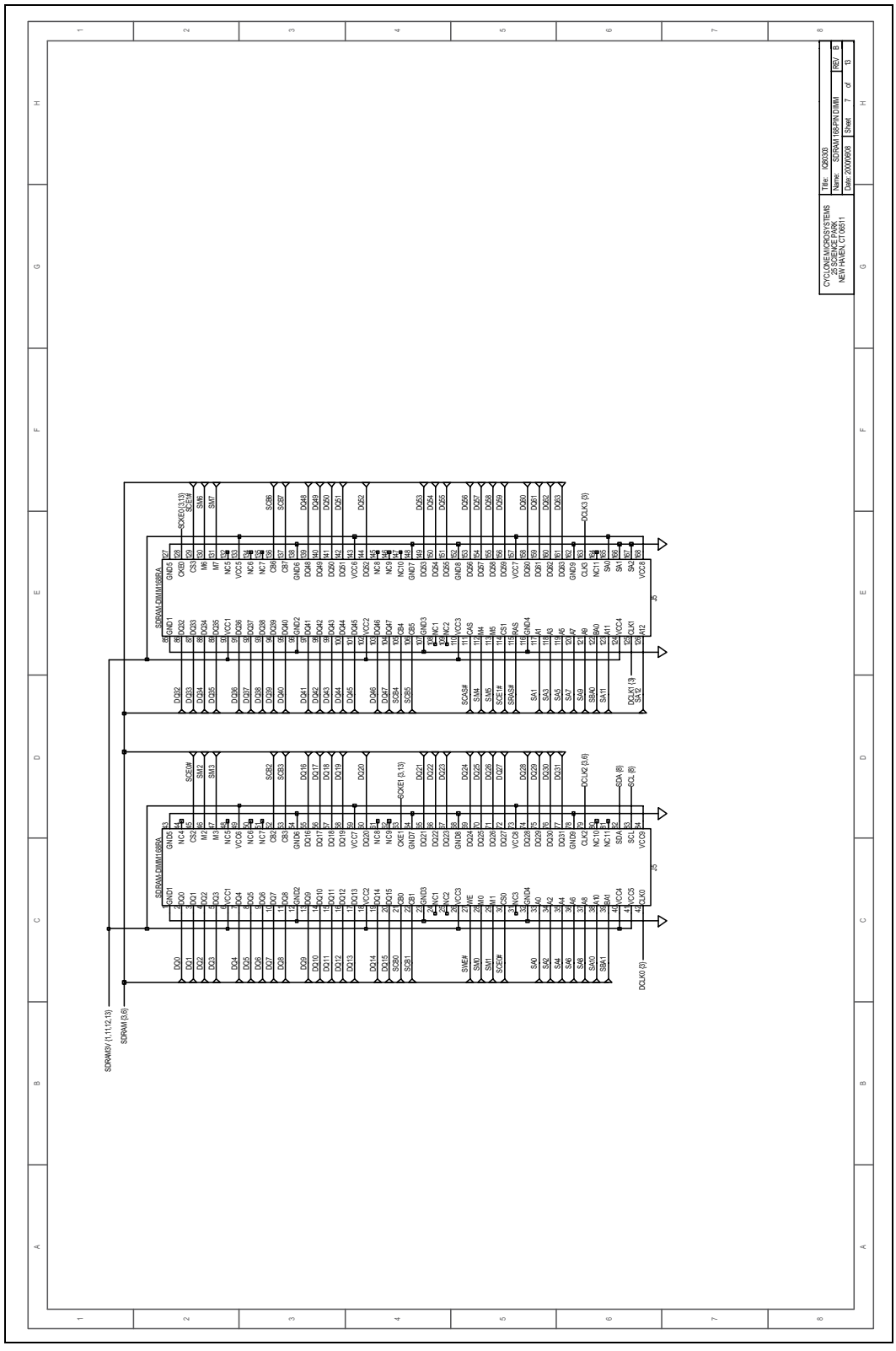


Figure 42. Secondary PCI/80960 Corel Schematic

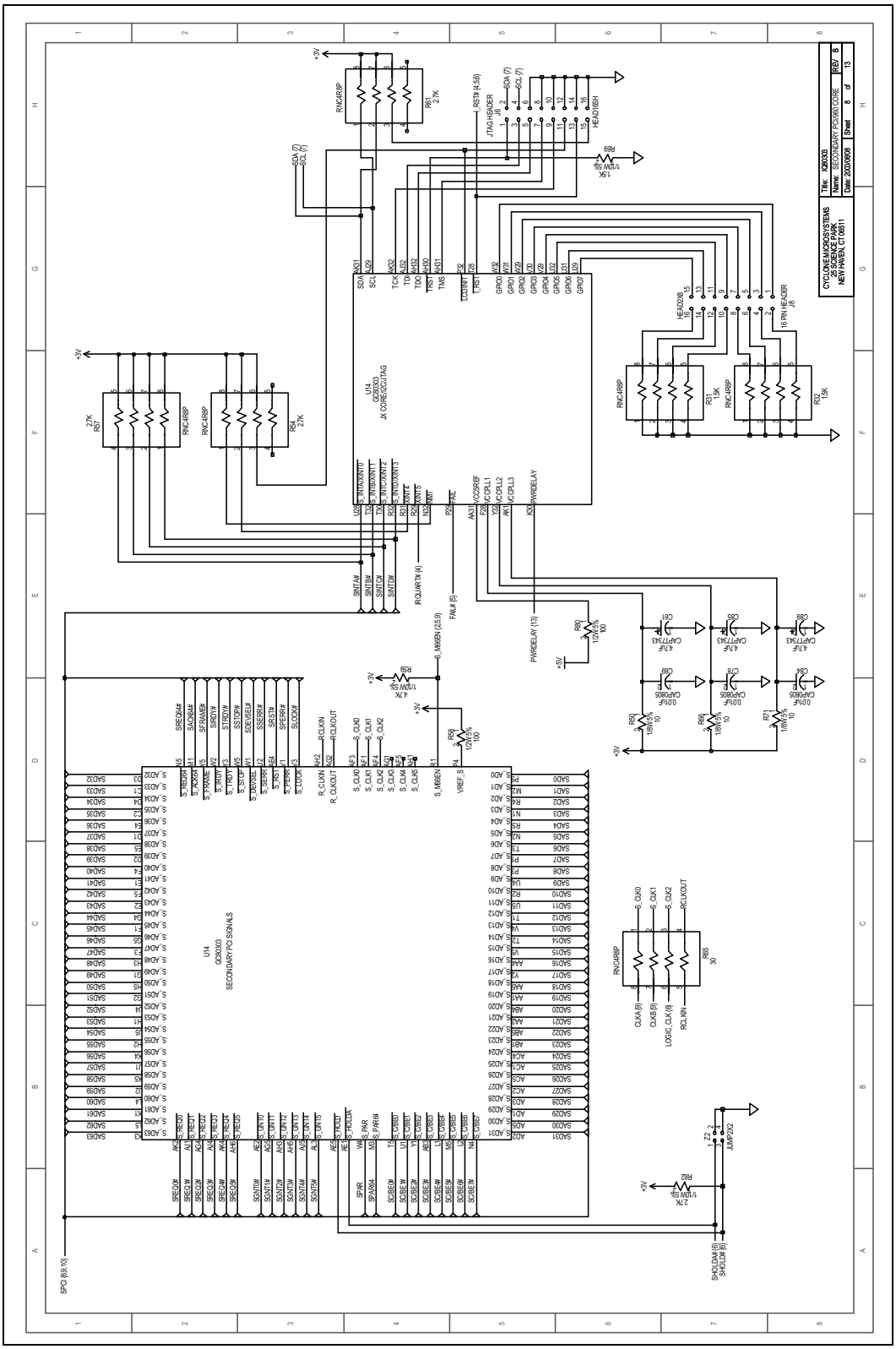


Figure 43. Secondary PCI Bus 1/2l Schematic

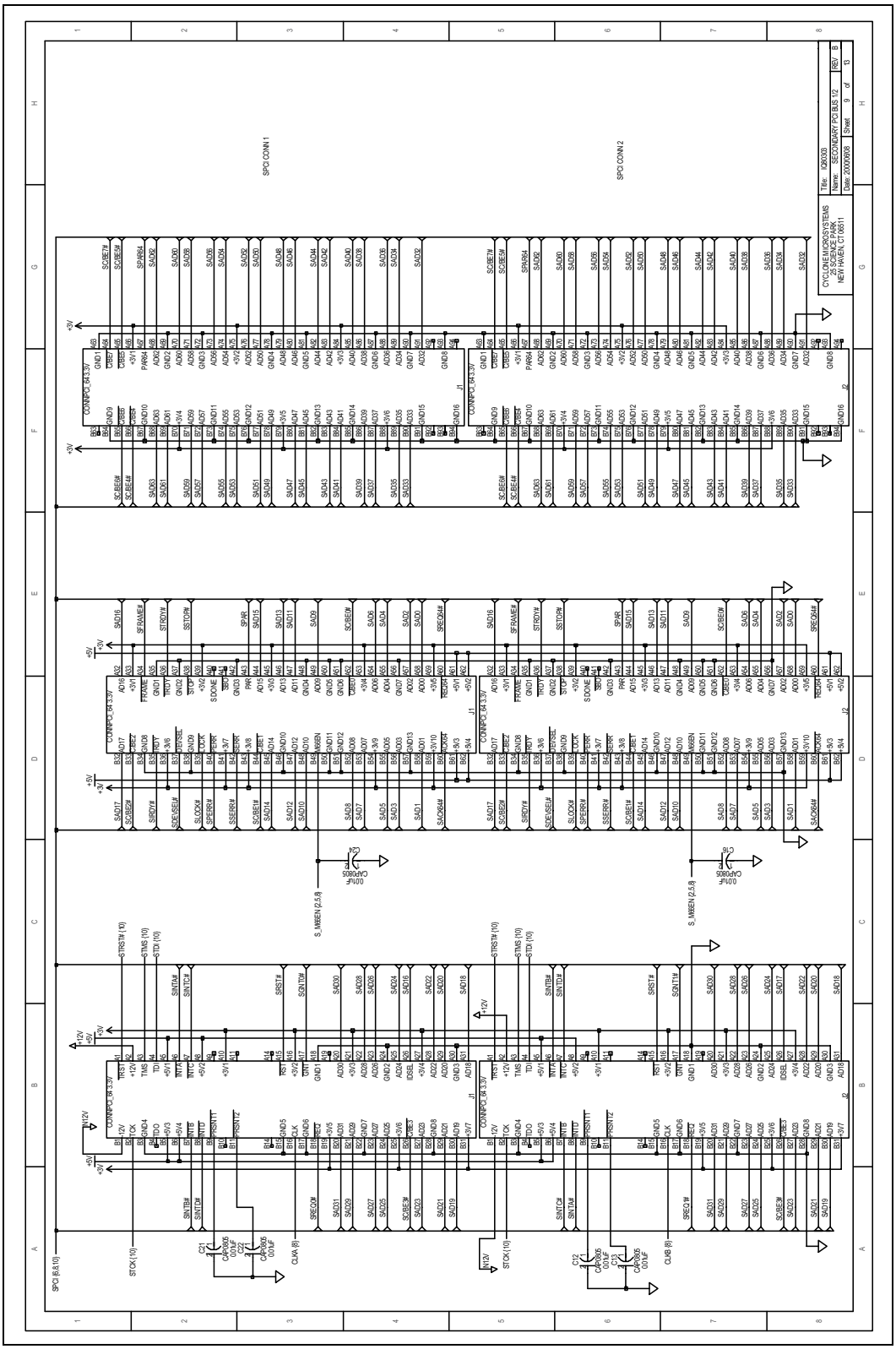


Figure 44. SPCI Pull-Upsl Schematic

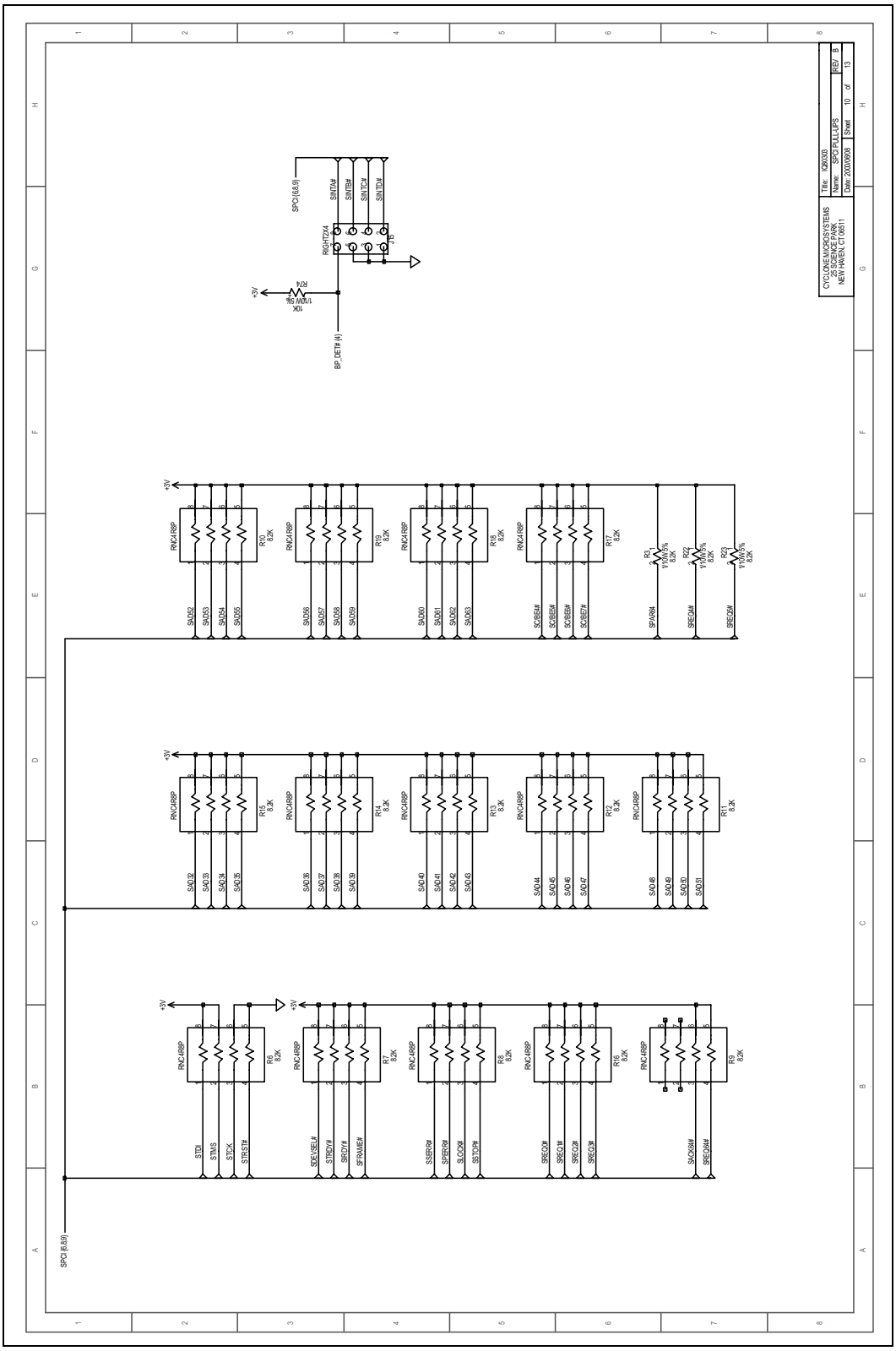


Figure 45. Barrtery/Monitorl Schematic

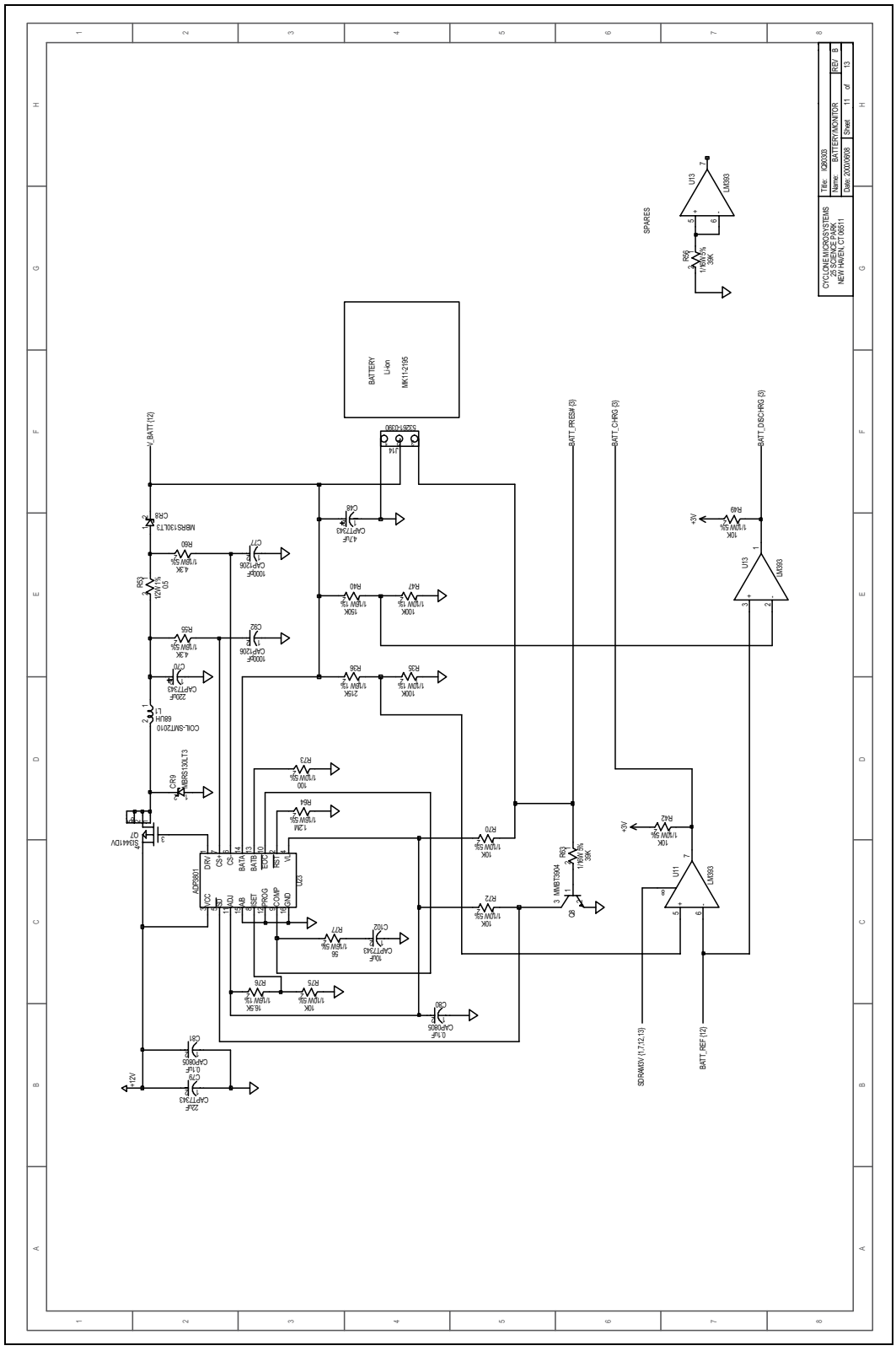


Figure 46. SDRAM +3.3 V Referencel Schematic

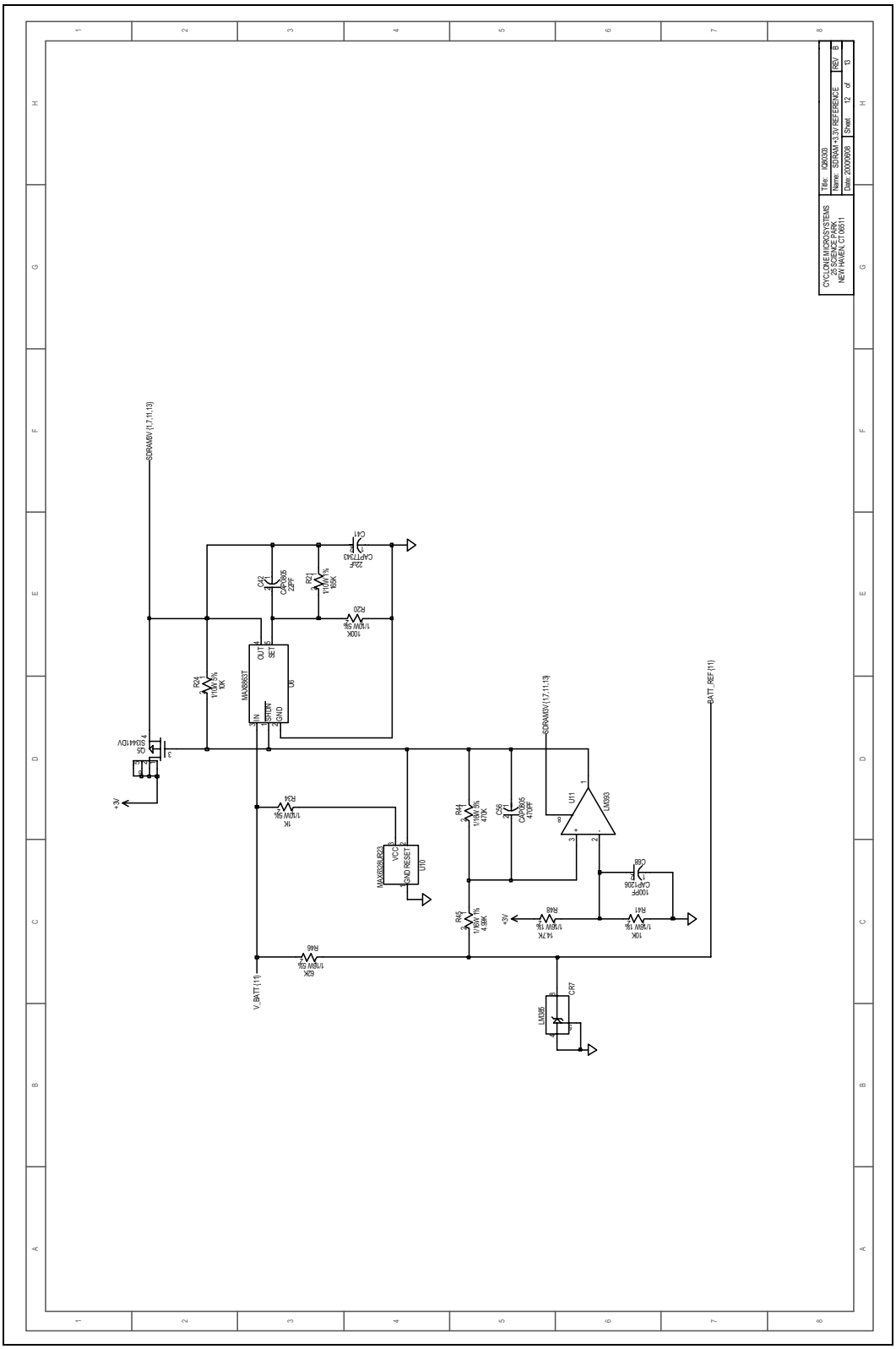
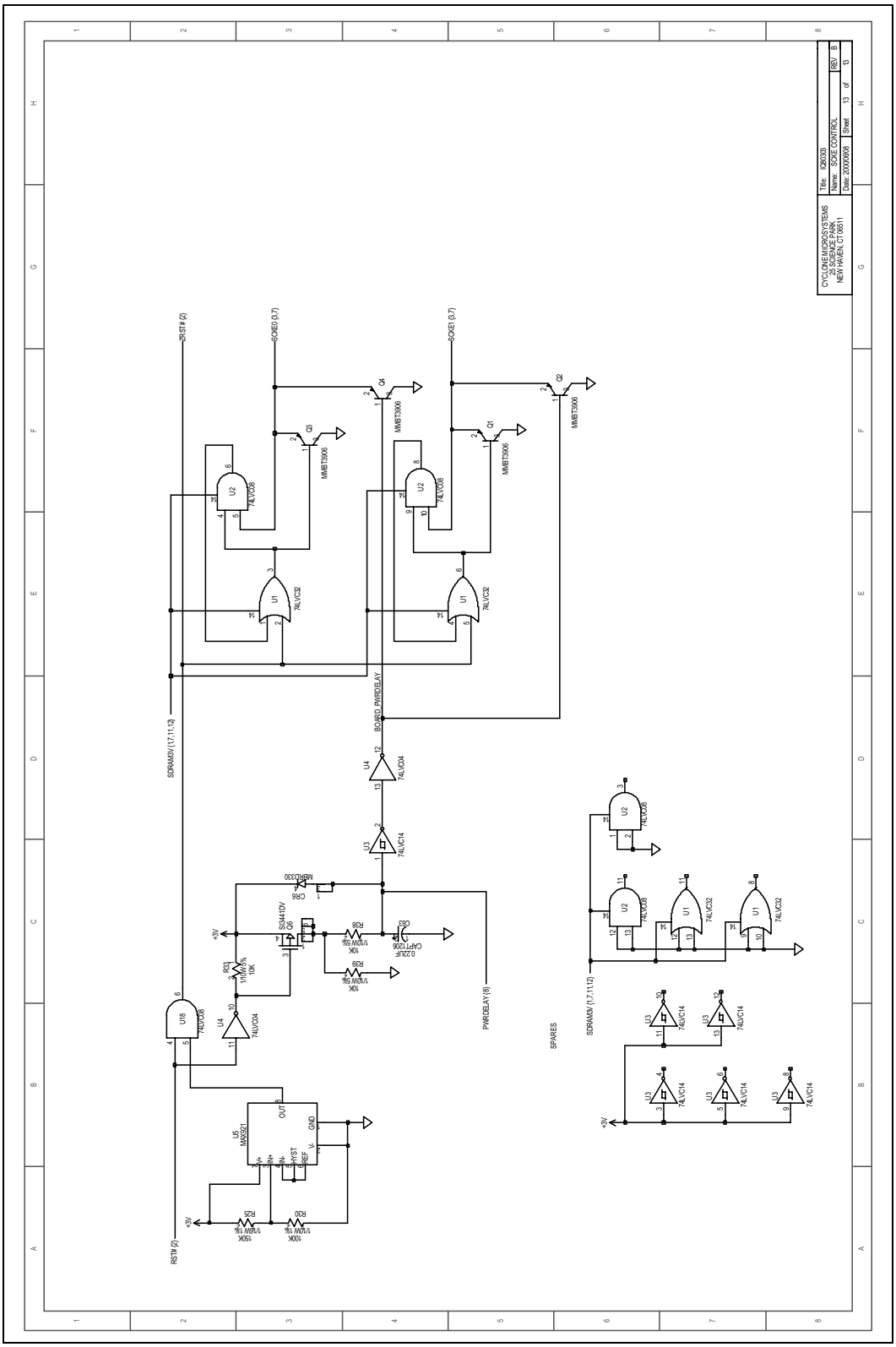


Figure 47. SCKE Control Schematic



IQ80303 Board Bill of Material B

This appendix identifies all components on the IQ80303 Evaluation Platform (Table 22).

Table 22. IQ80303 Bill of Materials (Sheet 1 of 3)

Location	Part Description	Qty	Manufacturer	Part Number
U4, U22	IC/SM 74LVC04D SOIC14 (3.3V)	2	Texas Instruments	SN74LVC04D
			Fairchild Semi.	74LVX04M
U2, U18	IC/SM 74LVC08 3.3V TSSOP-14	2	Texas Instruments	SN74LVC08APW
U3	IC/SM 74LVC14 3.3V TSSOP-14	1	Texas Instruments	SN74LVC14APW
			Philips	74LVC14APWDH
			Fairchild Semi.	74LCX14MTC
U25	IC/SM 74LVT125 (3.3V) SOIC-14	1	Texas Instruments	SN74LVT125D
			Philips	74LVT125D
U8, U9	IC/SM 74LVTH273 TSSOP-20 (3.3V)	2	Texas Instruments	SN74LVTH273PW
			Fairchild Semi.	74LVTH273MTC
U12, U19	IC/SM 74LVC573 SOIC20 No Bus H	2	Texas Instruments	SN74LVC573ADW
			Philips Semi	74LVC573AD
			Fairchild Semi	74LCX573WM
U1, U17, U21	IC/SM 74C32 TSSOP-14	3	Texas Instruments	SN74LVC32APW
			Fairchild	74LCX32MTC
Q5-Q7	IC/SM Si3441DV TSOP-6	3	Siliconix	Si3441DV
			Motorola	MGSF3441VT1
U11, U13	IC/SM LM393 Low Power SOIC-8	2	National Semi.	LM393M
			Texas Instruments	LM393D
			Motorola	LM393D
CR7	IC/SM LM385 SOIC-8	1	National Semi.	LM385M
			Texas Instruments	LM385D-1.2
			Linear Tech.	LM385S8-1.2
U23	IC/SM ADP380 Battery Charger	1	Analog Devices	ADP3801AR
U10	IC/SM MAX6328 SOT23-3	1	Maxim	MAX6328UR23-T
U5	IC/SM MAX921 SOIC-8	1	Maxim	MAX921CSA
U6	IC/SM MAX8863 SOT23-5	1	Maxim	MAX8863TEUK-T
U14	PROCESSOR 80303 (from Intel)	1	Intel	TBD
U16	VLSI I/O UART 16C550 PLCC (3.3V)	1	Texas Instruments	TL15C550CFN
			Exar	ST16C550CJ44
U7	VLSI I/O RS232 Transvr (3.3V)	1	Maxim	MAX3232ECUP
U15	MEM Flash E28F016S3-120 (3.3V)	1	Intel	E28F016S3-120
C114	CAP SM 20pF (chip 1206)	1		
C68	CAP SM 100pF (chip 1206)	1	AVX	1206A101JATMA
C77, C92	CAP SM 1000pF (chip 1206)	2	AVX	12061A102JATMA
C63	CAP TANT SM 0.22µF, 10V (1206)	1	AVX	TAJA244M035R
C70	CAP TANT SM 220µF, 10V (7343)	1	AVX	TPSE227K010R010
C95, C97, C99	CAP TANT SM 47µF, 16V (7343)	3	AVX	TPSD476K016R015

Table 22. IQ80303 Bill of Materials (Sheet 2 of 3)

Location	Part Description	Qty	Manufacturer	Part Number
C48, C61, C85, C89	CAP TANT SM 4.7µF, 35V (7343)	4	Sprague	293D475X9035D2T
			AVX	TAJD475K035R
C41, C79	CAP TANT SM 22µF, 20V (7343)	2	Sprague	293D226X9020D2T
C102	CAP TANT SM 10µF 25/35V (7343)	1	Sprague	293D1060025D2T
C2, C5, C7, C12, C13, C16, C19, C21, C22, C24, C26, C69, C78, C84, C106	CAP CERM SM, 0.01µF 50V (0805)	15		
C1, C3, C4, C6,				
C8-C11, C14, C15, C17				
C18, C20, C23, C25				
C27-C40, C43-C47				
C49-C55, C57-C60				
C62, C64-C67, C71-C76				
C80-C83, C86-C88, C90				
C91, C93, C94, C96, C98				
C100, C101, C103-C105				
C107-C113, C115-C128	"CAPCERM SM, 0.1µF (0805) 50V,10%	95		
C56	CAP CERM SM, 470pF (0805)	1	Murata	GRM40COG471JAT2A
			AVX	08055A471JAT2A
			Phillips	0805CG471JOBB2
C42	CAP CERM SM, 22pF (0805)	1	Kemet	C0805C220J5GACTU
R41	R/SM 1/16W 1% 10KΩ (0603)	1	Dale	CRCW06031002FT
R64	R/SM 1/16W 5% 1.2MΩ (0603)	1		
R48	R/SM 1/16W 1% 14.7KΩ (0603)	1	Dale	CRCW06031472FT
R25, R40	R/SM 1/16W 1% 150KΩ (0603)	2	KOA	RK73H1J1503FT
R76	R/SM 1/16W 1% 16.5KΩ (0603)	1	KOA	RK73H1J1652FT
R36	R/SM 1/16W 1% 215KΩ (0603)	1	Dale	CRCW06032153FT
R56, R63	R/SM 1/16W 5% 39KΩ (0603)	2		
R55, R60	R/SM 1/16W 5% 4.3KΩ (0603)	2		
R44	R/SM 1/16W 5% 470KΩ (0603)	1		
R45	R/SM 1/16W 1% 4.99KΩ (0603)	1	KOA	RK73H1J4991FT
R77	R/SM 1/16W 5% 56Ω (0603)	1		
R46	R/SM 1/16W 5% 62KΩ (0603)	1		
R67	R/SM 1/10W 5% 000Ω (0805)	1		
R73	R/SM 1/10W 5% 100Ω (0805)	1		
R34	R/SM 1/10W 5% 1KΩ (0805)	1		
R24, R33, R38, R39, R42, R49, R70, R72, R74, R75, R78	R/SM 1/10W 5% 10KΩ (0805)	11		
R30, R35, R47	R/SM 1/10W 1% 100KΩ (0805)	3	KOA	RK73H2A1003FT
R20	R/SM 1/10W 5% 100KΩ (0805)	1		
R69	R/SM 1/10W 5% 1.5KΩ (0805)	1		
R21	R/SM 1/10W 1% 165KΩ (0805)	1	Dale	CRCW08051653FT
R37, R81	R/SM 1/10W 5% 22Ω (0805)	2		
R82	R/SM 1/10W 5% 24Ω (0805)	1		
R52, R62	R/SM 1/10W 5% 2.7KΩ (0805)	2		
R26-R29	R/SM 1/10W 5% 330Ω (0805)	4		

Table 22. IQ80303 Bill of Materials (Sheet 3 of 3)

Location	Part Description	Qty	Manufacturer	Part Number
R59, R68	R/SM 1/10W 5% 4.7KΩ (0805)	2		
R3, R22, R23	R/SM 1/10W 5% 8.2KΩ (0805)	3		
R50, R66, R71	R/SM 1/8W 5% 10Ω chip 1206	3		
R58, R79, R80	Resistor/SM 1/2W 5% 100Ω	3	Beckman	BCR 1/2 101 JT
			Dale	CRCW 2010 101 J
			SEI	RMC 1/2 100 Ω 5%
R53	Res/SM 1/2W 1% 0.5Ω (2010)	1	Dale	WSL-2010 0.5 Ω
			IRC	LR2010,1%,0.5 Ω
R54, R57, R61	Resistor Pk SM RNC4R8P 2.7KΩ	3	CTS	742083272JTR
R31, R32, R43	Resistor Pk SM RNC4R8P 1.5KΩ	3	CTS	742083152JTR
R65	Resistor Pk SM RNC4R8P 30Ω	1	CTS	742083300JTR
R1, R2, R4, R5	Resistor Pk SM RNC4R8P 330Ω	4	KOA	CN1J4T3300J
R51	Resistor Pk SM RNC4R8P 24Ω	1	CTS	742083240JTR
R6-R19	Resistor Pk SM RNC4R8P 8.2KΩ	14	TBD	TBD
J9-J13	CONN SM/TH Mictor 38P Recptcl	5	AMP	767054-1
J1,J2	CONN PCI 64BIT 3.3V/PCB TH	2	AMP	145168-4
			Framatome	CEE2X92SC-V33Z14W
J5	CONN DIMM 168P/RAng/Socket/TH	1	Berg	88638-61102
			AMP	1-390171-6
J7	CONN/SM TJ 6/6 (Non-Shielded)	1	Kycon	GM-SMT2-N-66
J14	CONN 3P SM Battery Header RAng	1	Molex	53261-0390
J6	CONN Hdr 16 pin/w shell, pcb	1	AMP	103308-3
Z1, Z3	Jumper JUMP2X1	2	Molex	22-28-4023
Z2	Jumper JUMP2X2	1	Molex	10-89-6044
J15	Jumper JUMP2X4 (Right Angle)	1	Samtec	BCS-104-LDHE
J8	Jumper JUMP2X8	1	Molex	10-89-6164
L1	Inductor/SM 68µh 20%	1	Coiltronics	UP1B-680
S1, S2	Switch/SM DIP4 DHS-4S	2	Morse	DHS-4S
U20	OSC/SM 1.8432 MHz (3.3V)	1	MMD	MI3100HH-1.8432MHz
			Ecliptek	EC2600TS-1.8432M
			Connor-Winfield	HSM933 1.8432MHz
CR2, CR4, CR5	LED Green (0.125" height)	3	Hewlett Packard	HLMP-3507-D00B2
CR3	LED-Red	1	Hewlett Packard	HLMP3301$010
CR1	LED - Dual 7 Segment Display	1	Hewlett Packard	HDSP-G211
CR6	Diode/SM Schottky 3A/30V	1	Motorola	MBRD330
CR8, CR9	Diode/SM Schottky 1-2A/10V	2	Motorola	MBRS130LT3
Q8	Trnistr/SM General (NPN) (SOT23)	1	Motorola	MMBT3904LT1
			Fairchild	MMBT3904
Q1-Q4	Trnistr/SM General (PNP) (SOT23)	4	Motorola	MMBT 3906LT1
			Fairchild Semi.	MMBT 3906
			Central Semi.	CMPT 3906

Intel® 80303 I/O Processor PBGA Signal Ball Map C

Table 23 details the ball map for the 80303 I/O processor processor.

Table 23. 540 L H-PBGA - Ballpad Order (Sheet 1 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
A1	VSS	A32	VSS	B31	VSS
A2	VSS	B1	VSS	B32	VSS
A3	DQ31	B2	VSS	C1	S_AD33
A4	DQ30	B3	DQ63	C2	S_AD35
A5	DQ29	B4	VSS	C3	VCC
A6	DQ27	B5	DQ61	C4	VCC
A7	DQ25	B6	DQ28	C5	DQ62
A8	DQ23	B7	VSS	C6	VCC
A9	DQ22	B8	DQ24	C7	DQ26
A10	SCKE1	B9	VSS	C8	VCC
A11	DQ19	B10	DQ21	C9	DQ54
A12	DQ17	B11	VSS	C10	VCC
A13	SCB3	B12	DQ18	C11	DQ20
A14	SDQM3	B13	VCC	C12	VCC
A15	SBA1	B14	SCB2	C13	DQ16
A16	SA8	B15	VSS	C14	VCC
A17	SA6	B16	SA10	C15	SDQM2
A18	SA2	B17	VSS	C16	VCC
A19	SCE0#	B18	SA4	C17	SA11
A20	SDQM0	B19	VSS	C18	VCC
A21	SWE#	B20	SDQM1	C19	SA0
A22	SCB0	B21	VSS	C20	VCC
A23	DQ14	B22	SCB1	C21	SRAS#
A24	DQ12	B23	VSS	C22	VCC
A25	DQ11	B24	DQ13	C23	DQ15
A26	DQ9	B25	VCC	C24	VCC
A27	DQ7	B26	DQ10	C25	DQ46
A28	DQ5	B27	VSS	C26	VCC
A29	DQ4	B28	DQ6	C27	DQ8
A30	DQ3	B29	DQ38	C28	VCC
A31	VSS	B30	DQ37	C29	DQ39

Table 23. 540 L H-PBGA - Ballpad Order (Sheet 2 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
C30	VCC	E5	S_AD38	G2	S_AD51
C31	VCC	E6	DQ60	G3	VCC
C32	DQ2	E7	DQ58	G4	S_AD44
D1	S_AD37	E8	DQ57	G5	S_AD46
D2	S_AD39	E9	DQ55	G28	N/C
D3	S_AD32	E10	DQ53	G29	DQ32
D4	S_AD34	E11	DQ51	G30	VCC
D5	VSS	E12	DQ49	G31	DCLK3
D6	DQ59	E13	SCB7	G32	DCLK2
D7	VCC	E14	SCB6	H1	S_AD53
D8	DQ56	E15	SDQM7	H2	S_AD55
D9	VSS	E16	SCKE0	H3	S_AD48
D10	DQ52	E17	DCLKIN	H4	VSS
D11	DQ50	E18	SBA0	H5	S_AD50
D12	DQ48	E19	SA7	H28	DCLKOUT
D13	VSS	E20	SA5	H29	VSS
D14	SA13	E21	SA1	H30	N/C
D15	SDQM6	E22	SCE1#	H31	VSS
D16	SA12	E23	SDQM4	H32	N/C
D17	VSS	E24	SCB5	J1	S_AD57
D18	SA9	E25	DQ47	J2	S_AD59
D19	VCC	E26	DQ45	J3	VCC
D20	SA3	E27	DQ43	J4	S_AD52
D21	VSS	E28	DQ41	J5	S_AD54
D22	SDQM5	E29	DQ34	J28	N/C
D23	SCAS#	E30	VCC	J29	N/C
D24	SCB4	E31	DQ36	J30	VCC
D25	VSS	E32	DQ35	J31	VCC
D26	DQ44	F1	S_AD45	J32	N/C
D27	DQ42	F2	VSS	K1	S_AD61
D28	DQ40	F3	S_AD47	K2	VSS
D29	VSS	F4	S_AD40	K3	S_AD63
D30	DQ1	F5	S_AD42	K4	S_AD56
D31	VSS	F28	VCCPLL1	K5	S_AD58
D32	DQ0	F29	DQ33	K28	N/C
E1	S_AD41	F30	DCLK1	K29	N/C
E2	S_AD43	F31	VSS	K30	PWRDELAY
E3	VCC	F32	DCLK0	K31	VSS
E4	S_AD36	G1	S_AD49	K32	N/C

Table 23. 540 L H-PBGA - Ballpad Order (Sheet 3 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
L1	S_CBE4#	P32	LCDINIT#	V31	VSS
L2	S_CBE6#	R1	S_M66EN	V32	N/C
L3	VCC	R2	S_AD10	W1	S_DEVSEL#
L4	S_AD60	R3	VCC	W2	S_IRDY#
L5	S_AD62	R4	S_AD2	W3	VCC
L28	N/C	R5	S_AD4	W4	S_PAR
L29	N/C	R28	N/C	W5	S_STOP#
L30	VCC	R29	XINT5#	W28	VCC
L31	N/C	R30	VCC	W29	GPIO2
L32	N/C	R31	XINT4#	W30	VCC
M1	S_ACK64#	R32	XINT3#	W31	GPIO1
M2	S_AD1	T1	S_AD12	W32	GPIO0
M3	S_PAR64	T2	S_AD14	Y1	S_CBE2#
M4	VSS	T3	S_AD6	Y2	S_AD17
M5	S_CBE5#	T4	VSS	Y3	S_TRDY#
M28	VCC	T5	S_CBE0#	Y4	VSS
M29	VSS	T28	I_RST#	Y5	S_FRAME#
M30	N/C	T29	VSS	Y28	RAD8
M31	VSS	T30	XINT2#	Y29	VSS
M32	N/C	T31	VSS	Y30	VCC
N1	S_AD3	T32	XINT1#	Y31	VSS
N2	S_AD5	U1	S_CBE1#	Y32	VCCPLL2
N3	VCC	U2	S_SERR#	AA1	S_AD19
N4	S_CBE7#	U3	VCC	AA2	S_AD21
N5	S_REQ64#	U4	S_AD9	AA3	VCC
N28	N/C	U5	S_AD11	AA4	S_AD16
N29	N/C	U28	XINT0#	AA5	S_AD18
N30	VCC	U29	GPIO7	AA28	VCC
N31	N/C	U30	VCC	AA29	VCC
N32	NMI#	U31	GPIO6	AA30	VCC
P1	S_AD7	U32	GPIO5	AA31	VCC5REF
P2	VSS	V1	S_PERR#	AA32	RAD7
P3	S_AD8	V2	VSS	AB1	S_AD23
P4	VREF_S	V3	S_LOCK#	AB2	VSS
P5	S_AD0	V4	S_AD13	AB3	S_CBE3#
P28	VCC	V5	S_AD15	AB4	S_AD20
P29	FAIL#	V28	VCC	AB5	S_AD22
P30	VCC	V29	GPIO4	AB28	RAD6
P31	VSS	V30	GPIO3	AB29	RAD5

Table 23. 540 L H-PBGA - Ballpad Order (Sheet 4 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
AB30	RAD4	AF29	RAD9	AH26	P_AD40
AB31	VSS	AF30	RWE#	AH27	P_AD36
AB32	RAD3	AF31	VSS	AH28	P_AD32
AC1	S_AD25	AF32	RALE	AH29	VSS
AC2	S_AD27	AG1	S_CLK3	AH30	TRST#
AC3	VCC	AG2	R_CLKOUT	AH31	TMS
AC4	S_AD24	AG3	VCC	AH32	TDO
AC5	S_AD26	AG4	S_REQ2#	AJ1	S_REQ1#
AC28	RAD2	AG5	S_GNT1#	AJ2	VSS
AC29	RAD1	AG28	ROE#	AJ3	VCC
AC30	VCC	AG29	VCC	AJ4	S_REQ3#
AC31	RAD0	AG30	VCC	AJ5	S_GNT4#
AC32	RAD16	AG31	RCE1#	AJ6	VSS
AD1	S_AD29	AG32	RCE0#	AJ7	P_GNT#
AD2	S_AD31	AH1	S_CLK5	AJ8	VCC
AD3	S_AD28	AH2	R_CLKIN	AJ9	P_AD24
AD4	VSS	AH3	S_GNT2#	AJ10	VSS
AD5	S_AD30	AH4	VSS	AJ11	P_AD18
AD28	RAD15	AH5	S_GNT3#	AJ12	P_FRAME#
AD29	VSS	AH6	S_REQ5#	AJ13	P_STOP#
AD30	RAD14	AH7	P_AD30	AJ14	VSS
AD31	VSS	AH8	P_AD26	AJ15	P_AD11
AD32	RAD13	AH9	P_IDSEL	AJ16	P_CBE0#
AE1	S_HOLDA#	AH10	P_AD20	AJ17	P_AD4
AE2	S_GNT0#	AH11	P_AD16	AJ18	VSS
AE3	VCC	AH12	P_TRDY#	AJ19	P_REQ64#
AE4	S_RST#	AH13	P_PAR	AJ20	VCC
AE5	S_HOLD#	AH14	P_AD13	AJ21	P_AD62
AE28	RAD12	AH15	P_AD9	AJ22	VSS
AE29	VCC	AH16	P_AD6	AJ23	P_AD54
AE30	VCC	AH17	P_CLK	AJ24	P_AD50
AE31	RAD11	AH18	P_AD0	AJ25	P_AD46
AE32	RAD10	AH19	P_CBE7#	AJ26	VSS
AF1	S_CLK1	AH20	P_PAR64	AJ27	P_AD38
AF2	VSS	AH21	P_AD60	AJ28	P_AD34
AF3	S_CLK0	AH22	P_AD56	AJ29	SCL
AF4	S_CLK2	AH23	P_AD52	AJ30	VCC
AF5	S_CLK4	AH24	P_AD48	AJ31	VSS
AF28	VCC	AH25	P_AD44	AJ32	TDI

Table 23. 540 L H-PBGA - Ballpad Order (Sheet 5 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
AK1	VCCPLL3	AL1	VSS	AM1	VSS
AK2	S_REQ0#	AL2	VSS	AM2	VSS
AK3	VCC	AL3	S_GNT5#	AM3	P_INTB#
AK4	S_REQ4#	AL4	VSS	AM4	P_INTD#
AK5	VCC	AL5	P_INTA#	AM5	P_REQ#
AK6	P_RST#	AL6	P_INTC#	AM6	P_AD31
AK7	VCC	AL7	P_AD27	AM7	P_AD29
AK8	P_AD28	AL8	VSS	AM8	P_AD25
AK9	VCC	AL9	P_AD23	AM9	P_CBE3#
AK10	P_AD22	AL10	P_AD19	AM10	P_AD21
AK11	VCC	AL11	P_CBE2#	AM11	P_AD17
AK12	P_DEVSEL#	AL12	VSS	AM12	P_IRDY#
AK13	VCC	AL13	P_PERR#	AM13	P_LOCK#
AK14	P_AD15	AL14	VCC	AM14	P_SERR#
AK15	VCC	AL15	P_AD14	AM15	P_CBE1#
AK16	P_AD10	AL16	VSS	AM16	P_AD12
AK17	VCC	AL17	P_AD8	AM17	P_M66EN
AK18	P_AD2	AL18	P_AD5	AM18	P_AD7
AK19	VCC	AL19	P_AD1	AM19	P_AD3
AK20	P_CBE5#	AL20	VSS	AM20	VREF_P
AK21	VCC	AL21	P_CBE6#	AM21	P_ACK64#
AK22	P_AD58	AL22	P_AD63	AM22	P_CBE4#
AK23	VCC	AL23	P_AD59	AM23	P_AD61
AK24	P_AD55	AL24	VSS	AM24	P_AD57
AK25	VCC	AL25	P_AD51	AM25	P_AD53
AK26	P_AD42	AL26	VCC	AM26	P_AD49
AK27	VCC	AL27	P_AD45	AM27	P_AD47
AK28	P_AD41	AL28	VSS	AM28	P_AD43
AK29	VCC	AL29	P_AD37	AM29	P_AD39
AK30	VCC	AL30	P_AD33	AM30	P_AD35
AK31	SDA	AL31	VSS	AM31	VSS
AK32	TCK	AL32	VSS	AM32	VSS