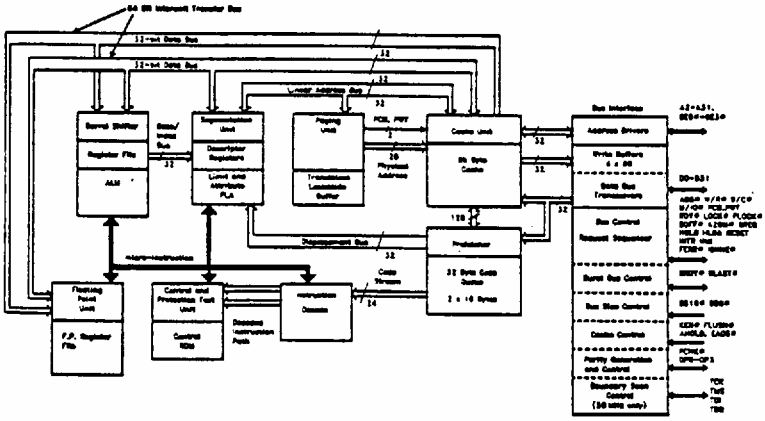
Preliminary

Radiation Hardened 80486DX2RP

High Speed CMOS 32-Bit Microprocessor

For Space Applications



SEI's 80486DX2RP (RP for RAD-PAK®)high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 80486DX2RP is fully equivalent to the commercial 80486DX2 from Intel. This device is a 32-bit architecture with on-chip memory mangement, floating point and cache memory units. On-chip cache memory allows frequently used data and code to be stored on-chip reducing accesses to the external bus. A clock doubler has been added to speed up internal operations to twice that of a device running with the same bus clock. The 80486DX2RP also contains a memory management unit (MMU) which consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. SEI's RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This device provides a total dose survivability of greater than 100 krad(Si). It is available in Class S packaging and screening.

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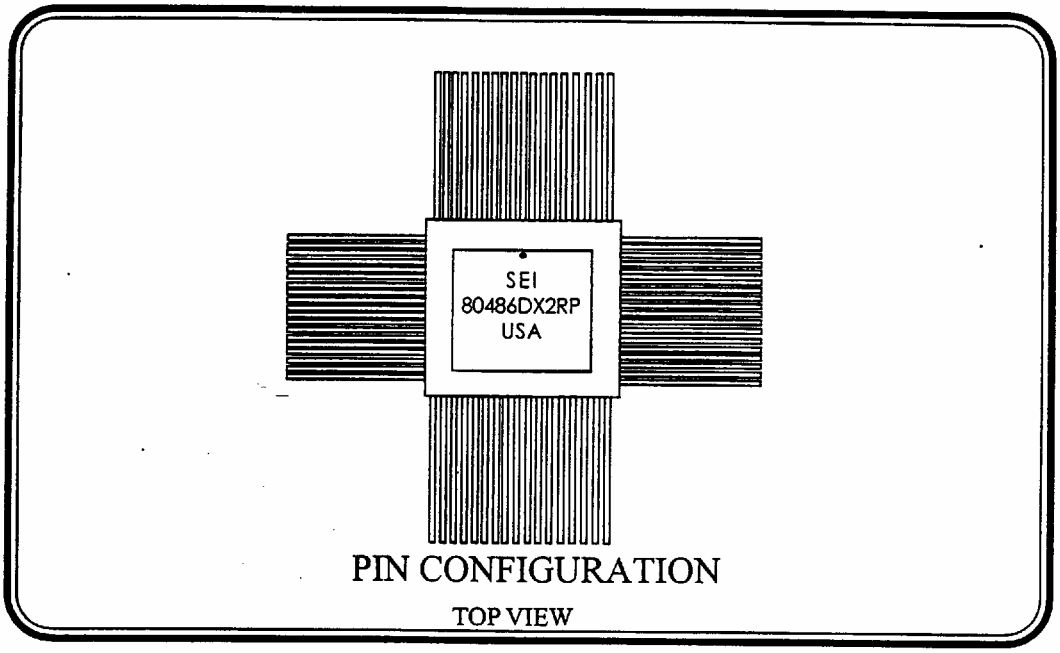
SEI 80486DX2RP 32-BIT MICROPROCESSOR

Radiation Hardened

80486DX2RP

High Speed CMOS
32-Bit Microprocessor



PIN CONFIGURATION

TOP VIEW

Features

- Pin Compatible with Intel 80486DX2
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- SEU Performance
  - LET Threshold = 5-6
- Package:
  - 172 Pin RAD-PAK® quad flat pack (2.50 in. x 2.50 in.)
  - Weight – 17 grams
- High Speed CHMOS V Technology
- 80, 106 Mbyte/sec Burst Bus
- 8 General Purpose 32 Bit Registers
- Very Large Address Space
  - 4 Gigabyte Physical
  - 64 Terabyte Virtual
- 5 V Only Power
- Multiprocessor Support
  - Cache Consistency Protocols
  - Support for Second Level Cache
- IEEE 1149.1 Boundary Scan Compatibility
- High Performance Design
  - 50 MHz/66 MHz Core Speed using 25 MHz/33 MHz Bus Clocks
  - Dynamic Bus Sizing for 8, 16, and 32-Bit Buses
- Self Test Capability
- On-Chip Debugging Aides
- Floating Point Unit
- Class S Screening per TM 5004
- QCI per TM5005

TQM
Total Quality Management

Sept. 1995

For Further Information Contact:

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