Low-voltage single-chip 8-bit microcontrollers 80CL31/80CL51

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, 1/0 in a single 40-lead DIL / mini-pack
- 4K x 8 ROM, expandable externally to 64K bytes
- 128 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 321/0 lines
- Two 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V (5.0V ±10% for P80C51)
- Frequency range of 0 to 16MHz (3.5MHz to 16MHz for P80C51)
- Very low current consumption
- Operating temperature range: -40 to +85ºC

DESCRIPTION

The 80CL51 is manufactured in an advanced CMOS technology. The instruction set of the 80CL51 is based on that of the 8051. The 80CL51 is a general purpose microcontroller especially suited for battery-powered applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The 80CL51 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 80CL51 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The P80CL31 is the ROMless version of the P80CL51. P80C51 is a 5V version of the low voltage P80CL51.

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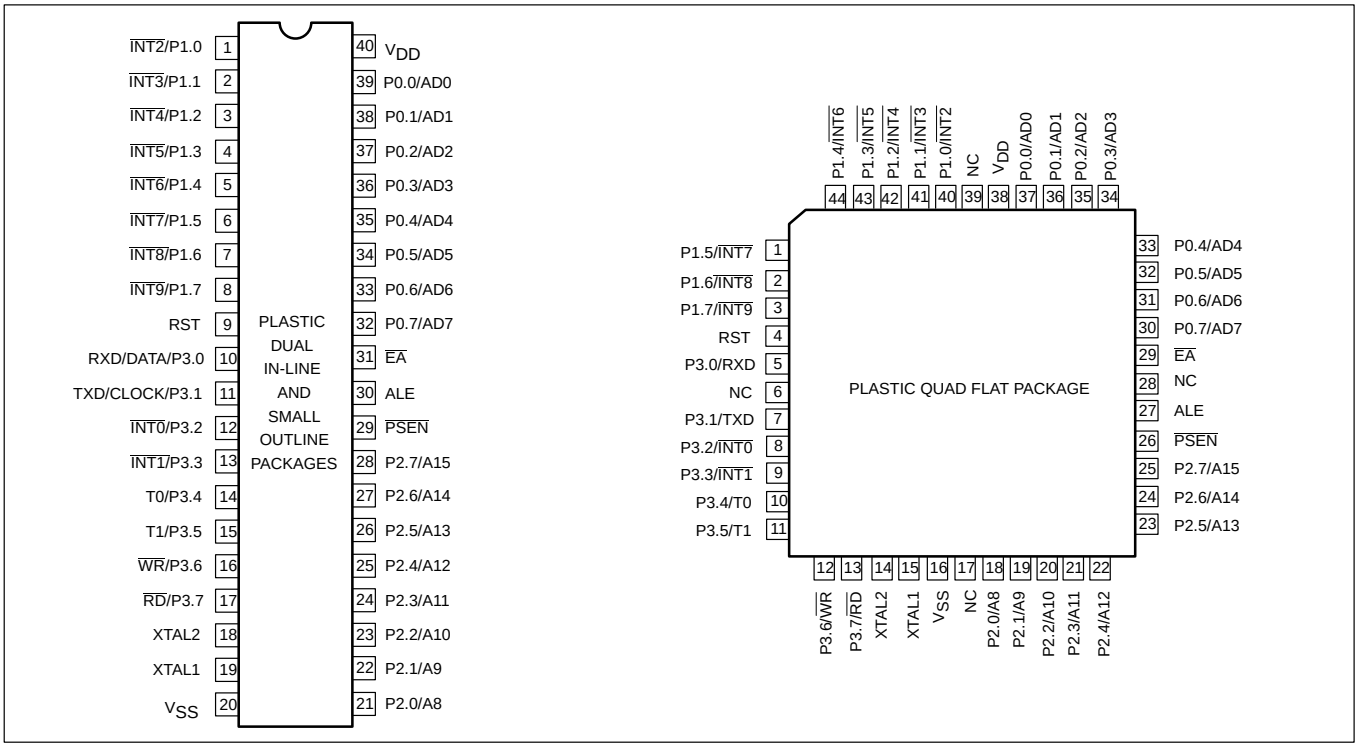
PIN CONFIGURATIONS



ORDERING INFORMATION

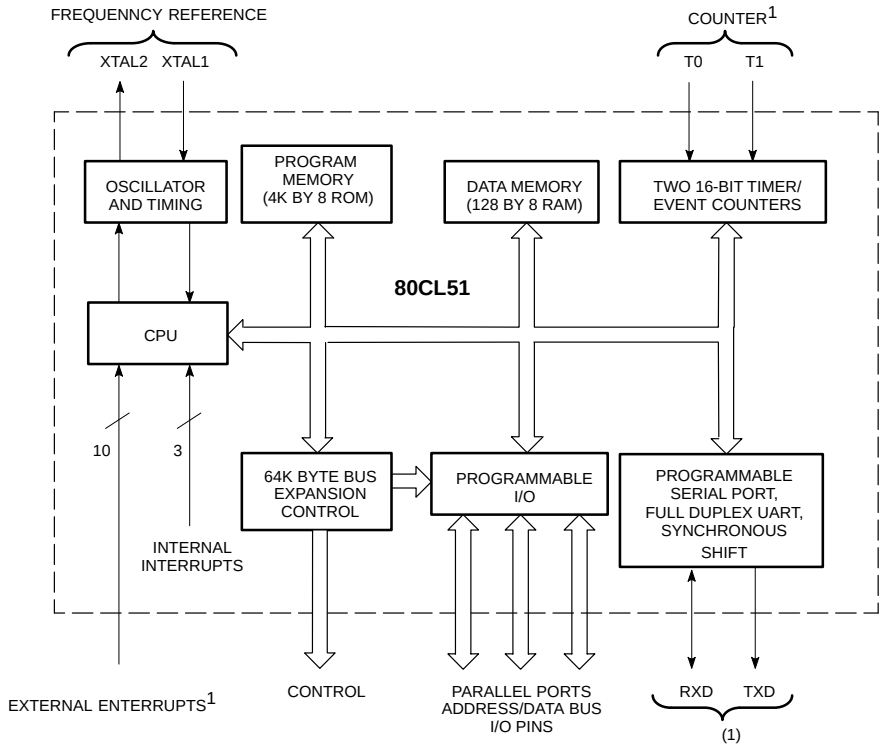
PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA [1] PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	DRAWING NUMBER
ROMless	ROM	ROMless	ROM		
P80CL31HFP	P80CL51HFP	P80CL31HFP N	P80CL51HFP N	–40 to +85; 40-lead Plastic Dual In-line Package (1.8V to 6V)	SOT129-1
P80CL31HFT	P80CL51HFT	P80CL31HFT D	P80CL51HFT D	–40 to +85; 40-lead Plastic Small Outline Package (1.8V to 6V)	SOT158-1
P80CL31HFH	P80CL51HFH	P80CL31HFH B	P80CL51HFH B	–40 to +85; 44-lead Plastic Quad Flat Package (1.8V to 6V)	SOT307-2
	P80C51HFP		P80C51HFP N	–40 to +85; 40-lead Plastic Dual In-line Package (5.0V ±10%)	SOT129-1
	P80C51HFT		P80C51HFT D	–40 to +85; 40-lead Plastic Small Outline Package (5.0V ±10%)	SOT158-1
	P80C51HFH		P80C51HFH B	–40 to +85; 44-lead Plastic Quad Flat Package (5.0V ±10%)	SOT307-2

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

PIN DESCRIPTIONS

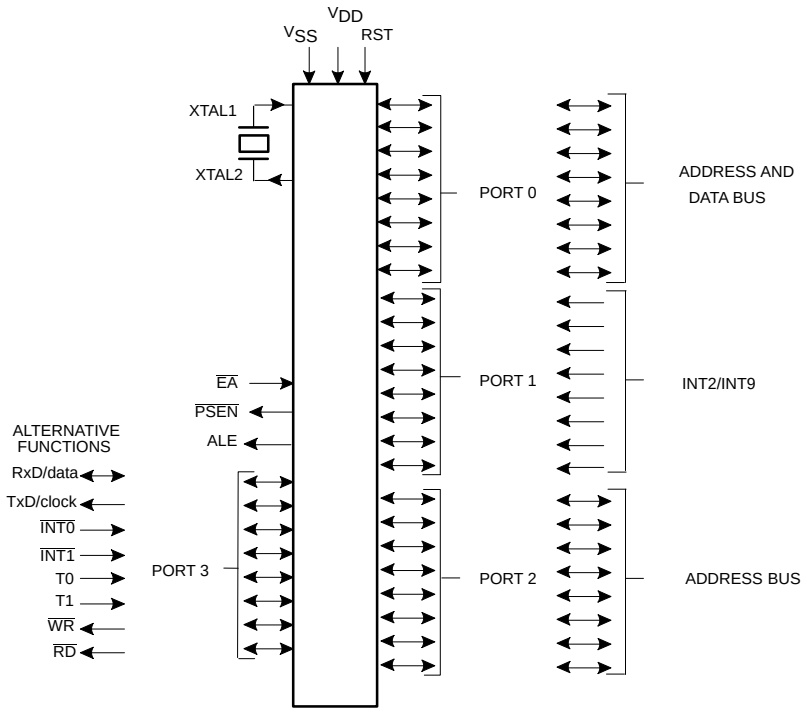
PIN		DESIGNATION	FUNCTION
QFP	DIP		
40	1	P1.O/INT2	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 1 output buffer can sink/source 4 LS TTL loads. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pullups. Port 1 also serves the alternative functions INT2 to INT9.
41	2	P1.1/INT3	
42	3	P1.2/INT4	
43	4	P1.3/INT5	
44	5	P1.4/INT6	
1	6	P1.5/INT7	
2	7	P1.6/INT8	
3	8	P1.7/INT9	
4	9	RST	**Reset:** A high level on this pin for two machine cycles while the oscillator is running resets the device.
5–13	10-17		**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pull ups.
5	10	P3.0/RXD/data	**RXD/data:** Serial port receiver data input (asynchronous)or data input/output (synchronous)
7	11	P3.1/TXD/clock	**TXD/clock:** Serial port transmitter data output (asynchronous) or clock output (synchronous)
8	12	P3.2/INT0	**INT0:** External interrupt 0.
9	13	P3.3/INT1	**INT1:** External interrupt 1.
10	14	P3.4/T0	**T0:** Timer 0 external input.
11	15	P3.5/T1	**T1:** Timer 1 external input.
12	16	P3.6/$\overline{WR}$	**$\overline{WR}$**: External data memory write strobe.
13	17	P3.7/$\overline{RD}$	**$\overline{RD}$**: External data memory read strobe.
14	18	XTAL2	**Crystal output:** Output of the inverting amplifier of the oscillator. Left open when external clock is used. **Crystal input:** Input to the inverting amplifier of the oscillator; also the input for an externally generated clock source.
15	19	XTAL1	**Crystal input:** Input to the inverting amplifier of the oscillator; also the input for an externally generated clock source.
16	20	Vss	**Ground:** Circuit ground potential.
18-25	21-28	P2.0-P2.7	**Port 2:** Port 2 is an 8-bit bidirectional 1/0 port with internal pullups. Port 2 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 2 output buffer can sink/source 4 LS TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 1 6-bit addresses (MOVX @DPTR). In this application it uses the strong internal pullups when emitting 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
26	29	PSEN	**Program store enable output:** Read strobe to external program memory. When executing code out of external program memory, PSEN is activated twice each machine cycle. However, during each access to external data memory two PSEN activations are skipped.
27	30	ALE	**Address Latch Enable:** Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of 1/6 of the oscillator frequency, and may be used for external timing or clocking purposes.
29	31	$\overline{EA}$	**External Access:** When EA is held High the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). Holding EA LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
30-37	32-39	P0.0-P00.7	**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. As an open drain output port it can sink 8 LS TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during access to external memory. In this application it uses strong internal pull-ups when emitting logic 1s.
38	40	V_{DD}	**Power supply.**

BLOCK DIAGRAM



1. Pins shared with parallels ports pins.

FUNCTIONAL DIAGRAM



1.0 FUNCTIONAL DESCRIPTION

General

The 80CL51 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 80CL51 contains a non-volatile 4K byte × 8 read-only program memory; a static 128 byte × 8 read/write data memory; 32 1/0 lines; two 16-bit timer/event counters; a thirteen- source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software selectable modes of reduced activity for power reduction: IDLE and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

The P80C51 is a 5V version of the low voltage microcontroller P80CL51. Hereafter the generic term P80CL51 will be used for the functional description of both types. The special features of the P80C51 are handled in chapter 1.9.

CPU timing

A machine cycle consists of a sequence of 6 states. Each state time lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1µs if the oscillator frequency is 12MHz.

1.1 Memory organization

The 80CL51 has a 4K Program Memory (ROM) plus 128 bytes of Data Memory (RAM) on board. The device has separate address spaces for Program and Data Memory (see Memory Map). Using Ports P0 and P2, the 80CL51 can address up to 64K bytes of external memory. The CPU generates both read and write signals (RD and WR) for external Data Memory accesses, and the read strobe (PSEN) for external Program Memory.

1.1.1 Program Memory

The 80CL51 contains 4K bytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 4K bytes of Program Memory can be implemented in either on- chip ROM or external Memory. If the EA pin is strapped to V_{DD}, then program memory fetches from addresses 000H through 0FFFH are directed to the internal ROM. Fetches from addresses 1000H through FFFFH are directed to external ROM. Program counter values greater than 0FFFH are automatically addressed to external memory regardless of the state of the EA pin.

1.1.2 Data Memory

The 80CL51 contains 128 bytes of internal RAM and 25 Special Function Registers (SFR). The Memory Map below shows the internal Data Memory space divided into the Lower 128, the Upper 128, and the SFR space.

The lower 128 bytes of the internal RAM are organized as mapped in Figure 1. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions refer to these registers R0 through R7. Two bits in the Program Status Word select which register bank is in use. The next 16 bytes above the register banks form a block of bit-addressable memory space. The 128 bits in this area can be directly addressed by the single-bit manipulation instructions. The remaining registers (30H to 7FH) are directly and indirectly byte addressable.

1.1.3 Special Function Registers

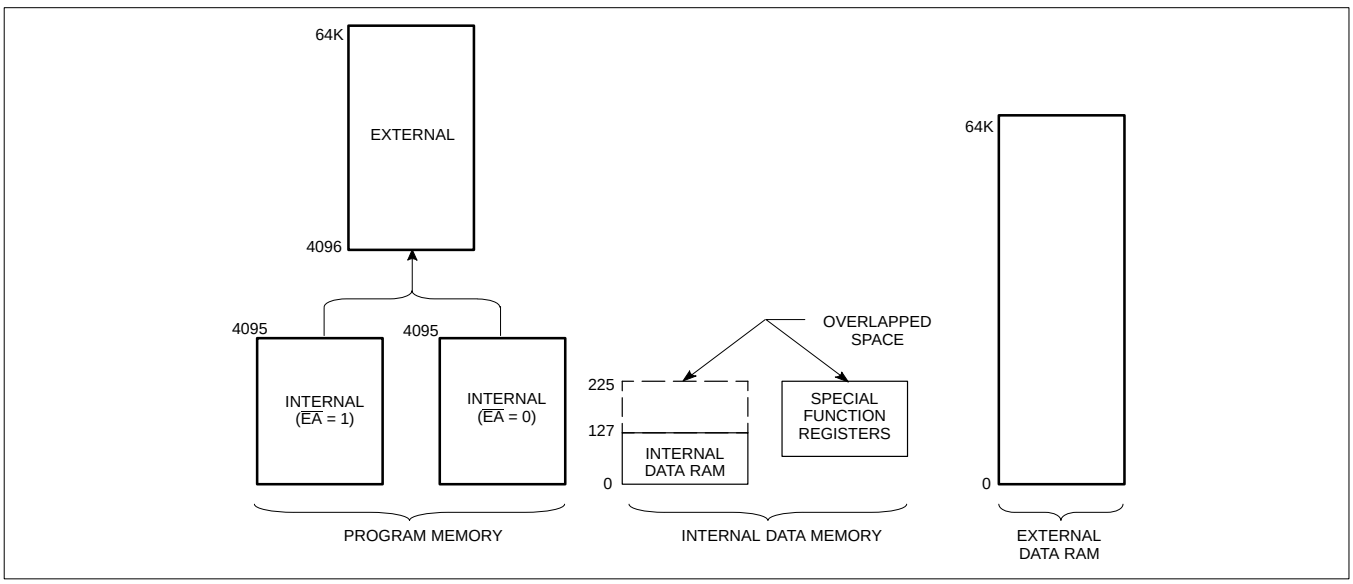
The upper 128 bytes are the address locations of the SFRs. Figure 2 shows the Special Function Register (SFR) space. SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 addressable locations in the SFR address space (SFRs with addresses divisible by eight).

1.1.4 Addressing

The 80CL51 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register-plus Index-Register-indirect

MEMORY MAP



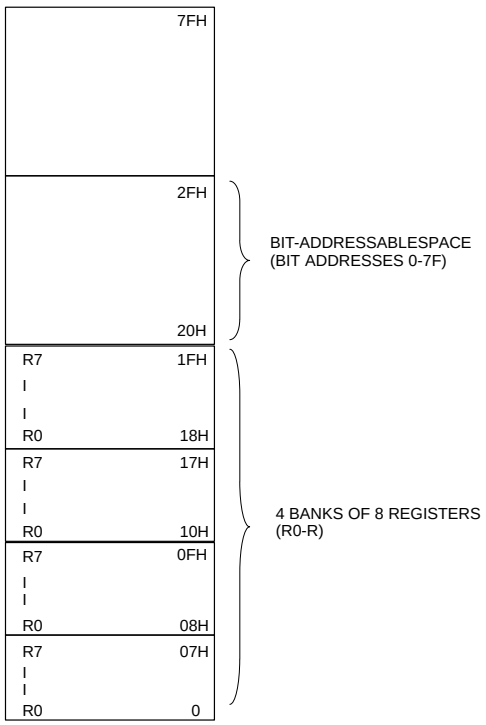


Figure 1. The Lower 128 Bytes of Internal RAM

The first three methods can be used for addressing destination operands. Most instructions have a “destination/source” filed that specifies data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or indirect.
- Internal RAM (128 bytes) through direct or register-indirect.
- Special Function Register through Direct.
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register-Plus Index-Register-Indirect.

1.2 I/O Facilities

1.2.1 Ports

The 80CL51 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8- bit addressable ports. Port 0, 1, 2 and 3 perform the following alternate functions:

Port 0: provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1: provides the inputs for the external interrupts INT2/INT9.

Port 2: provides the high-order address when expanding the device with external program or data memory.

Port 3: pins can be configured individually to provide:
(1) external interrupt request inputs
(2) counter input
(3) control signals to read and write to external memories
(4) UART input and output

To enable a Port 3 pin alternate function, the Port 3 bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and an input buffer. Ports 1,2,3 have internal pull ups. Figure 3(a) shows that the strong transistor p1 is turned on for only 2 oscillator periods after a 0-to-1 transition in the port latch. When on, it turns on p3 (a weak pull up) through the inverter. This inverter and p3 form a latch which hold the 1. In Port 0 the pull up p1 is only on when emitting 1s for external memory access. Writing a 1 to a Port 0 bit latch leaves both output transistors switched off so the pin can be used as a high-impedance input.

1.2.2 Port Options

The pins of port 1, port 2, and port 3 may be individually configured with one of the following options (see Figure 3):

Option 1: Standard Port; quasi-bidirectional I/O with pull up. The strong booster pull up p1 is turned on for two oscillator periods after a 0-to-1 transition in the port latch (see Figure 3(a)).

Option 2: Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull up resistor (see Figure 3(c)).

Option 3: Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs. See Figure 3(b).

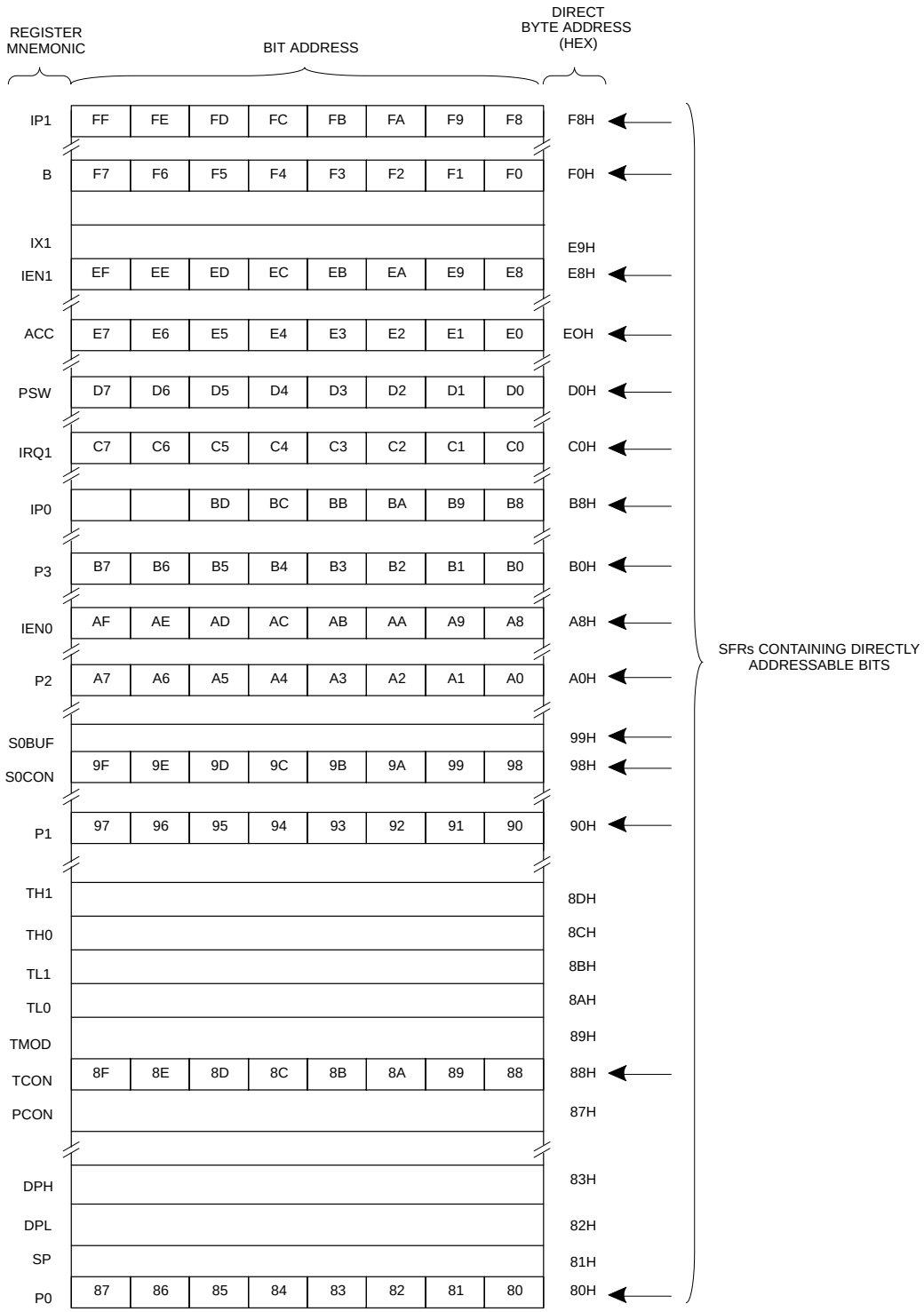


Figure 2. Special Function Registers

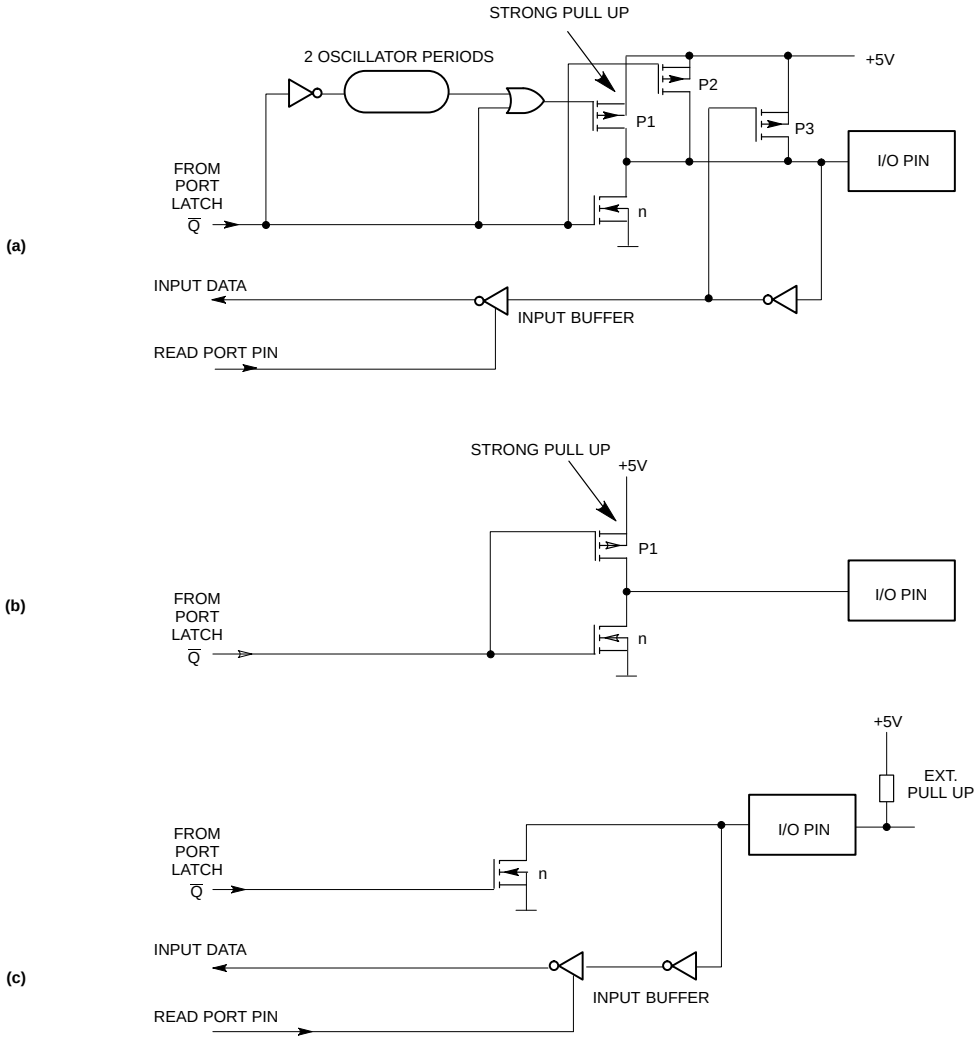


Figure 3. Ports

The definition of port options for port 0 is slightly different. Two cases have to be examined. First, accesses to external memory (EA=0 or access above the built -in memory boundary), second, I/O accesses.

External Memory Accesses

Option 1: True 0 and 1 are written as address to the external memory (strong pull up is used).

Option 2: An external pull up resistor is needed for external accesses.

Option 3: Not allowed for external memory access as the port can only be used as output.

I/O Accesses

Option 1: When writing a 1 to the port-latch, the strong pull up p1 will be on for 2 oscillator periods. No weak pull up exists. Without an external pull up, this option can be used as a high-impedance input.

Option 2: Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull up resistor (see Figure 3(c)).

Option 3: Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs.

Individual mask selection of the post-reset state is available on any of the above pins. Make your selection by appending “S” or “R” to option 1, 2, or 3 above (e.g. 1 S for a standard I/O to be set after RESET or 2R for an open-drain I/O to be reset after RESET).

1.3 Timer/event counter

The 80CL51 contains two 16-bit Timer/Counter registers, Timer 0 and Timer 1, which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupts requests

Timer 0 and Timer 1 can be independently programmed to operate as follows:

Mode 0 - 8-bit timer or counter with divide-by-32 prescaler

Mode 1 - 16-bit time-interval or event counter

Mode 2 - 8-bit time interval or event counter with automatic reload upon overflow

Mode 3 - Timer 0 establishes TL0 and TH0 as two separate counters.

In the “Timer” function, the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure a given level is sampled, it should be held for at least one full machine cycle.

1.4 Idle and Power-down operation

Idle mode operation permits the interrupt, serial port and timer blocks to continue functioning while the clock to the CPU is halted. The following functions remain active during Idle mode:

- Timer 0, Timer 1
- UART
- External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

1.4.1 Power control register

Power-down and Idle modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is byte addressable only.

PCON		
BIT	**POSITION**	**FUNCTION**
SMOD	PCON.7 PCON.4-PCON.6	Double baud-rate bit, see description of the UART, chapter 1.5. (reserved)
GF1	PCON.3	General purpose flag bit
GFO	PCON.2	General purpose flag bit
PD	PCON.1	Power-down activation bit
IDL	PCON.0	Idle mode activation bit

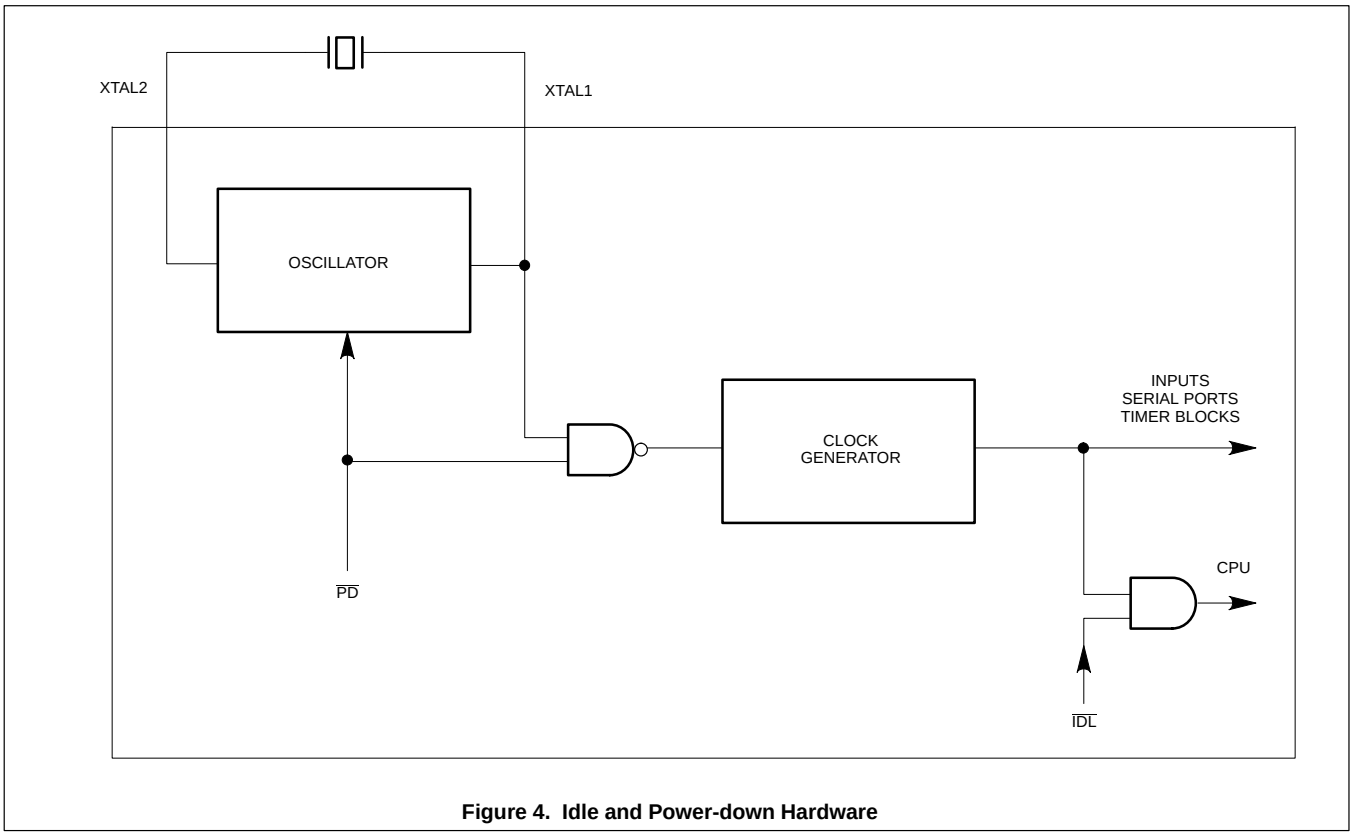


Figure 4. Idle and Power-down Hardware

1.4.2 Power-down mode

The instruction setting PCON.1 is the last executed prior to going into the Power-down mode. In Power-down mode the oscillator is stopped. The contents of the on-chip RAM and SFRs are preserved. The port pins output the values held by their respective SFRs. ALE and PSEN are held LOW.

In the Power-down mode V_{DD} may be reduced to minimize power consumption. However, the supply voltage must not be reduced until Power-down mode is active, and must be restored before the hardware reset is applied and frees the oscillator. Reset must be held active until the oscillator has restarted and stabilized.

The wake-up operation after power-down in this controller has two basic approaches:

1.4.2.1 Wake-up using INT2 to INT9

If INT2 to INT9 are enabled, the 80CL51 can be awakened from power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

1.4.2.2 Wake-up using RESET

To wake-up the 80CL51 the RESET pin has to be kept HIGH for a minimum of 24 oscillator periods. The on-chip delay counter is inactive. The user has to ensure that the oscillator is stable before any operation is attempted. Figure 5 illustrates the two possibilities for wake-up.

1.4.3 Idle mode

The instruction that sets PCON.0 is the last instruction executed before going into Idle mode. Once in the Idle mode, the internal clock is gated away from the CPU, but not from the Interrupt, Timer and Serial port functions. The CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The port pins retain the logical states they held at Idle mode activation. ALE and PSEN hold at the logic HIGH level.

There are two methods used to terminate the Idle mode. Activation of any enabled interrupt will cause PCON to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode.

Flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second method of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for only two machine cycles to complete the reset operation.

Reset redefines all SFRs, but does not affect the on-chip RAM.

The status of the external pins during Idle and Power-down mode is shown in Table 1. If the Power-down mode is activated while accessing external memory, port data held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull up transistor p1 (see Figure 3(a)).

Table 1. Status of the External Pins During Idle and Power-down Mode

MODE	MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	external	1	1	Floating	Port Data	Address	Port Data
Power-down	internal	0	0	Port Data	Port Data	Port Data	Port Data
Power-down	external	0	0	Floating	Port Data	Port Data	Port Data

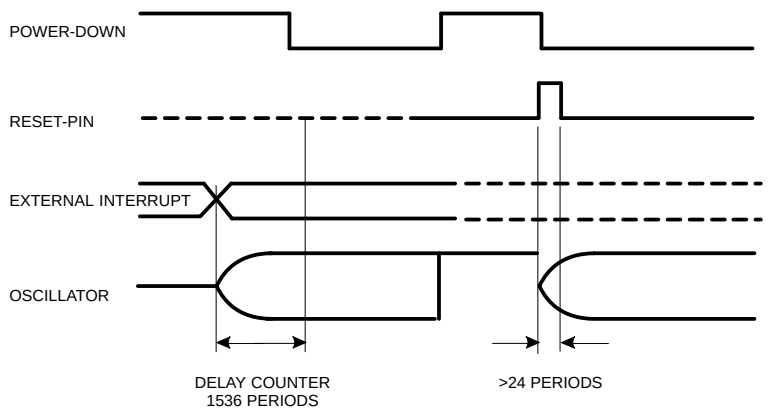


Figure 5. Wake-up Operation

1.5 Standard serial interface SI0: UART

This serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register S0BUF. Writing to S0BUF loads the transmit register, and reading S0BUF loads the transmit register, and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/ received (LSB first). The baud is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

1.5.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

1.5.2 Serial port control register

The serial port control and status register is the Special Function Register S0CON, shown in Figure 6. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (T1 and R1). See next page.

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency /12. The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency.

Mode 2 Baud Rate = $(2^{SMOD}/64)$(Oscillator Frequency)

The baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate.

Using Timer 1 to generate baud rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$(2^{SMOD}/32)$(Timer 1 Overflow Rate)

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$\{(2^{SMOD}/32)$ (Oscillator Frequency)$\}$ / {12 (256 - (TH 1)}

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring this Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Table 2 lists various commonly used baud rates and how they can be obtained from Timer 1.

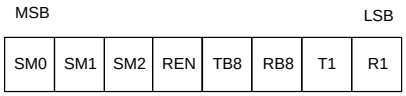
More about Mode 0

Figure 7 shows a simplified functional diagram of the serial port in Mode 0, and associated timing. Transmission is initiated by any instruction that uses S0BUF as a destination register. The "write to S0BUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that the one full machine cycle will elapse between "write to S0BUF", and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1 and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to S0BUF".

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.



Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	f_{OSC}/ 12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	f_{OSC}/64 or f_{OSC}/32
1	1	3	9-bit variable UART	

SM2 Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1 then Rl will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then R1 will not be activated if a valid stopbit was not received. In Mode 0, SM2 should be 0.

REN Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8 Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI Is transmit interrupt flag. Set by hardware at the end of the 8th time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception except (see SM2). Must be cleared by software.

Figure 6. Serial Port control (SCON) Register

Table 2. Timer 1 Generated Commonly Used Baud Rates

				TIMER 1	
BAUD RATE	**f_{OSC}**	**SMOD**	**C/T**	**MODE**	**RELOAD VALUE**
Mode 0 Max: 1.33 Mb/s	16 MHz	x	x	x	x
Mode 2 Max: 500 Kb/s	16 MHz	1	x	x	x
Modes 1,3: 83.3 Kb/s	16 MHz	1	0	2	FFH
19.2 Kb/s	11.059 MHz	1	0	2	FDH
9.6 Kb/s	11.059 MHz	0	0	2	FDH
4.8 Kb/s	11.059 MHz	0	0	2	FAH
2.4 Kb/s	11.059 MHz	0	0	2	F4H
1.2 Kb/s	11.059 MHz	0	0	2	E8H
137.5 Kb/s	11.986 MHz	0	0	2	1DH
110	6 MHz	0	0	2	72H
110	12 MHz	0	0	1	FEEBH

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT Clock makes transitions at S3P1 and S6P1 of every machine cycle. at S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load S0BUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More about Mode 1
Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 8051 the baud rate is determined by the Timer 1 overflow rate.

Figure 8 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit/receive.

Transmission is initiated by any instruction that uses S0BUF as a destination register. The “write to S0BUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to S0BUF” signal).

The transmission begins with activation of SEND which sends the start bit to pin TxD. One bit time later, DATA is activated, enabling the transmission of the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to S0BUF”. Reception is initiated by a detected 1 -to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times. The 16 states of the counter divide each bit time into 16th. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the left-most position in the shift register, (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, loads S0BUF and RB8, and set RI. The signal to load S0BUF and RB8, and to set RI, will generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. R1 = 0, and
2. Either SM2 = 0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into S0BUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

More about modes 2 and 3
Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 9 and 10 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses S0BUF as a destination register. The “write to S0BUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to S0BUF” signal). The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. Then TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contains zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to S0BUF”.

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed. As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the left-most position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load S0BUF and RB8, and set RI.

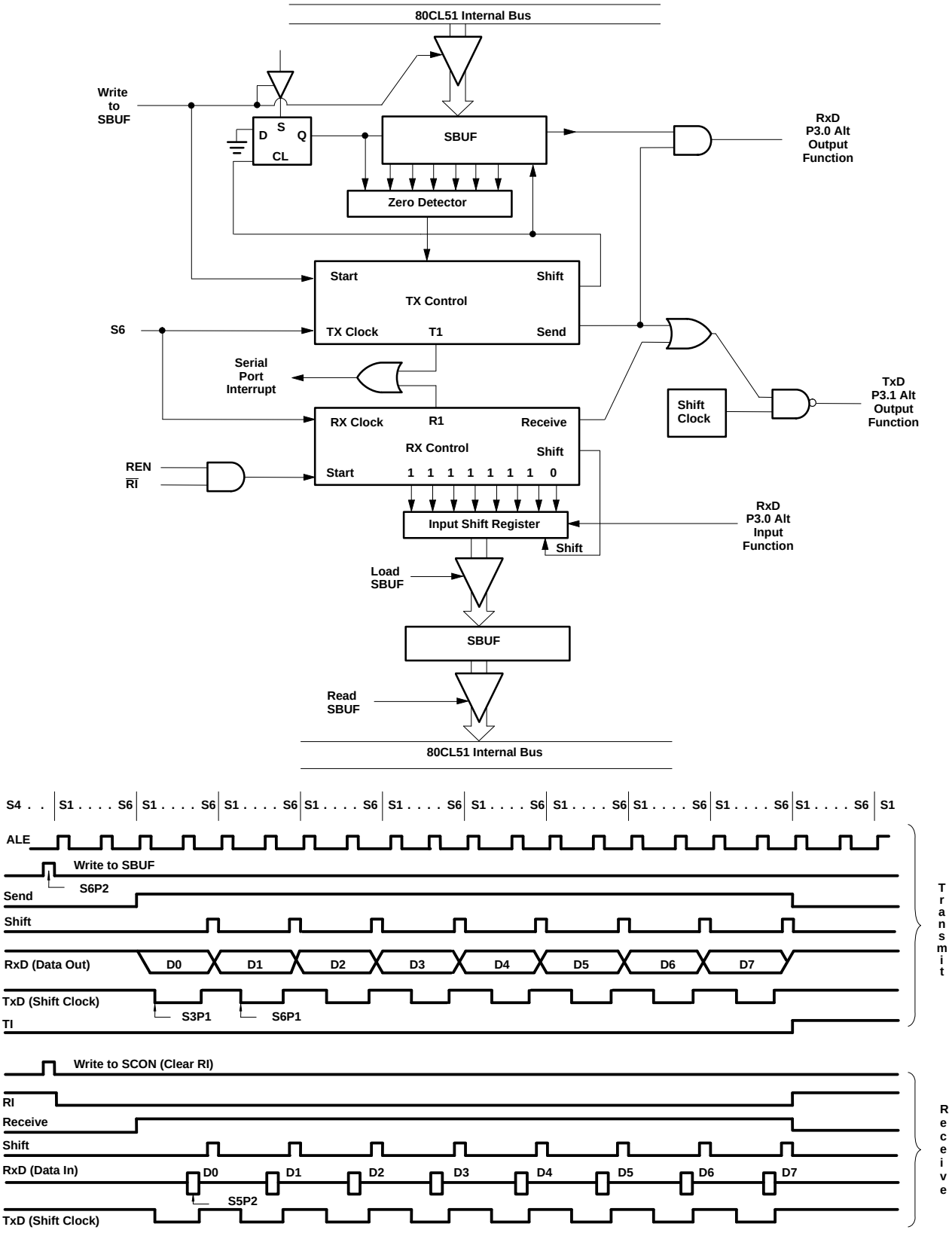


Figure 7. Serial Port Mode 0

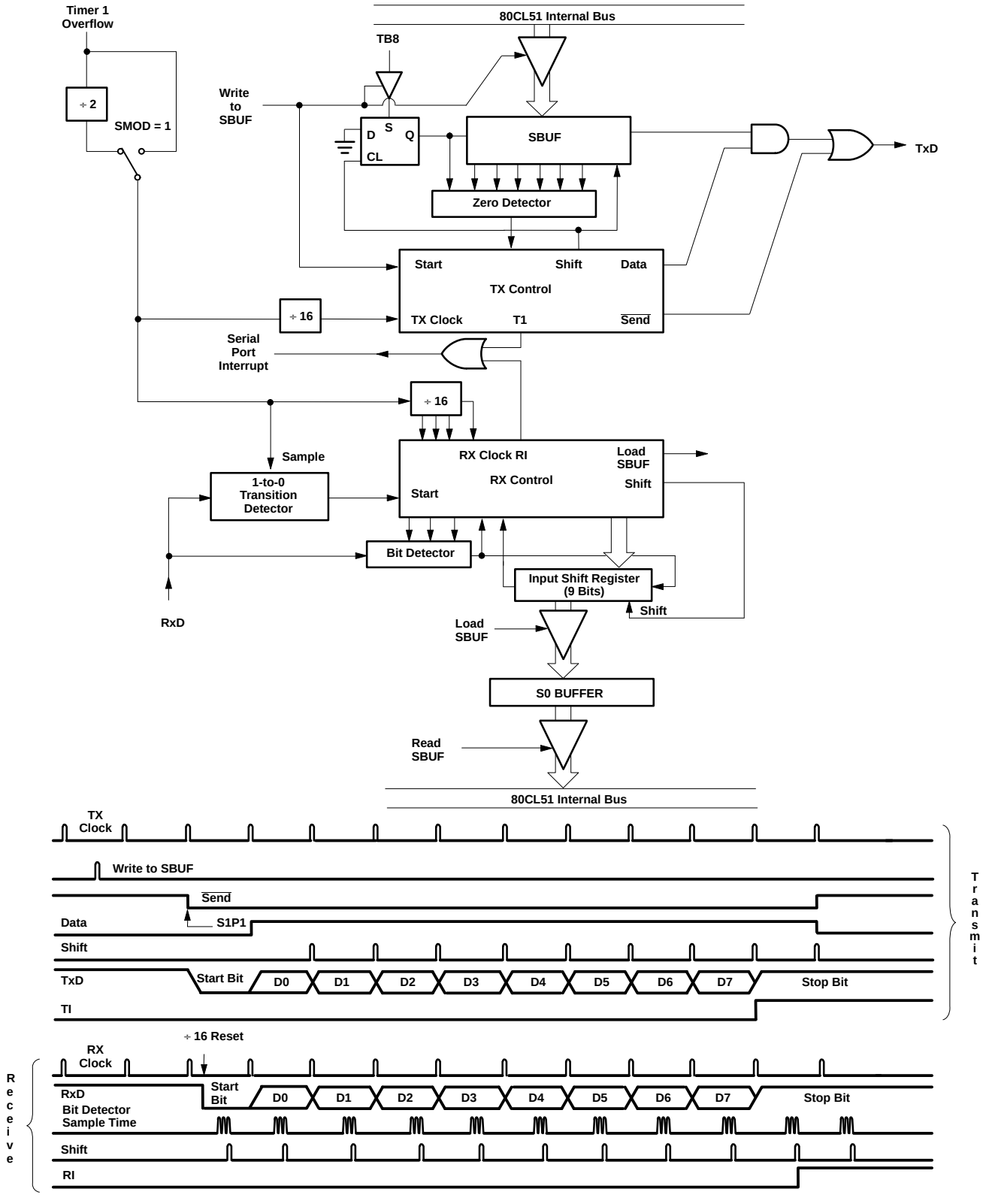


Figure 8. Serial Port Mode 1

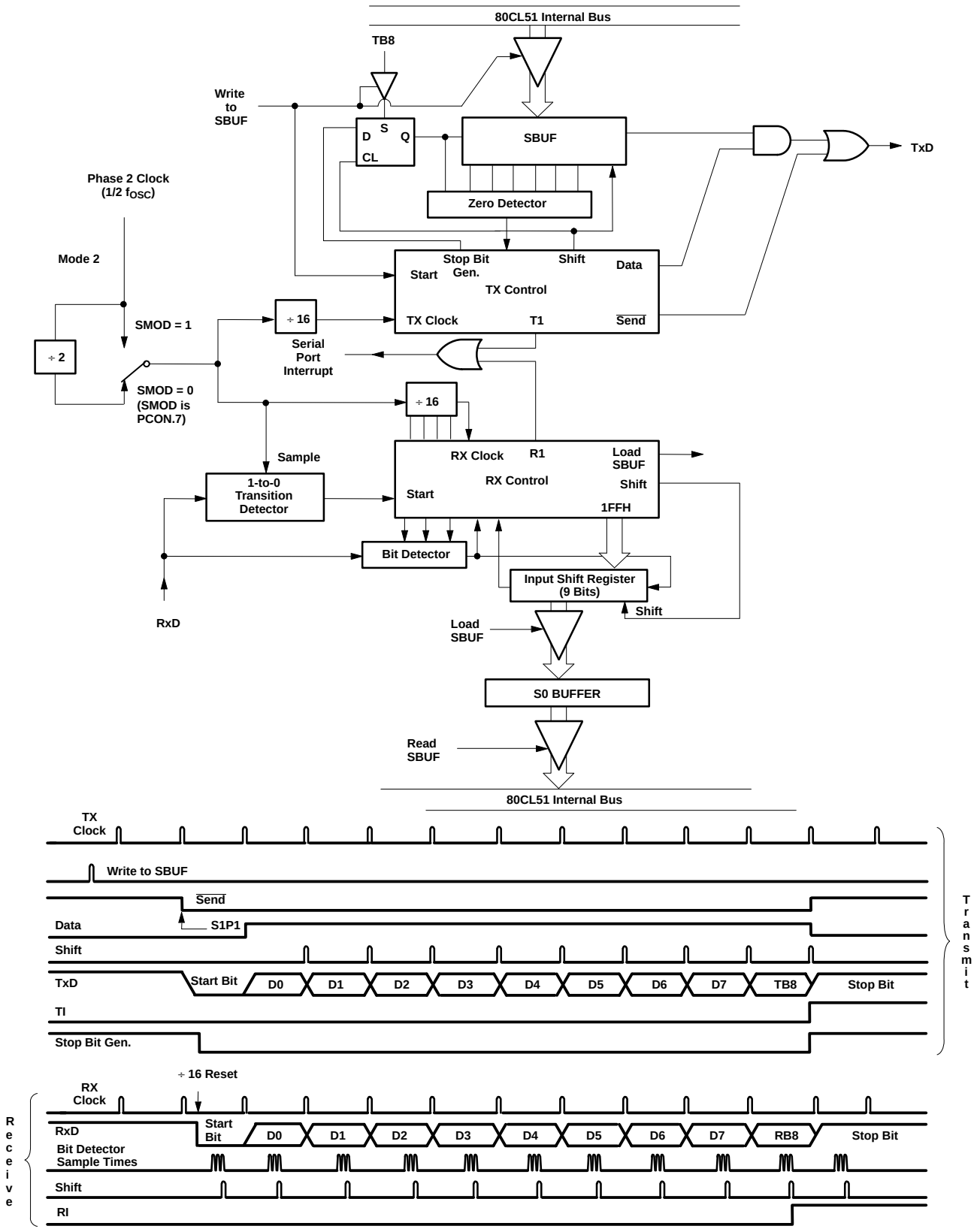


Figure 9. Serial Port Mode 2

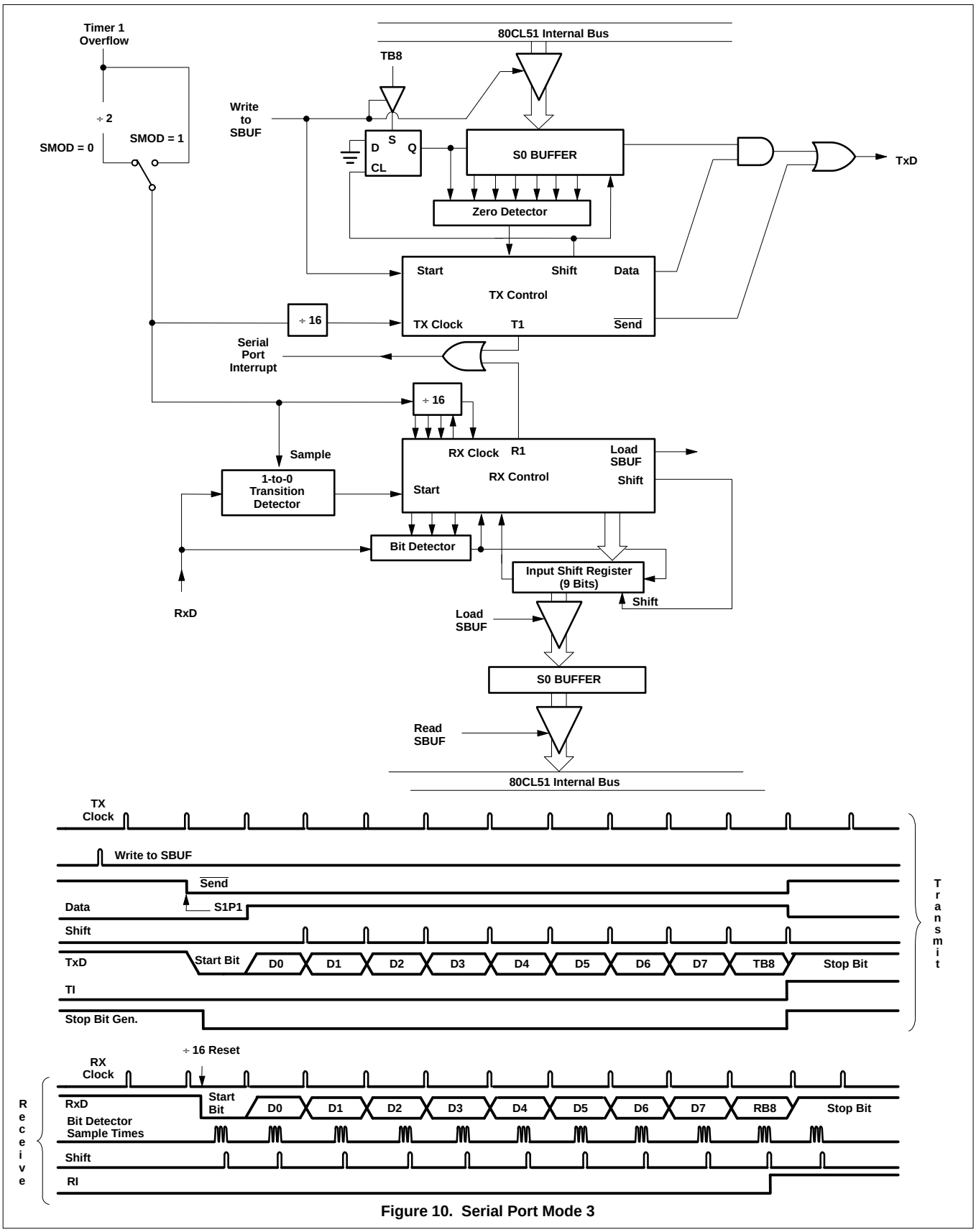


Figure 10. Serial Port Mode 3

The signal to load S0BUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. RI = 0, and
2. Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits 90 into S0BUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

1.6 Interrupt System

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to do execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a multiple-source, two-priority-level, nested interrupt system is provided. The 80CL51 acknowledges interrupt requests from thirteen sources as follows:

- INT0 and INT1
- Timer 0 and Timer 1
- UART serial I/O
- INT2 to INT9 (Port 1)

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IE, IEO). The priority level is selected via the Interrupt Priority register (IP0, IP1). All enabled sources can be globally disabled or enabled.

1.6.1 External Interrupts INT2/INT9

Port 1 lines serve an alternative purpose as eight additional interrupts INT2 to INT9. When enabled, each of these lines may “wake-up” the device from Power-down mode. Using the IX1 register, each pin may be initialized to either active HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

The Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on Interrupt Polarity Register IX1) on P1x is held active for at least one machine cycle. The Interrupt Request is not served until the next machine cycle.

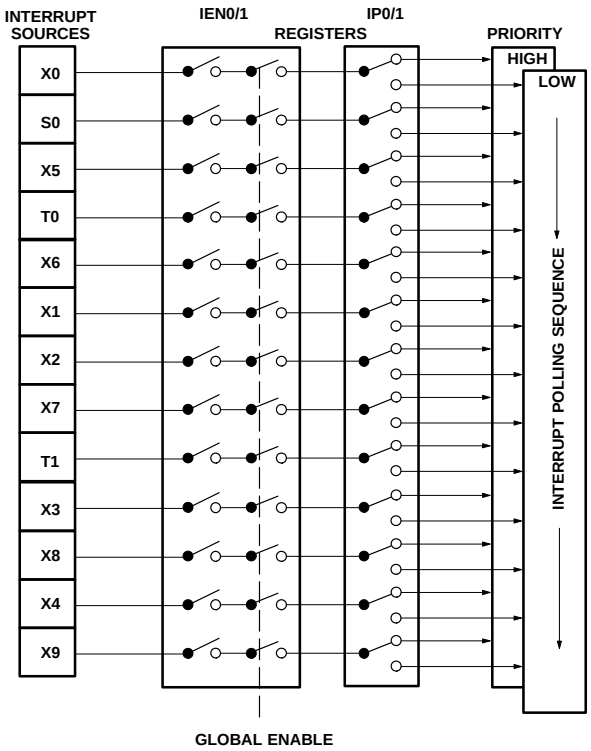


Figure 11. Interrupt System

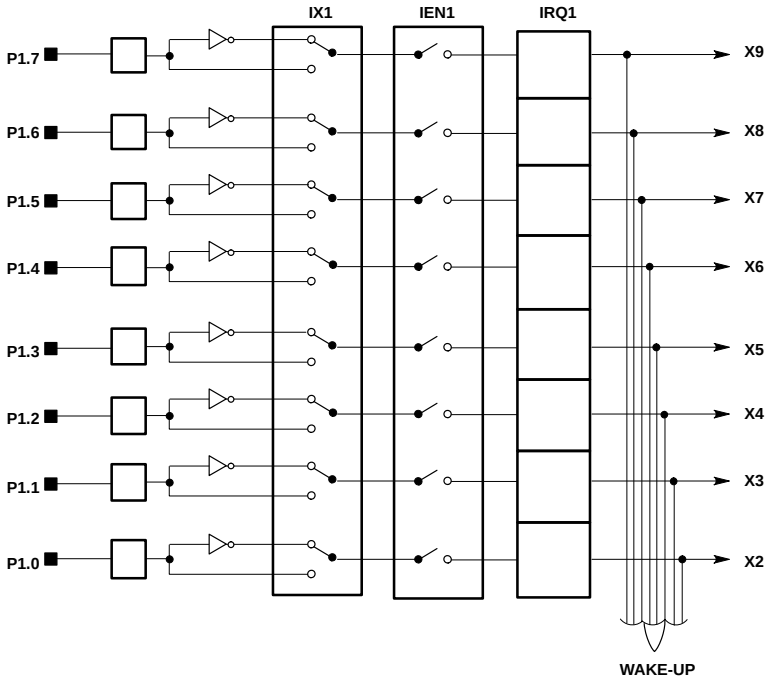


Figure 12. External Interrupt Configuration

Interrupt enable register IEN0, IEN1

IEN0 (A8H)

EA	-	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EA	General enable/disable control 0 = no interrupt is enabled 1 = any individually enabled interrupt will be accepted
IEN0.6	-	Unused
IEN0.5	ES1	Unused
IEN0.4	ES0	Enable UART SIO interrupt
IEN0.3	ET1	Enable timer T1 interrupt
IEN0.2	EX1	Enable external interrupt
IEN0.1	ET0	Enable Timer T0 interrupt
IEN0.0	EX0	Enable external interrupt 0

IEN1 (E8H)

EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Bit	Symbol	Function
IEN1.7	EX9	Enable external interrupt 9
IEN1.6	EX8	Enable external interrupt 8
IEN1.5	EX7	Enable external interrupt 7
IEN1.4	EX6	Enable external interrupt 6
IEN1.3	EX5	Enable external interrupt 5
IEN1.2	EX4	Enable external interrupt 4
IEN1.1	EX3	Enable external interrupt 3
IEN1.0	EX2	Enable external interrupt 2

where 0 = interrupt disabled
1 = interrupt enabled

Interrupt priority register IP0, IP1

IP0 (B8H)

-	-	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP0.7	-	Unused
IP0.6	-	Unused
IP0.5	PS1	Unused
IP0.4	PS0	UART SIO interrupt
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

IP1 (B8H)

PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Bit	Symbol	Function
IP1.7	PX9	External interrupt 9 priority level
IP1.6	PX8	External interrupt 8 priority level
IP1.5	PX7	External interrupt 7 priority level
IP1.4	PX6	External interrupt 6 priority level
IP1.3	PX5	External interrupt 5 priority level
IP1.2	PX4	External interrupt 4 priority level
IP1.1	PX3	External interrupt 3 priority level
IP1.0	PX2	External interrupt 2 priority level

Interrupt priority is as follows:
0 = low priority
1 = high priority

Interrupt polarity register IX1
IX1 (E9H)

IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Bit	Symbol	Function
IX1.7	IL9	External interrupt 9 polarity level
IX1.6	IL8	External interrupt 8 polarity level
IX1.5	IL7	External interrupt 7 polarity level
IX1.4	IL6	External interrupt 6 polarity level
IX1.3	IL5	External interrupt 5 polarity level
IX1.2	IL4	External interrupt 4 polarity level
IX1.1	IL3	External interrupt 3 polarity level
IX1.0	IL2	External interrupt 2 polarity level

Interrupt request flag register IRQ1
IRQ1 (C0H)

IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Bit	Symbol	Function
IRQ1.7	IQ9	External interrupt 9 request flag
IRQ1.6	IQ8	External interrupt 8 request flag
IRQ1.5	IQ7	External interrupt 7 request flag
IRQ1.4	IQ6	External interrupt 6 request flag
IRQ1.3	IQ5	External interrupt 5 request flag
IRQ1.2	IQ4	External interrupt 4 request flag
IRQ1.1	IQ3	External interrupt 3 request flag
IRQ1.0	IQ2	External interrupt 2 request flag

1.6.2 Interrupt Vectors

	Vector	Source
X0	0003H	External 0
S0	0023H	UART SIO
X5	0053H	External 5
T0	000BH	Timer 0
X6	005BH	External 6
X1	0013H	External 1
X2	003BH	External 2
X7	0063H	External 7
T1	001BH	Timer 1
X3	0043H	External 3
X8	006BH	External 8
X4	004BH	External 4
X9	0073H	External 9

Interrupt priority
Each interrupt priority source can be set to either high or low priority. If both priorities are requested simultaneously, the controller will branch to the high priority vector.

A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

1.6.3 Related registers
The following registers are used in conjunction with the interrupt system:

Register	Function
IX1	Interrupt polarity register
IRQ1	Interrupt enable register
IEN1	Interrupt enable register (INT2-INT9)
IP0	Interrupt priority register
IP1	Interrupt priority register (INT2-INT9)

1.7 Oscillator registers
The on-chip circuitry of the 80CL51 is a single-stage inverting amplifier biased by an internal feedback resistor (Figure 13). For operation as standard quartz oscillator, no external components are needed except at 32 KHz. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Figure 14 and oscillator options).

In the Power-down mode the oscillator is stopped XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at XTAL1. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Figure 14(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is split sing a flip-flop.

The following options are provided for optimum on-chip oscillator performance. Please state option when ordering.

1.7.1 Oscillator options (see Figure 14)
The following options are provided for optimum on-chip oscillator performance. Please state option when ordering.

Osc.1: Figure 14(c): An option for 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MQ bias resistor is needed for use in parallel with the crystal.

Osc. 2: Figure 14(e): An option for low-power, low-frequency operations using LC components.

Osc. 3: An option for medium frequency range applications.

Osc. 4: An option for high frequency range applications.

RC: Figure 14(g): An option for an RC oscillator.

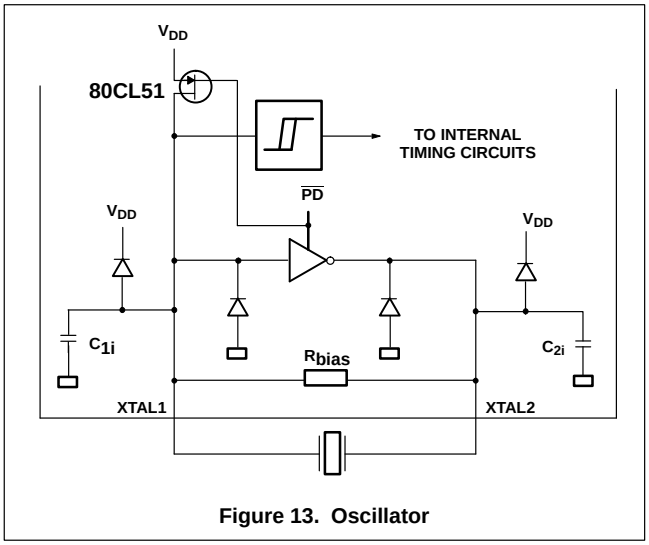


Figure 13. Oscillator

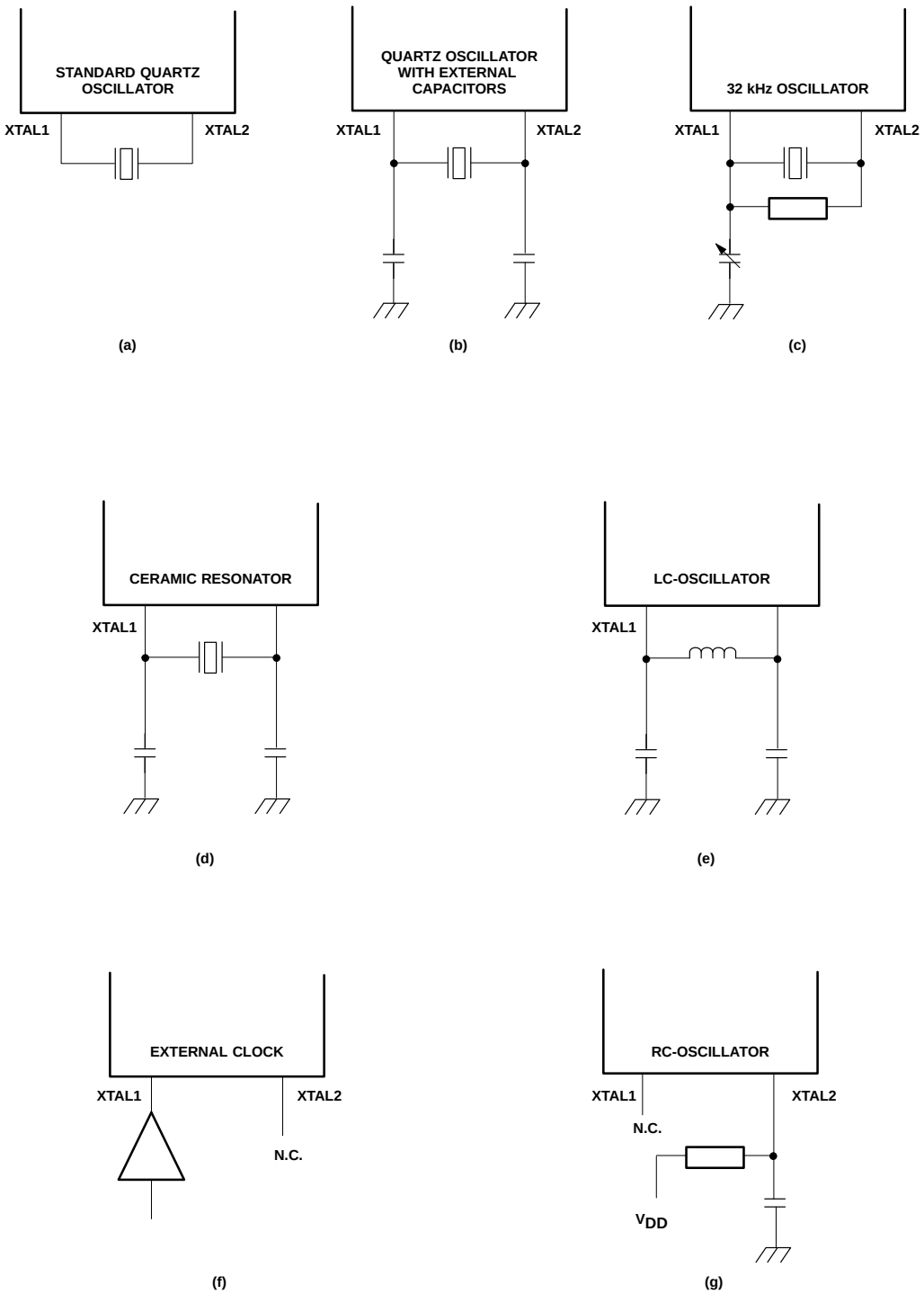


Figure 14. Alternative Oscillator Configurations

OSCILLATOR TYPE SELECTION GUIDE

RESONATOR	f(MHz)	OPTION	C1 EXT. (pF)		C2 EXT. (pF)		MAX. RESONATOR SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	OSC. 1	0	0	5	15	15 kΩ [1]
Quartz	1.0	OSC. 2	0	30	0	30	600 Ω
Quartz	3.58	OSC. 2	0	15	0	15	100 Ω
Quartz	4.0	OSC. 2	0	20	0	20	75 Ω
Quartz	6.0	OSC. 3	0	10	0	10	60 Ω
Quartz	10.0	OSC. 4	0	15	0	15	60 Ω
Quartz	12.0	OSC. 4	0	10	0	10	40 Ω
Quartz	16.0	OSC. 4	0	15	0	15	20 Ω
PXE	0.455	OSC. 2	40	50	40	50	10 Ω
PXE	1.0	OSC. 2	15	50	15	50	100 Ω
PXE	3.58	OSC. 2	0	40	0	40	10 Ω
PXE	4.0	OSC. 2	0	40	0	40	10 Ω
PXE	6.0	OSC. 2	0	20	0	20	5 Ω
PXE	10.0	OSC. 3	0	15	0	15	6 Ω
PXE	12.0	OSC. 4	10	40	10	40	6 Ω
LC		OSC. 2	20	90	20	90	10 µH = 1 Ω 100 µH = 5 Ω 1 mH = 75 Ω

NOTES:
1. 32 kHz quartz crystals with a series resistance higher than 15 kΩ will reduce the guaranteed supply voltage range to 2.5 -3.5V.
2. The equivalent circuit data of the internal oscillator compares with that of matched crystals.

OSCILLATOR EQUIVALENT CIRCUIT PARAMETERS (SEE FIGURE 15)

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	Transconductance	Osc.1	T = +25 °C; V_{DD} = 4.5V	-	15	-	µs
g_m		Osc.2	T = +25 °C; V_{DD} = 4.5V	200	600	1000	µs
g_m		Osc.3	T = +25 °C; V_{DD} = 4.5V	400	1500	4000	µs
g_m		Osc.4	T = +25 °C; V_{DD} = 4.5V	1000	4000	10000	µs
$C1_i$	Input Capacitance	Osc.1		-	3.0	-	pF
$C1_i$		Osc. 2		-	8.0	-	pF
$C1_i$		Osc. 3		-	8.0	-	pF
$C1_i$		Osc. 4		-	8.0	-	pF
$C2_i$	Output Capacitance	Osc.1		-	23	-	pF
$C2_i$		Osc. 2		-	8.0	-	pF
$C2_i$		Osc. 3		-	8.0	-	pF
$C2_i$		Osc. 4		-	8.0	-	pF
R2	Output Capacitance	Osc.1		-	3800	-	kΩ
R2		Osc. 2		-	65	-	kΩ
R2		Osc. 3		-	18	-	kΩ
R2		Osc. 4		-	5.0	-	kΩ

1.7.2 RC Oscillator (see Figure 16)

The externally adjustable RC-oscillator has a frequency range from 100 kHz to 500 kHz.

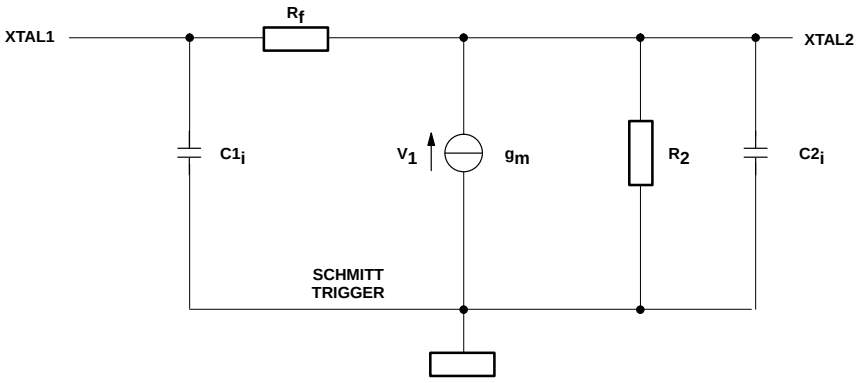


Figure 15. Equivalent Circuit Diagram

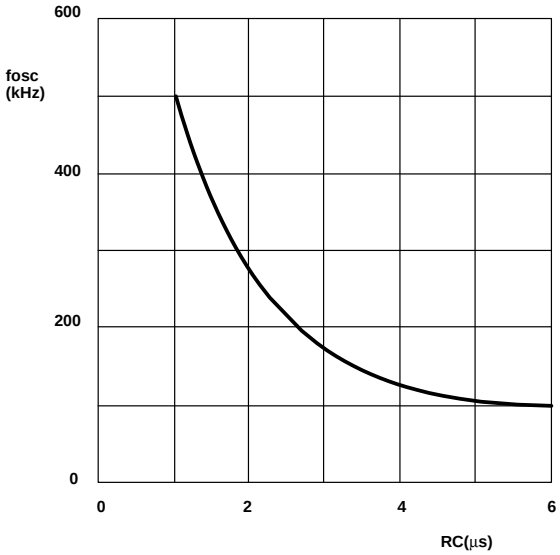


Figure 16. Frequency as a Function of RC

1.8 Reset Circuitry

To initialize the 80CL51, a reset is performed by either of two methods:

– via the RST pin

– via a power-on-reset

It leaves the internal registers as follows:

REGISTER	CONTENT
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IEN0	0000 0000
IEN1	0000 0000
IP0	XX00 0000
IP1	0000 0000
IX1	0000 0000
IRQ1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0XXX 0000
PSW	0000 0000
P0-P3	1111 1111
S0BUF	XXXX XXXX
S0CPN	0000 0000
SP	0000 0111
TCON	0000 0000
TH0, TH1	0000 0000
TL0, TH1	0000 0000
TL0, TL1	0000 0000
TMOD	0000 0000

The reset state of the port pins is mask- programmable and can therefore be defined by the user.

The standard reset value for port P0-P3 is 1111 1111.

The reset input to the 80CL51 is RST pin 9. A Schmitt trigger qualifies the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods), while the oscillator is running. The CPU responds by generating an internal reset. Port pins adopt their reset state immediately after RST goes HIGH. During reset ALE and PSEN are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during State 5, Phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated every cycle until RST goes LOW.

The internal RAM is not affected by reset. When V_{DD} is turned on the RAM contents are indeterminate.

1.8.1 Power-on reset

The 80CL51 contains on-chip circuitry which switch the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3V. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state.

A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation.

The on-chip Power-on circuitry can be switched off via the mask option “OFF”. This option reduces the power-down current to typically 800µA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset option, “OFF” should be chosen.

An automatic reset can be obtained at power-on by connecting the RST pin to V_{DD} via a 10µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor discharges through the internal resistor R_{RST} to ground. The larger the capacitor, the more slowly V_{RST} decreases V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

1.9 P80CL31: ROMless version of P80CL51

The P80CL31 is a low voltage ROMless version of the P80CL51 microcontroller. The mask options on the P80CL31 are fixed as follows:

- Port options: all ports have option “1S”, i.e., standard port, high after reset
- Oscillator option: OSC3
- Power-on Reset option: OFF

1.10 P80C51: 5V standard version

The P80C51 is a 5V version of the low voltage P80CL51 microcontroller. All functional features of the P80CL51 are maintained in the P80C51 with the exception of the mask options. The mask options on the P80C51 are as follows:

- Port options: all ports have option “1S”, i.e., standard port, high after reset.
- Oscillator options: OSC3
- Power-on Reset option: OFF

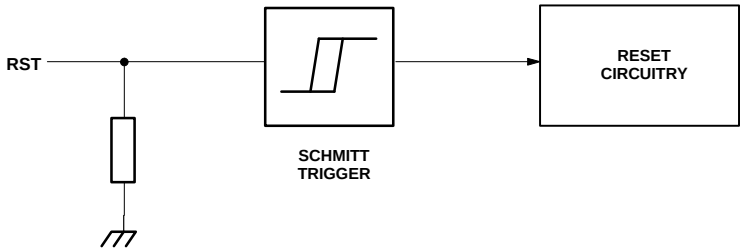


Figure 17. Reset Configuration at RST Pin

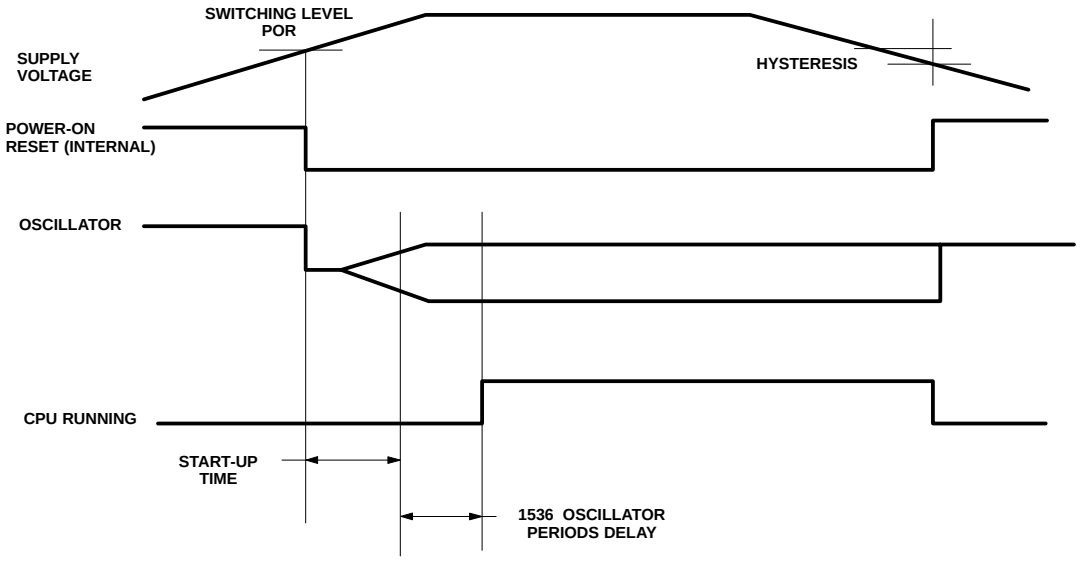


Figure 18. Power-on Reset Switching Level

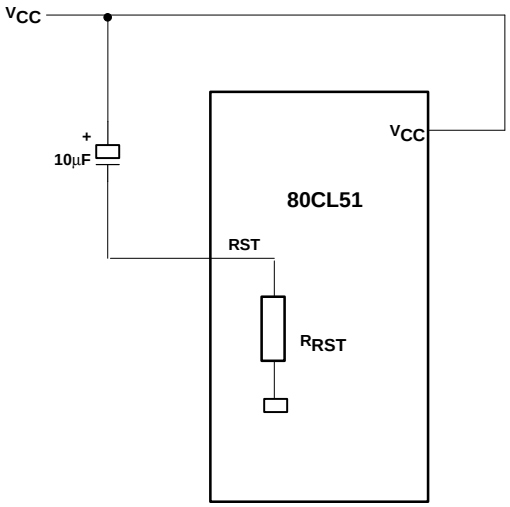


Figure 19. Recommended Power-on Reset Circuitry

2.0 RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage (pin 40)	-0.5	+ 6.5	V
V_I	All input voltages	-0.5	V_{DD}+0.5	V
I_I, I_O	DC current into any input or output	-	5	mA
P_{TOT}	Total power dissipation	-	300	mW
T_{STG}	Storage temperature range	-65	+150	°C
T_{AMB}	Operating ambient temperature range	-40	+85	°C
T_J	Operating junction temperature	-	125	°C

3.0 DC CHARACTERISTICS P80CL31/P80CL51

V_{SS} = 0V; T_{AMB} = -40 to +85°C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{SS} = 0V	1.8	-	6.0	V
V_{DD}	RAM retention in power down mode		1.0	–	–	V
Supply current operating (Note 1, Note 4)						
I_{DD}	OSC 1 option	f_{clk} = 32 KHz; V_{DD} = 1.8V T_{AMB} - 25°C	-	-	50	µA
I_{DD}	OSC 2 option	f_{clk} = 3.58 MHz; V_{DD} = 3V	-	-	2.5	mA
I_{DD}	OSC 3 option	f_{clk} = 16 MHz; V_{DD} = 5V	-	-	24	mA
I_{DD}	OSC 4 option	f_{clk} = 16 MHz; V_{DD} = 5V	-	-	26	mA
Idle Mode (Note 2, Note 4)						
I_{DD}	OSC 1 option	f_{clk} = 32 KHz; V_{DD} = 1.8V T_{AMB} = 25°C	-	-	25	µA
I_{DD}	OSC 2 option	f_{clk} = 3.58 MHz; V_{DD} = 3V	-	-	1.0	mA
I_{DD}	OSC 3 option	f_{clk} = 16 MHz; V_{DD} = 5V	-	-	10	mA
I_{DD}	OSC 4 option	f_{clk} = 16 MHz; V_{DD} = 5V	-	-	12	mA
I_{PD}	Power down (Note 3, Note 4)	V_{DD} = 1.8V, T_{AMB} = 25°C	-		10	µA
Inputs						
V_{IL}	Input voltage LOW		V_{SS}	-	0.3V_{DD}	V
V_{IH}	Input voltage HIGH		0.7V_{DD}	-	V_{DD}	V
I_{IL}	Input current logic 0 (Port 1, 2, 3)	V_{DD} = 5V, V_{IN} = 0.4V	-	-	100	µA
		V_{DD} = 2.5V, V_{IN} = 0.4V	-	-	50	µA
I_{TL}	Input current logic 1 to 0 transition (Port 1, 2, 3)	V_{DD} = 5V, V_{IN} = V_{DD}/2	-	-	1.0	mA
		V_{DD} = 2.5V, V_{IN} = V_{DD}/2	-	-	500	µA
+/I_{IL}	Input leakage current (Port 0, EA)	V_{SS} < V_I < V_{DD}	-	-	10	µA
Outputs						
I_{OL}	Output sink current LOW	V_{DD} = 5V, V_{OL} = 0.4V	1.6	-	-	mA
		V_{DD} = 2.5V, V_{OL} = 0.4V	0.7	-	-	mA
-I_{OH}	Output source current HIGH (push-pull options only)	V_{DD} = 5V; V_{OH} = V_{DD} -0.4V	1.6	-	-	mA
		V_{DD} = 2.5V; V_{OH} = V_{DD} -0.4V	0.7	-	-	mA
R_{RST}	RST pull-down resistor		10	–	200	kΩ

NOTES:

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS}; V_{IH} = V_{DD}; XTAL 2 not connected; EA = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS}. XTAL 2 not connected; EA = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL 1 not connected; EA = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
4. Circuits with Power-on Reset option “OFF” are tested at V_{DD} minimum = 1.8V; with option “ON” (typically 1.3V) they are tested at V_{DD} minimum = 2.3V. Please note, option “ON” is only available on P80CL51.

4.0 DC CHARACTERISTICS P80C51

V_{SS} = 0V; V_{DD} = 5V ± 10%; f_{clk} = 3.5 to 16MHz; T_{AMB} = -40 to +85°C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{SS} = 0V	4.5	-	5.5	V
Supply Current						
I_{DD}	Operating (Note 1)	f_{CLK} = 16MHz, V_{DD} = 5V	–	–	24	mA
I_{DD}	Idle mode (Note 2)	f_{CLK} = 16MHz, V_{DD} = 5V	–	–	10	mA
I_{PD}	Power down (Note 3)	V_{DD} = 5V	–	–	50	µA
Inputs						
V_{IL}	Input voltage LOW		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	Input current logic 0 (Port 1, 2, 3)	V_{IN} = 0.4V	–	–	100	µA
I_{IL}	Input current logic 1 to 0 transition (Port 1, 2, 3)	$V_{IN} = V_{DD}/2$	–	–	1.0	mA
I_{IL}	Input leakage current (Port 0, EA)	$V_{SS} < V_I < V_{DD}$	–	–	10	µA
Outputs						
I_{OL}	Output sink current LOW	V_{OL} = 0.4V	1.6	–	–	mA
I_{OH}	Output source current HIGH (push-pull options only)	$V_{OH} = V_{DD} – 0.4V$	1.6	–	–	mA
R_{RST}	RST pull-down resistor		10	–	200	kΩ

NOTES:

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_R = t_F$ = 10ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL 2 not connected; EA = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_R = t_F$ = 10ns; $V_{IL} = V_{SS}$. XTAL 2 not connected; EA = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL 1 not connected; EA = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
4. Please note, option “ON” is only available on P80CL51.

5.0 AC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0V; T_{amb} = -40 to +85°C; C_L = 50 pF for Port 0, ALE and PSEN; C_L = 40pF for all other outputs, unless otherwise specified.

PROGRAM MEMORY (See Figure 20)

SYMBOL	PARAMETER			VARIABLE CLOCK	
		MIN.	TYP.	MAX.	UNIT
t_{LL}	ALE pulse duration	$2T_{CK}$-40	-	-	ns
t_{AL}	Address set-up time to ALE	T_{CK}-40	-	-	ns
t_{LA}	Address hold time to ALE	T_{CK}-35	-	-	ns
t_{LC}	Time from ALE to control pulse PSEN	T_{CK}-25	-	-	ns
t_{LIV}	Time from ALE to valid instruction input	-	-	$4T_{CK}$-100	ns
t_{CC}	Control pulse duration PSEN	$3T_{CK}$-35	-	-	ns
t_{CIV}	Time from PSEN to valid instruction input	-	-	$3T_{CK}$-125	ns
t_{CI}	Input instruction hold time after PSEN	0	-	-	ns
t_{CIF}	Input instruction float delay after PSEN	-	-	T_{CK}-20	ns
t_{AIV}	Address to valid instruction input	-	-	$5T_{CK}$-115	ns
t_{AFC}	Address float time to PSEN	0	-	-	ns

EXTERNAL DATA MEMORY (See Figures 21 and 22)

SYMBOL	PARAMETER			VARIABLE CLOCK	
		MIN.	TYP.	MAX.	UNIT
t_{RR}	RD pulse duration	$6T_{CK}$-100	-	-	ns
t_{WW}	WR pulse duration	$6T_{CK}$-100	-	-	ns
t_{LA}	Address hold time after ALE	T_{CK}-35	-	-	ns
t_{RD}	RD to valid data input	T_{CK}-35	-	$5T_{CK}$-165	ns
t_{DFR}	Data float delay after RD	-	-	$2T_{CK}$-70	ns
t_{LD}	Time from ALE to valid data input	-	-	$8T_{CK}$-150	ns
t_{AD}	Address to valid data input	-	-	$9T_{CK}$-165	ns
t_{LW}	Time from ALE to RD and WR	$3T_{CK}$-50	-	$3T_{CK}$+50	ns
t_{AW}	Time from address to RD and WR	$4T_{CK}$-130	-	-	ns
t_{WHLH}	Time from RD or WR HIGH to ALE HIGH	T_{CK}-40	-	T_{CK}-40	ns
t_{DWX}	Data valid to WR transition	T_{CK}-60	-	-	ns
t_{DW}	Data set-up time before WR	T_{CK}-150	-	-	ns
t_{WD}	Data hold time after WR	T_{CK}-50	-	-	ns
t_{WAFR}	Address float delay after RD (Note 1)	-	-	12	ns

NOTE:
1. Interfacing the 80CL51 or P80C51 to devices with float times up to 75ns is permitted. This limited bus connection will not cause damage to Port 0 drivers.

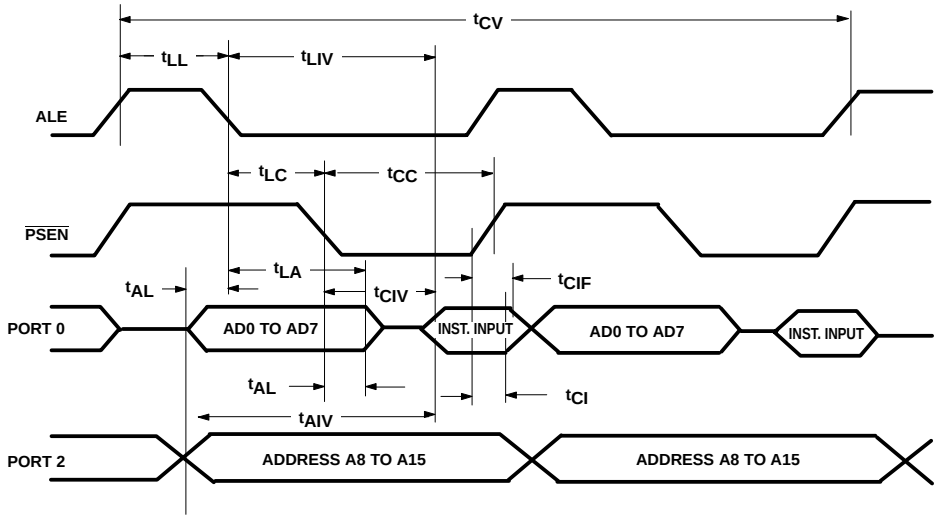


Figure 20. Read from Program Memory

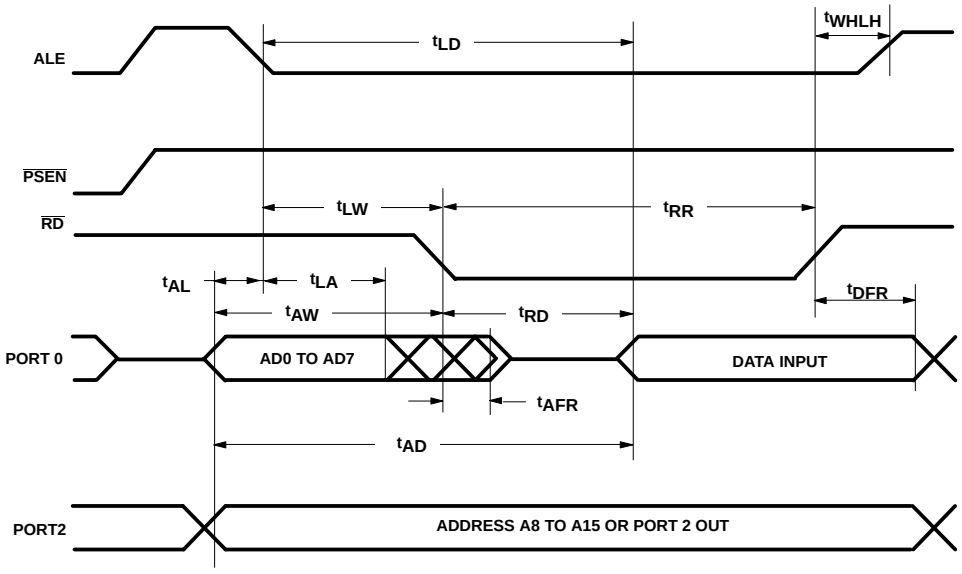


Figure 21. Read from Data Memory

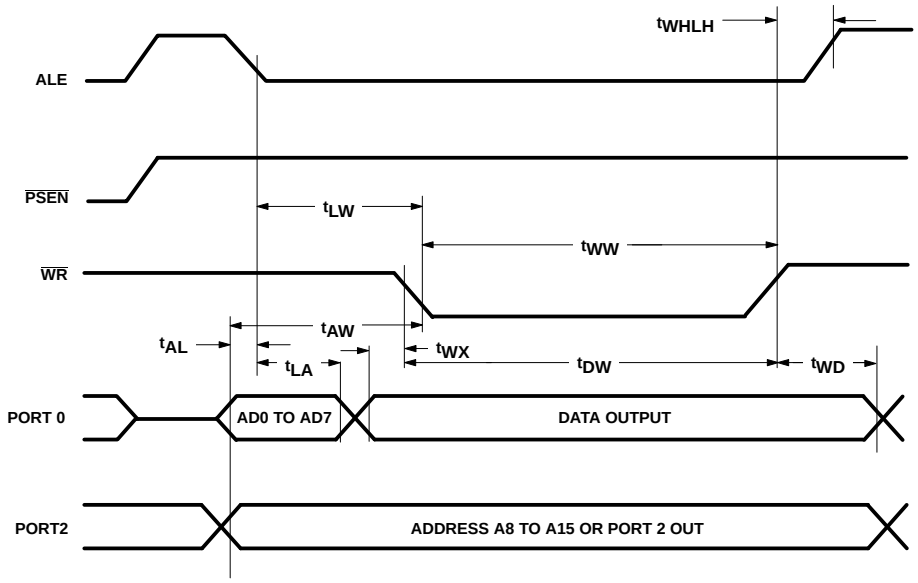


Figure 22. Write to Data Memory

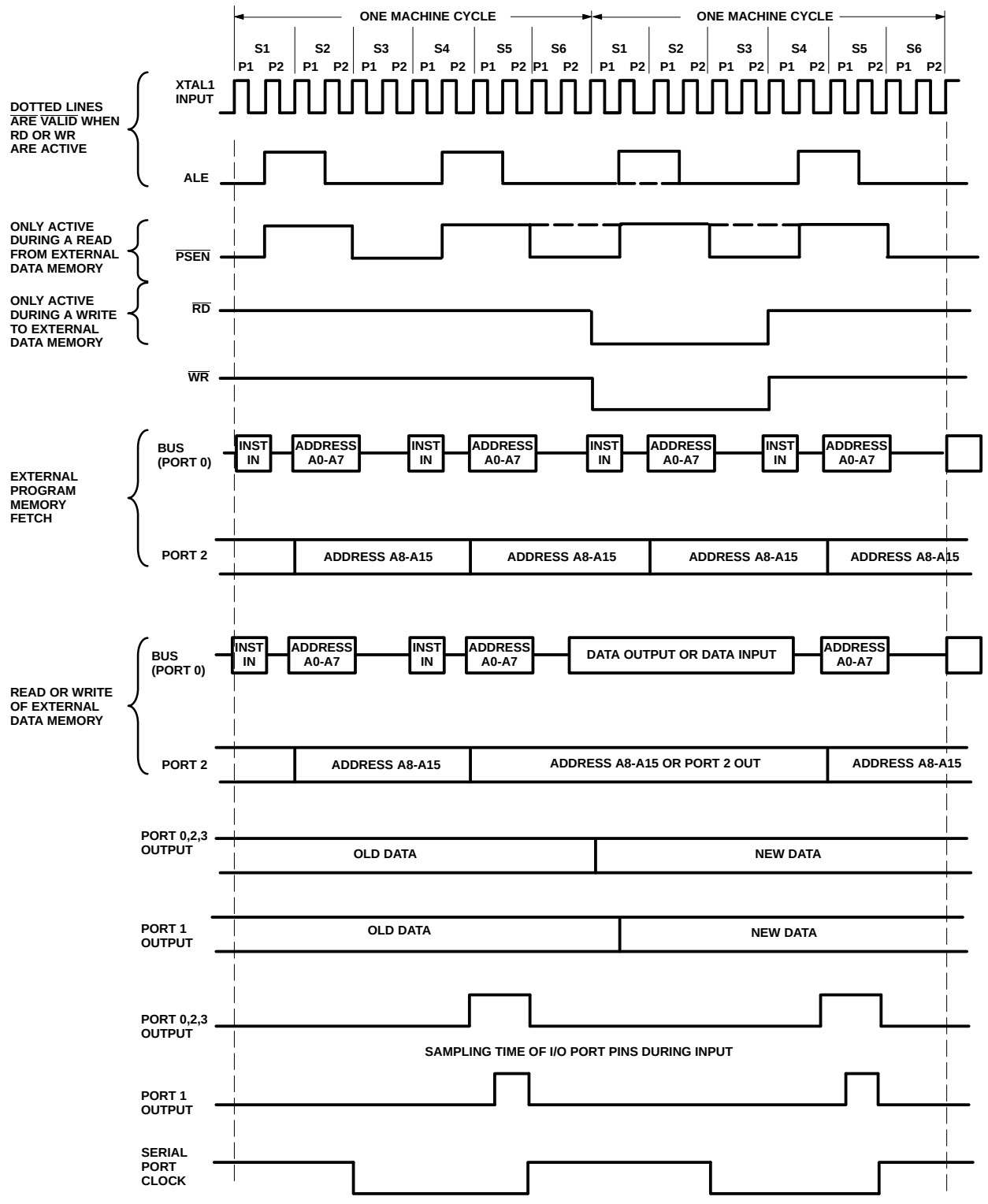


Figure 23. Instruction Cycle Timing

6.0 CHARACTERISTICS CURVES

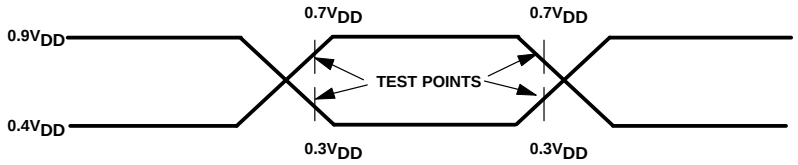


Figure 24. AC Testing Input Waveform

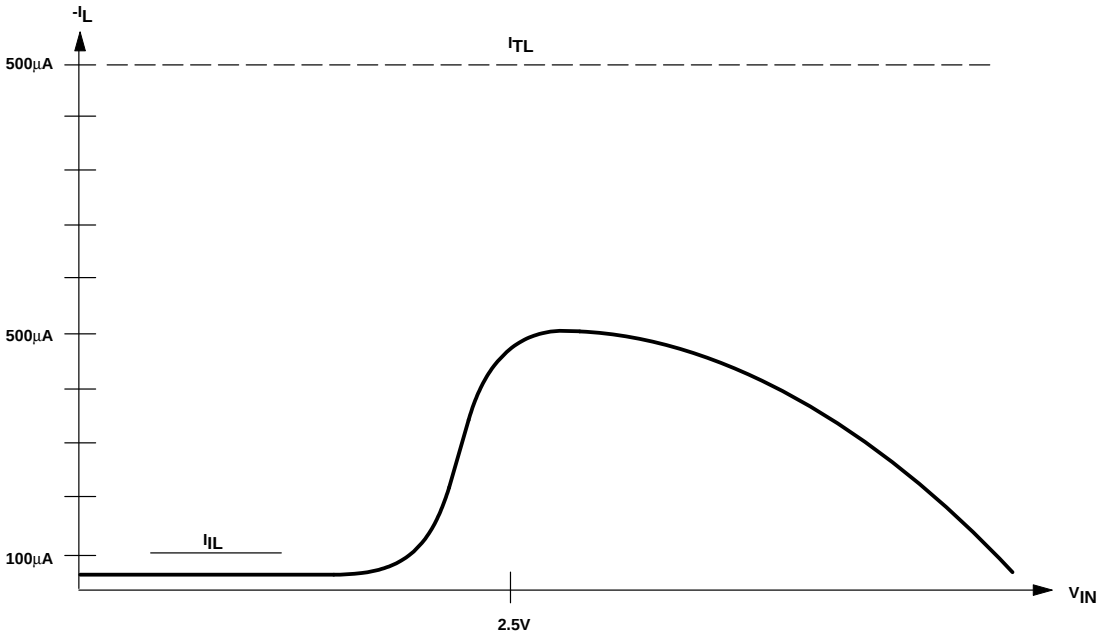


Figure 25. Input Current at V_{DD} = 5V

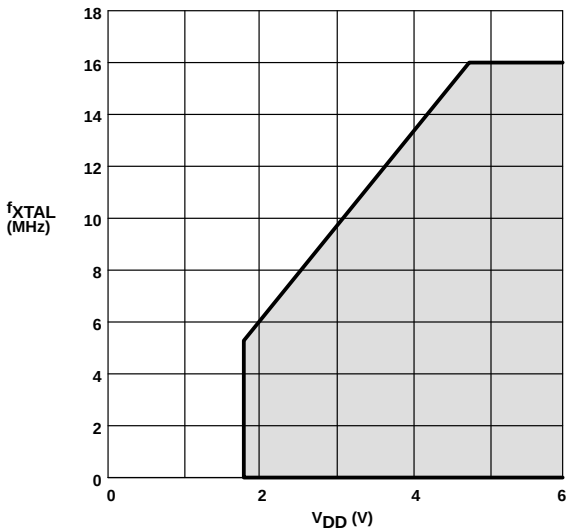


Figure 26. P80CL51/31 Frequency Operating Range

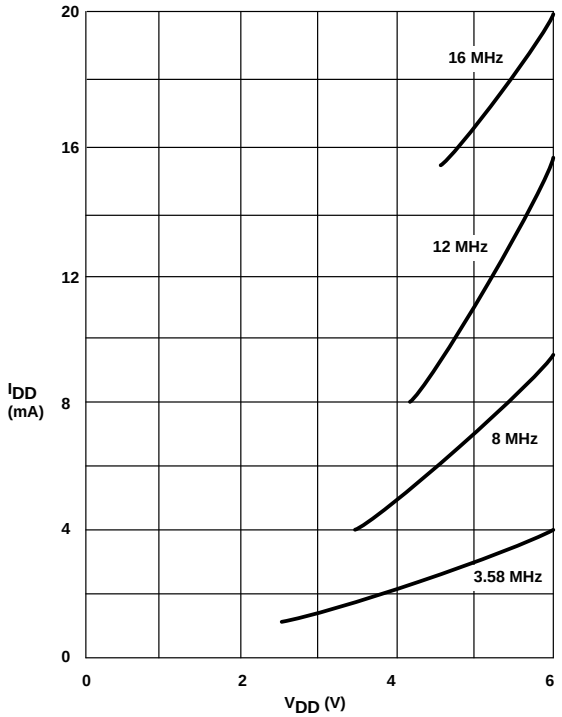


Figure 27. P80CL51/31 Typical Operating Current vs Frequency and V_{DD}, T_{amb} = 25°C.

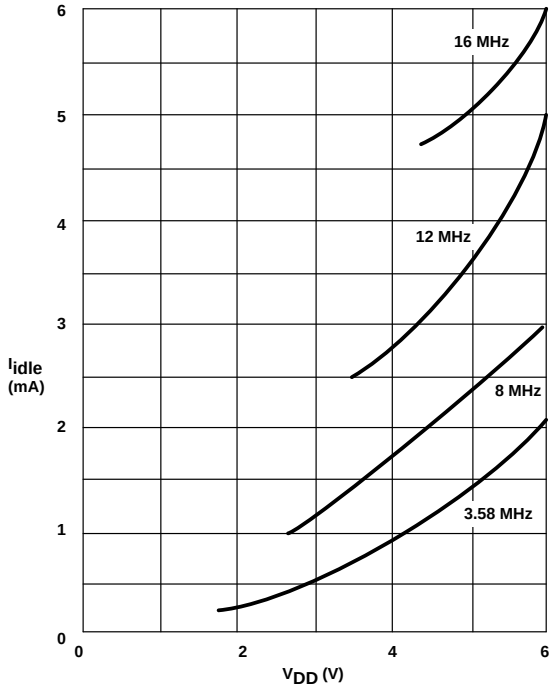


Figure 28. P80CL51/31 Typical Idle Current vs Frequency and V_{DD}, T_{amb} = 25°C.

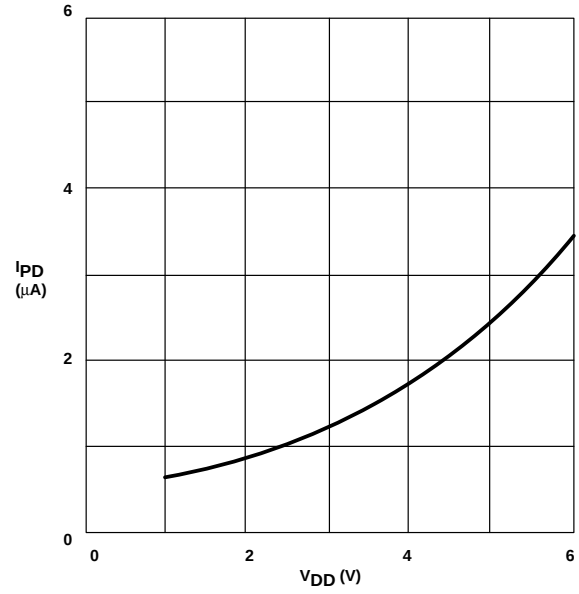
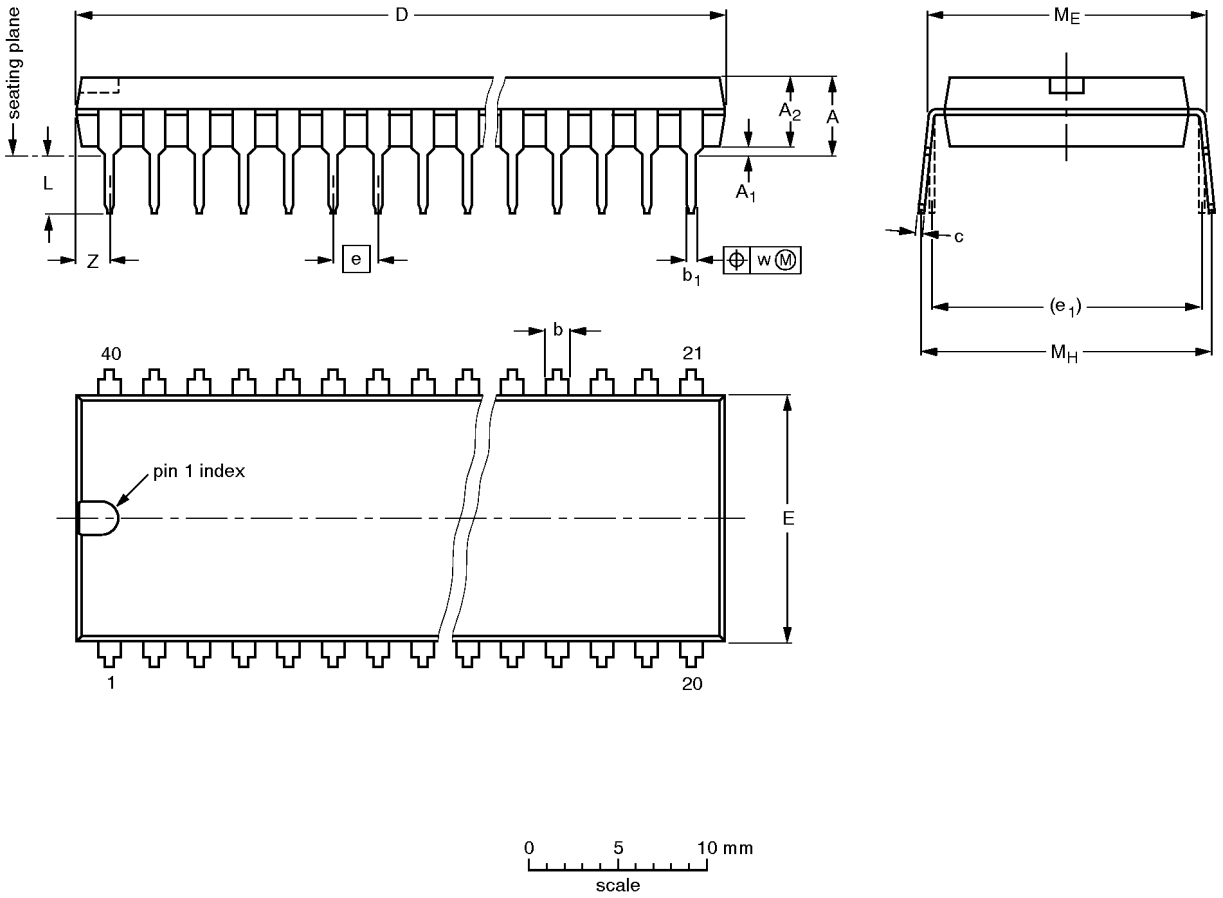


Figure 29. P80CL51/31 Typical Power-Down Current vs Frequency and V_{DD}, T_{amb} = 25°C.

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

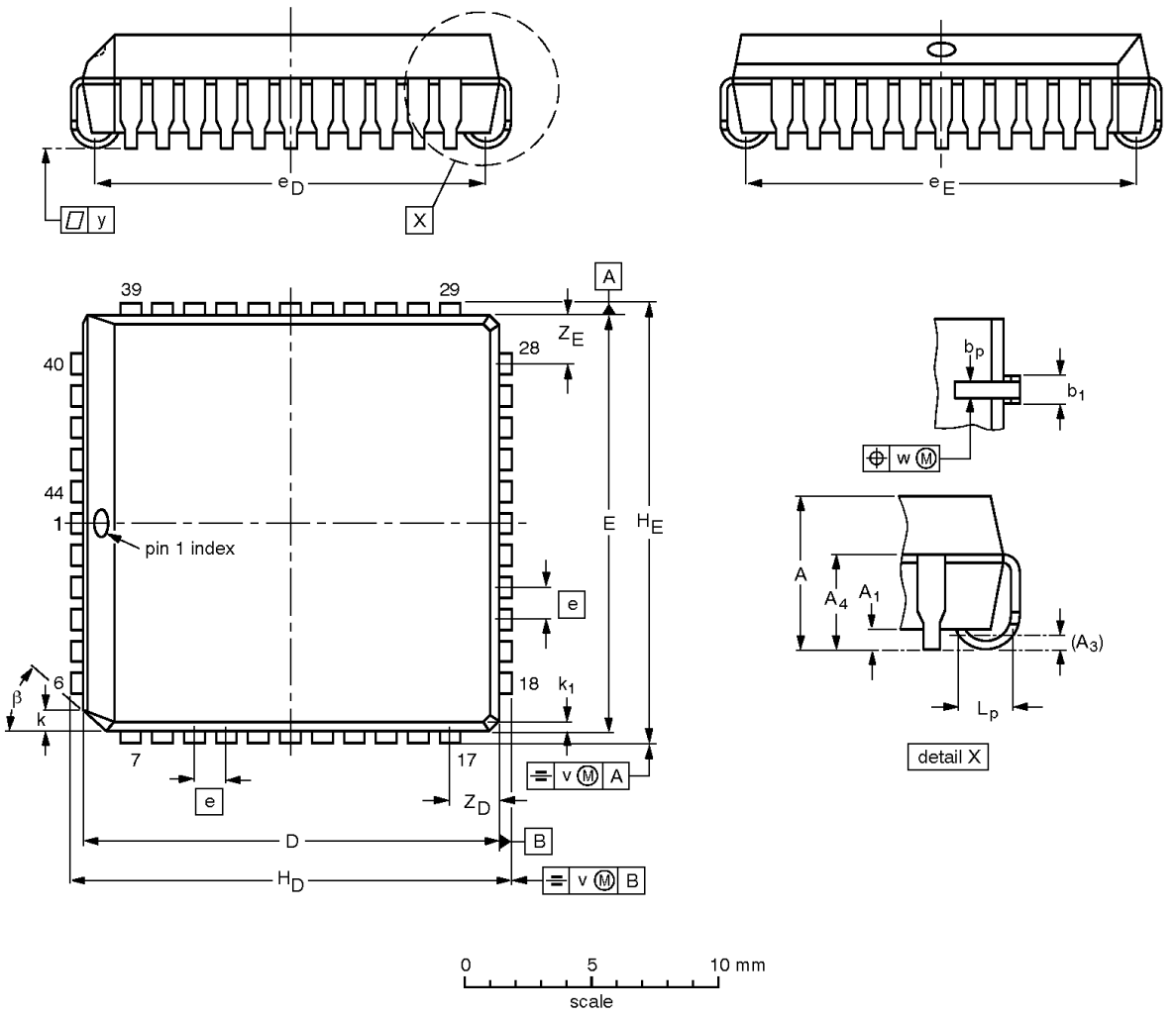
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

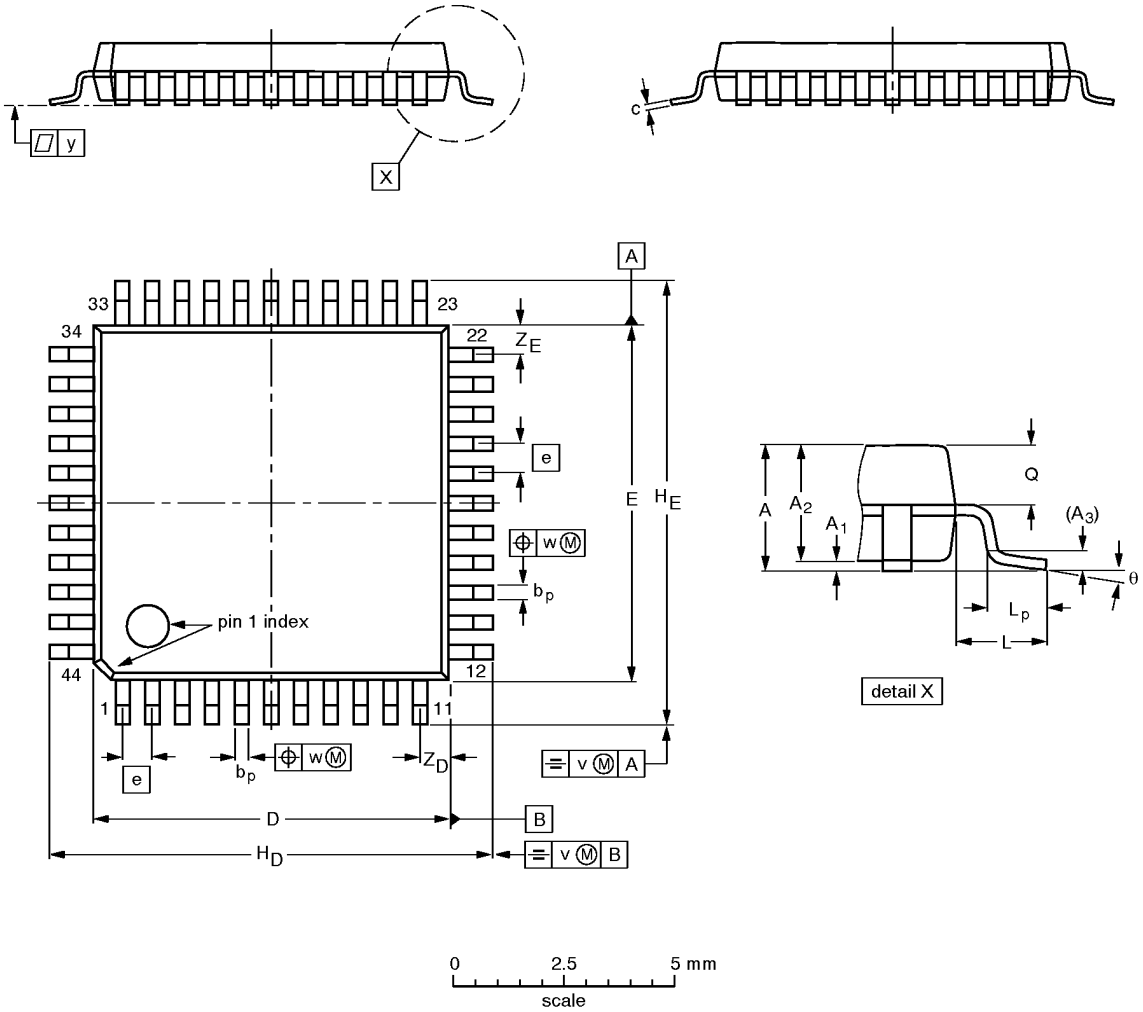
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

NOTES

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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