82439TX System Controller (MTXC)

SmartDie® Product Specification

- **Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3 V and 2.5 V**
- **PCI 2.1 Compliant**
- **Integrated Data Path**
- **Integrated DRAM Controller**
  - **— 4 Mbytes to 256 Mbytes Main Memory**
  - **— 64-Mbit DRAM/SRAM Technology Support**
  - **— FPM (Fast Page Mode), EDO, and SDRAM DRAM support**
  - **— 6 RAS Lines Available**
  - **— Integrated Programmable Strength for DRAM Interface**
  - **— CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO**
  - **— CAS-Before-RAS and Self Refresh for SDRAM**
- **Integrated L2 Cache Controller**
  - **— 64 Mbyte DRAM Cacheability**
  - **— Direct Mapped Organization–Write Back Only**
  - **— Supports 256 Kbyte and 512 Kbyte Pipelined Burst SRAM and DRAM Cache**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1**
  - **— Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1**
  - **— 64 K x 32 SRAM Also Supported**
- **Fully Synchronous, Minimum Latency 30/33 MHz PCI Bus Interface**
  - **— Five PCI Bus Masters (Including PIIX4)**
  - **— 10 DWord PCI-to-DRAM Read Prefetch Buffer**
  - **— 18 Dword PCI-DRAM Post Buffer**
  - **— Multi-Transaction Timer to Support Multiple Short PCI Transactions**
- **Power Management**
  - **— PCI CLKRUN# Support**
  - **— Dynamic Stop Clock Support**
  - **— Suspend to RAM (STR)**
  - **— Suspend to Disk (STD)**
  - **— Power On Suspend (POS)**
  - **— Internal Clock Control**
  - **— SDRAM and EDO Self Refresh During Suspend**
  - **— ACPI Support**
  - **— Compatible SMRAM (C-SMRAM) and Extended SMRAM (E-SMRAM)**
  - **— SMM Write-Back Cacheable in E_SMRAM Mode up to 1 Mbyte**
  - **— 3.3/5 V DRAM, 3.3/5 V PCI, 3.3/5 V Tag, and 3.3/2.5 V SRAM Support**
- **Test Features**
  - **— NAND Tree Support for All Pins**
- **Supports the Universal Serial Bus (USB)**
- **Intel SmartDie® Product**
  - **— Full AC/DC Testing at Die Level**
  - **— 0°C to 105°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 16. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please refer to the standard package datasheet (order number 290559) for product information and specifications not found in this document.

August 1997 **Order Number:** 273005-002

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation

P.O. Box 7641

Mt. Prospect IL 60056-764

or call 1-800-548-4725

82439TX System Controller (MTXC)

SmartDie® Product Specification

1.0 DIE SPECIFICATIONS

The die photo in Figure 1 and the plot in Figure 2 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "88TX1A" appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

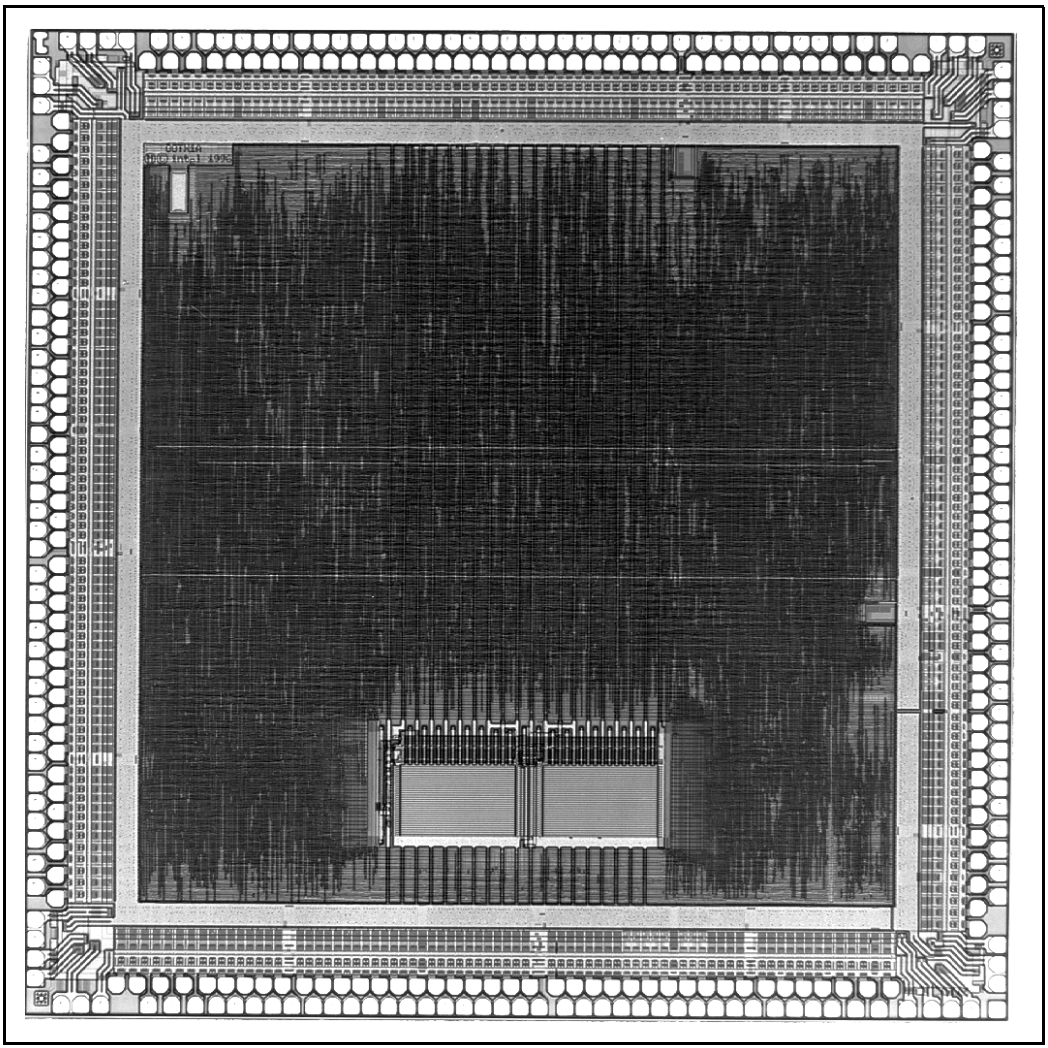


Figure 1. 82439TX System Controller Die Photo

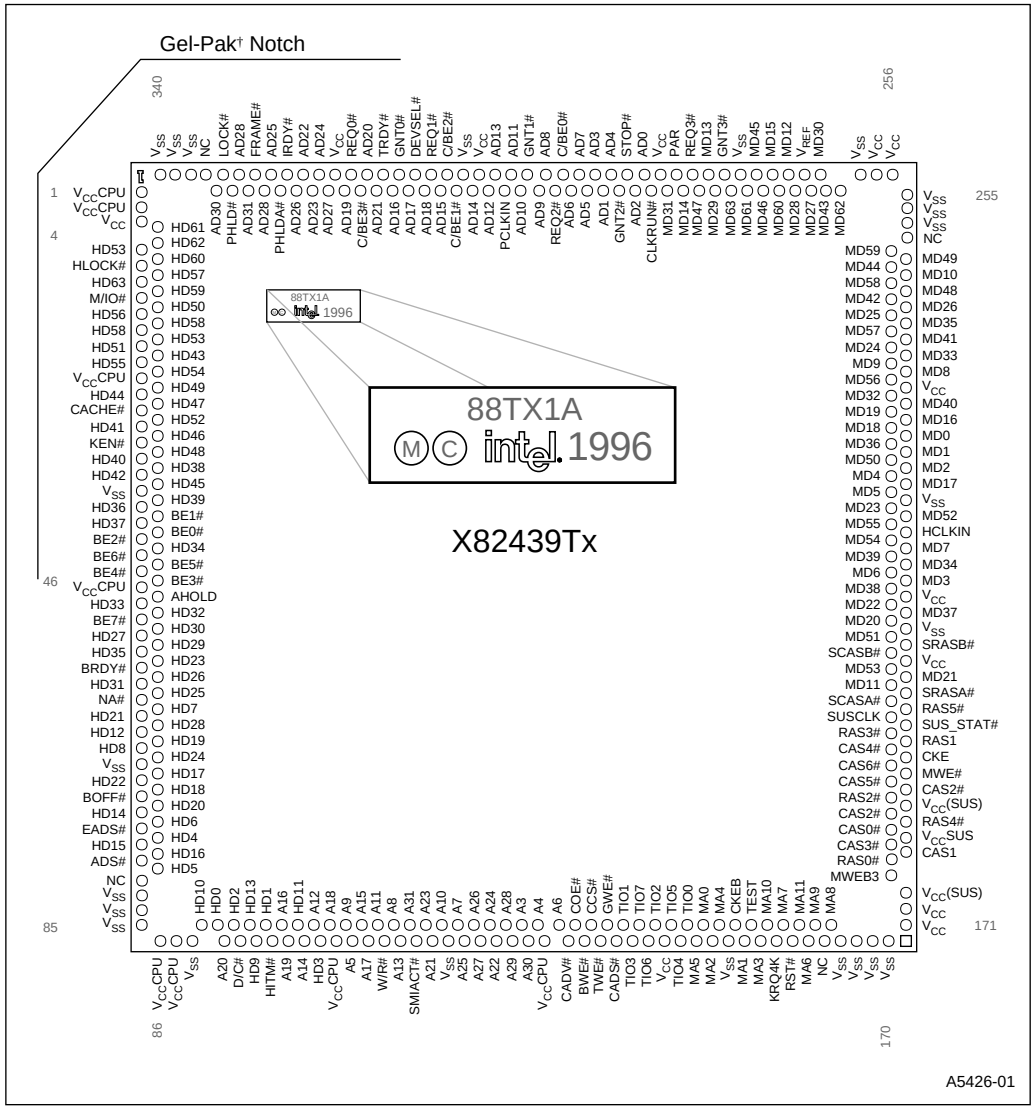


Figure 2. 82439TX System Controller Die/Bond Pad Layout

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 1 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
1	V_{CC}CPU	-120.93	115.16	-3072.20	2925.81
2	V_{CC}CPU	-120.93	110.23	-3072.20	2800.41
3	V_{CC}	-120.93	105.29	-3072.20	2675.01
4	HD61	-115.94	101.29	-2945.57	2573.36
5	HD62	-115.94	96.05	-2945.57	2440.07
6	HD53	-120.93	93.09	-3072.20	2365.02
7	HD60	-115.94	90.14	-2945.57	2289.97
8	HLOCK#	-120.93	87.18	-3072.20	2214.92
9	HD57	-115.94	84.23	-2945.57	2139.87
10	HD63	-120.93	81.27	-3072.20	2064.82
11	HD59	-115.94	78.32	-2945.57	1989.77
12	M/IO#	-120.93	75.96	-3072.20	1929.73
13	HD50	-115.94	73.59	-2945.57	1869.69
14	HD56	-120.93	71.23	-3072.20	1809.65
15	HD58	-115.94	68.87	-2945.57	1749.61
16	HD51	-120.93	66.50	-3072.20	1689.57
17	HD43	-115.94	64.14	-2945.57	1629.53
18	HD55	-120.93	61.78	-3072.20	1569.49
19	HD54	-115.94	59.41	-2945.57	1509.45
20	V_{CC}CPU	-120.93	57.04	-3072.20	1449.03
21	HD49	-115.94	53.90	-2945.57	1369.33
22	HD44	-120.93	51.54	-3072.20	1309.29
23	HD47	-115.94	49.17	-2945.57	1249.25
24	CACHE#	-120.93	46.81	-3072.20	1189.21
25	HD52	-115.94	44.45	-2945.57	1129.17
26	HD41	-120.93	41.44	-3072.20	1052.79
27	HD46	-115.94	39.08	-2945.57	992.75
28	KEN#	-120.93	36.71	-3072.20	932.71
29	HD48	-115.94	34.35	-2945.57	872.67
30	HD40	-120.93	31.99	-3072.20	812.63
31	HD38	-115.94	29.62	-2945.57	752.59

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 2 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
32	HD42	-120.93	27.26	-3072.20	692.55
33	HD45	-115.94	24.90	-2945.57	632.51
34	V_{SS}	-120.93	22.14	-3072.20	562.49
35	HD39	-115.94	19.38	-2945.57	492.48
36	HD36	-120.93	17.02	-3072.20	432.44
37	BE1#	-115.94	14.66	-2945.57	372.40
38	HD37	-120.93	12.30	-3072.20	312.36
39	BE0#	-115.94	9.93	-2945.57	252.32
40	BE2#	-120.93	7.57	-3072.20	192.28
41	HD34	-115.94	5.21	-2945.57	132.24
42	BE6#	-120.93	2.84	-3072.20	72.20
43	BE5#	-115.94	0.48	-2945.57	12.16
44	BE4#	-120.93	-1.88	-3072.20	-47.88
45	BE3#	-115.94	-4.25	-2945.57	-107.92
46	V_{CC}CPU	-120.93	-6.61	-3072.20	-167.96
47	AHOLD	-115.94	-10.80	-2945.57	-274.36
48	HD33	-120.93	-13.16	-3072.20	-334.40
49	HD32	-115.94	-15.53	-2945.57	-394.44
50	BE7#	-120.93	-17.89	-3072.20	-454.48
51	HD30	-115.94	-20.25	-2945.57	-514.52
52	HD27	-120.93	-22.62	-3072.20	-574.56
53	HD29	-115.94	-24.98	-2945.57	-634.60
54	HD35	-120.93	-27.34	-3072.20	-694.64
55	HD23	-115.94	-29.71	-2945.57	-754.68
56	BRDY#	-120.93	-32.07	-3072.20	-814.72
57	HD26	-115.94	-34.43	-2945.57	-874.76
58	HD31	-120.93	-36.80	-3072.20	-934.80
59	HD25	-115.94	-39.16	-2945.57	-994.84
60	NA#	-120.93	-41.52	-3072.20	-1054.88
61	HD7	-115.94	-43.89	-2945.57	-1114.92
62	HD21	-120.93	-46.25	-3072.20	-1174.96
63	HD28	-115.94	-48.61	-2945.57	-1235.00

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 3 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
64	HD12	-120.93	-50.97	-3072.20	-1295.04
65	HD19	-115.94	-53.34	-2945.57	-1355.08
66	HD8	-120.93	-55.70	-3072.20	-1415.12
67	HD24	-115.94	-58.06	-2945.57	-1475.16
68	V_{SS}	-120.93	-60.44	-3072.20	-1535.58
69	HD17	-115.94	-63.58	-2945.57	-1615.28
70	HD22	-120.93	-65.94	-3072.20	-1675.32
71	HD18	-115.94	-68.31	-2945.57	-1735.36
72	BOFF#	-120.93	-70.67	-3072.20	-1795.40
73	HD20	-115.94	-73.03	-2945.57	-1855.44
74	HD14	-120.93	-75.40	-3072.20	-1915.48
75	HD6	-115.94	-77.76	-2945.57	-1975.52
76	EADS#	-120.93	-80.12	-3072.20	-2035.56
77	HD4	-115.94	-83.08	-2945.57	-2110.61
78	HD15	-120.93	-86.03	-3072.20	-2185.66
79	HD16	-115.94	-88.99	-2945.57	-2260.71
80	ADS#	-120.93	-91.94	-3072.20	-2335.76
81	HD5	-115.94	-94.89	-2945.57	-2410.81
82	NC	-120.93	-100.22	-3072.20	-2546.14
83	V_{SS}	-120.93	-105.16	-3072.20	-2671.54
84	V_{SS}	-120.93	-110.09	-3072.20	-2796.94
85	V_{SS}	-120.93	-115.01	-3072.20	-2921.77
86	V_{CC}CPU	-114.46	-121.63	-2907.85	-3090.16
87	V_{CC}CPU	-109.52	-121.63	-2782.45	-3090.16
88	V_{SS}	-104.59	-121.63	-2657.05	-3090.16
89	HD10	-100.58	-116.65	-2555.40	-2963.52
90	HD0	-95.34	-116.65	-2422.12	-2963.52
91	A20	-92.38	-121.63	-2347.07	-3090.16
92	HD2	-89.43	-116.65	-2272.02	-2963.52
93	D/C#	-86.48	-121.63	-2196.97	-3090.16
94	HD13	-83.52	-116.65	-2121.92	-2963.52
95	HD9	-80.57	-121.63	-2046.87	-3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 4 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
96	HD1	-77.61	-116.65	-1971.82	-2963.52
97	HITM#	-75.25	-121.63	-1911.78	-3090.16
98	A16	-72.89	-116.65	-1851.74	-2963.52
99	A19	-70.52	-121.63	-1791.70	-3090.16
100	HD11	-68.16	-116.65	-1731.66	-2963.52
101	A14	-65.80	-121.63	-1671.62	-3090.16
102	A12	-63.43	-116.65	-1611.58	-2963.52
103	HD3	-61.07	-121.63	-1551.54	-3090.16
104	A18	-58.71	-116.65	-1491.50	-2963.52
105	V_{CC}CPU	-56.33	-121.63	-1431.08	-3090.16
106	A9	-53.19	-116.65	-1351.37	-2963.52
107	A5	-50.83	-121.63	-1291.33	-3090.16
108	A15	-48.47	-116.65	-1231.29	-2963.52
109	A17	-46.10	-121.63	-1171.25	-3090.16
110	A11	-43.74	-116.65	-1111.21	-2963.52
111	W/R#	-41.38	-121.63	-1051.17	-3090.16
112	A8	-39.01	-116.65	-991.13	-2963.52
113	A13	-36.65	-121.63	-931.09	-3090.16
114	A31	-34.29	-116.65	-871.05	-2963.52
115	SMIACT#	-31.92	-121.63	-811.01	-3090.16
116	A23	-29.56	-116.65	-750.97	-2963.52
117	A21	-27.20	-121.63	-690.93	-3090.16
118	A10	-24.83	-116.65	-630.89	-2963.52
119	V_{SS}	-22.47	-121.63	-570.85	-3090.16
120	A7	-20.11	-116.65	-510.81	-2963.52
121	A25	-17.74	-121.63	-450.77	-3090.16
122	A26	-15.38	-116.65	-390.73	-2963.52
123	A27	-13.02	-121.63	-330.69	-3090.16
124	A24	-10.65	-116.65	-270.65	-2963.52
125	A22	-8.29	-121.63	-210.61	-3090.16
126	A28	-5.93	-116.65	-150.57	-2963.52
127	A29	-3.56	-121.63	-90.53	-3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 5 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
128	A3	-1.20	-116.65	-30.49	-2963.52
129	A30	1.16	-121.63	29.54	-3090.16
130	A4	3.53	-116.65	89.58	-2963.52
131	V_{CC}CPU	5.89	-121.63	149.62	-3090.16
132	A6	10.08	-116.65	256.02	-2963.52
133	CADV#	12.44	-121.63	316.06	-3090.16
134	COE#	14.80	-116.65	376.10	-2963.52
135	BWE#	17.17	-121.63	436.14	-3090.16
136	CCS#	19.53	-116.65	496.18	-2963.52
137	TWE#	21.89	-121.63	556.22	-3090.16
138	GWE#	24.26	-116.65	616.26	-2963.52
139	CADS#	26.62	-121.63	676.30	-3090.16
140	TIO1	28.98	-116.65	736.34	-2963.52
141	TIO3	31.35	-121.63	796.38	-3090.16
142	TIO7	33.71	-116.65	856.42	-2963.52
143	TIO6	36.07	-121.63	916.46	-3090.16
144	TIO2	38.44	-116.65	976.50	-2963.52
145	V_{CC}	40.80	-121.63	1036.54	-3090.16
146	TIO5	43.16	-116.65	1096.58	-2963.52
147	TIO4	45.53	-121.63	1156.62	-3090.16
148	TIO0	47.89	-116.65	1216.66	-2963.52
149	MA5	50.25	-121.63	1276.70	-3090.16
150	MA0	52.62	-116.65	1336.74	-2963.52
151	MA2	54.98	-121.63	1396.78	-3090.16
152	MA4	57.34	-116.65	1456.82	-2963.52
153	V_{SS}	59.72	-121.63	1517.24	-3090.16
154	CKEB	62.86	-116.65	1596.95	-2963.52
155	MA1	65.22	-121.63	1656.99	-3090.16
156	TEST	67.59	-116.65	1717.03	-2963.52
157	MA3	69.95	-121.63	1777.07	-3090.16
158	MA10	72.31	-116.65	1837.11	-2963.52
159	KRQAK	74.68	-121.63	1897.15	-3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 6 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
160	MA7	77.04	-116.65	1957.19	-2963.52
161	RST#	79.40	-121.63	2017.23	-3090.16
162	MA11	82.36	-116.65	2092.28	-2963.52
163	MA6	85.31	-121.63	2167.33	-3090.16
164	MA9	88.26	-116.65	2242.38	-2963.52
165	NC	91.22	-121.63	2317.43	-3090.16
166	MA8	94.17	-116.65	2392.48	-2963.52
167	V_{SS}	98.39	-121.63	2499.69	-3090.16
168	V_{SS}	104.45	-121.63	2653.59	-3090.16
169	V_{SS}	109.39	-121.63	2778.99	-3090.16
170	V_{SS}	114.30	-121.63	2903.82	-3090.16
171	V_{CC}	120.93	-115.16	3072.20	-2925.81
172	V_{CC}	120.93	-110.23	3072.20	-2800.41
173	V_{CC}(SUS)	120.93	-105.29	3072.20	-2675.01
174	MWEB#	115.94	-101.29	2945.57	-2573.36
175	RAS0#	115.94	-96.05	2945.57	-2440.07
176	CAS1#	120.93	-93.09	3072.20	-2365.02
177	CAS3#	115.94	-90.14	2945.57	-2289.97
178	V_{CC}(SUS)	120.93	-87.18	3072.20	-2214.92
179	CAS0#	115.94	-84.23	2945.57	-2139.87
180	RAS4#	120.93	-81.27	3072.20	-2064.82
181	CAS2#	115.94	-78.32	2945.57	-1989.77
182	V_{CC}(SUS)	120.93	-75.96	3072.20	-1929.73
183	RAS2#	115.94	-72.82	2945.57	-1850.03
184	CAS7#	120.93	-70.46	3072.20	-1789.99
185	CAS5#	115.94	-68.09	2945.57	-1729.95
186	MWE#	120.93	-65.73	3072.20	-1669.91
187	CAS6#	115.94	-63.37	2945.57	-1609.87
188	CKE	120.93	-61.00	3072.20	-1549.83
189	CAS4#	115.94	-58.64	2945.57	-1489.79
190	RAS1#	120.93	-56.28	3072.20	-1429.75
191	RAS3#	115.94	-53.91	2945.57	-1369.71

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 7 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
192	SUS_STAT1#	120.93	-51.55	3072.20	-1309.67
193	SUSCLK	115.94	-49.19	2945.57	-1249.63
194	RAS5#	120.93	-46.82	3072.20	-1189.59
195	SCASA#	115.94	-43.80	2945.57	-1112.83
196	SRASA#	120.93	-41.44	3072.20	-1052.79
197	MD11	115.94	-39.08	2945.57	-992.75
198	MD21	120.93	-36.71	3072.20	-932.71
199	MD53	115.94	-34.35	2945.57	-872.67
200	V_{CC}	120.93	-31.59	3072.20	-802.65
201	SCASB#	115.94	-28.84	2945.57	-732.64
202	SRASB#	120.93	-26.47	3072.20	-672.60
203	MD51	115.94	-24.11	2945.57	-612.56
204	V_{SS}	120.93	-20.83	3072.16	-529.29
205	MD20	115.94	-17.56	2945.57	-446.12
206	MD37	120.93	-15.20	3072.20	-386.08
207	MD22	115.94	-12.83	2945.57	-326.04
208	V_{CC}	120.93	-10.47	3072.20	-266.00
209	MD38	115.94	-8.11	2945.57	-205.96
210	MD3	120.93	-5.74	3072.20	-145.92
211	MD6	115.94	-3.38	2945.57	-85.88
212	MD34	120.93	-1.02	3072.20	-25.84
213	MD39	115.94	1.35	2945.57	34.20
214	MD7	120.93	3.71	3072.20	94.24
215	MD54	115.94	6.07	2945.57	154.28
216	HCLKIN	120.93	8.44	3072.20	214.32
217	MD55	115.94	10.80	2945.57	274.36
218	MD52	120.93	13.16	3072.20	334.40
219	MD23	115.94	15.53	2945.57	394.44
220	V_{SS}	120.93	17.89	3072.20	454.48
221	MD5	115.94	20.25	2945.57	514.52
222	MD17	120.93	22.62	3072.20	574.56
223	MD4	115.94	24.98	2945.57	634.60

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 8 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
224	MD2	120.93	27.34	3072.20	694.64
225	MD50	115.94	29.71	2945.57	754.68
226	MD1	120.93	32.07	3072.20	814.72
227	MD36	115.94	34.43	2945.57	874.76
228	MD0	120.93	36.80	3072.20	934.80
229	MD18	115.94	39.16	2945.57	994.84
230	MD16	120.93	41.52	3072.20	1054.88
231	MD19	115.94	43.89	2945.57	1114.92
232	MD40	120.93	46.25	3072.20	1174.96
233	MD32	115.94	48.61	2945.57	1235.00
234	V_{CC}	120.93	50.99	3072.20	1295.42
235	MD56	115.94	54.13	2945.57	1375.12
236	MD8	120.93	56.49	3072.20	1435.16
237	MD9	115.94	58.85	2945.57	1495.20
238	MD33	120.93	61.22	3072.20	1555.24
239	MD24	115.94	63.58	2945.57	1615.28
240	MD41	120.93	65.94	3072.20	1675.32
241	MD57	115.94	68.31	2945.57	1735.36
242	MD35	120.93	70.67	3072.20	1795.40
243	MD25	115.94	73.03	2945.57	1855.44
244	MD26	120.93	75.40	3072.20	1915.48
245	MD42	115.94	77.76	2945.57	1975.52
246	MD48	120.93	80.12	3072.20	2035.56
247	MD58	115.94	83.08	2945.57	2110.61
248	MD10	120.93	86.03	3072.20	2185.66
249	MD44	115.94	88.99	2945.57	2260.71
250	MD49	120.93	91.94	3072.20	2335.76
251	MD59	115.94	94.89	2945.57	2410.81
252	NC	120.93	100.22	3072.20	2546.14
253	V_{SS}	120.93	105.16	3072.20	2671.54
254	V_{SS}	120.93	110.09	3072.20	2796.94
255	V_{SS}	120.93	115.01	3072.20	2921.77

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 9 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
256	V_{CC}	114.46	121.63	2907.85	3090.16
257	V_{CC}	109.52	121.63	2782.45	3090.16
258	V_{SS}	104.59	121.63	2657.05	3090.16
259	MD62	100.58	116.65	2555.40	2963.52
260	MD43	95.19	116.65	2418.32	2963.52
261	MD30	92.24	121.63	2343.27	3090.16
262	MD27	89.28	116.65	2268.22	2963.52
263	V_{REF}	86.33	121.63	2193.17	3090.16
264	MD28	83.37	116.65	2118.12	2963.52
265	MD12	80.42	121.63	2043.07	3090.16
266	MD60	77.46	116.65	1968.02	2963.52
267	MD15	75.10	121.63	1907.98	3090.16
268	MD46	72.74	116.65	1847.94	2963.52
269	MD45	70.37	121.63	1787.90	3090.16
270	MD61	68.01	116.65	1727.86	2963.52
271	V_{SS}	65.63	121.63	1667.44	3090.16
272	MD63	62.50	116.65	1587.73	2963.52
273	GNT3#	60.13	121.63	1527.69	3090.16
274	MD29	57.77	116.65	1467.65	2963.52
275	MD13	55.41	121.63	1407.61	3090.16
276	MD47	53.04	116.65	1347.57	2963.52
277	REQ3#	50.68	121.63	1287.53	3090.16
278	MD14	48.32	116.65	1227.49	2963.52
279	PAR	45.95	121.63	1167.45	3090.16
280	MD31	43.59	116.65	1107.41	2963.52
281	V_{CC}	40.31	121.63	1024.15	3090.11
282	CLKRUN#	37.04	116.65	940.97	2963.52
283	AD0	34.67	121.63	880.93	3090.16
284	AD2	32.31	116.65	820.89	2963.52
285	STOP#	29.95	121.63	760.85	3090.16
286	GNT2#	27.59	116.65	700.81	2963.52
287	AD4	25.22	121.63	640.77	3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 10 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
288	AD1	22.86	116.65	580.73	2963.52
289	AD3	20.50	121.63	520.69	3090.16
290	AD5	18.13	116.65	460.65	2963.52
291	AD7	15.77	121.63	400.61	3090.16
292	AD6	13.41	116.65	340.57	2963.52
293	C/BE0#	11.04	121.63	280.53	3090.16
294	REQ2#	8.68	116.65	220.49	2963.52
295	AD8	6.32	121.63	160.45	3090.16
296	AD9	3.95	116.65	100.41	2963.52
297	GNT1#	1.59	121.63	40.37	3090.16
298	AD10	-0.77	116.65	-19.66	2963.52
299	AD11	-3.14	121.63	-79.70	3090.16
300	PCLKIN	-5.50	116.65	-139.74	2963.52
301	AD13	-7.86	121.63	-199.78	3090.16
302	AD12	-10.23	116.65	-259.82	2963.52
303	V_{CC}	-12.59	121.63	-319.86	3090.16
304	AD14	-14.95	116.65	-379.90	2963.52
305	V_{SS}	-17.32	121.63	-439.94	3090.16
306	C/BE1#	-19.68	116.65	-499.98	2963.52
307	C/BE2#	-22.04	121.63	-560.02	3090.16
308	AD15	-24.41	116.65	-620.06	2963.52
309	REQ1#	-26.77	121.63	-680.10	3090.16
310	AD18	-29.13	116.65	-740.14	2963.52
311	DEVSEL#	-31.50	121.63	-800.18	3090.16
312	AD17	-33.86	116.65	-860.22	2963.52
313	GNT0#	-36.22	121.63	-920.26	3090.16
314	AD16	-38.59	116.65	-980.30	2963.52
315	TRDY#	-40.95	121.63	-1040.34	3090.16
316	AD21	-43.31	116.65	-1100.38	2963.52
317	AD20	-45.68	121.63	-1160.42	3090.16
318	C/BE3#	-48.04	116.65	-1220.46	2963.52
319	REQ0#	-50.40	121.63	-1280.50	3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

Table 1. 82439TX System Controller Bond Pad Center Data (Sheet 11 of 11)

PAD#	SIGNAL[2,3]	Pad Center[1]			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
320	AD19	-52.77	116.65	-1340.54	2963.52
321	V_{CC}	-55.14	121.63	-1400.96	3090.16
322	AD27	-58.28	116.65	-1480.67	2963.52
323	AD24	-60.64	121.63	-1540.71	3090.16
324	AD23	-63.01	116.65	-1600.75	2963.52
325	AD22	-65.37	121.63	-1660.79	3090.16
326	AD26	-67.73	116.65	-1720.83	2963.52
327	IRDY#	-70.10	121.63	-1780.87	3090.16
328	PHLDA#	-72.46	116.65	-1840.91	2963.52
329	AD25	-74.82	121.63	-1900.95	3090.16
330	AD29	-77.19	116.65	-1960.99	2963.52
331	FRAME#	-79.55	121.63	-2021.03	3090.16
332	AD31	-82.51	116.65	-2096.08	2963.52
333	AD28	-85.46	121.63	-2171.13	3090.16
334	PHLD#	-88.41	116.65	-2246.18	2963.52
335	LOCK#	-91.37	121.63	-2321.23	3090.16
336	AD30	-94.32	116.65	-2396.28	2963.52
337	NC	-99.51	121.63	-2528.19	3090.16
338	V_{SS}	-104.45	121.63	-2653.59	3090.16
339	V_{SS}	-109.39	121.63	-2778.99	3090.16
340	V_{SS}	-114.30	121.63	-2903.82	3090.16

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent package unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAK with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Smart Die
- Intel Part Number
- Assembly Process Order/Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines the 82439TX System Controller physical specifications.

Table 2. 82439TX System Controller Physical Specifications

Die Revision:	A-2 Step
Post-Saw Die Dimensions:	Mils: X = 254.7 ± 0.5, Y= 256.1 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	60/120 microns (see die plot for more detail)
Pad Passivation Opening Size:	Microns: 95 x 95 (Note: pad size is not perfect square)
Bond Pad Metallization: (outermost layer first)	14,000 Angstroms Aluminum (0.5% Copper), 1000 Angstroms Titanium
Pads per Die:	340
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 150 Angstroms Chrome
Passivation: (outermost layer first)	3.3 microns polyimide, 4500 Angstroms nitride
Intel Fabrication Process:	CMOS

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature .....0°C to +70°C
Junction Temperature Under Bias .....-65°C to +110°C

OPERATING CONDITIONS†

T_J (Junction Temperature Under Bias) ..... 0°C to 105°C(1)
Substrate Bias ..... Float (Self Biasing to V_{SS}), Alternative is to Drive V_{SS}
Core Operating Frequency .....60, 66 MHz

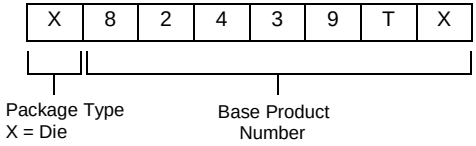
NOTES:

1. Average die surface temperature

NOTICE: This datasheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



VALID COMBINATIONS:
X82439TX

5.0 REFERENCE INFORMATION

Document Title	Order #
82439TX System Controller (MTXC) datasheet	290559

6.0 REVISION HISTORY

Revision	Date	Description
002	8/97	In Table 1, the labels for Mils and Microns were reversed and are correct in this revision. (Revision 001 showed the Mils data with the Microns label and vice versa.)
001	2/97	Initial Release