82562EP 10/100 Mbps Platform LAN Connect (PLC)

Networking Silicon

Datasheet

Product Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR tree mode support
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- Alert on LAN functionality
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- Lead-free[1] 64-pin Plastic Ball Grid Array Package for both leaded and lead-free designs. (Devices that are lead-free are marked with a circled “e1” and have the product code prefix: PCxxxxxx).

[1] This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS)-banned materials, is available at:
`ftp://download.intel.com/design/packtech/material_content_IC_Package.pdf#pagemode=bookmarks`
In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device.

For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative.

Revision 2.0
September 2005

Revision History

Revision	Revision Date	Description
1.0	August 2000	Initial release (Intel Secret).
1.4	May 2001	Finialized signal descriptions and pinouts.
1.5	October 2001	Changed document status to Intel Confidential - Controlled Access.
1.6	December 2003	Removed confidential status.
2.0	September 2005	Updated or new revision information includes: • Lead-free information. • Product codes. • Bias reference resistor values (RBIAS 10 and RBIAS 100). • Crystal input/output clock values. • Signal termination section.

Contents

Figures

Tables

1.0 Introduction

1.1 Overview

The Intel® 82562EP is a highly-integrated Platform LAN Connect (PLC) device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82562EP complies with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82562EP also includes a PHY interface compliant to the current PLC interface.

1.2 References

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers.
- LAN Connect Interface Specification. Intel Corporation.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.

Programming information can be obtained through your local Intel representatives.

1.3 Product Codes

The product ordering code for a lead-free device is: PC82562EP.

The product ordering code for a leaded device is: RC82562EP.

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2.0 82562EP Architectural Overview

The 82562EP is a highly integrated Platform LAN Connect device that combines 10BASE-T and 100BASE-TX physical layer interfaces. The 82562EP supports a single interface fully compliant with the IEEE 802.3 standard. Figure 1 shows a block diagram of the 82562EP architecture.

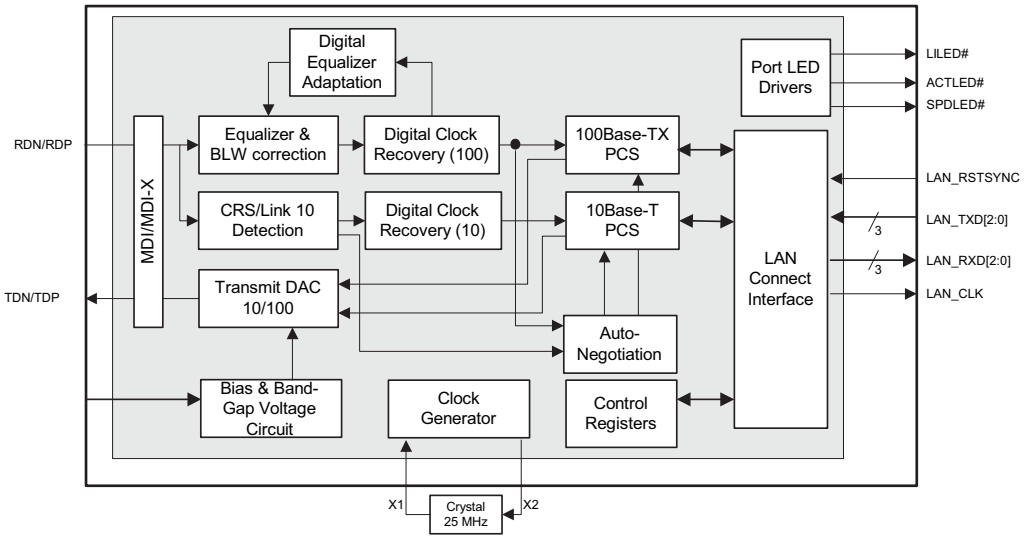


Figure 1. 82562EP PLC Block Diagram

2.1 LAN Connect Interface

The 82562EP supports a LAN Connect Interface (LCI) as specified in the LCI Specification. The LAN Connect is the I/O Control Hub 2 (ICH2) interface to the 82562EP. The LCI uses an 8-pin interface, which reduces the pin count from 15, for an Media Independent Interface (MII) PHY. In addition, its signaling protocol provides greater functionality, such as dynamic power reduction, from a PLC in comparison to a standard MII PHY.

Figure 2 shows how the 82562EP can be used in a 10/100 Mbps ICHx design.

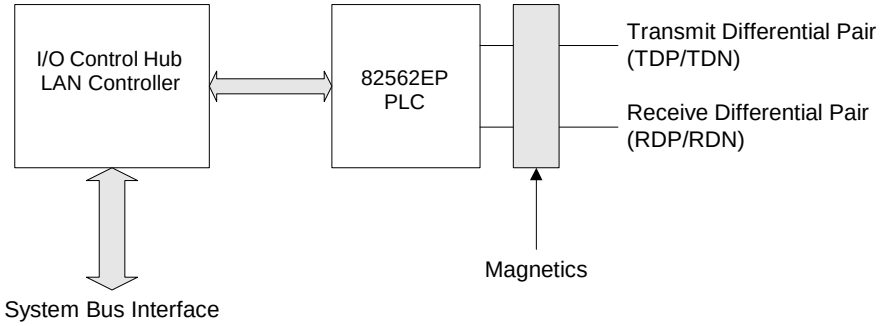


Figure 2. 82562EP PLC 10/100 Mbps Ethernet Solution

2.2 Hardware Configuration

Four pins, test Enable (TESTEN), Test Clock (ISOL_TCK), Test Input (ISOL_TI), and Test Execute (ISOL_TEX), define the general operation of the device. Table 1 shows the pin settings for the different modes of operation.

Table 1. 82562EP Hardware Configuration

Mode of Operation	TESTEN	ISOL_TCK	ISOL_TI	ISOL_TEX	Comments
Normal Operating Mode	0	0	0	0	The ISOL_TCK, ISOL_TI, and ISOL_TEX pins can remain floating.
Isolate Mode (Tri-State and Full Power-Down Mode)	0	1	1	1	The device is in tri-state and power-down mode.
	1	1	1	1	The device is in tri-state and power-down mode.
XOR Tree	1	0	0	0	The XOR tree is used for board testing and tri-state mode.

NOTE: Combinations not shown in Table 1 are reserved and should not be used.

3.0 82562EP Signal Descriptions

3.1 Signal Type Definitions

Type	Name	Description
I	Input	Input pin to the 82562EP.
O	Output	Output pin from the 82562EP.
I/O	Input/Output	Multiplexed input and output pin to and from the 82562EP.
MLT	Multi-level analog I/O	Multi-level analog pin used for input and output.
B	Bias	Bias pin used for ground connection through a resistor or an external voltage reference.
DPS	Digital Power Supply	Digital power or ground pin for the 82562EP.
APS	Analog Power Supply	Analog power or ground pin for the 82562EP.

3.2 Twisted Pair Ethernet (TPE) Pins

Pin Name	Pin Number	Type	Description
TDP TDN	G3 H3	MLT	**Transmit Differential Pair.** The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with the isolation transformer.
RDP RDN	H6 G6	MLT	**Receive Differential Pair.** The receive differential pair receive the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with an isolation transformer.

3.3 External Bias Pins

Pin Name	Pin Number	Type	Description
RBIAS10	F2	B	**Reference Bias Resistor (10 Mbps).** This pin should be connected to a pull-down resistor.[a]
RBIAS100	F1	B	**Reference Bias Resistor (100 Mbps).** This pin should be connected to a pull-down resistor.[a]

a. Based on some board designs, RBIAS100 and RBIAS10 values may need to be increased/decreased to compensate for high/low MDI transmit amplitude. See Section 4.0 for more information.

3.4 Clock Pins

Pin Name	Pin Number	Type	Description
X1	C2	I	**Crystal Input Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30 PPM or better. Otherwise, X1 is driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	C1	O	**Crystal Output Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30 PPM or better.

3.5 Platform LAN Connect Interface Pins

Pin Name	Pin Number	Type	Description
LAN_CLK	A4	O	**LAN Connect Clock.** The LAN Connect Clock is driven by the 82562EP on two frequencies depending on operation speed. When the 82562EP is in 100BASE-TX mode, LAN_CLK drives a 50 MHz clock. Otherwise, LAN_CLK drives a 5 MHz clock for 10BASE-T. The LAN_CLK does not stop during normal operation.
LAN_RSTSYNC	B3	I	**Reset/Synchronize.** This is a multiplexed pin and is driven by the Media Access Control (MAC) layer device. Its functions are: • Reset. When this pin is asserted beyond one LAN Connect Clock period, the 82562EP uses this signal as Reset. To ensure the 82562EP is reset, this signal should remain active for at least 500 µs. • Synchronize. When this pin is activated synchronously for only one LAN Connect Clock period, it is used to synchronize the MAC and PHY on PLC word boundaries.
LAN_TXD[2:0]	B1 B2 A2	I	**LAN Connect Transmit Data.** The PLC transmit pins are used to transfer data from the MAC device to the 82562EP. These pins are used to move transmitted data and real time control and management data. They also transmit out of band control data from the MAC to the PHY. These pins should be fully synchronous to LAN_CLK.
LAN_RXD[2:0]	A5 A6 B6	O	**LAN Connect Receive Data.** The PLC receive pins are used to transfer data from the 82562EP to the MAC device. These pins are used to move received data and real time control and management data. They also move out of band control data from the PHY to the MAC. These pins are synchronous to LAN_CLK.

3.6 LED Pins

Pin Name	Type	Description
LILED#	O	**Link Integrity LED.** The LED is active low and the Link Integrity LED pin indicates link status in either 10BASE-T or 100BASE-TX mode. If a link is present in either mode, the LILED# is asserted.
ACTLED#	O	**Activity LED.** The LED is active low and the Activity LED signal indicates either receive or transmit activity. When no activity is present, the LED is off. The Activity LED will flicker when activity is present. The flicker rate depends on the activity load. The individual address LED control bit in the ICH2 EEPROM (Word Ah, bit 4) can select the ACTLED# behavior. It controls the Activity LED (ACTLED) functionality in Wake on LAN (WOL) mode. 0b = In WOL mode, the ACTLED is activated by the transmission and reception of broadcast and individual address match packets. 1b = In WOL mode, the ACTLED is activated by the transmission and reception of individual address match packets only. This bit is configured by the OEM and is activated by a transmission and reception of individual address match packets.
SPDLED#	O	**Speed LED.** The LED is active low and the Speed LED signal indicates the speed of operation, either 10 Mbps or 100 Mbps. The Speed LED is on during 100BASE-TX operation and off in 10BASE-T mode.

3.7 Miscellaneous Control Pins

Pin Name	Type	Description
ADV10	I	**Advertise 10 Mbps Only.** The this signal is asserted high, the 82562EP advertises only 10BASE-T technology during Auto-Negotiation processes in this state. Otherwise, the 82562EP advertises all of its technologies. **Note:** ADV10 has an internal pull-down resistor.
ISOL_TCK	I	**Test Clock.** The Test Clock signal sets the device into asynchronous test mode in conjunction with the Test Input, Test Execute and Test Enable pins (refer to Table 1). In the manufacturing test mode, it acts as the test clock. **Note:** ISOL_TCK has an internal pull-down resistor.
ISOL_TI	I	**Test Input.** The Test Input signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Execute and Test Enable pins (refer to Table 1). In the manufacturing test mode, it acts as the test data input pin. Note: ISOL_TI has an internal pull-down resistor.
ISOL_TEX	I	**Test Execute.** The Test Execute signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Input, and Test Enable pins (refer to Table 1). In the manufacturing test mode, it places the command that was entered through the ISOL_TI pin in the instruction register. Note: ISOL_TEX has an internal pull-down resistor.
TOUT	O	**Test Output.** The Test Output pin is used for Boundary XOR scan output. In the manufacturing test mode, it acts as the test output port.
TESTEN	I	**Test Enable.** The Test Enable pin is used to enable test mode and should be tied to the pull-down resistor for normal operation.

3.8 Power and Ground Connections

Pin Name	Pin Number	Type	Description
VCC VCCA VCCA2 VCCP VCCT	A1, A8, E7, F7, F8 G1, H1 D2, E2 B4, B5 G4, G5, H4, H5	DPS	**Digital 3.3 V Power.** These pins should be connected to the main digital power supply.
VSS VSSA VSSA2 VSSP	C3, C6, D3, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6 G2, H2 D1, E1 C4, C5	DPS	**Digital Ground.** These pins should be connected to the main digital ground.
VCCR	G8, H8	APS	**Analog Power.** These pins should be isolated from the main power using a resistor-capacitor (RC) filter. A ferrite bead may also be used in place of the resistor.
VSSR	G7, H7	APS	**Analog Ground.** These pins should not be isolated from the main digital.

4.0 Signal Terminations

4.1 Terminating Resistors

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace.

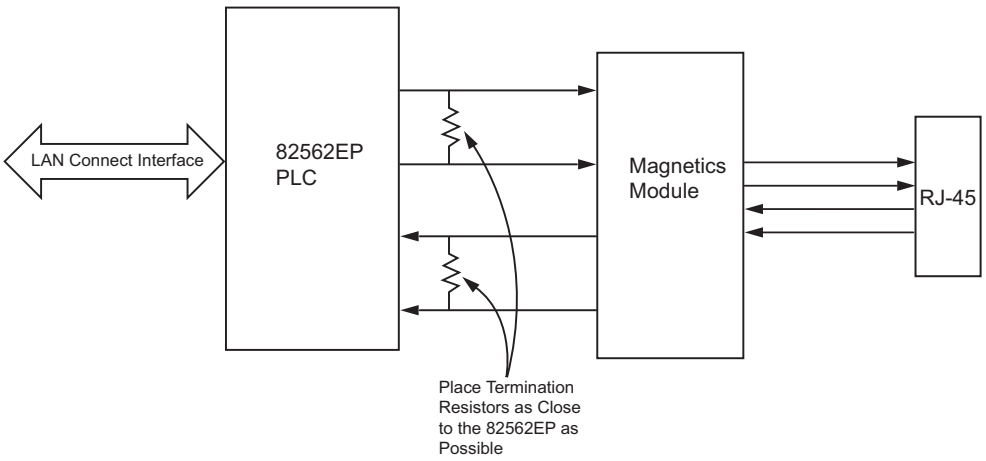
Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

Figure 3. Termination Resistors Placement (Integrated Magnetics Solution)



4.1.1 Termination Plane

Resistors are used to terminate noise from the unused inputs of both the RJ45 connector and the magnetics module to the termination plane. The netname “termplane” is provided as a guide to the termination plane. A termplane is a plane fabricated into the PCB substrate. This plane, which has no DC termination, acts like one-half of a capacitor that provides a path for the coupled noise.

4.1.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP and TDN and RDP and RDN) from the unused pairs of the RJ45. Pads may be placed for additional capacitance, which may be required if failure occurs during electrical fast transient testing.

Note: This capacitor must be designed to tolerate 2 KV voltage injections to meet International Special Committee on Radio Interference (CISPR) Electrostatic Discharge (ESD) specifications.

5.0 82562EP Test Port Functionality

The 82562EPG's XOR Tree Test Access Port (TAP) is the access point for test data to and from the device. The port provides the ability to perform basic production level testing.

5.1 Asynchronous Test Mode

An asynchronous test mode is supported for system level design use. The modes are selected through the use of the Test Port input pins (TESTEN, ISOL_TCK, ISOL_TI and ISOL_TEX) in static combinations. During normal operation the test pins must be pulled down through a resistor (pulling Test high enables the test mode). All other port inputs may have a pull-down at the designers discretion.

5.2 Test Function Description

The 82562EP TAP mode supports several tests that can be used in board level design. These tests can help verify basic functionality and test the integrity of solder connections on the board. The tests are described in the following sections.

The XOR Tree test mode is the most useful of the asynchronous test modes. It enables the placement of the 82562EP to be validated at board test. The XOR Tree was chosen for its speed advantages. Modern Automated Test Equipment (ATE) can perform a complete peripheral scan without support at the board level. This command connects all output signals of the input buffers in the device periphery into an XOR Tree scheme. All output drivers of the output-buffers, except the test output (TOUT) pin, are put into high-Z mode. These pins are driven to affect the tree's output. Any hard strapped pins will prevent the tester from scanning correctly. The XOR Tree test mode is obtained by placing the test pins in the following configuration (refer to Table 2):

TESTEN = 1

ISOL_TCK = 0

ISOL_TI = 0

ISOL_TEX = 0.

Table 2. XOR Tree Chain Order

Chain Order	Chain
1	LAN_TXD2
2	LAN_TXD1
3	LAN_TXD0
4	LAN_RSTSYNC
5	ADV10
6	LAN_CLK
7	LAN_RXD2
8	LAN_RXD1
9	LAN_RXD0
10	ACTLED#

Table 2. XOR Tree Chain Order

Chain Order	Chain
11	SPDLED#
12	LILED#
XOR Tree Output	TOUT

The following pins are not included in the XOR Tree chain: X1, ISOL_TCK, ISOL_TEX, ISOL_TI and TESTEN.

6.0 Electrical and Timing Specifications

6.1 Absolute Maximum Ratings

Maximum ratings are listed below:

Case Temperature under Bias . . . . . 0° C to 135° C
Storage Temperature . . . . . -65° C to 150° C
Supply Voltage with respect to V_{SS} . . . . . -0.5 V to 3.45 V
Output Voltages . . . . . -0.50 V to 3.45 V
Input Voltages . . . . . -0.5 V to 3.45 V

Stresses above the listed absolute maximum ratings may cause permanent damage to the 82562EP device. This is a stress rating only and functional operations of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

Table 3. General DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CC}	Supply Voltage		3.0	3.3	3.45	V	
T	Temperature	Minimum/Maximum Case Temperature	0		85	C	
P	Power Consumption	10/100 Mb/s (transmitter on)		300		mW	
		Reduced Power		50		mW	
		Auto-Negotiation		200		mW	

6.2.1 X1 Clock DC Specifications

Table 4. X1 Clock DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{ILIH}	Input Leakage Currents	$0 < V_{IN} < V_{CC}$			±10	µA	
C_I	Input Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

6.2.2 LAN Connect Interface DC Specifications

Table 5. LAN Connect Interface DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CCJ}	Input/Output Supply Voltage		3.0		3.45	V	
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CCJ}$	V	
V_{IH}	Input High Voltage		$0.6V_{CCJ}$		V_{CCJ} + 0.5	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CCJ}$			±10	µA	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{CCJ}$	V	
V_{OH}	Output High Voltage	I_{OUT} = -500 µA	$0.9V_{CCJ}$			V	
C_{IN}	Input Pin Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

6.2.3 LED DC Specifications

Table 6. LED DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OLLED}	Output Low Voltage	I_{OUT} = 10 mA			0.7	V	
V_{OHLED}	Output High Voltage	I_{OUT} = -10 mA	2.4			V	

6.2.4 10BASE-T Voltage and Current DC Specifications

Table 7. 10BASE-T Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD10}	Output Differential Peak Voltage	R_L = 100 Ω	2.2		2.8	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 8. 10BASE-T Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID10}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA10}	Input Differential Accept Peak Voltage	5 MHz ≤ f ≤ 10 MHz	585		3100	mV	
V_{IDR10}	Input Differential Reject Peak Voltage	5 MHz ≤ f ≤ 10 MHz			300	mV	
V_{ICM10}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

6.2.5 100BASE-TX Voltage and Current DC Specifications

Table 9. 100BASE-TX Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD100}	Output Differential Peak Voltage	R_L = 100 Ω	0.95	1.0	1.05	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 10. 100BASE-TX Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID100}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA100}	Input Differential Accept Peak Voltage		±500		1200	mV	
V_{IDR100}	Input Differential Reject Peak Voltage				±100	mV	
V_{ICM100}	Input Common Mode Voltage			$V_{CC}/^2$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

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7.0 Package and Pinout Information

7.1 Package Information

The 82562EP is a lead or lead-free 64-pin Plastic Ball Grid Array (PBGA). The package dimensions are shown in Figure 4 and Figure 5. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local sales office.

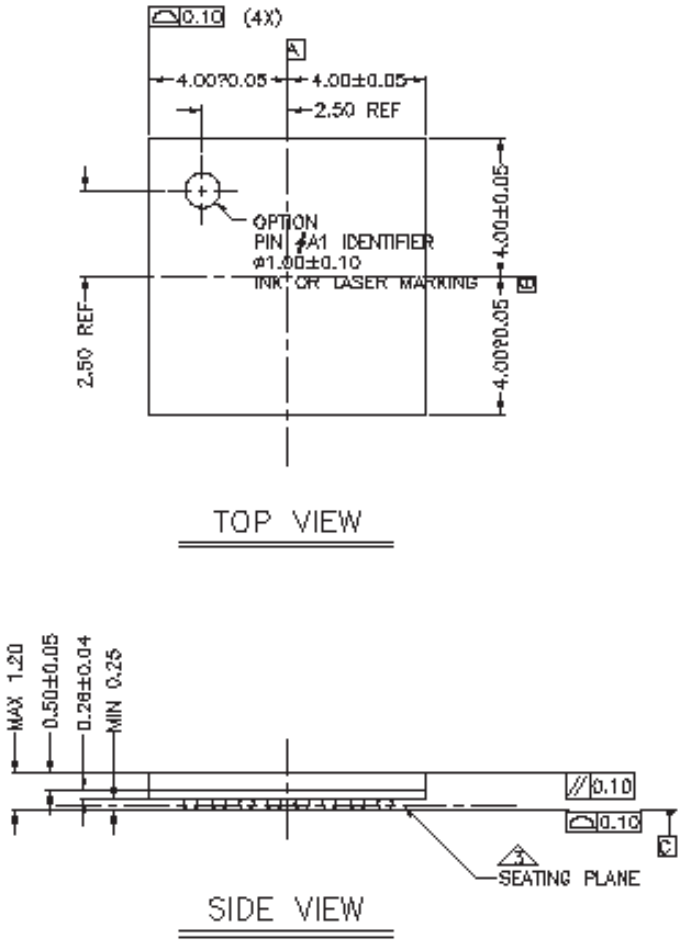
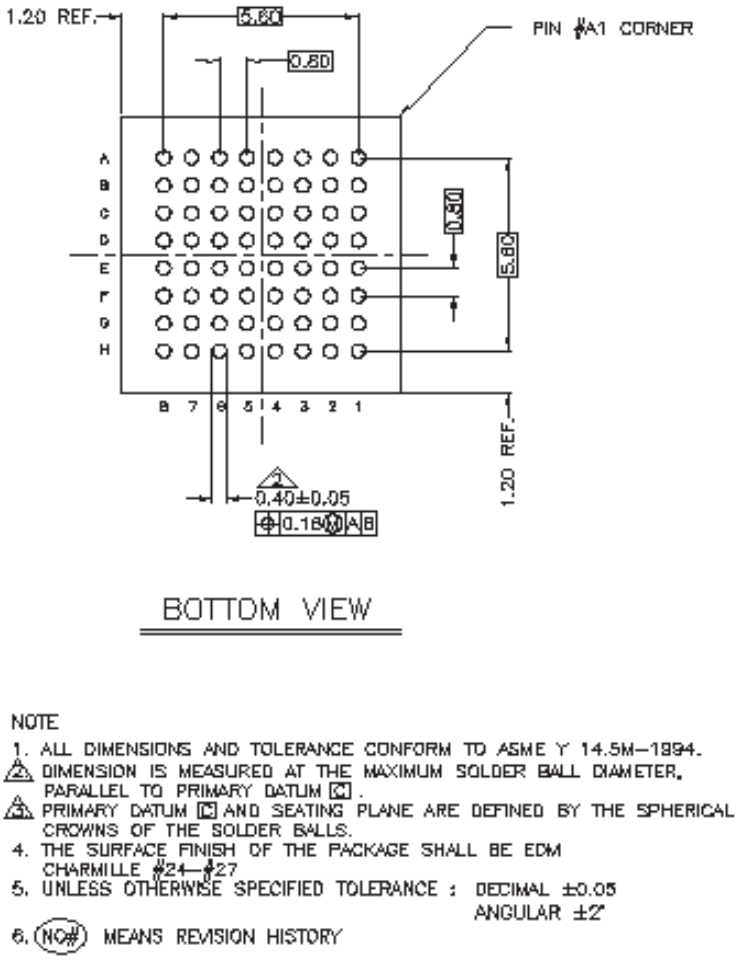


Figure 4. Dimension Diagram for the 82562EP 64-pin PBGA (1 of 2)



NOTE
1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M–1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARMILLE #24–#27
5. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05
   ANGULAR ±2°
6. (NO#) MEANS REVISION HISTORY

Figure 5. Dimension Diagram for the 82562EP 64-pin PBGA (2 of 2)

7.1.1 82562EP Pin Assignments

Table 11. 82562EP Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	Vcc	C1	X2	E1	Vssa2	G1	Vcca
A2	LAN_TXD0	C2	X1	E2	Vssa2	G2	Vssa
A3	ADV10	C3	Vss	E3	Vss	G3	TCP
A4	LAN_CLK	C4	Vssp	E4	Vss	G4	Vcct
A5	LAN_RXD2	C5	Vssp	E5	Vss	G5	Vcct
A6	LAN_RXD1	C6	Vss	E6	Vss	G6	RDN
A7	ACTLED#	C7	ISOL_TEX	E7	Vcc	G7	Vssr
A8	Vcc	C8	ISOL_TI	E8	TESTEN	G8	Vccr
B1	LAN_TXD2	D1	Vcca2	F1	RBIAS100	H1	Vcca
B2	LAN_TXD1	D2	Vcca2	F2	RBIAS10	H2	Vssa
B3	LAN_RSTSYNC	D3	Vss	F3	Vss	H3	TDN
B4	Vccp	D4	Vss	F4	Vss	H4	Vcct
B5	Vccp	D5	Vss	F5	Vss	H5	Vcct
B6	LAN_RXD0	D6	Vss	F6	Vss	H6	RDP
B7	SPDLED#	D7	Tout	F7	Vcc	H7	Vssr
B8	ISOL_TCK	D8	LILED#	F8	Vcc	H8	Vccr

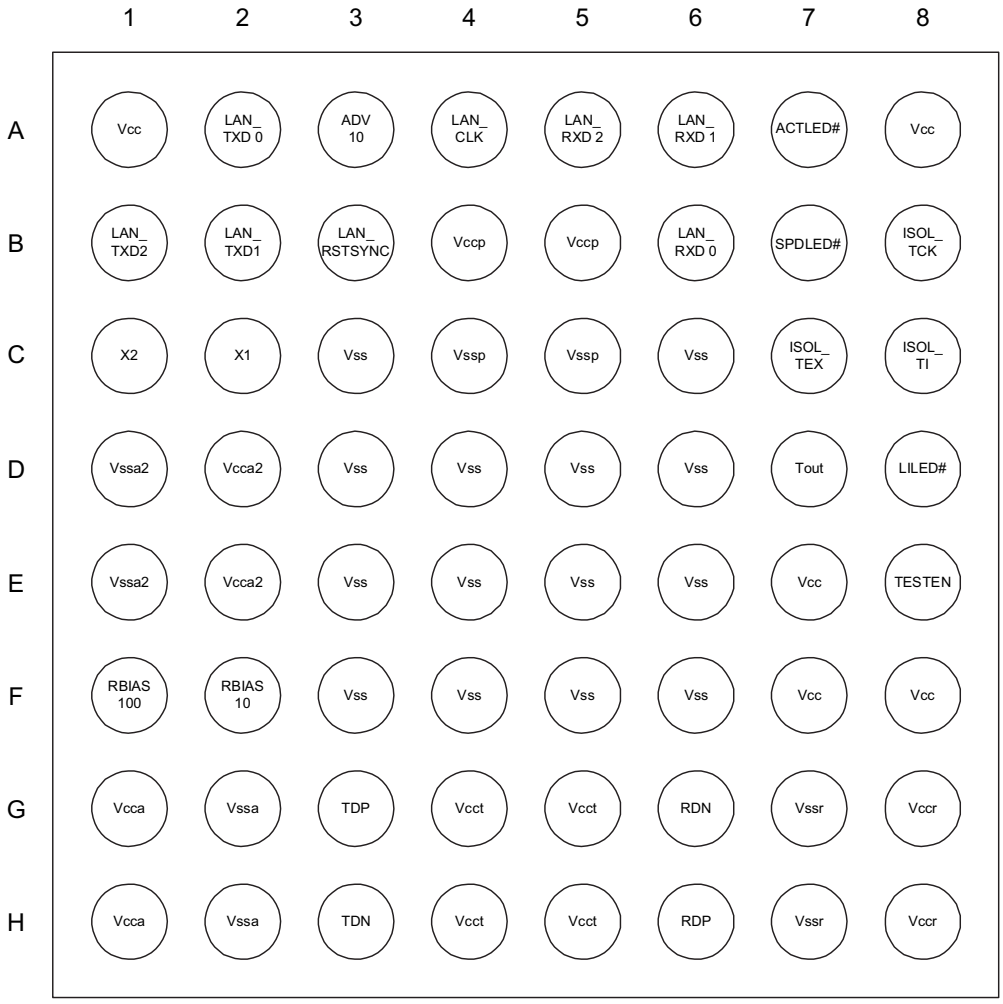


Figure 6. 82562EP Pinout Diagram