8259A

Programmable Interrupt Controller
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5-V supply (no clocks)
- 28-pin dual-in-line package

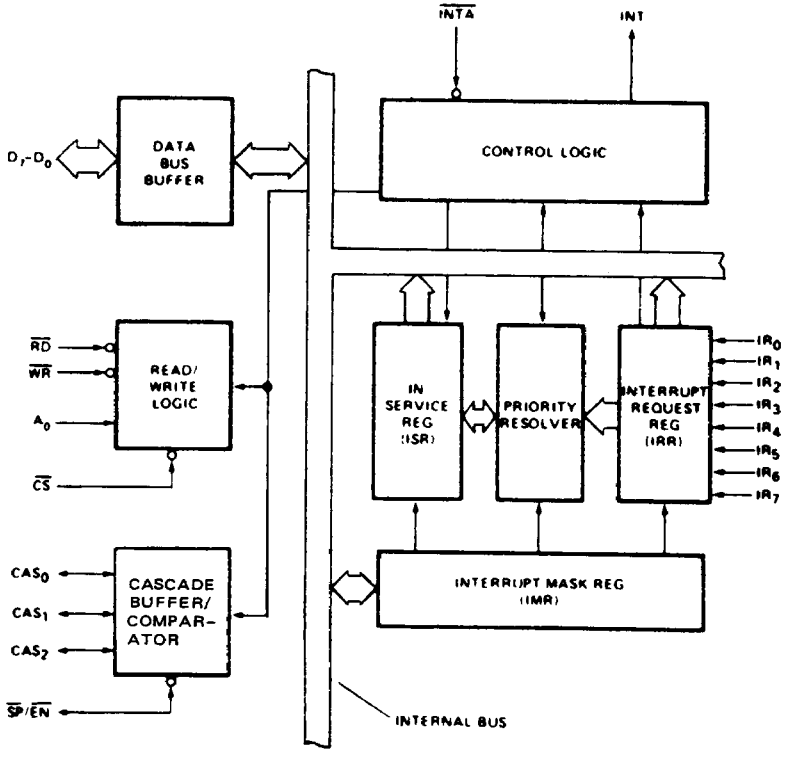
GENERAL DESCRIPTION

The 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology, and requires a single +5-V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward-compatible with the 8259. Software originally written for the 8259 will operate the 8259A in all 8259-equivalent modes.

BLOCK DIAGRAM



BD003541

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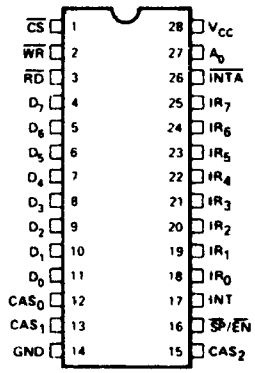
Issue Date: November 1987

CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87518 01 X X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
X = 28-Pin Ceramic DIP (CD 028)

b. MILITARY DEVICE TYPE
01 = 5 MHz (8259A)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87518
Programmable Interrupt Controller

Valid Combinations	
5962-8751801	XX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

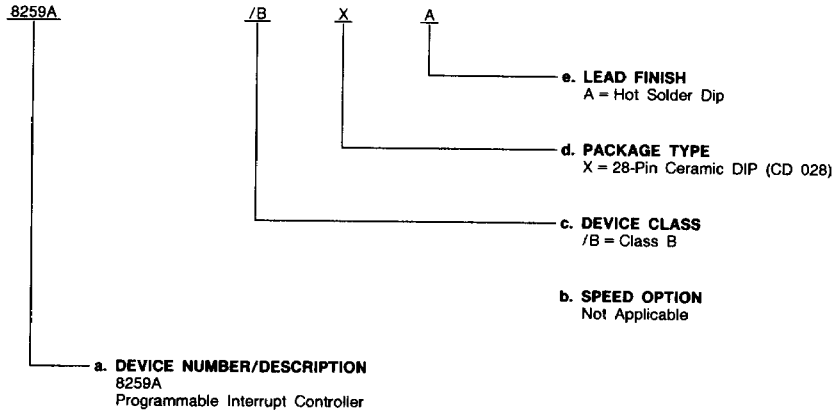
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8259A	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 4.5 V to 5.5 V	−0.5*	0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5 V to 5.5 V	2.3	V_{CC} + 0.5 V*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.2 mA, V_{CC} = 4.5 V		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
$V_{OH(INT)}$	Interrupt Output HIGH Voltage	I_{OH} = −100 μA, V_{CC} = 4[illegible] V	3.5		V
		I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
I_{LI}	Input Load Current	V_{IN} = 5.5 V and 0 V	−10	+10	μA
I_{LOL}, I_{LOH}	Output Leakage Current	V[illegible] V, V_{OUT} = 5.5 V and 0.45 V	−10	+10	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5 V (Note 1)		125	mA

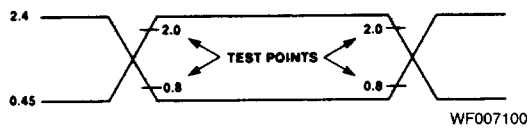
Notes: 1. I_{CC} measured in a stati[illegible] condition with outputs in worst-case state, having standard I_{OL}/I_{OH} loads applied.

CAPACITANCE (T[illegible] = 25°C, V_{CC} = GND = 0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}†	Input Capacitance	fc = 1 MHz		10*	pF
$C_{I/O}$†	I/O Capacitance	Unmeasured pins returned to V_{SS}		20*	pF

*Guaranteed by design; not tested.
†Not included in Group A tests.

SWITCHING TEST WAVEFORM



Input/Output

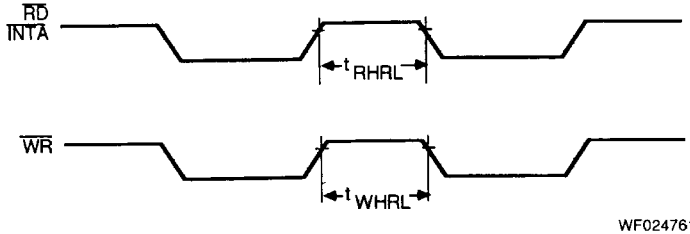
Note: AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted).

No.	Parameter Symbol	Parameter Description	Test Conditions	8259A Min.	8259A Max.	Unit
TIMING REQUIREMENTS						
1	t_{AHRL}	$A_0/\overline{CS}$ Setup to $\overline{RD}/\overline{INTA}\downarrow$	(Note 1)	0		ns
2	t_{RHAX}	$A_0/\overline{CS}$ Hold after $\overline{RD}/\overline{INTA}\uparrow$		0		ns
3	t_{RLRH}	$\overline{RD}$ Pulse Width		235		ns
4	t_{AHWL}	$A_0/\overline{CS}$ Setup to $\overline{WR}\downarrow$		0		ns
5	t_{WHAX}	$A_0/\overline{CS}$ Hold after $\overline{WR}\uparrow$		0		ns
6	t_{WLWH}	$\overline{WR}$ Pulse Width		290		ns
7	t_{DVWH}	Data Setup to $\overline{WR}\uparrow$		240		ns
8	t_{WHDX}	Data Hold after $\overline{WR}\uparrow$		0		ns
9	t_{JLJH}	Interrupt Request Width (LOW)		100		ns
10	t_{CVIAL}	Cascade Setup Second or Third $\overline{INTA}\downarrow$ (Slave Only)		55		ns
11	t_{RHRL}	End of $\overline{RD}$ to next Command		300		ns
12	t_{WHRL}	End of $\overline{WR}$ to next Command		370		ns
TIMING RESPONSES						
13	t_{RLDV}	Data Valid from $\overline{RD}/\overline{INTA}\downarrow$	(Notes 1 and 2)		200	ns
14	t_{RHDZ}	Data Float after $\overline{RD}/\overline{INTA}\uparrow$		10	100	ns
15	t_{JHIH}	Interrupt Output Delay			350	ns
16	t_{IALCV}	Cascade Valid from First $\overline{INTA}\downarrow$ (Master Only)			565	ns
17	t_{RLEL}	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$			125	ns
18	t_{RHEH}	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$			150	ns
19	t_{AHDV}	Data Valid from Stable Address			200	ns
20	t_{CVDV}	Cascade Valid to Valid Data			300	ns

Notes: 1. Test Conditions: V_{CC} = 4.5 V to 5.5 V
V_{IL} = 0.45 V, V_{IH} = 2.4 V; V_{OL} = 0.8 V, V_{OH} = = 2.0 V
I_{OL} = 2.2 mA, I_{OH} = −400 μA
2. Test Condition: C_L = 100 pF ±20 pF.



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Other Timing (Military)