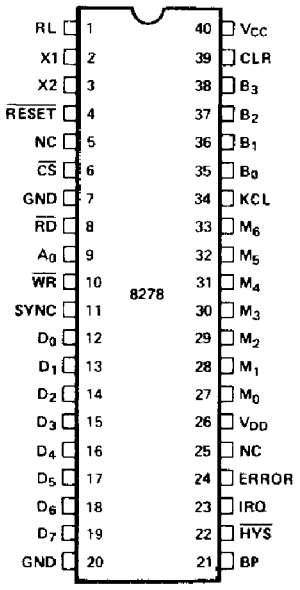
8278
PROGRAMMABLE KEYBOARD INTERFACE

- **Simultaneous Keyboard and Display Operations**
- **Interface Signals for Contact and Capacitive Coupled Keyboards**
- **128-Key Scanning Logic**
- **10.7 msec Matrix Scan Time for 128 Keys and 6 MHz Clock**
- **8-Character Keyboard FIFO**
- **N-Key Rollover with Programmable Error Mode on Multiple New Closures**
- **16-Character 7-Segment Display Interface**
- **Right or Left Entry Display RAM**
- **Depress/Release Mode Programmable**
- **Interrupt Output on Key Entry**

The Intel® 8278 is a general purpose programmable keyboard and display interface device designed for use with 8-bit microprocessors such the MDS-80™ and MCS-85™. The keyboard portion can provide a scanned interface to 128-key contact or capacitive-coupled keyboards. The keys are fully debounced with N-key rollover and programmable error generation on multiple new key closures. Keyboard entries are stored in an 8-character FIFO with overrun status indication when more than 8 characters are entered. Key entries set an interrupt request output to the master CPU.

The display portion of the 8278 provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric displays and simple indicators may be used. The 8278 has a 16X4 display RAM which can be loaded or interrogated by the CPU. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

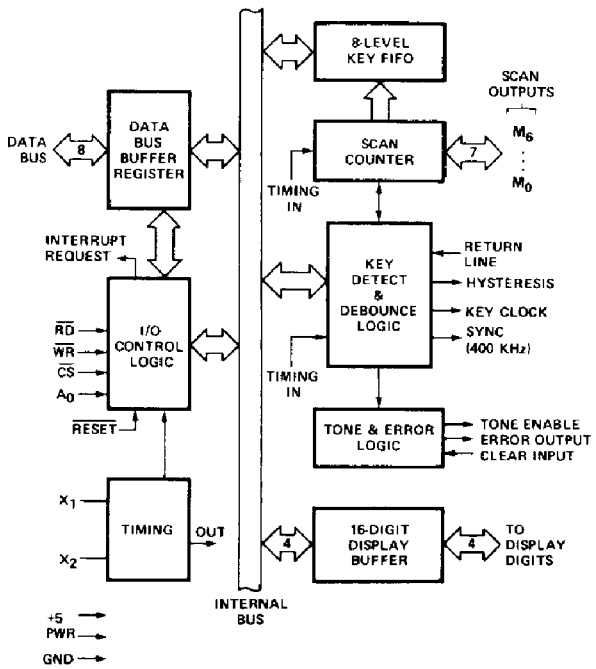
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS
$\overline{RD}$, $\overline{WR}$	READ, WRITE STROBES
$\overline{CS}$	CHIP SELECT
A_0	CONTROL/DATA SELECT
$\overline{RESET}$	RESET INPUT
X_1, X_2	FREQ. REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT CLOCK
RL	KEYBOARD RETURN LINE
CLR	CLEAR ERROR
KCL	KEY CLOCK
M_6–M_0	MATRIX SCAN LINES
B_3-B_0	DISPLAY OUTPUTS
ERROR	ERROR SIGNAL
IRQ	INTERRUPT REQUEST
HYS	HYSTERESIS
BP	TONE ENABLE

BLOCK DIAGRAM



PIN DESCRIPTION

The 8278 is packaged in a 40-pin DIP. The following is a brief functional description of each pin.

Signal	Pin No.	Description
D_0-D_7	12-19	Three-state, bi-directional data bus lines used to transfer data and commands between the CPU and the 8278.
$\overline{WR}$	10	Write strobe which enables the master CPU to write data and commands between the CPU and the 8278.
$\overline{RD}$	8	Read strobe which enables the master CPU to read data and status from the 8278 internal registers.
$\overline{CS}$	6	Chip select input used to enable reading and writing to the 8278.
A_0	9	Address input used by the CPU to indicate control or data.
$\overline{RESET}$	4	A low signal on this pin resets the 8278.
X_1, X_2	2,3	Inputs for crystal, L-C or external timing signal to determine internal oscillator frequency.
IRQ	23	Interrupt Request Output to the master CPU. In the keyboard mode the IRQ line goes low with each FIFO read and returns high if there is still information in the FIFO or an ERROR has occurred.
M_0-M_6	27-33	Matrix scan outputs. These outputs control a decoder which scans the key matrix columns and the 16 display digits. Also, the Matrix scan outputs are used to multiplex the return lines from the key matrix.
RL	1	Input from the multiplexer which indicates whether the key currently being scanned is closed.
$\overline{HYS}$	22	Hysteresis output to the analog detector. (Capacitive keyboard configuration). A "0" means the key currently being scanned has already been recorded.
KCL	34	Key clock output to the analog detector (capacitive keyboard configuration) used to reset the detector before scanning a key.
SYNC	11	High frequency (400 KHz) output signal used in the key scan to detect a closed key (capacitive keyboard configuration).
B_0-B_3	35-38	These four lines contain binary coded decimal display information synchronized to the keyboard column scan. The outputs are for multiplexed digital displays.
ERROR	24	Error signal. This line is high whenever two new key closures are detected during a single scan or when too many characters are entered into the keyboard FIFO. It is reset by a system RESET pulse or by a "1" input on the CLR pin or by the CLEAR ERROR command.
CLR	39	Input used to clear an ERROR condition in the 8278.
BP	21	Tone enable output. This line is high for 10ms following a valid key closure; it is set high and remains high during an ERROR condition.
V_{CC}, V_{DD}	40,26	+5 volt power input: +5V ± 10%.
GND	20,7	Signal ground.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$, and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers (see Table 1). All data flow to and from the 8278 is enabled by $\overline{CS}$. The 8-bits of information being transferred by the CPU is identified by A_0. A logic one means information is command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Bus Buffer (DBB). The DBB register is a bi-directional 8-bit buffer register which connects the internal 8278 bus buffer register to the external bus. When the chip is not selected ($\overline{CS}$ = 1) the DBB is in the high impedance state. The DBB acts as an input when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (1, 0, 0) and an output when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (0, 1, 0).

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Condition
0	0	1	0	Read DBB Data
0	1	1	0	Read STATUS
0	0	0	1	Write Data to DBB
0	1	0	1	Write Command to DBB
1	X	X	X	Disable 8278 Bus is High Impedance

Scan Counter

The scan counter provides the timing to scan the keyboard and display. The four MSB's (M_3-M_6) scan the display digits and provide column scan to the keyboard via a 4 to 16 decoder. The three LSB's (M_0-M_2) are used to multiplex the row return lines into the 8278.

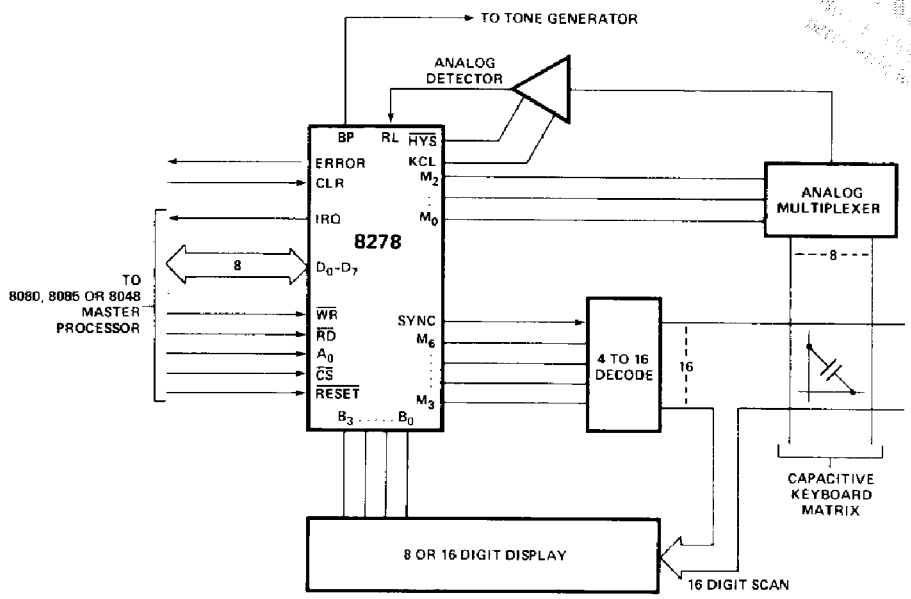


Figure 1. System Configuration for Capacitive-Coupled Keyboard

Keyboard Debounce and Control

The 8278 system configuration is shown in Figure 2. The rows of the matrix are scanned and the outputs are multiplexed by the 8278. When a key closure is detected, the debounce logic waits about 12 msec to check if the key remains closed. If it does, the address of the key in the matrix is transferred into a FIFO buffer.

FIFO and FIFO Status

The 8278 contains an 8X8 FIFO character buffer. Each new entry is written into a successive FIFO location and each is then read out in the order of entry. A FIFO status register keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or key entries will be recognized as an error. The status can be read by a $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides a IRQ signal to the master processor whenever the FIFO is not empty.

Display Address Registers and Display RAM

The display Address registers hold the address of the word currently being written or read by the CPU and the 4-bit nibble being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The display RAM can be directly read by the CPU after the correct mode and address is set. Data entry to the display can be set to either left or right entry.

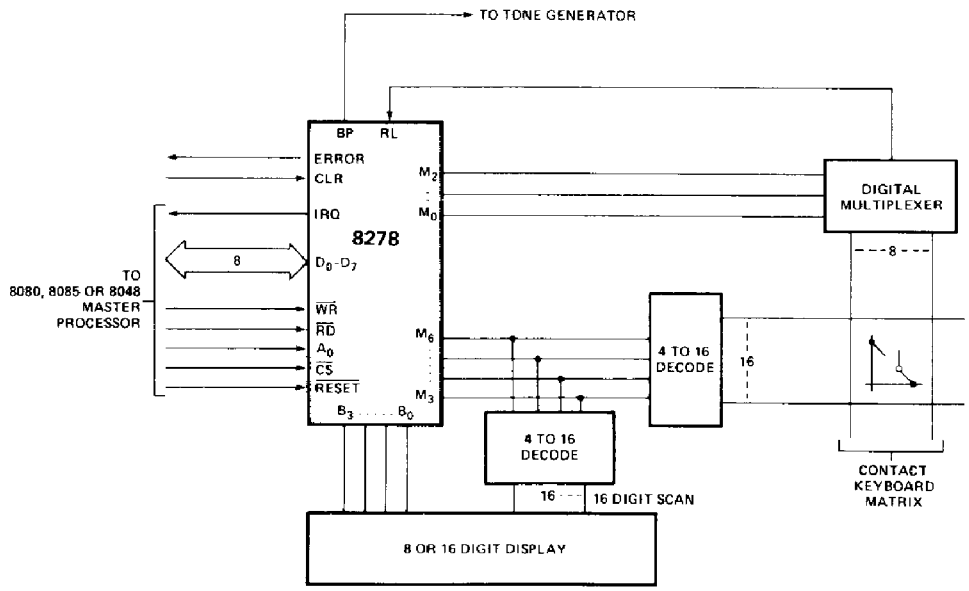
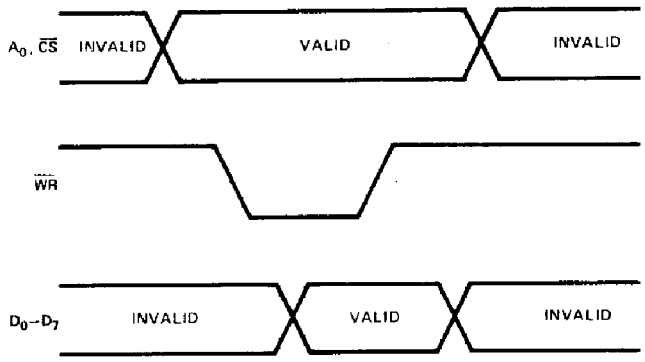


Figure 2. System Configuration for Contact Keyboard

8278 COMMANDS

The 8278 operating mode is programmed by the master CPU using the A_0, WR, and D_0-D_7 inputs as shown below:



The master CPU presents the proper command on the D_0-D_7 data lines with A_0=1 and then sends a $\overline{WR}$ pulse. The command is latched by the 8278 on the rising edge of the $\overline{WR}$ and is decoded internally to set the proper operating mode.

COMMAND SUMMARY

Keyboard/Display Mode Set

CODE	0	0	0	N	E	I	D	K

where the mode set bits are defined as follows:

K — the keyboard mode select bit
0 — normal key entry mode
1 — special function mode: Entry on key closure and on key release

D — the display entry mode select bit
0 — left display entry
1 — right display entry

I — the interrupt request (IRQ) output enable bit.
0 — enable IRQ output
1 — disable IRQ output

E — the error mode select bit
0 — error on multiple key depression
1 — no error on multiple key depression

N — the number of display digits select
0 — 16 display digits
1 — 8 display digits

NOTE: The default mode following a RESET input is all bits zero:

0	0	0	0	0	0	0	0

Read FIFO Command

CODE	0	1	0	0	0	0	0	0

Read Display Command

CODE	0	1	1	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be read out.

AI=1 AUTO increment
AI=0 no AUTO increment

Write Display Command

CODE	1	0	0	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be written.

Clear/Blank Command

CODE	1	0	1	UD	BD	CD	CF	CE

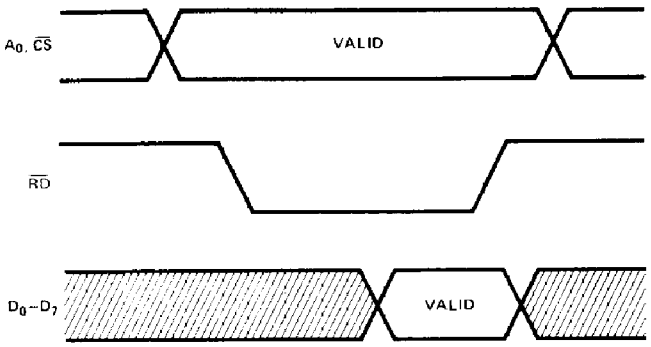
Where the command bits are defined as follows:

CE = Clear ERROR
CF = Clear FIFO
CD = Clear Display RAM to all High
BD = Blank Display to all High (Display RAM unaffected)
UD = Unblank Display

The display is cleared and blanked following a Reset.

8278 Status Read

The status register in the 8278 can be read by the master CPU using the A_0, $\overline{RD}$, and D_0-D_7 inputs as shown below:



The 8278 places 8-bits of status information on the D_0-D_7 lines following (A_0, $\overline{CS}$, $\overline{RD}$) = 1, 0 , 0 inputs from the master.

Status Format

S_3	S_2	S_1	S_0	B	KE	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Where the status bits are defined as follows:

OBF = Output Buffer Full Flag
IBF = Input Buffer Full Flag
KE = Keyboard Error Flag (multiple depression)
B = BUSY Flag
S_3-S_0 = FIFO Status

Status Description

The S_3-S_0 status bits indicate the number of entries (0 to 8) in the 8-level FIFO. A FIFO overrun will lock status at 1111. The overrun condition will prevent further key entries until cleared.

A multiple key closure error will set the KE flag and prevent further key entries until cleared.

The IBF and OBF flags signify the status of the 8278 data buffer registers used to transfer information (data, status or commands) to and from the master CPU.

The IBF flag is set when the master CPU writes Data or Commands to the 8278. The IBF flag is cleared by the 8278 during its response to the Data or Command.

The OBF flag is set when the 8278 has output data ready for the master CPU. This flag is cleared by a master CPU Data READ.

The Busy flag in the status register is used as a LOCK-OUT signal to the master processor during response to any command or data write from the master.

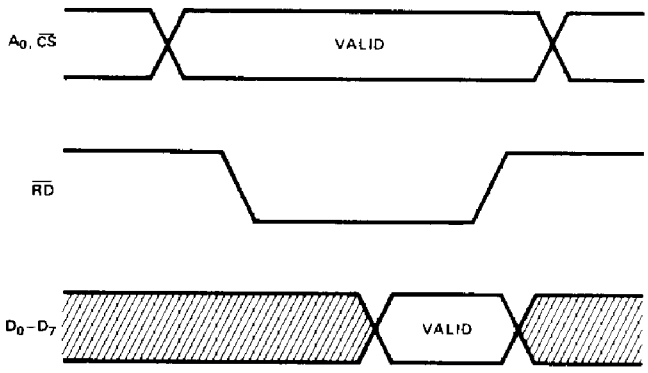
The master must test the Busy flag before each read (during a sequence) to be sure that the 8278 is ready with valid DATA.

The ERROR and TONE outputs from the 8278 are set high for either type of error. Both types of error are cleared by the CLR input, by the CLEAR ERROR command, or by a reset. The FIFO and Display buffers are cleared independently of the Errors.

FIFO status is used to indicate the number of characters in the FIFO and to indicate whether an error has occurred. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO. The character read will be the last one entered. FIFO status will remain at 0000 and the error condition will not be set.

8278 Data Read

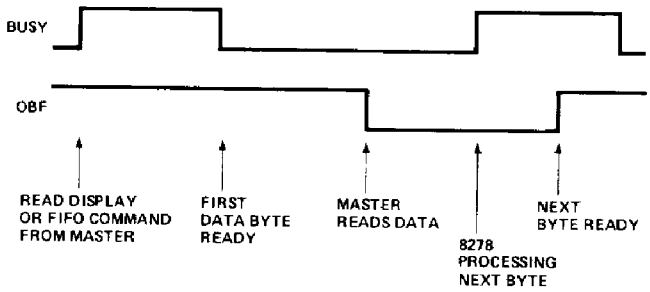
The master CPU can read DATA from the 8278 FIFO or Display buffers by using the A_0, $\overline{RD}$, and D_0-D_7 inputs as follows:



The master sends a $\overline{RD}$ pulse with A_0=0 and CS=0 and the 8278 responds by outputing data on lines D_0-D_7. The data is strobed by the trailing edge of $\overline{RD}$.

Data Read Sequence

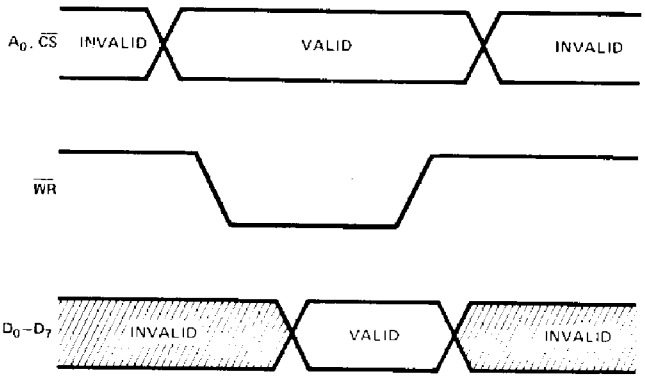
Before reading data, the master CPU must send a command to select FIFO or Display data. Following the command, the master must read STATUS and test the BUSY flag and the OBF flag to verify that the 8278 has responded to the previous command. A typical DATA READ sequence is as follows:



After the first read following a Read Display or Read FIFO command, successive reads may occur as soon as OBF rises.

8278 Data Write

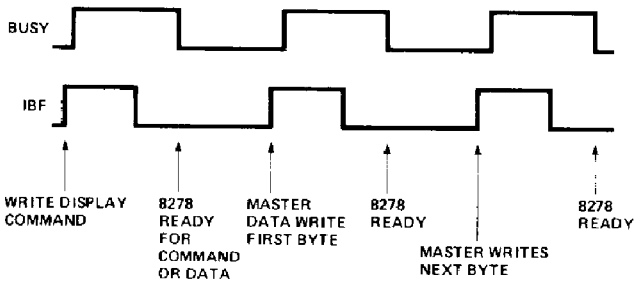
The master CPU can write DATA to the 8278 Display buffers by using the A_0, $\overline{WR}$ and D_0-D_7 inputs as follows:



The master CPU presents the Data on the D_0-D_7 lines with A_0=0 and then sends a $\overline{WR}$ pulse. The data is latched by the 8278 on the rising edge of $\overline{WR}$.

Data Write Sequence

Before writing data to the 8278, the master CPU must first send a command to select the desired display entry mode and to specify the address of the next data byte. Following the commands, the master must read STATUS and test the BUSY flag (B) and IBF flag to verify that the 8278 has responded. A typical sequence is shown below:



INTERFACE CONSIDERATIONS

Scanned Keyboard Mode

With N-key rollover each key depression is treated independently from all others. When a key is depressed the debounce logic waits for a full scan of 128 keys and then checks to see if the key is still down. If it is, the key is entered into the FIFO.

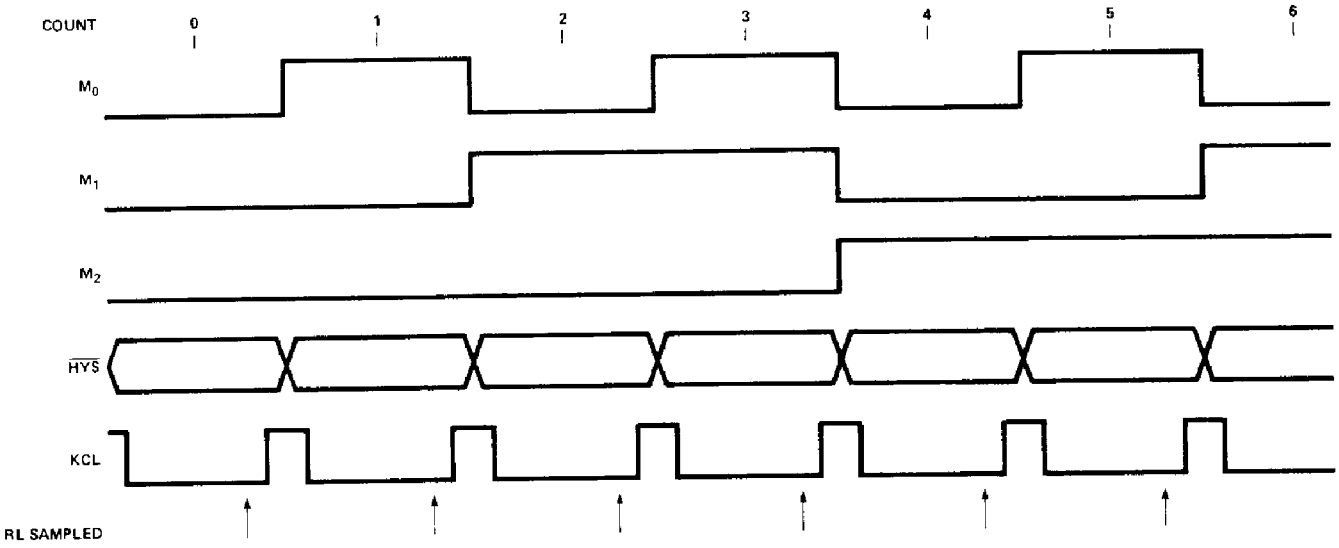


Figure 3. Keyboard Timing

If two key closures occur during the same scan the ERROR output is set, the KE flag is set in the Status word, the TONE output is activated and IRQ is set, and no further inputs are accepted. This condition is cleared by a high signal on the CLEAR input or by a system $\overline{RESET}$ input or by the CLEAR ERROR command.

In the special function mode both the key closure and the key release cause an entry to the FIFO. The release is entered with the MSB=1.

Any key entry triggers the TONE output for 10ms.

The $\overline{HYS}$ and KCL outputs enable the analog multiplexer and detector to be synchronized for interface to capacitive coupled keyboards.

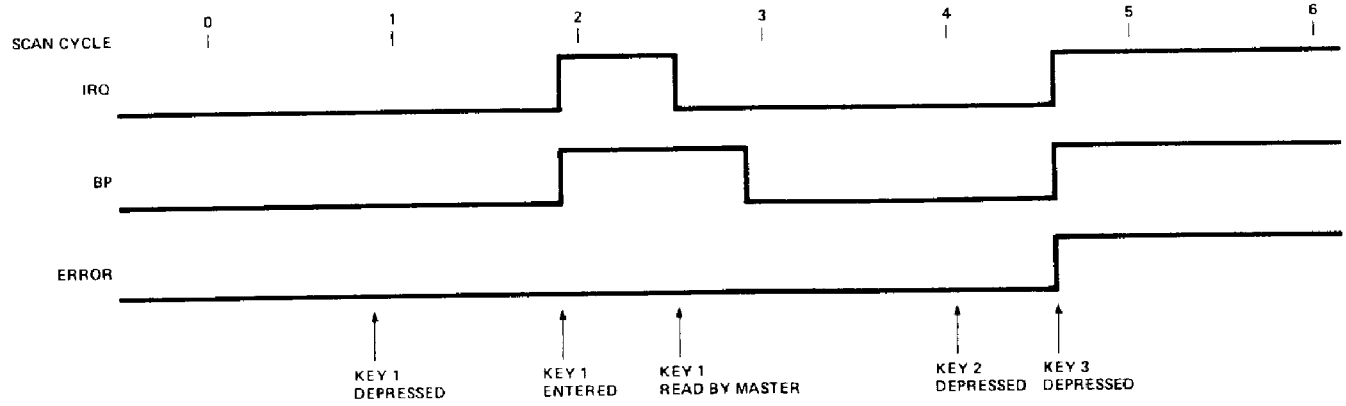
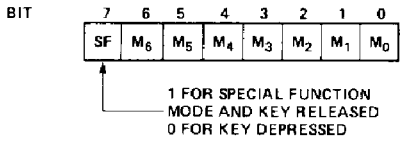


Figure 4. Key Entry and Error Timing

Data Format

In the scanned keyboard mode, the code entered into the FIFO corresponds to the position or address of the switch in the keyboard. The MSB is relevant only for special function keys in which code "0" signifies closure and "1" signifies release. The next four bits are the column count which indicates which column the key was found in. The last three bits are from the row counter.

KEY CODING



Display

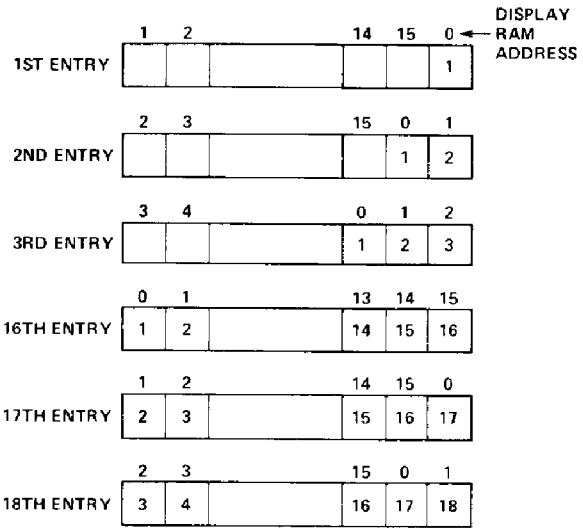
Display data is entered into a 16x4 display register and may be entered from the left, from the right or into specific locations in the display register. A new data character is put out on B_0-B_3 each time the M_6-M_3 lines change (i.e., once every 0.75ms with a 6 MHz crystal). Data is blanked during the time the column select lines change by raising the display outputs. Output data is positive true.

Left Entry

The left entry mode is the simplest display format in that each display position in the display corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 is the right-most display character. Entering characters from position zero causes the display to fill from the left. The 17th character is entered back in the left-most position and filling again proceeds from there.

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right-most display character. The next entry is also placed in the right-most character after the display is shifted left one character. The left-most character is shifted off the end and is lost.



Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended. A Clear Display command should be given before display data is entered if the number of data characters is not equal to 16 (or 8) in this mode.

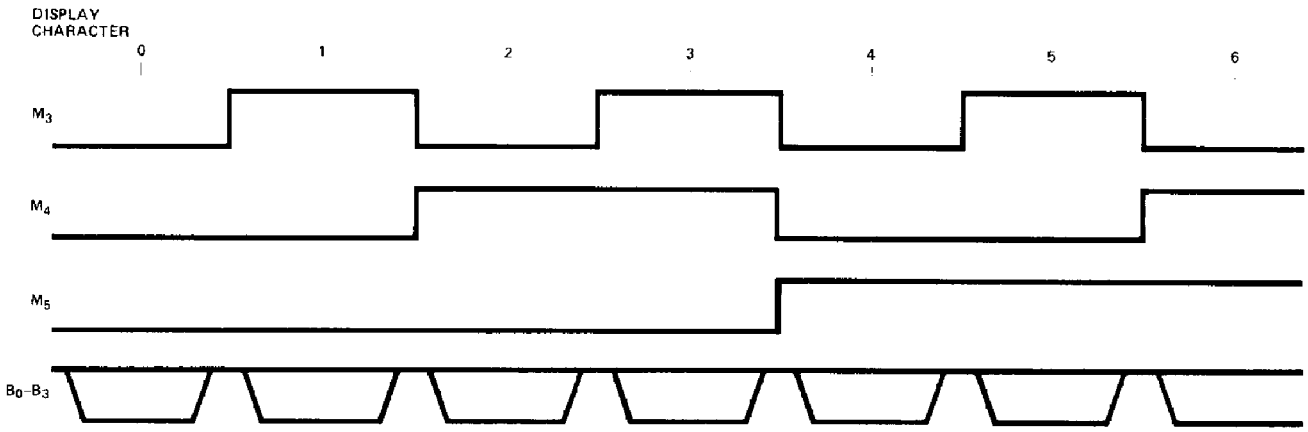
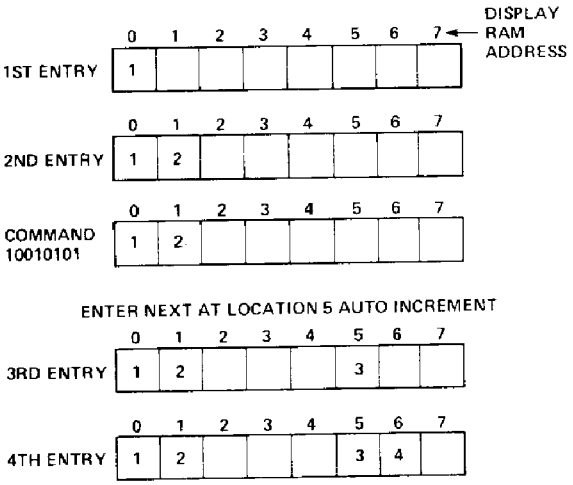


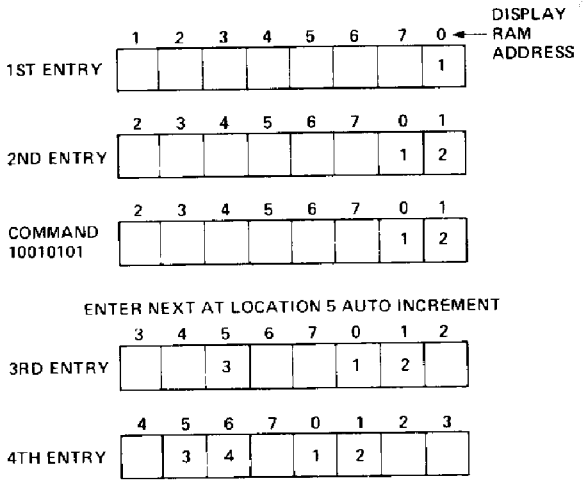
Figure 5. Display Timing

Auto Increment

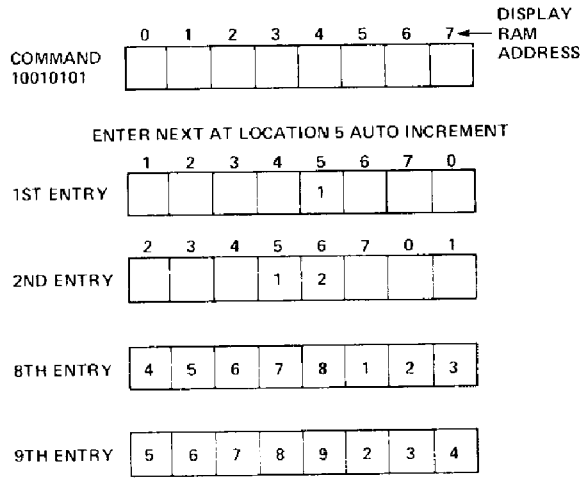
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Left Entry — Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except that the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1.5 Watt

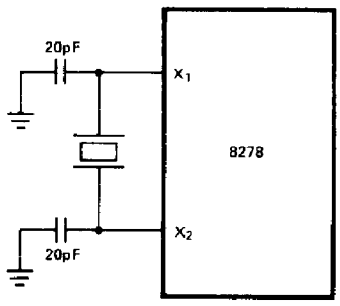
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

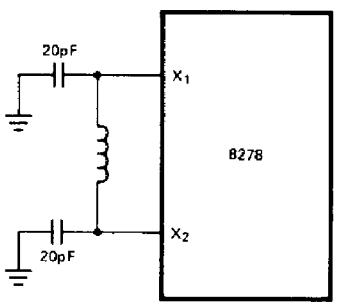
Commercial: T_A = 0°C to 70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Condition
V_{IL}	Input Low Voltage (All Inputs Except X_1, X_2)	-0.5	0.8	V	
V_{IH1}	Input High Voltage (All Inputs Except X_1, X_2, $\overline{RESET}$	2.0	V_{CC}	V	
V_{IH2}	$\overline{RESET}$ High Voltage	3.0	V_{CC}	V	
V_{OL1}	Output Low Voltage (D_0-D_7)		0.45	V	I_{OL} = 2.0mA
V_{OL2}	Output Low Voltage (All Other Outputs)		0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage (D_0-D_7)	2.4		V	I_{OH} = -400μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4		V	I_{OH} = -50μA
I_{IL}	Input Leakage Current (All Inputs Except $\overline{RESET}$)		±10	μA	V_{IN} = V_{CC}
I_{OL}	Output Leakage Current (D_0-D_7)		±10	μA	V_{IN} = V_{SS} + 0.45V or V_{IN} = V_{CC}
I_{DD} + I_{CC}	Total Supply Current		135	mA	V_{CC} = 5.5V
I_{DD}	V_{DD} Supply Current		25	mA	V_{CC} = 5.5V
I_{LI}	Low Input Source Current ($\overline{RESET}$)		0.2	mA	V_{IL} = 0.8V

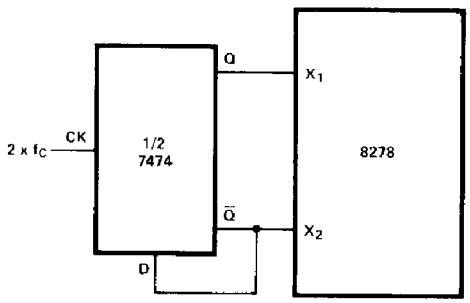
8278 CLOCK OPTIONS



1-6 MHz CRYSTAL



40 μh-130 μh INDUCTOR



EXTERNAL CLOCK

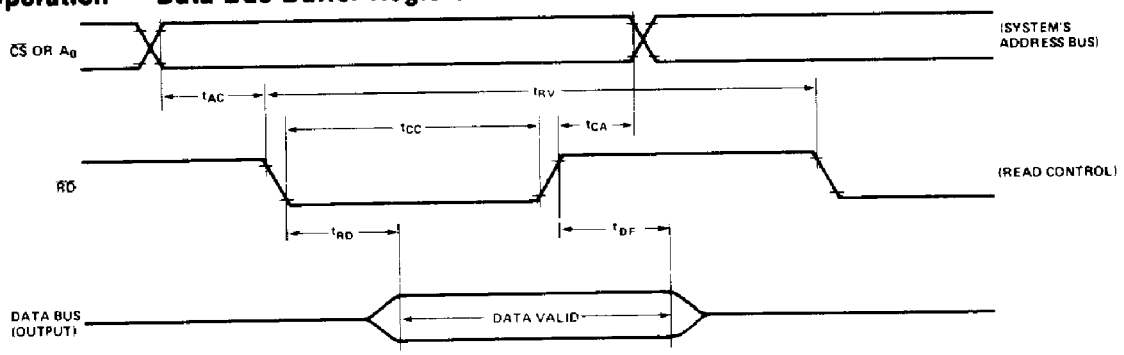
A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5V ±10%; V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Condition
t_{AC}	Address ($\overline{CS}$, A_0) Setup to Control ($\overline{RD}$, $\overline{WR}$)	0		ns	D_0-D_7, C_L = 150pF
t_{CA}	Address Hold from Control	0		ns	
t_{CC}	Control Pulse Width	250		ns	
t_{DW}	Data in Setup to $\overline{WR}$ T.E.	150		ns	
t_{WD}	Data in Hold After $\overline{WR}$ T.E.	0		ns	
t_{RD}	$\overline{RD}$ L.E. to Data Out Valid		150	ns	
t_{DF}	$\overline{RD}$ T.E. to Data Out Float	10	100	ns	
t_{MCY}	Matrix Cycle Time		10.7	ms	With 6MHz Crystal
t_{RV}	Recovery Time Between Reads and/or Writes	1		μs	

WAVEFORMS

Read Operation — Data Bus Buffer Register



Write Operation — Data Bus Buffer Register