Intel® 865G/865GV Chipset

Datasheet

Intel® 82865G/82865GV Graphics and Memory Controller Hub (GMCH)

February 2004

Document Number: 252514-005

Contents

Figures

Tables

Revision History

Revision	Description	Date
-001	• Initial Release	May 2003
-002	• Corrected A0-A3 ACAPID Register Default Value in Table 6, Section 3.5.	June 2003
-003	• Corrected bit A1 in Table 24, RAM Address Translation, 512mb, 64Mx8, from bit 15 to 16.	June 2003
-004	• Added 82865GV information	September 2003
-005	• Replaced Figure 19 in Section 7.2	February 2004

Intel® 82865G GMCH Features

- Host Interface Support
  - — Intel® Pentium® 4 processors with 512-KB L2 cache on 0.13 micron process / Pentium 4 processor on 90 nm process
  - — VTT 1.1 V – 1.55 V ranges
  - — 64-bit FSB frequencies of 400 MHz (100 MHz bus clock), 533 MHz (133 MHz bus clock), and 800 MHz (200 MHz bus clock). Maximum theoretical BW of 6.4 GB/s.
  - — FSB Dynamic Bus Inversion on the data bus
  - — 32-bit addressing for access to 4 GB of memory space
  - — 12-deep In Order Queue
  - — AGTL+ On-die Termination (ODT)
  - — Hyper-Threading Technology
- System Memory Controller Support
  - — Dual-channel (128 bits wide) DDR memory interface
  - — Single-channel (64 bits wide) DDR operation supported
  - — Symmetric and asymmetric memory dual-channel upgrade supported
  - — 128-Mb, 256-Mb, 512-Mb technologies implemented as x8, x16 devices
  - — Four bank devices
  - — Non-ECC, un-buffered DIMMS only
  - — Maximum of two DIMMs per channel, with each DIMM having one or two rows
  - — Up to 4 GB system memory
  - — Supports up to 16 simultaneously-open pages (four per row) in dual-channel mode and up to 32 open pages in single-channel mode
  - — 4-KB to 64-KB page sizes (4 KB to 32 KB in single-channel, 8 KB to 64 KB in dual-channel)
  - — Supports opportunistic refresh
  - — Suspend-to-RAM support using CKE
  - — SPD (Serial Presence Detect) Scheme for DIMM Detection supported
  - — Supports selective Command-Per-Clock (selective CPC) Accesses
  - — DDR (Double Data Rate type 1) Support
    - Supports maximum of two DDR DIMMs per channel, single-sided and/or double-sided
    - Supports DDR266, DDR333, DDR400 DIMM modules
    - Supports DDR channel operation at 266 MHz, 333 MHz and 400 MHz with a Peak BW of 2.1 GB/s, 2.7 GB/s, and 3.2GB/s respectively per channel
    - Burst length of 4 and 8 for single-channel (32 or 64 bytes per access, respectively); for dual-channel a burst of 4 (64 bytes per access)
    - Supports SSTL_2 signaling
- Communication Streaming Architecture (CSA) Interface
  - — Gigabit Ethernet (GbE) communication devices supported on the CSA interface (e.g., Intel® 82547EI GbE controller)
  - — Supports 8-bit Hub Interface 1.5 electrical/transfer protocol
  - — 266 MB/s point-to-point connection
  - — 1.5 V operation
- Hub Interface (HI)
  - — Supports Hub Interface 1.5 electrical/transfer protocol
  - — 266 MB/s point-to-point connection to the ICH5
  - — 66 MHz base clock
  - — 1.5 V operation
- AGP Interface Support
  - — A single AGP device
  - — AGP 3.0 with 4X / 8X AGP data transfers and 4X / 8X fast writes, respectively
  - — 32-bit 4X/8X data transfers and 4X/8X fast writes
  - — Peak BW of 2 GB/s.
  - — 0.8 V and 1.5 V AGP signalling levels; no 3.3 V support
  - — AGP 2.0 1X/4X AGP data transfers and 4X fast writes
  - — 32-deep AGP request queue
- Integrated Graphics
  - — Core Frequency of 266 MHz
  - — VGA/UMA Support
  - — High Performance 3D Setup and Render Engine
  - — High-Quality/Performance Texture Engine
  - — 3D Graphics Rendering Enhancements
  - — 2D Graphics
  - — Video DVD/PC-VCR
  - — Video Overlay
  - — Video Mixer Render Supported (VMR)
  - — Bi-Cubic Filter Support
- Display Interfaces
  - — AGP signals multiplexed with two DVO ports (ADD card supported)
  - — Multiplexed Digital Display Channels (Supported with ADD Card)
- Analog Display Support
  - — 350 MHz Integrated 24-bit RAMDAC
  - — Up to 2048x1536 @ 75 Hz refresh
  - — Hardware Color Cursor
  - — DDC2B Compliant Interface
  - — Simultaneous Display options with digital display
- Digital Display Channels
  - — Two channels multiplexed with AGP
  - — 165 MHz dot clock on each 12-bit interface
  - — Can combine two, 12-bit channels to form one, 24-bit interface Supports flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1920x1080 @ 85 Hz
  - — Supports Hot Plug and Display
  - — Supports LVDS, TMDS transmitters or TV-out encoders
  - — ADD card utilizes AGP connector
  - — Supports one additional flat panel (dCRT) and/or one TV (only when using internal GFX)
  - — Three Display Control interfaces (I^2C/DDC) multiplexed on AGP
- GMCH Package
  - — 37.5 mm x 37.5 mm Flip Chip Ball Grid Array (FC-BGA) package
  - — 932 solder balls with variable ball pitch

This page is intentionally left blank.

Introduction 1

The Intel® 82865G and the Intel®82865GV chipsets are designed for use in desktop systems based on an Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package or the Intel® Pentium® 4 processor on 90 nm process, and supports FSB frequencies of 400 MHz, 533 MHz, and 800 MHz. The 82865G GMCH is part of the Intel® 865G chipset, the 82865GV GMCH is part of the Intel® 865GV chipset. Each chipset contains two main components: Graphics and Memory Controller Hub (GMCH) for the host bridge and I/O Controller Hub for the I/O subsystem. The GMCH provides the processor interface, system memory interface, hub interface, CSA interface and other additional interfaces in an 865G/ 865GV chipset desktop platform. Each GMCH contains an integrated graphics controller (IGD). The 865G /865GV chipset use either the 82801EB ICH5 or 82801ER ICH5R for the I/O Controller Hub. This document is the datasheet for the 82865G and the 82865GV Graphics and Memory Controller Hub (GMCH) component.

The following are the key feature differences between the 82865G GMCH and 82865GV GMCH:

- AGP Interface
  - — 82865G supports AGP. The AGP interface signals are multiplexed with the Intel® DVO interface signals. The 82865GV does not support AGP.

The Intel® 865G/865GV chipset platform supports the following processors:

- Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package.
- Intel® Pentium® 4 processor on 90 nm process.

Note: Unless otherwise specified, the term processor in this document refers to the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in the 478-pin package and the Pentium 4 processor on 90 nm process.

Note: Unless otherwise specified, the term ICH5 in this document refers to both the 82801EB ICH5 and 82801ER ICH5R.

Chapter 1 through Chapter 8 describe the 82865G GMCH. The 82865GV GMCH is described in Chapter 9 through Chapter 11.

1.1 Terminology

This section provides the definitions of some of the terms used in this document.

Table 1. General Terminology (Sheet 1 of 2)

Terminology	Description
AGP	Accelerated Graphics Port. In this document AGP refers to the AGP/PCI interface that is in the GMCH. The GMCH AGP interface supports only 0.8 V/1.5 V AGP 2.0/AGP 3.0 compliant devices using PCI (66 MHz), AGP 1X (66 MHz), 4X (266 MHz), and 8X (533 MHz) transfers. GMCH does **not** support any 3.3 V devices. For AGP 2.0, PIPE# and SBA addressing cycles and their associated data phases are generally referred to as AGP transactions. FRAME# cycles are generally referred to as AGP/PCI transactions.
Bank	DRAM chips are divided into multiple banks internally. Commodity parts are all 4 bank, which is the only type the GMCH supports. Each bank acts somewhat like a separate DRAM, opening and closing pages independently, allowing different pages to be open in each. Most commands to a DRAM target a specific bank, but some commands (i.e., Precharge All) are targeted at all banks. Multiple banks allows higher performance by interleaving the banks and reducing page miss cycles.
Channel	In the GMCH a DRAM channel is the set of signals that connect to one set of DRAM DIMMs. The GMCH has two DRAM channels, (a pair of DIMMs added at a time, one on each channel).
Chipset Core	The GMCH internal base logic.
Column Address	The column address selects one DRAM location, or the starting location of a burst, from within the open page on a read or write command.
Double-Sided DIMM	Terminology often used to describe a DIMM that contains two DRAM rows. Generally, a double-sided DIMM contains two rows, with the exception noted above. This terminology is not used in this document.
DDR	Double Data Rate SDRAM. DDR describes the type of DRAMs that transfer two data items per clock on each pin. This is the only type of DRAM supported by the GMCH.
Full Reset	A Full GMCH Reset is defined in this document when RSTIN# is asserted.
GART	Graphics Aperture Re-map Table. GART is a table in memory containing the page re-map information used during AGP aperture address translations.
GMCH	Graphics and Memory Controller Hub. The GMCH component contains the processor interface, SDRAM controller, AGP interface, CSA interface and an integrated 3D/2D/display graphics core. It communicates with the I/O controller hub (Intel® ICH5) over a proprietary interconnect called HI.
GTLB	Graphics Translation Look-aside Buffer. A cache used to store frequently used GART entries.
Graphics Core	The internal graphics related logic in the GMCH.
HI	Hub Interface. HI is the proprietary hub interface that connects the GMCH to the ICH5. In this document HI cycles originating from or destined for the primary PCI interface on the ICH5 are generally referred to as HI/PCI or simply HI cycles.
Host	This term is used synonymously with processor.
Intel® ICH5	Fifth generation IO Controller Hub component that contains additional functionality compared to the ICH4.
IGD	Integrated Graphics Device. IGD refers to the graphics device integrated into the GMCH.
Primary PCI	The physical PCI bus that is driven directly by the ICH5 component. Communication between PCI and the GMCH occurs over the hub interface. Note that even though the Primary PCI bus is referred to as PCI, it is **not** PCI Bus 0 from a configuration standpoint.
FSB	Processor Front-Side Bus. This is the processor system bus.
Row	A group of DRAM chips that fill out the data bus width of the system and are accessed in parallel by each DRAM command.

Table 1. General Terminology (Sheet 2 of 2)

Terminology	Description
Row Address	The row address is presented to the DRAMs during an Activate command, and indicates which page to open within the specified bank (the bank number is presented also).
Scalable Bus	Processor-to-GMCH interface. The compatible mode of the Scalable Bus is the P6 Bus. The enhanced mode of the Scalable Bus is the P6 Bus plus enhancements primarily consisting of source synchronous transfers for address and data, and FSB interrupt delivery. The Intel® Pentium® 4 processor implements a subset of the enhanced mode.
Single-Sided DIMM	Terminology often used to describe a DIMM that contains one DRAM row. Usually one row fits on a single side of the DIMM allowing the backside to be empty.
SDR	Single Data Rate SDRAM.
SDRAM	Synchronous Dynamic Random Access Memory.
Secondary PCI	The physical PCI interface that is a subset of the AGP bus driven directly by the GMCH. It supports a subset of 32-bit, 66 MHz PCI 2.0 compliant components, but only at 1.5 V (not 3.3 V or 5 V).
SSTL_2	Stub Series Terminated Logic for 2.6 Volts (DDR)

1.2 Related Documents

Document	Document Number/ Location
Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/252518.htm
Intel® 865G/865GV/865PE/865P Chipset Thermal Design Guide	http://developer.intel.com/design/chipsets/designex/252519.htm
Intel® 865G/865GV/865PE/865P Chipset Schematics	http://developer.intel.com/design/chipsets/schematics/252813.htm
Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 processor on 90 nm Process w/Loadline A Platforms - 2 Phase VR	http://developer.intel.com/design/chipsets/schematics/300683.htm
Intel® 865G/865GV/865PE/865P Chipset CRB Schematics Addendum for the Intel® Pentium® 4 processor on 90 nm Process w/Loadline A Platforms - 3 Phase VR	http://developer.intel.com/design/chipsets/schematics/300684.htm
Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet	http://developer.intel.com/design/chipsets/specupdt/252517.htm
Intel® Pentium® 4 processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet	http://developer.intel.com/design/pentium4/datashts/298643.htm
Intel® Pentium® 4 processor on 90 nm Process Datasheet	http://developer.intel.com/design/pentium4/datashts/300561.htm
Intel® Pentium® 4 processor on 90 nm Process Thermal and Mechanical Design Guide	http://developer.intel.com/design/Pentium4/guides/300564.htm
JEDEC Double Data Rate (DDR) SDRAM Specification	www.jedec.org

Document	Document Number/ Location
Intel® PC SDRAM Specification	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
Accelerated Graphics Port Interface Specification, Revision 2.0	http://www.intel.com/technology/agp/agp_index.htm
Digital Visual Interface (DVI) Specification, Revision 1.0	http://www.ddwg.org/downloads.html

NOTE: For additional related documents, refer to the *Intel® 865G//865GV865PE/865P Chipset Platform Design Guide*.

1.3 Intel® 865G Chipset System Overview

Figure 1 shows an example block diagram of an 865G chipset-based platform. The 865G chipset is designed for use in a desktop system based on a Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor on 90 nm process. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol. The GMCH provides the processor interface, system memory interface, CSA interface, AGP interface, hub interface, and additional interfaces. The GMCH contains and integrated graphics device.

The 865G chipset platform supports either an integrated graphics device (IGD) or an external graphics device on AGP. The IGD has 3D, 2D, and video capabilities. The IGD also has two multiplexed Intel DVO ports to support DVO devices. The GMCH's AGP interface supports 1X/4X/8X AGP data transfers and 4X/8X AGP Fast Writes, as defined in the *Accelerated Graphics Port Interface Specification, Revision 3.0*.

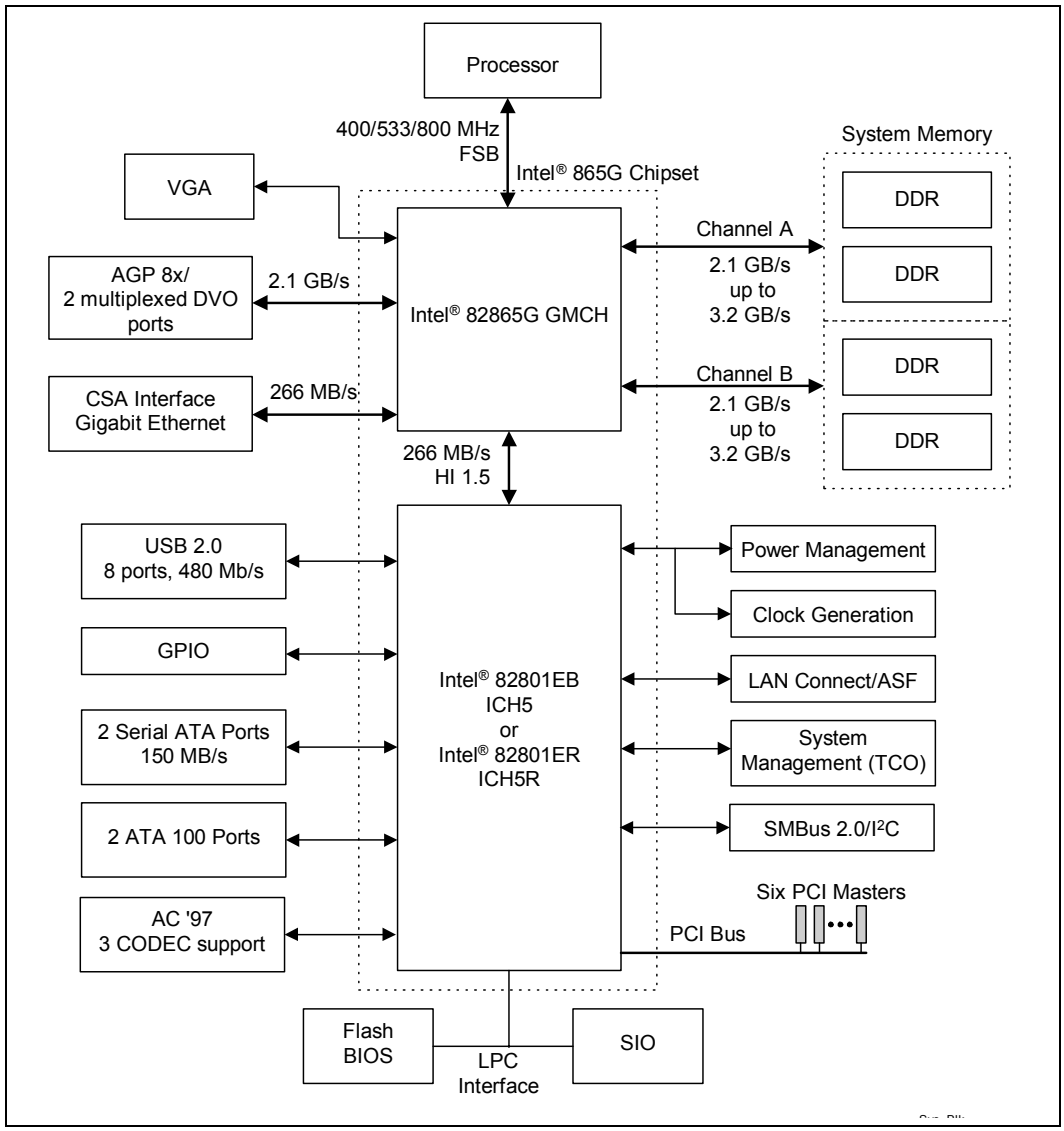
The GMCH provides a Communications Streaming Architecture (CSA) Interface that connects the GMCH to a Gigabit Ethernet (GbE) controller.

The 865G chipset platform supports 4 GB of system memory and has a maximum bandwidth of 6.4 GB/s using DDR400 in dual-channel mode.

The 82801EB ICH5 integrates an Ultra ATA 100 controller, two Serial ATA host controllers, one EHCI host controller, and four UHCI host controllers supporting eight external USB 2.0 ports, LPC interface controller, flash BIOS interface controller, PCI interface controller, AC '97 digital controller, integrated LAN controller, an ASF controller and a hub interface for communication with the GMCH. The ICH5 component provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance. The 82801ER ICH5R elevates Serial ATA storage performance to the next level with Intel® RAID Technology.

The ACPI compliant ICH5 platform can support the Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH5 also supports Alert Standard Format for remote management.

Figure 1. Intel® 865G Chipset System Block Diagram



1.4 Intel® 82865G GMCH Overview

The GMCH provides the host bridge interfaces and has an integrated graphics device with display interfaces. The GMCH contains advanced desktop power management logic.

The GMCH's role in a system is to provide high performance integrated graphics and manage the flow of information between its six interfaces: the processor front side bus (FSB), the memory attached to the SDRAM controller, the AGP 3.0 port, the hub interface, CSA interface, and display interfaces. This includes arbitrating between the six interfaces when each initiates an operation. While doing so, the GMCH supports data coherency via snooping and performs address translation for accesses to the AGP aperture memory. To increase system performance, the GMCH incorporates several queues and a write cache.

1.4.1 Host Interface

The GMCH supports a single, Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol. The GMCH supports FSB frequencies of 400/533/800 MHz (100 MHz, 133 MHz, and 200 MHz HCLK, respectively) using a scalable FSB VCC_CPU. It supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space.

Host-initiated I/O cycles are decoded to AGP/PCI_B, Hub Interface, or the GMCH configuration space. Host-initiated memory cycles are decoded to AGP/PCI_B, Hub Interface or system memory. All memory accesses from the host interface that hit the graphics aperture are translated using an AGP address translation table. AGP/PCI_B device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from AGP/PCI_B using PCI semantics and from hub interface to system SDRAM will be snooped on the host bus.

1.4.2 System Memory Interface

The GMCH integrates a system memory DDR controller with two, 64-bit wide interfaces (up to two channels of DDR). Only Double Data Rate (DDR) SDRAM memory is supported; thus, the buffers support only SSTL_2 signal interfaces. The memory controller interface is fully configurable through a set of control registers.

System Memory Interface

- Supports one or two 64-bit wide DDR data channels
- Available bandwidth up to 3.2 GB/s (DDR400) for single-channel mode and 6.4 GB/s (DDR400) in dual-channel mode.
- Support for non ECC DIMMs
- Supports 128-Mb, 256-Mb, 512-Mb DDR technologies
- Supports only x8, x16, DDR devices with 4-banks
- Registered DIMMs not supported
- Supports opportunistic refresh
- Up to 16 simultaneously open pages (four per row, four rows maximum)
- SPD (Serial Presence Detect) scheme for DIMM detection support
- Suspend-to-RAM support using CKE
- Supports configurations defined in the JEDEC DDR1 DIMM specification only

Single-Channel DDR Configuration

- Up to 4.0 GB of DDR
- Supports up to four DDR DIMMs (2 DIMMs per channel), single-sided and/or double-sided
- Supports DDR266, DDR333, and DDR400 unregistered non-ECC DIMMs
- Supports up to 32 simultaneous open pages
- Does not support mixed-mode / uneven double-sided DDR DIMMs

Dual-Channel DDR Configuration - Lockstep

- Up to 4.0 GB of DDR
- Supports up to four DDR DIMMs, single-sided and/or double-sided
- DIMMS must be populated in identical pairs for dual-channel operation
- Supports 16 simultaneous open pages (four per row)
- Supports DDR266, DDR333, and DDR400 unregistered non-ECC DIMMs

1.4.3 Hub Interface

Communication between the GMCH and the ICH5 occurs over the hub interface. The GMCH supports HI 1.5 that uses HI 1.0 protocol with HI 2.0 electrical characteristics. The hub interface runs at 266 MT/s (with 66 MHz base clock) and uses 1.5 V signaling. Acceses between hub interface and AGP/PCI_B are limited to hub interface-originated memory writes to AGP.

1.4.4 Communications Streaming Architecture (CSA) Interface

The CSA interface connects the GMCH with a Gigabit Ethernet (GbE) controller. The GMCH supports HI 1.5 over the interface that uses HI 1.0 protocol with HI 2.0 electrical characteristics. The CSA interface runs at 266 MT/s (with 66 MHz base clock) and uses 1.5 V signaling.

1.4.5 Multiplexed AGP and Intel® DVO Interface

The GMCH multiplexes an AGP interface with two Intel® DVOs ports.

AGP Interface

A single AGP or PCI 66 component or connector (not both) is supported by the GMCH's AGP interface. Support for AGP 3.0 includes 0.8 V and 1.5 V AGP electrical characteristics. Support for a single PCI-66 device is limited to the subset supported by the AGP 2.0 specification. An external graphics accelerator is not a requirement due to the GMCH's integrated graphics capabilities. The BIOS will disable the IGD if an external AGP device is detected. The AGP PCI_B buffers operate only in the 1.5 V mode and support the AGP 1.5 V connector.

The AGP/PCI_B interface supports up to 8X AGP signaling and up to 8X Fast Writes. AGP semantic cycles to system DDR are not snooped on the host bus. PCI semantic cycles to system DDR are snooped on the host bus. The GMCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. The GMCH contains a 32 deep AGP request queue. High-priority accesses are supported.

DVO Multiplexed Interface

The GMCH supports two multiplexed DVO ports that each drive pixel clocks up to 165 MHz. The DVO ports can each support a single-channel DVO device. If both ports are active in single-channel mode, they will have identical display timings and data. Alternatively, the DVO ports can be combined to support dual-channel devices that have higher resolutions and refresh rates. The GMCH can make use of these digital display channels via an AGP Digital Display (ADD) card.

1.4.6 Graphics Overview

The GMCH provides an integrated graphics accelerator delivering cost competitive 3D, 2D, and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, BLT and Stretch BLT operations, motion compensation, overlay, and display control. The GMCH's video engines support video conferencing and other video applications. The GMCH does **not** support a dedicated local graphics memory interface; it may only be used in a UMA configuration. The GMCH also has the capability to support external graphics accelerators via AGP; The IGD cannot work concurrently with an external AGP graphics device.

High bandwidth access to data is provided through the system memory port. The GMCH can access local and AGP graphics data located in system memory to 4.2 GB/s (DDR266), 5.4 GB/s (DDR333), or 6.4 GB/s (DDR400) depending on whether single/dual channel memory configuration.

The GMCH also provides 2D hardware acceleration for block-level transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces processor load, and thus improves performance. The internal graphics device incorporated in the GMCH is incapable of operating in parallel with an attached AGP device.

The graphics features on the GMCH include the following:

- **Core Frequency of 266 MHz**
- **VGA/UMA Support**
- **High Performance 3D Setup and Render Engine**
  - — Setup matching processor geometry delivery rates
  - — Triangle Lists, Strips and Fans Support
  - — Indexed Vertex and Flexible Vertex Formats
  - — Vertex Cache
  - — Pixel Accurate Fast Scissoring and Clipping Operation
  - — Backface Culling Support
  - — Supports D3D and OGL Pixelization Rules
  - — Anti-aliased Lines Support
  - — Sprite Points Support
- **High-Quality/Performance Texture Engine**
  - — Per Pixel Perspective Corrected Texture Mapping
  - — Single Pass Quad Texture Compositing
  - — Enhanced Texture Blending Functions
  - — 12 Level of Detail MIP Map Sizes from 1x1 to 2Kx2K
  - — All texture formats including 32-bit RGBA and 8-bit palettes
  - — Alpha and Luminance Maps
  - — Texture Color-keying/ChromaKeying
  - — Bilinear, Trilinear and Anisotropic MIP-Mapped Filtering
  - — Cubic Environment Reflection Mapping
  - — Embossed and DOT3 Bump-Mapping
  - — DXTn Texture Decompression
  - — FXT1 Texture Compression
  - — Non-power of 2 Texture
  - — Render to Texture
- **2D Graphics**
  - — Optimized 256-bit BLT Engine
  - — Alpha Stretch Blitter
  - — Anti-aliased Lines
  - — 32-bit Alpha Blended Cursor
  - — Color Space Conversion
  - — Programmable 3-Color Transparent Cursor
  - — 8-, 16- and 32-bit Color
  - — ROP Support
- **3D Graphics Rendering Enhancements**
  - — Flat and Gouraud Shading
  - — Color Alpha Blending For Transparency
  - — Vertex and Programmable Pixel Fog and Atmospheric Effects
  - — Color Specular Lighting
  - — Z Bias Support
  - — Dithering
  - — Line and Full-scene Anti-Aliasied
  - — 16- and 24-bit Z Buffering
  - — 16- and 24-bit W Buffering
  - — 8-bit Stencil Buffering
  - — Double and Triple Render Buffer Support
  - — 16- and 32-bit Color
  - — Destination Alpha
  - — Vertex Cache
  - — Maximum 3D Resolution Supported: 1600x1200x32 @ 85Hz
  - — Fast Clear Support
- **Video DVD/PC-VCR**
  - — Hardware Motion Compensation for MPEG2
  - — Dynamic Bob and Weave Support for Video Streams
  - — Synclock Display and TV-out to video source
  - — Source Resolution up to 1280x720 with 3-vertical taps and 1920x1080 with 2-vertical taps
  - — Software DVD At 30 fps, Full Screen
  - — Supports 720x480 DVD Quality Encoding at low processor Utilization for PC-VCR or home movie recording and editing
  - — Video Overlay
  - — Single High Quality Scalable Overlay
  - — Multiple Overlay Functionality provided via Stretch Blitter (PIP, Video Conferencing, etc.)
  - — 5-tap Horizontal, 3-tap Vertical Filtered Scaling
  - — Independent Gamma Correction
  - — Independent Brightness/Contrast/Saturation
  - — Independent Tint/Hue Support
  - — Destination Color-keying
  - — Source ChromaKeying
  - — Maximum Source Resolution: 720x480x32
  - — Maximum Overlay Display Resolution: 2048x1536x32
- **Video Mixer Render Supported (VMR)**
- **Bi-Cubic Filter Support**

1.4.7 Display Interface

The GMCH provides interfaces to a progressive scan analog monitor and two DVOs (multiplexed with AGP) capable of driving an ADD card. The digital display channels are capable of driving a variety of DVO devices (e.g., TMDS, LVDS, and TV-Out).

- The GMCH has an integrated 350 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 2048x1536 @ 75Hz.
- The GMCH provides two multiplexed DVOs that are capable of driving a 165 MHz pixel clock. It is possible to combine the two multiplexed DVO ports to drive larger digital displays.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

1.5 Clock Ratios

Table 2 lists the supported system memory clock ratios. AGP, CSA, and HI run at 66 MHz common clock and are asynchronous to the chipset core. There is no required skew or ratio between FSB/chipset core and 66 MHz system clocks.

Table 2. System Memory Clock Ratios

Host Clock	DRAM Clock	Ratios	DRAM Data Rate	DRAM Type	Peak Bandwidth
100 MHz	133 MHz	3/4	266 MT/s	DDR-DRAM	2.1 GB/s
133 MHz	133 MHz	1/1	266 MT/s	DDR-DRAM	2.1 GB/s
200 MHz	133 MHz	3/2	266 MT/s	DDR-DRAM	2.1 GB/s
133 MHz	166 MHz	4/5	333 MT/s	DDR-DRAM	2.7 GB/s
200 MHz	160 MHz	5/4	320 MT/s	DDR-DRAM	2.6 GB/s
200 MHz	200 MHz	1/1	400 MT/s	DDR-DRAM	3.2 GB/s

Signal Description 2

This chapter provides a detailed description of the GMCH signals. The signals are arranged in functional groups according to their associated interface (see Figure 2).

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
s/t/s	Sustained Tri-state. This pin is driven to its inactive state prior to tri-stating.

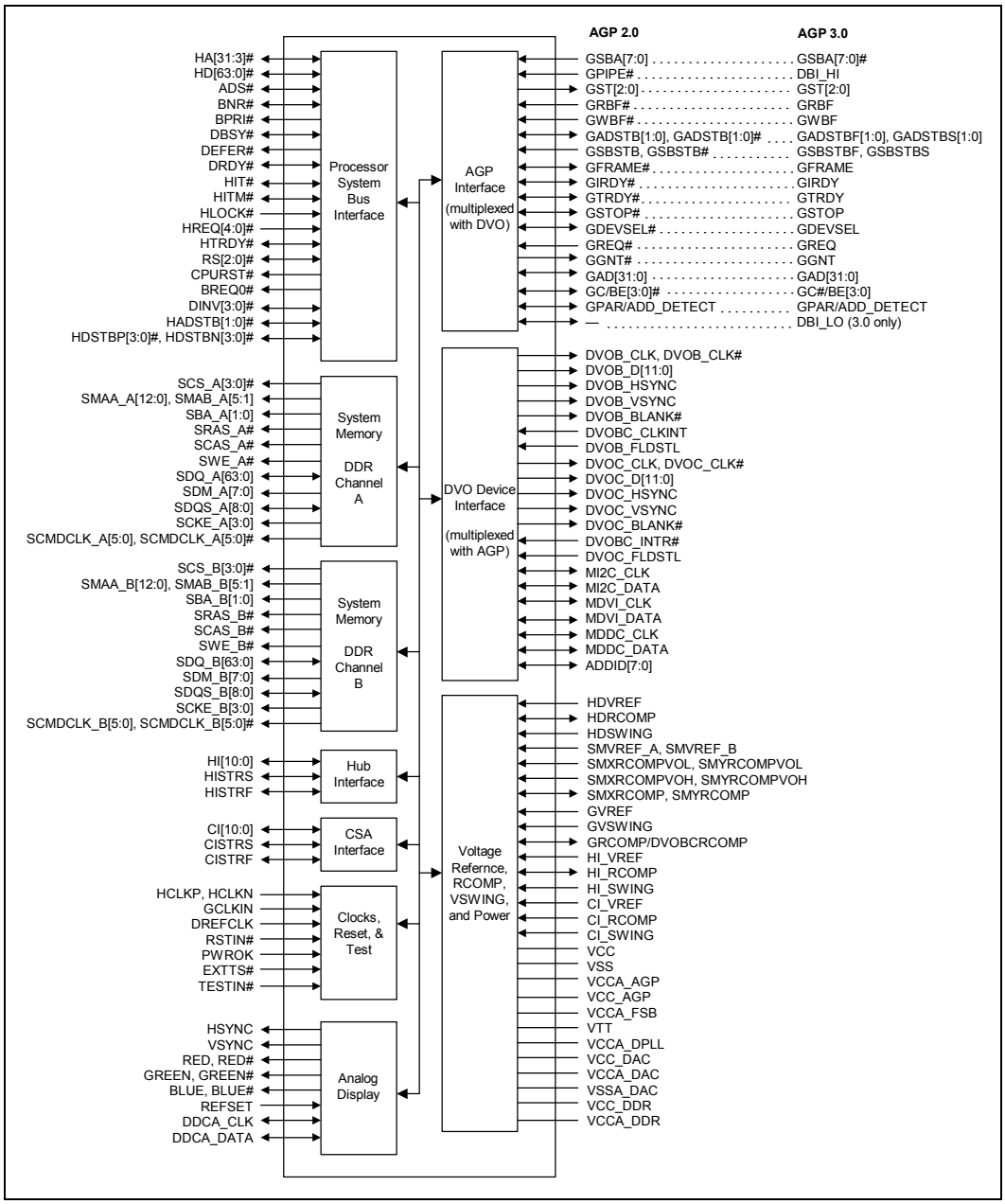
The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and supports VTT from 1.15 V to 1.55 V (not including guard banding)
AGP	AGP interface signals. These signals are compatible with AGP 2.0 1.5 V signaling and AGP 3.0 0.8 V swing signaling Environment DC and AC Specifications. The buffers are not 3.3 V tolerant.
HI15	Hub Interface 1.5 compatible signals
LVTTL	Low Voltage TTL 3.3 V compatible signals
SSTL_2	Stub Series Terminated Logic 2.6 V compatible signals.
2.6 VGPIO	2.6 V buffers used for misc GPIO signals
3.3 VGPIO	3.3 V buffers used for DAC/DCC signals
CMOS	CMOS buffers.

Host interface signals that perform multiple transfers per clock cycle may be marked as either "4X" (for signals that are "quad-pumped") or 2X (for signals that are "double-pumped").

Note that the processor address and data bus signals are logically inverted signals. In other words, the actual values are inverted from what appears on the processor bus. This has been taken into account in the 865G chipset and the address and data bus signals are inverted inside the GMCH host bridge. All processor control signals follow normal convention. A 0 (zero) indicates an active low level (low voltage) if the signal name is followed by # symbol; a 1 (one) indicates an active high level (high voltage) if the signal has no # suffix.

Figure 2. Intel® 82865G GMCH Interface Block Diagram



2.1 Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The processor bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** BNR# is used to block the current request bus owner from issuing a new requests. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	O AGTL+	**Priority Agent Bus Request:** The GMCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ0# signal low during CPURST#. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. BREQ0# should be terminated high (pulled up) after the hold time requirement has been satisfied. **NOTE:** This signal is called BR0# in the Intel® Pentium® 4 processor specifications.
BSEL[1:0]	I CMOS	**Core / FSB Frequency (FSBFREQ) Select Strap:** This strap is latched at the rising edge of PWROK. These pins has no default internal pull-up resistor. 00 = Core frequency is 100 MHz, FSB frequency is 400 MHz 01 = Core frequency is 133 MHz, FSB frequency is 533 MHz 10 = Core frequency is 200 MHz, FSB frequency is 800 MHz 11 = Reserved
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RSTIN# (PCIRST# from Intel® ICH5) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processors to begin execution in a known state. Note that the ICH5 must provide processor frequency select strap setup and hold times around CPURST#. This requires strict synchronization between GMCH CPURST# deassertion and ICH5 driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** DEFER#, when asserted, indicates that the GMCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DINV[3:0]#	I/O AGTL+ 4X	**Dynamic Bus Inversion:** DINV[3:0]# are driven along with the HD[63:0]# signals. They Indicate if the associated data signals are inverted. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV[x]# — Data Bits** DINV3# — HD[63:48]# DINV2# — HD[47:32]# DINV1# — HD[31:16]# DINV0# — HD[15:0]# **NOTE:** This signal is called DBI[3:0] in the processor specifications.

Signal Name	Type	Description
DRDY#	I/O AGTL+	**Data Ready:** DRDY# is asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of HI and AGP/Secondary PCI initiators. HA[31:3]# are transferred at 2X rate. Note that the address is inverted on the processor bus. **NOTE:** The GMCH drives HA7#, which is then sampled by the processor and the GMCH on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HADSTB[1:0]# are source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at the 2X transfer rate. **Strobe** — **Address Bits** HADSTB0# — A[16:3]#, REQ[4:0]# HADSTB1# — A[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0]# is transferred at a 4X rate. Note that the data signals may be inverted on the processor bus, depending on the DINV[3:0] signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Differential Host Data Strobes:** These signals are differential source synchronous strobes used to transfer HD[63:0]# and DINV[3:0]# at the 4X transfer rate. **Strobe** — **Data Bits** HDSTBP3#, HDSTBN3# — HD[63:48]#, DINV3# HDSTBP2#, HDSTBN2# — HD[47:32]#, DINV2# HDSTBP1#, HDSTBN1# — HD[31:16]#, DINV1# HDSTBP0#, HDSTBN0# — HD[15:0]#, DINV0#
HIT#	I/O AGTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Hit# is also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. HITM# is also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., *no HI or AGP/PCI snoopable access* to system memory are allowed when HLOCK# is asserted by the processor).
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2X rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half of the request phase the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.

Signal Name	Type	Description
HTRDY#	O AGTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
PROCHOT#	I/0 AGTL+	**Processor Hot:** This signal informs the chipset when the processor Tj is greater than the thermal Monitor trip point.
RS[2:0]#	I/O AGTL+	**Response Signals:** RS[2:0]# indicate the type of response according to the following: **Encoding** — **Response Type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by GMCH) 100 — Hard Failure (not driven by GMCH) 101 — No data response 110 — Implicit Writeback 111 — Normal data response

The following table lists the processor bus interface signals that are **not** supported by the GMCH.

Signal Name Not Supported	Function Not Supported	Thus, GMCH Does Not Support
AP[1:0]#	Address bus parity	Parity protection on address bus
DP[3:0]#	Data parity	Data parity errors on host interface
HA[35:32]	Upper address bits	Only supports a 4-GB system address space
RSP#	Response (RS) parity	Response parity errors on host interface
IERR#	Processor Internal Error	Responding to processor internal error
BINIT#	Bus Initialization Signal	Reset of the Host Bus state machines.
MCERR#	Machine Check Error	Signaling or recognition of Machine Check Error

2.2 Memory Interface

2.2.1 DDR SDRAM Channel A

The following DDR signals are for DDR channel A.

Signal Name	Type	Description
SCMDCLK_A[5:0]	O SSTL_2	**Differential DDR Clock**: SCMDCLK_Ax and SCMDCLK_Ax# are differential clock output pairs. The crossing of the positive edge of SCMDCLK_Ax and the negative edge of SCMDCLK_Ax# is used to sample the address and control signals on the SDRAM. There are three pairs to each DIMM.
SCMDCLK_A[5:0]#	O SSTL_2	**Complementary Differential DDR Clock**: These are the complementary Differential DDR Clock signals.
SCS_A[3:0]#	O SSTL_2	**Chip Select:** These signals select particular SDRAM components during the active state. There is one SCS_Ax# for each SDRAM row, toggled on the positive edge of SCMDCLK_Ax.
SMAA_A[12:0]	O SSTL_2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SMAB_A[5:1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMAA_A[5:1] and are used to reduce loading for Selective CPC (clock-per-command).
SBA_A[1:0]	O SSTL_2	**Bank Select (Bank Address):** These signals define which banks are selected within each SDRAM row. Bank select and memory address signals combine to address every possible location within an SDRAM device.
SRAS_A#	O SSTL_2	**Row Address Strobe:** SRAS_A# is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL_2	**Column Address Strobe:** SCAS_A# is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL_2	**Write Enable:** SWE_A# is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL_2	**Data Lines:** SDQ_Ax signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax for every eight data lines. SDM_Ax can be sampled on both edges of the data strobes.
SDQS_A[7:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS_Ax is centered in data. During reads, SDQS_Ax is edge aligned with data. The following lists the data strobe with the data bytes. **Data Strobe** — **Data Byte** SDQS_A7 — SDQ_A[63:56] SDQS_A6 — SDQ_A[55:48] SDQS_A5 — SDQ_A[47:40] SDQS_A4 — SDQ_A[39:32] SDQS_A3 — SDQ_A[31:24] SDQS_A2 — SDQ_A[23:16] SDQS_A1 — SDQ_A[15:8] SDQS_A0 — SDQ_A[7:0]
SCKE_A[3:0]	O SSTL_2	**Clock Enable:** SCKE_A[3:0] are used to initialize DDR SDRAM during power-up and to place all SDRAM rows into and out of self-refresh during Suspend-to-RAM. SCKE_A[3:0] are also used to dynamically power down inactive SDRAM rows. There is one SCKE_Ax per SDRAM row, toggled on the positive edge of SCMDCLK_Ax.

2.2.2 DDR SDRAM Channel B

The following DDR signals are for DDR channel B.

Signal Name	Type	Description
SCMDCLK_B[5:0]	O SSTL_2	**Differential DDR Clock**: SCMDCLK_Bx and SCMDCLK_Bx# are differential clock output pairs. The crossing of the positive edge of SCMDCLK_Bx and the negative edge of SCMDCLK_Bx# is used to sample the address and control signals on the SDRAM. There are three pairs to each DIMM.
SCMDCLK_B[5:0]#	O SSTL_2	**Complementary Differential DDR Clock**: These are the complementary Differential DDR Clock signals.
SCS_B[3:0]#	O SSTL_2	**Chip Select:** These signals select particular SDRAM components during the active state. There is one SCS_Bx# for each SDRAM row, toggled on the positive edge of SCMDCLK_Bx.
SMAA_B[12:0]	O SSTL_2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SMAB_B[5:1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMAA_B[5:1] and are used to reduce loading for Selective CPC (clock-per-command).
SBA_B[1:0]	O SSTL_2	**Bank Select (Bank Address):** These signals define which banks are selected within each SDRAM row. Bank select and memory address signals combine to address every possible location within an SDRAM device.
SRAS_B#	O SSTL_2	**Row Address Strobe:** SRAS_B# is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SCAS_B#	O SSTL_2	**Column Address Strobe:** SCAS_B# is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL_2	**Write Enable:** SWE_B# is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL_2	**Data Lines:** SDQ_B signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx for every eight data lines. SDM_Bx can be sampled on both edges of the data strobes.
SDQS_B[7:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS_Bx is centered in data. During reads, SDQS_Bx is edge aligned with data. The following list matches the data strobe with the data bytes. **Data Strobe** — **Data Byte** SDQS_B7 — SDQ_B[63:56] SDQS_B6 — SDQ_B[55:48] SDQS_B5 — SDQ_B[47:40] SDQS_B4 — SDQ_B[39:32] SDQS_B3 — SDQ_B[31:24] SDQS_B2 — SDQ_B[23:16] SDQS_B1 — SDQ_B[15:8] SDQS_B0 — SDQ_B[7:0]
SCKE_B[3:0]	O SSTL_2	**Clock Enable:** SCKE_B[3:0] are used to initialize DDR SDRAM during power-up and to place all SDRAM rows into and out of self-refresh during Suspend-to-RAM. SCKE_B[3:0] are also used to dynamically power down inactive SDRAM rows. There is one SCKE_Bx per SDRAM row, toggled on the positive edge of SCMDCLK_Bx.

2.3 Hub Interface

Signal Name	Type	Description
HI[10:0]	I/O sts HI15	**Packet Data:** HI[10:0] are data signals used for hub interface read and write operations.
HISTRS	I/O sts HI15	**Packet Strobe:** HISTRS is one of two differential strobe signals used to transmit or receive packet data over the hub interface.
HISTRF	I/O sts HI15	**Packet Strobe Complement:** HISTRF is one of two differential strobe signals used to transmit or receive packet data over the hub interface.

2.4 Communication Streaming Architecture (CSA) Interface

Signal Name	Type	Description
CI[10:0]	I/O sts HI15	**Packet Data:** CI[10:0] are data signals used for CI read and write operations.
CISTRS	I/O sts HI15	**Packet Strobe:** CISTRS is one of two differential strobe signals used to transmit or receive packet data over CI.
CISTRF	I/O sts HI15	**Packet Strobe Complement:** CISTRF is one of two differential strobe signals used to transmit or receive packet data over CI.

2.5 AGP Interface

2.5.1 AGP Addressing Signals

Signal Name	Type	Description
GPIPE# *(2.0)* DBI_HI *(3.0)*	I/O AGP	**Pipelined Read:** This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master enqueues one request each rising clock edge while GPIPE# is asserted. When GPIPE# is deasserted, no new requests are enqueued across the GAD bus. GPIPE# may be used in AGP 2.0 signaling modes, but is not permitted by the AGP 3.0 specification. When operating in AGP 3.0 signaling mode, GPIPE# is used for DBI_HI. GPIPE# is a sustained tri-state signal from the master *(*graphics controller*)* and is an input to the GMCH. In AGP 3.0 signaling mode this signal is Dynamic Bus Inversion HI. **Dynamic Bus Inversion HI**: This signal goes along with GAD[31:16] to indicate whether GAD[31:16] must be inverted on the receiving end. • DBI_HI = 0: GAD[31:16] are not inverted so receiver may use as is. • DBI_HI = 1: GAD[31:16] are inverted so receiver must invert before use. The GADSTBF1 and GADSTBS1 strobes are used with DBI_HI. In AGP 3.0 4X data rate mode dynamic bus inversion is disabled by the GMCH while transmitting (data never inverted and BI_HI driven low); dynamic bus inversion is enabled when receiving data. For 8X data rate, dynamic bus inversion is enabled when transmitting and receiving data.
GSBA[7:0] *(2.0)* GSBA[7:0]# *(3.0)*	I AGP	**Sideband Address:** This bus provides an additional bus to pass address and command to the GMCH from the AGP master. **NOTE:** In AGP 2.0 signaling mode, when sideband addressing is disabled, these signals are isolated. When sideband addressing is enabled, internal pull-ups are enabled to prevent indeterminate values on them in cases where the Graphics Card may not have its GSBA[7:0] output drivers enabled yet.

NOTES:
1. The table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. When *GPIPE#* is used to queue addresses the master is not allowed to queue addresses using the SB bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.
2. The term *(2.0)* following a signal name indicates its function in AGP 2.0 signaling mode (1.5 V swing).
3. The term *(3.0)* following a signal name indicates its function in AGP 3.0 signaling mode (0.8 V swing).

2.5.2 AGP Flow Control Signals

Signal Name	Type	Description
GRBF# *(2.0)* GRBF *(3.0)*	I AGP	**Read Buffer Full:** This signal indicates if the master is ready to accept previously requested low priority read data. When GRBF(#) is asserted, the GMCH is not allowed to return low priority read data to the AGP master on the first block. GRBF(#) is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data, then it is not required to implement this signal.
GWBF# *(2.0)* GWBF *(3.0)*	I AGP	**Write Buffer Full:** This signal indicates if the master is ready to accept Fast Write data from the GMCH. When GWBF(#) is asserted, the GMCH is not allowed to drive Fast Write data to the AGP master. GWBF(#) is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data, then it is not required to implement this signal.

NOTE:
1. The term *(2.0)* following a signal name indicates its function in AGP 2.0 signaling mode (1.5 V swing).
2. The term *(3.0)* following a signal name indicates its function in AGP 3.0 signaling mode (0.8 V swing).

2.5.3 AGP Status Signals

Signal Name	Type	Description
GST[2:0] *(2.0)* GST[2:0] *(3.0)*	O AGP	**Status:** These signals provides information from the arbiter to an AGP Master on what it may do. GST[2:0] only have meaning to the master when its GGNT(#) is asserted. When GGNT(#) is deasserted, these signals have no meaning and must be ignored. GST[2:0] are always an output from the GMCH and an input to the master. **Encoding** — **Meaning** 000 — Previously requested low priority read data (Async read for AGP 3.0 Signaling mode) is being returned to the master. 001 — Previously requested high priority read data is being returned to the master. Reserved in AGP 3.0 signaling mode. 010 — The master is to provide low priority write data (Async write for AGP 3.0 signaling mode) for a previously queued write command. 011 — The master is to provide high priority write data for a previously queued write command. Reserved in AGP 3.0 signaling mode. 100 — Reserved. 101 — Reserved. 110 — Reserved. 111 — The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting GPIPE# (4X signaling mode) or start a PCI transaction by asserting GFRAME(#).

2.5.4 AGP Strobes

Signal Name	Type	Description
GADSTB0 *(2.0)* GADSTBF0 *(3.0)*	I/O (s/t/s) AGP	**AD Bus Strobe-0:** GADSTB0 provides timing for 4X clocked data on GAD[15:0] and GC/BE[1:0]# in AGP 2.0 signaling mode. The agent that is providing data drives this signal. **AD Bus Strobe First-0:** In AGP 3.0 signaling mode GADSTBF0 strobes the first and all odd numbered data items with a low-to-high transition. It is used with GAD[15:0] and GC#/BE[1:0].
GADSTB0# *(2.0)* GADSTBS0 *(3.0)*	I/O (s/t/s) AGP	**AD Bus Strobe-0 Complement:** GADSTB0# is the differential complement to the GADSTB0 signal. It is used to provide timing for 4X clocked data in AGP 2.0 signaling mode. **AD Bus Strobe Second-0:** In AGP 3.0 signaling mode GADSTBS0 strobes the second and all even numbered data items with a low-to-high transition.
GADSTB1 *(2.0)* GADSTBF1 *(3.0)*	I/O (s/t/s) AGP	**AD Bus Strobe-1:** GADSTB1 provides timing for 4X clocked data on GAD[31:16] and GC/BE[3:2]# in AGP 2.0 signaling mode. The agent that is providing data drives this signal. **AD Bus Strobe First-1:** In AGP 3.0 signaling mode GADSTBF1 strobes the first and all odd numbered data items with a low-to-high transition. It is used with GAD[31:16], GC#/BE[3:2], DBI_HI, and DBI_LO.
GADSTB1# *(2.0)* GADSTBS1 *(3.0)*	I/O (s/t/s) AGP	**AD Bus Strobe-1 Complement:** GADSTB1# is the differential complement to the GADSTB1 signal. It is used to provide timing for 4X clocked data in AGP 2.0 signaling mode. **AD Bus STrobe Second-1:** In AGP 3.0 signaling mode GADSTBS1 strobes the second and all even numbered data items with a low-to-high transition.
GSBSTB *(2.0)* GSBSTBF *(3.0)*	I AGP	**Sideband Strobe:** GSBSTB provides timing for 4X clocked data on the GSBA[7:0] bus in AGP 2.0 signaling mode. It is driven by the AGP master after the system has been configured for 4X clocked sideband address delivery. **Sideband Strobe First:** In AGP 3.0 signaling mode GSBSTBF strobes the first and all odd numbered data items with a low-to-high transition.
GSBSTB# *(2.0)* GSBSTBS *(3.0)*	I AGP	**Sideband Strobe Complement:** GSBSTB# is the differential complement to the GSBSTB signal. It is used to provide timing for 4X clocked data in AGP 2.0 signaling mode. **Sideband Strobe Second:** In AGP 3.0 signaling mode GSBSTBS strobes the second and all even numbered data items with a low-to-high transition.

NOTE:
1. The term *(2.0)* following a signal name indicates its function in AGP 2.0 signaling mode (1.5 V swing).
2. The term *(3.0)* following a signal name indicates its function in AGP 3.0 signaling mode (0.8 V swing).

2.5.5 PCI Signals–AGP Semantics

PCI signals are redefined when used in AGP transactions carried using AGP protocol extension. For transactions on the AGP interface carried using the PCI protocol, these signals completely preserve PCI 2.1 semantics. The exact roles of all PCI signals during AGP transactions are defined in the following table.

Signal Name	Type	Description
GFRAME# *(2.0)* GFRAME *(3.0)*	I/O s/t/s AGP	**GFRAME(#):** This signal is driven by the current master to indicate the beginning and duration of a standard PCI protocol (“frame based”) transaction and during fast writes. It is not used, and must be inactive during AGP transactions.
GIRDY# *(2.0)* GIRDY *(3.0)*	I/O s/t/s AGP	**GIRDY(#):** This signal is used for both GFRAME(#) based and AGP transactions. During AGP transactions, it indicates the AGP compliant master is ready to provide *all* write data for the current transaction. Once GIRDY(#) is asserted for a write operation, the master is not allowed to insert wait states. The assertion of GIRDY(#) for reads indicates that the master is ready to transfer to a subsequent block (4 clocks) of read data. The master is **never** allowed to insert a wait state during the initial data transfer (first 4 clocks) of a read transaction. However, it may insert wait states after each 4 clock block is transferred. **NOTE:** There is no GFRAME(#) – GIRDY(#) relationship for AGP transactions.
GTRDY# *(2.0)* GTRDY *(3.0)*	I/O s/t/s AGP	**GTRDY(#):** This signal is used for both GFRAME(#) based and AGP transactions. During AGP transactions, it indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 4 clocks) or is ready to transfer the initial or subsequent block (4 clocks) of data when the transfer size is greater than 4 clocks. The target is allowed to insert wait states after each block (4 clocks) is transferred on both read and write transactions.
GSTOP# *(2.0)* GSTOP *(3.0)*	I/O s/t/s AGP	**GSTOP(#):** This signal is used during GFRAME(#) based transactions by the target to request that the master stop the current transaction. GSTOP(#) is Not used during AGP transactions.
GDEVSEL# *(2.0)* GDEVSEL *(3.0)*	I/O s/t/s AGP	**Device Select:** During GFRAME(#) based accesses, GDEVSEL(#) is driven active by the target to indicate that it is responding to the access. GDEVSEL(#) is Not used during AGP transactions.
GREQ# *(2.0)* GREQ *(3.0)*	I AGP	**Request:** This signal is an output of an AGP device. Used to request access to the bus to initiate a PCI (GFRAME(#)) or AGP(GPIPE(#)) request. GREQ(#) is Not required to initiate an AGP request via SBA.
GGNT# *(2.0)* GGNT *(3.0)*	O AGP	**Grant:** This signal is an output of the GMCH, either granting the bus to the AGP device to initiate a GFRAME(#) or GPIPE(#) access (in response to GREQ(#) active) or to indicate that data is to be transferred for a previously enqueued AGP transaction. GST[2:0] indicates the purpose of the grant.
GAD[31:0] *(2.0)* GAD[31:0] *(3.0)*	I/O AGP	**Address/Data:** GAD[31:0] provide the address for GFRAME(#) and GPIPE(#) transactions and the data for all transactions. These signals operate at a 1X data rate for GFRAME(#) based cycles, and operate at the specified channel rate (1X, 4X, or 8X) for AGP data phases and fast write data phases.

Signal Name	Type	Description
GC/BE[3:0]# *(2.0)* GC#/BE[3:0] *(3.0)*	I/O AGP	**Command/Byte Enables:** These signals provide the command during the address phase of a GFRAME(#) or GPIPE(#) transaction and byte enables during data phases. Byte enables are not used for read data of AGP 1X and 2X and 4X and 8X reads. These signals operate at the same data rate as the GAD[31:0] signals at any given time.
GPAR/ ADD_DETECT	I/O AGP	**Parity:** GPAR is not used on AGP transactions. It is used during GFRAME(#) based transactions as defined by the PCI specification. GPAR is not used during fast writes. **Add Detect:** The GMCH multiplexes an ADD_DETECT signal with the GPAR signal on the AGP bus. This signal acts as a strap and indicates whether the interface is in AGP or DVO mode. The GMCH has an internal pull-up on this signal that will naturally pull it high. If an ADD card is present, the signal will be pulled low on the ADD card and the AGP/DVO multiplex select bit in the GMCHCFG register will be set to DVO mode. Motherboards that do not use an AGP connector should have a pull-down resistor on ADD_DETECT if they have digital display devices connected to the interface.
DBI_LO *(3.0 only)*	I/O AGP	**Dynamic Bus Inversion LO:** This AGP 3.0 only signal goes along with GAD[15:0] to indicate whether GAD[15:0] must be inverted on the receiving end. • DBI_LO= 0: GAD[15:0] are not inverted so receiver may use as is. • DBI_LO= 1: GAD[15:0] are inverted so receiver must invert before use. The GADSTBF1 and GADSTBS1 strobes are used with the DBI_LO. Dynamic bus inversion is used in AGP 3.0 signaling mode only.

NOTES:
1. PCIRST# from the ICH5 is connected to RSTIN# and is used to reset AGP interface logic in the GMCH. The AGP agent will also typically use PCIRST# provided by the ICH5 as an input to reset its internal logic.
2. LOCK# signal is **not** supported on the AGP interface (even for PCI operations).
3. The term *(2.0)* following a signal name indicates its function in AGP 2.0 signaling mode (1.5 V swing).
4. The term *(3.0)* following a signal name indicates its function in AGP 3.0 signaling mode (0.8 V swing).

2.5.5.1 PCI Pins during PCI Transactions on AGP Interface

PCI signals described in a previous table behave according to PCI 2.1 specifications when used to perform PCI transactions on the AGP interface.

2.5.6 Multiplexed Intel® DVOs on AGP

The following signals are multiplexed on the AGP signals.

Signal Name	Type	Description
DVOB_CLK; DVOB_CLK#	O AGP	**DVOB Clock Output:** These pins provide a differential pair reference clock that can run up to 165 MHz. Care should be taken to be sure that DVOB_CLK is connected to the primary clock receiver of the Intel® DVO device.
DVOB_D[11:0]	O AGP	**DVOB Data:** This data bus is used to drive 12-bit pixel data on each edge of DVOB_CLK(#). This provides 24-bits of data per clock.
DVOB_HSYNC	O AGP	**Horizontal Sync:** HSYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_VSYNC	O AGP	**Vertical Sync:** VSYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_BLANK#	O AGP	**Flicker Blank or Border Period Indication:** DVOB_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.

Signal Name	Type	Description
DVOBC_CLKINT	I AGP	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to the dot clock PLL (DPLL) for the multiplexed DVOs. This pin may also be programmed to be an interrupt input for either of the multiplexed DVOs.
DVOB_FLDSTL	I AGP	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
DVOC_CLK; DVOC_CLK#	O AGP	**DVOC Clock Output:** These pins provide a differential pair reference clock that can run up to 165 MHz. Care should be taken to be sure that DVOC_CLK is connected to the primary clock receiver of the DVO device.
DVOC_D[11:0]	O AGP	**DVOC Data:** This data bus is used to drive 12-bit pixel data on each edge of DVOC_CLK(#). This provides 24-bits of data per clock.
DVOC_HSYNC	O AGP	**Horizontal Sync:** HSYNC signal for the DVOC interface. The active polarity of the signal is programmable.
DVOC_VSYNC	O AGP	**Vertical Sync:** VSYNC signal for the DVOC interface. The active polarity of the signal is programmable.
DVOC_BLANK#	O AGP	**Flicker Blank or Border Period Indication:** DVOC_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.
DVOBC_INTR#	I AGP	**DVOBC Interrupt:** This pin may be used as an interrupt input for either of the multiplexed DVOs.
DVOC_FLDSTL	I AGP	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
MI2C_CLK	I/O AGP	**MI2C_CLK:** The specific function is I2C_CLK for a multiplexed digital display. This signal is tri-stated during a hard reset.
MI2C_DATA	I/O AGP	**MI2C_DATA:** The specific function is I2C_DATA for a multiplexed digital display. This signal is tri-stated during a hard reset.
MDVI_CLK	I/O AGP	**MDVI_CLK:** The specific function is DVI_CLK (DDC) for a multiplexed digital display connector. This signal is tri-stated during a hard reset.
MDVI_DATA	I/O AGP	**MDVI_DATA:** The specific function is DVI_DATA (DDC) for a multiplexed digital display connector. This signal is tri-stated during a hard reset.
MDDC_CLK	I/O AGP	**MDDC_CLK:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
MDDC_DATA	I/O AGP	**MDDC_DATA:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
ADDID[7:0]	I/O AGP	**ADD Card ID:** These signals will be strapped on the ADD card for SW identification purposes. These signals may need pull-up or pull-down resistors in a DVO down scenario.

2.5.7 Intel® DVO-to-AGP Pin Mapping

The GMCH multiplexes an ADD_DETECT signal with the GPAR signal on the AGP bus. This signal acts as a strap and indicates whether the interface is in AGP or DVO mode (See ADD_DETECT signal description for further information). GSBA(7:0) act as straps for an ADD_ID. When an ADD card is present, ADD_DETECT = 0 (DVO mode), the ADD_ID register (offset 71408h) will hold a valid ADD PROM ID.

Table 3 shows the DVO-to-AGP pin mapping. The AGP signal name column only shows the AGP 2.0 signal names.

Table 3. Intel® DVO-to-AGP Pin Mapping

DVO Signal Name	AGP Signal Name	DVO Signal Name	AGP Signal Name
DVOB_D0	GAD3	DVOC_D0	GAD19
DVOB_D1	GAD2	DVOC_D1	GAD20
DVOB_D2	GAD5	DVOC_D2	GAD21
DVOB_D3	GAD4	DVOC_D3	GAD22
DVOB_D4	GAD7	DVOC_D4	GAD23
DVOB_D5	GAD6	DVOC_D5	GC/BE3#
DVOB_D6	GAD8	DVOC_D6	GAD25
DVOB_D7	GC/BE0#	DVOC_D7	GAD24
DVOB_D8	GAD10	DVOC_D8	GAD27
DVOB_D9	GAD9	DVOC_D9	GAD26
DVOB_D10	GAD12	DVOC_D10	GAD29
DVOB_D11	GAD11	DVOC_D11	GAD28
DVOB_CLK	GADSTB0	DVOC_CLK	GADSTB1
DVOB_CLK#	GADSTB0#	DVOC_CLK#	GADSTB1#
DVOB_HSYNC	GAD0	DVOC_HSYNC	GAD17
DVOB_VSYNC	GAD1	DVOC_VSYNC	GAD16
DVOB_BLANK#	GC/BE1#	DVOC_BLANK#	GAD18
DVOBC_CLKINT	GAD13	DVOBC_INTR#	GAD30
DVOB_FLDSTL	GAD14	DVOC_FLDSTL	GAD31
DVOBCRCOMP	AGP_RCOMP	ADDID[7:0]	GSBA[7:0]
MI2CCLK	GIRDY#	MDVI_DATA	GFRAME#
MI2CDATA	GDEVSEL#	MDDC_CLK	GSTOP#
MDVI_CLK	GTRDY#	MDDC_DATA	GAD15

2.6 Analog Display Interface

Signal Name	Type	Description
HSYNC	O 3.3 V GPIO	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval.” This signal may need to be level shifted.
VSYNC	O 3.3 V GPIO	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). This signal may need to be level shifted.
RED	O Analog	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω equivalent load on each signal (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O Analog	**RED# Analog Output:** This signal is an analog video output from the internal color palette DAC. It is connected to a 37.5 Ω resistor to ground. This signal is used to provide noise immunity.
GREEN	O Analog	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω equivalent load on each signal (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
GREEN#	O Analog	**GREEN# Analog Output:** This signal is an analog video output from the internal color palette DAC. It is connected to a 37.5 Ω resistor to ground. This signal is used to provide noise immunity.
BLUE	O Analog	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω equivalent load on each signal (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O Analog	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. It is connected to a 37.5 Ω resistor to ground. This signal is used to provide noise immunity.
REFSET	I Analog	**Resistor Set:** Set point resistor for the internal color palette DAC. A 169 Ω, 1% resistor is required between REFSET and motherboard ground.
DDCA_CLK	I/O 3.3 V GPIO	**Analog DDC Clock:** Clock signal for the I^2C style interface that connects to Analog CRT Display. **NOTE:** This signal may need to be level shifted to 5 Volts.
DDCA_DATA	I/O 3.3 V GPIO	**Analog DDC Data:** Data signal for the I^2C style interface that connects to Analog CRT Display. **NOTE:** This signal may need to be level shifted to 5 Volts.

2.7 Clocks, Reset, and Miscellaneous Signals

Signal Name	Type	Description
HCLKP HCLKN	I CMOS	**Differential Host Clock In:** These pins receive a low voltage differential host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that is in the Host clock domain 0.7 V.
GCLKIN	I LVTTL	**66 MHz Clock In:**. This pin receives a 66 MHz clock from the clock synthesizer. This clock is used by AGP/PCI and HI clock domains. **NOTE:** This clock input is required to be 3.3 V tolerant.
DREFCLK	I LVTTL	**Display Clock Input:** This pin provides a 48 MHz input clock to the Display PLL that is used for 2D/Video/Flat Panel and DAC. **NOTE:** This clock input is required to be 3.3 V tolerant.
RSTIN#	I LVTTL	**Reset In:** When asserted this signal will asynchronously reset the GMCH logic. This signal is connected to the PCIRST# output of the ICH5. All AGP/PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications. This input should have a Schmitt trigger to avoid spurious resets. **NOTE:** This input needs to be 3.3 V tolerant.
PWROK	I LVTTL	**Power OK:** When asserted, PWROK is an indication to the GMCH that the core power and GCLKIN have been stable for at least 10 µs.
EXTTS#	I LVTTL	**External Thermal Sensor Input**: Open-Drain signal indicating an Over-Temp condition in the platform. This signal should remains asserted for as long as the Over-temp Condition exists. This input pin can be programmed to activate hardware management of memory reads and writes and/or trigger software interrupts.
TESTIN#	I	Test Input. This signal is used in the GMCH XOR test mode. See Chapter 8 for use.

2.8 RCOMP, VREF, VSWING Signals

Signal Name	Type	Description
HDVREF	I	**Host Data Reference Voltage:** This signal is the reference voltage input for the data signals of the Host AGTL+ interface.
HDRCOMP	I/O CMOS	**Host RCOMP:** HDRCOMP is used to calibrate the Host AGTL+ I/O buffers.
HDSWING	I	**Host Voltage Swing:** These signals provide a reference voltage used by the FSB RCOMP circuit.
SMVREF_A	I	**Memory Reference Voltage for Channel A:** SMVREF_A is the reference voltage input for system memory Interface. This signal is tied internally to SMVREF_B. Thus, only one of these signals needs to be the SMVREF and the other should be decoupled.
SMXRCOMPVOL	I	**Memory RCOMP for Channel A:** This signal is used to Calibrate VOL.
SMXRCOMPVOH	I	**Memory RCOMP for Channel A**: This signal is used to Calibrate VOH.
SMXRCOMP	I/O CMOS	**Memory RCOMP for Channel A:** This signal is used to calibrate the memory I/O buffers.
SMVREF_B	I	**Memory Reference Voltage for Channel B:** SMVREF_B is the reference voltage input for System Memory Interface. This signal is tied internally to SMVREF_A. Thus, only one of these signals needs to be the SMVREF and the other should be decoupled.
SMYRCOMPVOL	I	**Memory RCOMP for Channel B**: This signal is used to Calibrate VOL.
SMYRCOMPVOH	I	**Memory RCOMP for Channel B**: This signal is used to Calibrate VOH.
SMYRCOMP	I/O CMOS	**Memory RCOMP for Channel B:** This signal is used to calibrate the memory I/O buffers.
GVREF	I	**AGP Reference:** The reference voltage for the AGP/DVO I/O buffers is 0.75 V.
GVSWING	I	**AGP Voltage Swing**: This signal provides a reference voltage for GRCOMP in AGP mode.
GRCOMP/ DVOBCRCOMP	I/O CMOS	**Compensation for AGP/DVOB:** This signal is used to calibrate the AGP/ DVO buffers. This signal should be connected to ground through a 43 Ω pull-up resistor to VDDQ
HI_VREF	I	**HI Reference:** HI_VREF is the reference voltage input for the hub interface.
HI_RCOMP	I/O CMOS	**Compensation for HI:** This signal is used to calibrate the hub interface I/O buffers.
HI_SWING	I	**HI Voltage Swing:** This signal provides a reference voltage used by the HI_RCOMP circuit.
CI_VREF	I	**CSA Reference:** CI_VREF is the reference voltage input for the CSA interface.
CI_RCOMP	I/O CMOS	**Compensation for CSA:** This signal is used to calibrate the CSA I/O buffers.
CI_SWING	I	**CSA Voltage Swing:** This signal provides a reference voltage used by the CI_RCOMP circuit.

NOTE:
1. Reference the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for platform design information.

2.9 Power and Ground Signals

Signal Name	Description
VCC	**VCC Supply:** This is the 1.5 V core.
VSS	**Gnd Supply**
VCCA_AGP	**AGP PLL Power**
VCC_AGP	**VCC for AGP:** This value can be either 0.8 V or 1.5 V as the GMCH supports both AGP electrical characteristics.
VCCA_FSB	**Analog VCC for Host PLL:** This 1.5 V supply requires special filtering. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for details.
VTT	**VTT:** This is the supply for the FSB.
VCCA_DPLL	**Analog VCC for Display PLL:** This 1.5 V supply requires special filtering. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for details.
VCC_DAC	**DAC VCC Supply:** This signal is the 3.3 V VCC for the DAC.
VCCA_DAC	**Analog DAC VCC:** This is the 1.5 V analog supply for the DAC. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for supply requirements.
VSSA_DAC	**Analog DAC VSS:** This supply should go directly to motherboard ground.
VCC_DDR	**VCC For DDR:** This signal is the 2.6 V supply for system memory.
VCCA_DDR	**Analog VCC for DDR:** This signal is the analog 1.5 V supply for the system memory PLLs. This supply requires special filtering. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for details.

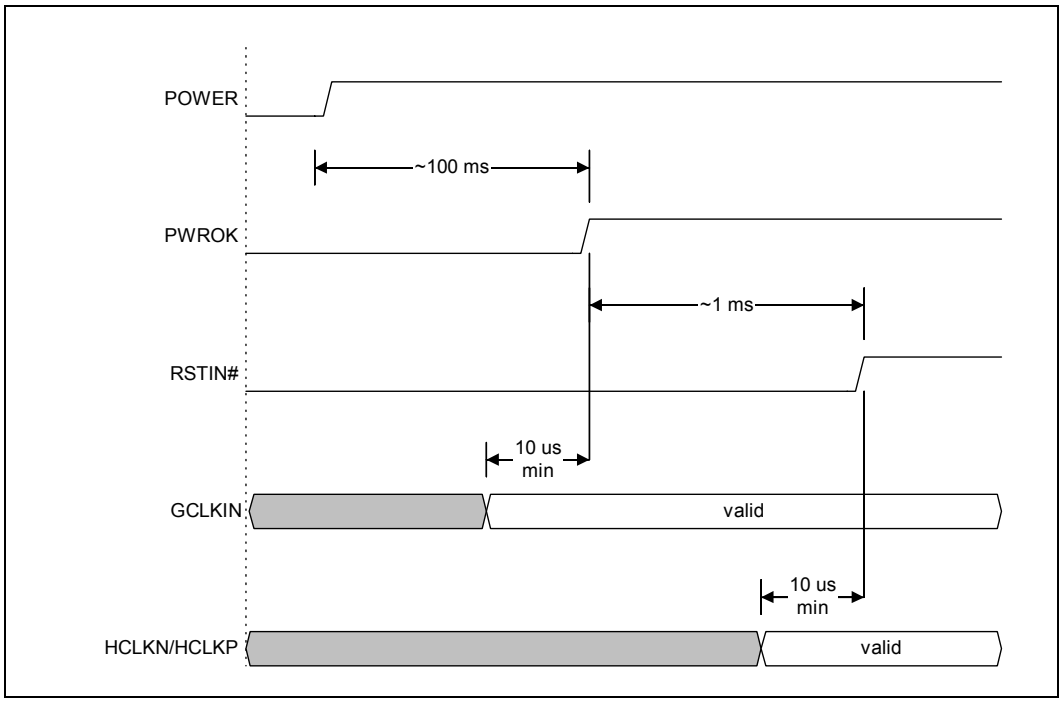
2.10 GMCH Sequencing Requirements

Power Plane and Sequencing Requirements:

- Clock Valid Timing:
- GCLKIN must be valid at least 10 µs prior to the rising edge of PWROK.
- HCLKN/HCLKP must be valid at least 10 µs prior to the rising edge of RSTIN#.

There is no DREFCLK timing requirements relative to reset.

Figure 3. Intel® 865G Chipset System Clock and Reset Requirements



The GMCH uses the rising edge of PWROK to latch straps values. During S3, when power is not valid, the GMCH requires that PWROK de-assert and then re-assert when power is valid so that it can properly re-latch the straps.

2.11 Signals Used As Straps

2.11.1 Functional Straps

Signal Name	Strap Name	Description
HA7#	FSB IOQ Depth	**System Bus IOQ Depth Strap:** The value on HA7# is sampled by all processor bus agents, including the GMCH, on the deasserting edge of CPURST#. **NOTE:** For HA7#, the minimum setup time is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. The latched value determines the maximum IOQ depth supported on the processor bus. • 0 (low voltage) = BUS IOQ depth on the bus is 1 • 1 (high voltage) = BUS IOQ depth on the bus is the maximum of 12
GPAR/ ADD_DETECT	AGP/DVO	**AGP Operating Mode Select Strap:** This strap selects the operating mode of the AGP signals (controls only AGP I/O muxes): • 0 (low voltage) = ADD Card (2X DVO) • 1 (high voltage) = AGP The ADD_DETECT strap is flow-through while RSTIN# is asserted and latched on the de-asserting edge of RSTIN#. RSTIN# is used to make sure that the AGP card is not driving the GPAR/ADD_DETECT signal when it is latched. **NOTE:** DVO detection mechanism needs to be switched off in AGP 3.0 mode; otherwise, the GMCH will wake up in DVO mode when GVREF is 0.35 V
SBA[7:0]	ADD Card ID	**ID Bit Select Strap:** This strap signal is used in flow-through fashion while PWROK is de-asserted and is latched on the asserting edge of PWROK. • 0 (low voltage) = ID bit is set to 0 • 1 (high voltage) = ID bit is set to 1

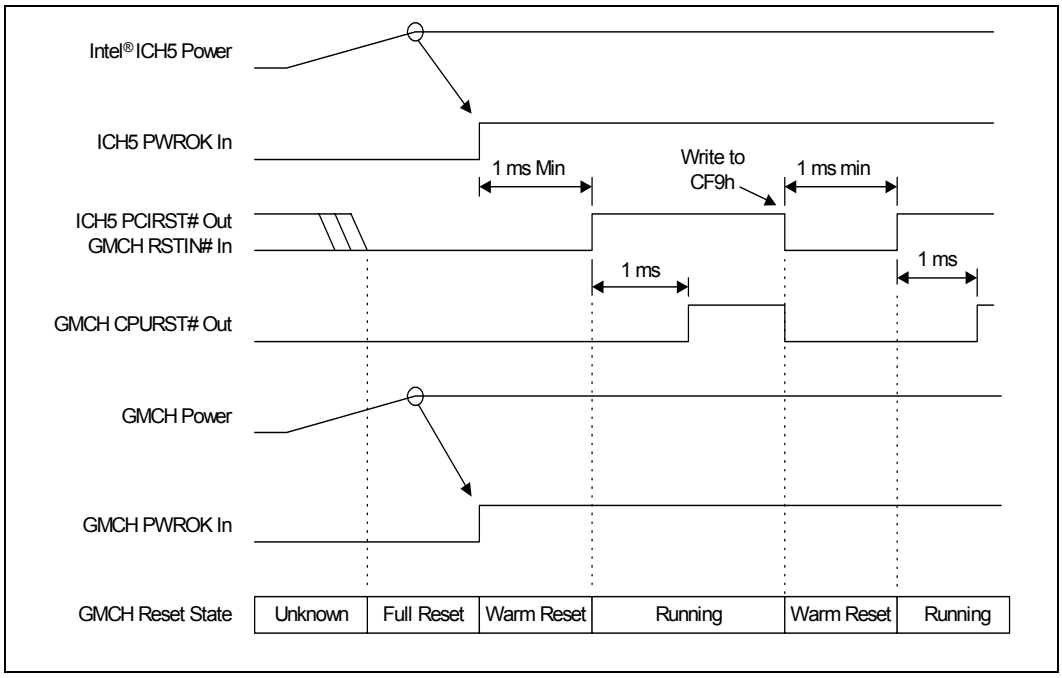
NOTE:
1. All straps, have internal 8 kΩ pull-ups (HA7# has GTL pull-up) enabled during their sampling window. Therefore, a strap that is not connected or not driven by external logic will be sampled high.

2.11.2 Strap Input Signals

Signal Name	Type	Description
BSEL[1:0]	I CMOS	**Core / FSB Frequency (FSBFREQ) Select Strap:** This strap is latched at the rising edge of PWROK. These pins has no default internal pull-up resistor. 00 = Core frequency is 100 MHz, FSB frequency is 400 MHz 01 = Core frequency is 133 MHz, FSB frequency is 533 MHz 10 = Core frequency is 200 MHz, FSB frequency is 800 MHz 11 = Reserved

2.12 Full and Warm Reset States

Figure 4. Full and Warm Reset Waveforms



All register bits assume their default values during full reset. PCIRST# resets all internal flip flops and state machines (except for a few configuration register bits). A full reset occurs when PCIRST# (GMCH RSTIN#) is asserted and PWROK is deasserted. A warm reset occurs when PCIRST# (GMCH RSTIN#) is asserted and PWROK is also asserted. The following table describes the reset states.

Reset State	RSTIN#	PWROK
Full Reset	L	L
Warm Reset	L	H
Does Not Occur	H	L
Normal Operation	H	H

Register Description 3

The GMCH contains two sets of software accessible registers, accessed via the host processor I/O address space:

- Control registers that are I/O mapped into the processor I/O space control access to PCI and AGP configuration space.
- Internal configuration registers residing within the GMCH are partitioned into three logical device register rests (“logical” since they reside within a single physical device). The first register set is dedicated to Host-Hub Interface functionality (controls PCI bus #0 operations including DRAM configuration, other chipset operating parameters, and optional features). The second register block is dedicated to Host-AGP/PCI_B Bridge functions (controls AGP/PCI_B interface configurations and operating parameters). The third register block is dedicated to the Integrated Graphics Device (IGD).

This configuration scheme is necessary to accommodate the existing and future software configuration model supported by Microsoft where the host bridge functionality will be supported and controlled via dedicated and specific driver and virtual PCI-to-PCI bridge functionality will be supported via standard PCI bus enumeration configuration software. The term “virtual” is used to designate that no real physical embodiment of the PCI-to-PCI bridge functionality exists within the GMCH, but that GMCH’s internal configuration register sets are organized in this particular manner to create that impression to the standard configuration software.

The GMCH supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism 1 in the PCI specification. The GMCH internal registers (both I/O mapped and configuration registers) are accessible by the host processor. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS which can only be accessed as a DWord. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field).

3.1 Register Terminology

Term	Description
RO	**Read Only**. If a register is read only, writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be read and written.
R/W/L	**Read/Write/Lock**. A register with this attribute can be read, written, and Locked.
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
L	**Lock.** A register bit with this attribute becomes Read Only after a lock bit is set.
Reserved Bits	Some of the GMCH registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that software does not need to perform a read-merge-write operation for the Configuration Address (CONFIG_ADDRESS) register.

Term	Description
Reserved Registers	In addition to reserved bits within a register, the GMCH contains address locations in the configuration space of the Host-HI Bridge entity that are marked either “Reserved” or “Intel Reserved”. The GMCH responds to accesses to reserved address locations by completing the host cycle. When a reserved register location is read, a zero value is returned. (reserved registers can be 8, 16, or 32 bits in size). Writes to reserved registers have no effect on the GMCH. ***Caution:*** Register locations that are marked as “Intel Reserved” must **not** be modified by system software. Writes to “Intel Reserved” register locations may cause system failure. Reads to “Intel Reserved” register locations may return a non-zero value.
Default Value upon a Reset	Upon a reset, the GMCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the SDRAM configurations, operating parameters and optional system features that are applicable, and to program the GMCH registers accordingly.

3.2 Platform Configuration Structure

In some previous chipsets, the GMCH and the I/O Controller Hub (ICHx) were physically connected by PCI bus 0. From a configuration standpoint, both components appeared to be on PCI bus 0, which was also the system’s primary PCI expansion bus. The GMCH contained two PCI devices while the ICHx bridge was considered one PCI device with multiple functions.

In the 865G chipset platform, the configuration structure is significantly different. The GMCH and the ICH5 are physically connected by a hub interface (HI); thus, from a configuration standpoint, HI is logically PCI bus 0. As a result, all devices internal to the GMCH and ICH5 appear to be on PCI bus 0. The system’s primary PCI expansion bus is physically attached to ICH5 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge; therefore, it has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI_A in this document and is **not** PCI bus 0 from a configuration standpoint. The AGP appears to system software to be a real PCI bus behind PCI-to-PCI bridges resident as devices on PCI bus 0.

The GMCH contains four PCI devices within a single physical component. The configuration registers for the four devices are mapped as devices residing on PCI bus 0.

- **Device 0:** Host-HI Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI bus 0. Physically, Device 0 contains the standard PCI registers, SDRAM registers, the Graphics Aperture controller, configuration for HI, and other GMCH specific registers.
- **Device 1:** Host-AGP Bridge. Logically this appears as a “virtual” PCI-to-PCI bridge residing on PCI bus 0. Physically, Device 1 contains the standard PCI-to-PCI bridge registers and the standard AGP/PCI configuration registers (including the AGP I/O and memory address mapping).
- **Device 2:** Integrated Graphics Controller. Logically this appears as a PCI device residing on PCI bus 0. Physically, Device 2 contains the configuration registers for 3D, 2D, and display functions.
- **Device 3:** Communications Streaming Architecture (CSA) Port. Appears as a virtual PCI-CSA (PCI-to-PCI) bridge device
- **Device 6:** Function 0: Overflow Device. The sole purpose of this device is to provide additional configuration register space for Device 0.

Table 4 shows the Device # assignment for the various internal GMCH devices.

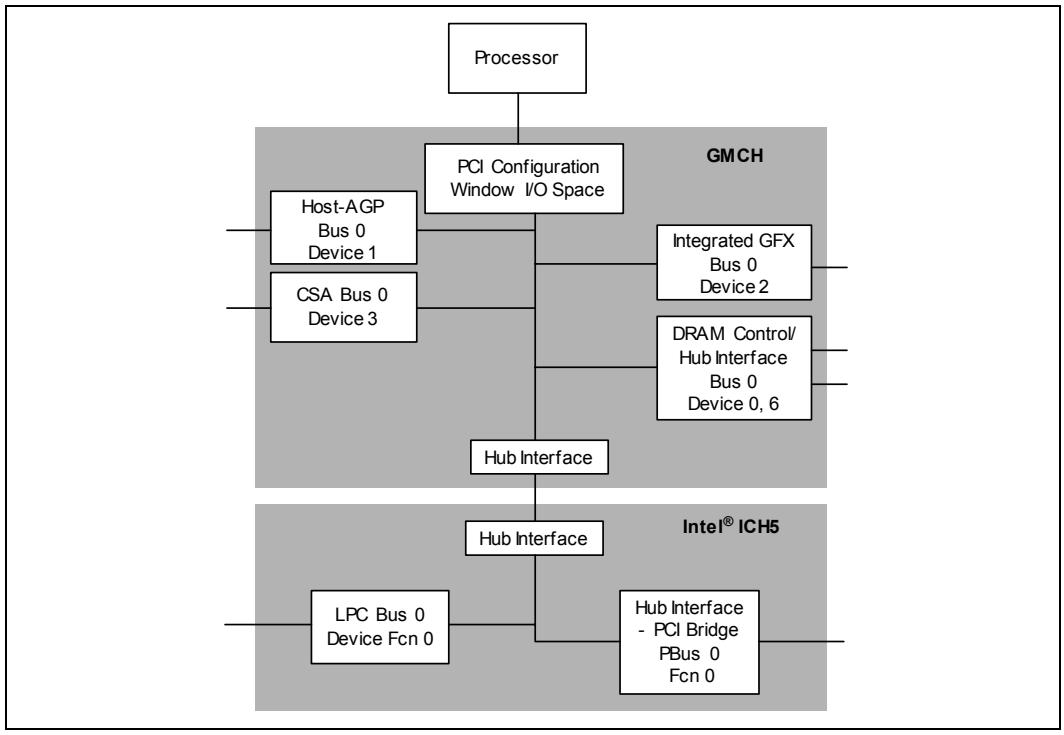
Table 4. Internal GMCH Device Assignment

GMCH Function	Bus #0, Device #
DRAM Controller/8-bit HI Controller	Device 0
Host-to-AGP Bridge (virtual PCI-to-PCI)	Device 1
Integrated Graphics Controller	Device 2
Intergrated GBE (CSA)	Device 3
Overflow	Device 6

Logically, the ICH5 appears as multiple PCI devices within a single physical component also residing on PCI bus 0. One of the ICH5 devices is a PCI-to-PCI bridge. Logically, the primary side of the bridge resides on PCI 0 while the secondary side is the standard PCI expansion bus.

Note: A physical PCI bus 0 does not exist; HI and the internal devices in the GMCH and ICH5 logically constitute PCI Bus 0 to configuration software.

Figure 5. Conceptual Intel® 865G Chipset Platform PCI Configuration Diagram



3.3 Routing Configuration Accesses

The GMCH supports two bus interfaces: HI and AGP/PCI. PCI configuration cycles are selectively routed to one of these interfaces. The GMCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to ICH5 internal devices and Primary PCI (including downstream devices) are routed to the ICH5 via HI. AGP/PCI_B configuration cycles are routed to AGP. The AGP/PCI_B interface is treated as a separate PCI bus from a configuration point of view. Routing of configuration AGP/PCI_B is controlled via the standard PCI-to-PCI bridge mechanism using information contained within the Primary Bus Number, the Secondary Bus Number, and the Subordinate Bus Number registers of the corresponding PCI-to-PCI bridge device.

A detailed description of the mechanism for translating processor I/O bus cycles to configuration cycles on one of the buses is described in the following sub-sections.

3.3.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the GMCH. The PCI 2.3 specification defines the configuration mechanism to access configuration space. The configuration access mechanism uses the CONFIG_ADDRESS register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DWord I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the GMCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The GMCH is responsible for translating and routing the processor’s I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal GMCH configuration registers, HI, or AGP/PCI_B.

3.3.2 PCI Bus #0 Configuration Mechanism

The GMCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0, the configuration cycle is targeting a PCI Bus 0 device. The Host-HI Bridge entity within the GMCH is hardwired as Device 0 on PCI Bus 0. The Host-AGP/PCI_B Bridge entity within the GMCH is hardwired as Device 1 on PCI Bus 0. Device 6 contains test configuration registers.

3.3.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and is less than the value in the Host-AGP/PCI_B device’s Secondary Bus Number register or greater than the value in the Host-AGP/PCI_B device’s Subordinate Bus Number register, the GMCH generates a Type 1 HI Configuration

Cycle. A[1:0] of the HI request packet for the Type 1 configuration cycle is 01. Bits 31:2 of the CONFIG_ADDRESS register are translated to the A[31:2] field of the HI request packet of the configuration cycle as shown in Figure 7. This HI configuration cycle is sent over HI.

If the cycle is forwarded to the ICH5 via HI, the ICH5 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH5's HIs, or a downstream PCI bus.

3.3.4 AGP/PCI_B Bus Configuration Mechanism

From the chipset configuration perspective, AGP/PCI_B is seen as PCI bus interfaces residing on a Secondary Bus side of the virtual PCI-to-PCI bridges referred to as the GMCH Host-PCI_B/AGP bridge. On the Primary bus side, the virtual PCI-to-PCI bridge is attached to PCI Bus 0. Therefore, the Primary Bus Number register is hardwired to 0. The virtual PCI-to-PCI bridge entity converts Type 1 PCI Bus Configuration cycles on PCI Bus 0 into Type 0 or Type 1 configuration cycles on the AGP/PCI_B interface. Type 1 configuration cycles on PCI Bus 0 that have a Bus Number that matches the Secondary Bus Number of the GMCH's "virtual" Host-to-PCI_B/AGP bridge are translated into Type 0 configuration cycles on the PCI_B/AGP interface. The GMCH decodes the Device Number field [15:11] and assert the appropriate GAD signal as an IDSEL in accordance with the PCI-to-PCI bridge Type 0 configuration mechanism. The remaining address bits are mapped as described in Figure 6.

Figure 6. Configuration Mechanism Type 0 Configuration Address-to-PCI Address Mapping

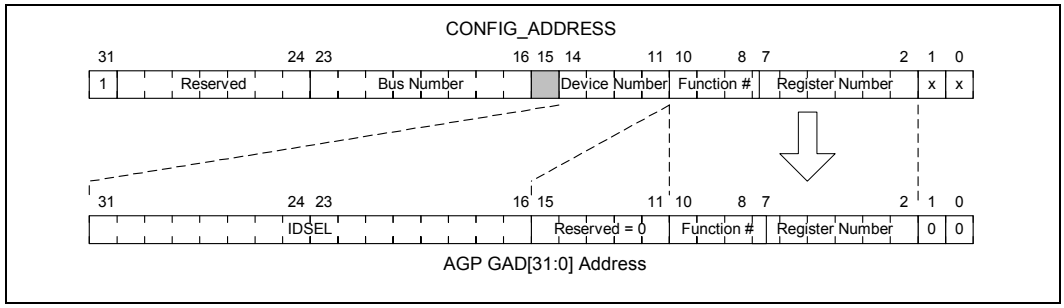


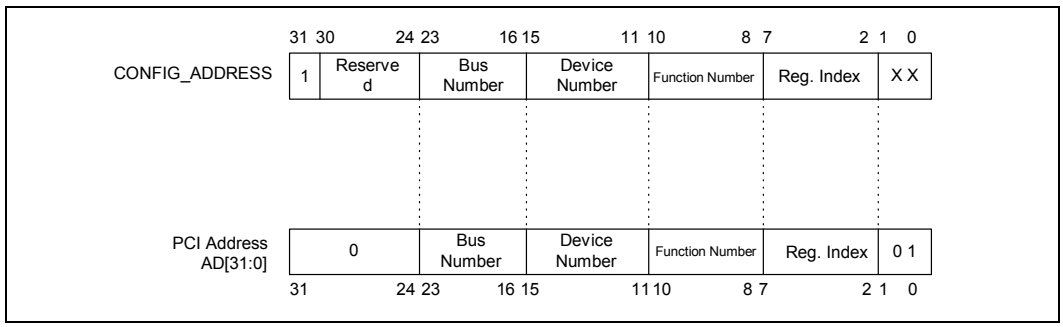
Table 5. Configuration Address Decoding

Config Addr AD[15:11]	AGP GAD[31:16] IDSEL
00000	0000 0000 0000 0001
00001	0000 0000 0000 0010
00010	0000 0000 0000 0100
00011	0000 0000 0000 1000
00100	0000 0000 0001 0000
00101	0000 0000 0010 0000
00110	0000 0000 0100 0000
00111	0000 0000 1000 0000

Config Addr AD[15:11]	AGP GAD[31:16] IDSEL
01000	0000 0001 0000 0000
01001	0000 0010 0000 0000
01010	0000 0100 0000 0000
01011	0000 1000 0000 0000
01100	0001 0000 0000 0000
01101	0010 0000 0000 0000
01110	0100 0000 0000 0000
01111	1000 0000 0000 0000
1xxxx	0000 0000 0000 0000

If the Bus Number is non-zero, greater than the value programmed into the Secondary Bus Number register, and less than or equal to the value programmed into the Subordinate Bus Number register, the configuration cycle is targeting a PCI bus downstream of the targeted interface. The GMCH generates a Type 1 PCI configuration cycle on PCI_B/AGP. The address bits are mapped as shown in Figure 7.

Figure 7. Configuration Mechanism Type 1 Configuration Address-to-PCI Address Mapping



To prepare for mapping of the configuration cycles on AGP/PCI_B, initialization software goes through the following sequence:

1. Scans all devices residing on the PCI Bus 0 using Type 0 configuration accesses.
2. For every device residing at bus 0 that implements PCI-PCI bridge functionality, it will configure the secondary bus of the bridge with the appropriate number and scan further down the hierarchy. This process includes the configuration of the virtual PCI-to-PCI bridges within the GMCH used to map the AGP device's address spaces in a software specific manner.

Note: Although initial AGP platform implementations will not support hierarchical buses residing below AGP, this specification still must define this capability to support PCI-66 compatibility. Note also that future implementations of the AGP devices may support hierarchical PCI or AGP-like buses coming out of the root AGP device.

3.4 I/O Mapped Registers

The GMCH contains two registers that reside in the processor I/O address space: the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h–0CFBh (Accessed as a DWord)
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DWord. A Byte or Word reference will "pass through" the Configuration Address register and HI onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** 1 = Enable 0 = Disable
30:24	Reserved. These bits are read only and have a value of 0.
23:16	**Bus Number.** When the Bus Number is programmed to 00h, the target of the configuration cycle is a HI agent (GMCH, ICH5, etc.). The configuration cycle is forwarded to HI if the Bus Number is programmed to 00h and the GMCH is not the target (i.e., the device number is not equal to 0, 1, 2, 3, 6 or 7). If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number register of Device 1, a Type 0 PCI configuration cycle will be generated on AGP/PCI_B. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of Device 1 and less than or equal to the value programmed into the Subordinate Bus Number register of Device 1, a Type 1 PCI configuration cycle will be generated on AGP/PCI_B. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1's Secondary Bus Number or Subordinate Bus Number register, then a HI Type 1 configuration cycle is generated.
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00, the GMCH decodes the Device Number field. The GMCH is always Device Number 0 for the Host-HI bridge entity and Device Number 1 for the Host-PCI_B/AGP entity. Therefore, when the Bus Number = 0 and the Device Number equals 0,1, 2, 3, 6, the internal GMCH devices are selected. If the Bus Number is non-zero and matches the value programmed into the Device1 Secondary Bus Number register, a Type 0 PCI configuration cycle is generated on AGP/PCI_B. The Device Number field is decoded and the GMCH asserts one and only one GADxx signal as an IDSEL. GAD16 is asserted to access Device 0, GAD17 for Device 1, and so forth up to Device 15 for which will assert AD31. All device numbers higher than 15 cause a type 0 configuration access with no IDSEL asserted; this will result in a Master Abort reported in the GMCH's virtual PCI-to-PCI bridge registers. For Bus Numbers resulting in HI configuration cycles, the GMCH propagates the Device Number field as A[15:11]. For Bus Numbers resulting in AGP/PCI_B Type 1 configuration cycles, the Device Number is propagated as GAD[15:11].
10:8	**Function Number.** This field is mapped to GAD[10:8] during AGP/PCI_B configuration cycles and A[10:8] during HI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH ignores configuration cycles to its internal devices if the function number is not equal to 0.
7:2	**Register Number.** This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address register. This field is mapped to GAD[7:2] during AGP/PCI_B Configuration cycles and A[7:2] during HI configuration cycles.
1:0	Reserved. These bits are read only.

3.4.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh–0CFFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to CONFIG_DATA are mapped to configuration space using the contents of CONFIG_ADDRESS.

3.5 DRAM Controller/Host-Hub Interface Device Registers (Device 0)

This section contains the DRAM Controller and Host-Hub Interface PCI configuration registers listed in order of ascending offset address. The register address map is shown in Table 6.

Table 6. DRAM Controller/Host-Hub Interface Device Register Address Map (Device 0) (Sheet 1 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2570h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	See register description	RO
09h	—	Intel Reserved	—	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0C	—	Intel Reserved	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh	—	Intel Reserved	—	—
10–13h	APBASE	Aperture Base Configuration	00000008h	RO, R/W
14–2Bh	—	Intel Reserved	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
30–33h	—	Intel Reserved	—	—
34h	CAPPTR	Capabilities Pointer	E4h	RO
35–50h	—	Intel Reserved	—	RO
51h	AGPM	AGP Miscellaneous Configuration	00h	R/W
52h	GC	Graphics Control	0000_1000b	R/W
53h	CSABCONT	CSA Basic Control	00h	RO, R/W
54-5Fh	—	Intel Reserved	—	—
60h	FPLLCONT	FPLL Clock Control	00h	R/W, RO
61–89h	—	Intel Reserved	—	—
90h	PAM0	Programmable Attribute Map 0	00h	RO, R/W
91h	PAM1	Programmable Attribute Map 1	00h	RO, R/W
92h	PAM2	Programmable Attribute Map 2	00h	RO, R/W
93h	PAM3	Programmable Attribute Map 3	00h	RO, R/W
94h	PAM4	Programmable Attribute Map 4	00h	RO, R/W

Table 6. DRAM Controller/Host-Hub Interface Device Register Address Map (Device 0) (Sheet 2 of 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
95h	PAM5	Programmable Attribute Map 5	00h	RO, R/W
96h	PAM6	Programmable Attribute Map 6	00h	RO, R/W
97h	FDHC	Fixed SDRAM Hole Control	00h	RO, R/W
98–9Ch	—	Intel Reserved	—	—
9Dh	SMRAM	System Management RAM Control	02h	RO, R/W, L
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RO, R/W, RWC, L
9Fh	—	Intel Reserved	—	—
A0–A3h	ACAPID	AGP Capability Identifier	00300002h	RO
A4–A7h	AGPSTAT	AGP Status	See register description	RO
A8–ABh	AGPCMD	AGP Command	See register description	RO, R/W
AC–AFh	—	Intel Reserved	—	—
B0-B3h	AGPCTRL	AGP Control	0000 0000h	RO, R/W
B4h	APSIZE	Aperture Size	00h	RO, R/W
B5–B7h	—	Intel Reserved	—	—
B8–BBh	ATTBASE	Aperture Translation Table	00000000h	R/W
BCh	AMTT	AGP MTT Control	10h	***RO,*** R/W
BDh	LPTT	AGP Low Priority Transaction Timer	10h	R/W
BE–C3h	—	Intel Reserved	—	—
C4–C5h	TOUD	Top of Used DRAM	0400h	RO, R/W
C6–C7h	GMCHCFG	GMCH Configuration	0000h	R/WO, RO, R/W
C8–C9h	ERRSTS	Error Status	0000h	R/WC
CA–CEh	ERRCMD	Error Command	0000h	RO, R/W
CF–DDh	—	Intel Reserved	—	—
DE–DFh	SKPD	Scratchpad Data	0000h	R/W
E0–E3h	—	Intel Reserved	—	—
E4–E8h	CAPREG	Capability Identification	FF_F104_A009h	RO
E9–FFh	—	Intel Reserved	—	—

3.5.1 VID—Vendor Identification Register (Device 0)

Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Vendor Identification (VID)—RO.** This register field contains the PCI standard identification for Intel, 8086h.

3.5.2 DID—Device Identification Register (Device 0)

Address Offset: 02–03h
Default Value: 2570h
Access: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Device Identification Number (DID)—RO.** This is a 16-bit value assigned to the GMCH Host-HI Bridge Function 0.

3.5.3 PCICMD—PCI Command Register (Device 0)

Address Offset: 04–05h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since GMCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented. Writes to non-implemented bits have no effect.

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back Enable (FB2B)—RO.** Hardwired to 0. This bit controls whether or not the master can do fast back-to-back writes. Since Device 0 is strictly a target, this bit is not implemented and is hardwired to 0.
8	**SERR Enable (SERRE)—R/W.** This bit is a global enable bit for Device 0 SERR messaging. The GMCH does not have a SERR signal. The GMCH communicates the SERR condition by sending a SERR message over HI to the ICH5. 0 = Disable. The SERR message is not generated by the GMCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR HI message mechanism. 1 = Enable. The GMCH is enabled to generate SERR messages over HI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers.
7	**Address/Data Stepping Enable (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0. The PERR# signal is not implemented by the GMCH.
5	**VGA Palette Snoop Enable (VGASNOOP)—RO.** Hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0. The GMCH will never issue memory write and invalidate commands.
3	**Special Cycle Enable (SCE)—RO.** Not implemented; hardwired to 0.
2	**Bus Master Enable (BME)—RO.** Hardwired to 1. GMCH is always enabled as a master on HI.
1	**Memory Access Enable (MAE)—RO.** Hardwired to 1. The GMCH always allows access to main memory.
0	**I/O Access Enable (IOAE)—RO.** Hardwired to 0.

3.5.4 PCISTS—PCI Status Register (Device 0)

Address Offset: 06–07h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device 0's PCI interface. Since GMCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0.
14	**Signaled System Error (SSE)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to it. 1 = GMCH Device 0 generated a SERR message over HI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers.
13	**Received Master Abort Status (RMAS)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to it. 1 = GMCH generated a HI request that receives a Master Abort completion packet or Master Abort Special Cycle.
12	**Received Target Abort Status (RTAS)—R/WC.** 0 = Software sets this bit to 0 by writing a 1 to it. 1 = GMCH generated a HI request that receives a Target Abort completion packet or Target Abort Special Cycle.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The GMCH will not generate a Target Abort HI completion packet or Special Cycle.
10:9	**DEVSEL Timing (DEVT)—RO.** Hardwired to 00. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the GMCH.
8	**Master Data Parity Error Detected (DPD)—RO.** Hardwired to 0. PERR signaling and messaging are not implemented by the GMCH.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the GMCH.
6:5	Reserved.
4	**Capability List (CLIST)—RO.** Hardwired to 1. A 1 indicates to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides.
3:0	Reserved.

3.5.5 RID—Revision Identification Register (Device 0)

Address Offset: 08h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH Device 0.

Bit	Descriptions
7:0	**Revision Identification Number (RID)—RO.** This is an 8-bit value that indicates the revision identification number for the GMCH Device 0. 02h = A-2 stepping

3.5.6 SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the GMCH Device 0.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of bridge for the GMCH. 00h = Host bridge.

3.5.7 BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh
Default Value: 06h
Access: RO
Size: 8 bits

This register contains the Base Class Code of the GMCH Device 0.

Bit	Descriptions
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the Base Class Code for the GMCH. 06h = Bridge device.

3.5.8 MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the GMCH is not a PCI master. Therefore, this register is not implemented.

Bit	Descriptions
7:0	Reserved.

3.5.9 HDR—Header Type Register (Device 0)

Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**PCI Header (HDR)—RO.** This field always returns 0 to indicate that the GMCH is a single function device with standard header layout.

3.5.10 APBASE—Aperture Base Configuration Register (Device 0)

Address Offset: 10–13h
Default Value: 00000008h
Access: RO, R/W
Size: 32 bits

The APBASE is a standard PCI base address register that is used to set the base of the graphics aperture. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0 or behave as hardwired to 0). To allow for flexibility (of the aperture) an additional register called APSIZE is used as a "back-end" register to control which bits of the APBASE will behave as hardwired to 0. This register will be programmed by the GMCH specific BIOS code that will run before any of the generic configuration software is run.

Note: Bit 1 of the AGPM register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and the appropriate translation table structure has been established in the main memory.

Bit	Descriptions
31:28	**Upper Programmable Base Address (UPBITS)—R/W.** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits [31:28] of the base address in the processor's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write.
27:22	**Middle Hardwired/Programmable Base Address (MIDBITS)—R/W.** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits [27:4] of the base address in the processor's address space that cause a graphics aperture translation to be inserted into the path of any memory read or write. These bits can behave as though they were hardwired to 0 if programmed to do so by the APSIZE bits of the APSIZE register. This causes configuration software to understand that the granularity of the graphics aperture base address is either finer or more coarse, depending upon the bits set by GMCH-specific configuration software in APSIZE.
21:4	**Lower Bits (LOWBITS)—RO.** Hardwired to 0s. This forces the minimum aperture size selectable by this register to be 4 MB, without regard to the aperture size definition enforced by the APSIZE register.
3	**Prefetchable (PF)—RO.** Hardwired to 1 to identify the graphics aperture range as a prefetchable as per the PCI specification for base address registers. This implies that there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and the GMCH may merge processor writes into this range without causing errors.
2:1	**Addressing Type (TYPE)—RO.** Hardwired to 00 to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	**Memory Space Indicator (MSPACE)—RO.** Hardwired to 0 to identify the aperture range as a memory range as per the specification for PCI base address registers.

3.5.11 SVID—Subsystem Vendor Identification Register (Device 0)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)—R/WO.** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.5.12 SID—Subsystem Identification Register (Device 0)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)—R/WO.** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.5.13 CAPPTR—Capabilities Pointer Register (Device 0)

Address Offset: 34h
Default Value: E4h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	**Capabilities Pointer Address— RO.** This field contains the pointer to the offset of the first capability ID register block. In this case the first capability is the Product-Specific Capability, which is located at offset E4h.

3.5.14 AGPM—AGP Miscellaneous Configuration Register (Device 0)

Address Offset: 51h
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Descriptions
7:2	Reserved.
1	**Aperture Access Global Enable (APEN)—R/W.** This bit is used to prevent access to the graphics aperture from any port (processor, HI, or AGP/PCI_B) before the aperture range is established by the configuration software and the appropriate translation table in the main SDRAM has been initialized. 0 = Disable.The default value is 0, so this field must be set after system is fully configured to enable aperture accesses. 1 = Enable.
0	Reserved.

3.5.15 GC—Graphics Control Register (Device 0)

Address Offset: 52h
Default Value: 0000_1000h
Access: R/W, R/W/L
Size: 8 bits

Bit	Descriptions
7	Reserved
6:4	**Graphics Mode Select (GMS)—R/W/L.** This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. (Default) 001 = DVMT (UMA) mode:1 MB of memory pre-allocated for frame buffer. 010 = Reserved 011 = DVMT (UMA) mode:8 MB of memory pre-allocated for frame buffer. 100 = DVMT (UMA) mode:16 MB of memory pre-allocated for frame buffer. 101 =Reserved 110 = Reserved 111 = Reserved **NOTE:** These register bits are locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
3	**Integrated Graphics Disable (IGDIS)—R/W.** 0 = IGD Enable. When this bit is 0, the GMCH's Device 1 is disabled such that all configuration cycles to Device 1 flow through to HI. Also, the Next_Pointer field in the CAPREG register (Dev 0, Offset E4h) will be RO at A0h. 1 = IGD is disabled and AGP Graphics is enabled (default). The GMCH's Device 2 and associated spaces are disabled; all configuration cycles to Device 2 flow through to HI. **NOTE:** When writing a new value to this bit, software must perform a clock synchronization sequence.
2	Reserved
1	**IGD VGA Disable (IVD)—R/W.** 0 = IGD claims VGA memory and I/O cycles; the Sub-Class Code within Device 2 Class Code register is 00h. (Default) 1 = IGD does not claim VGA cycles (Memory and I/O); the Sub-Class Code field within Device 2 Class Code register is 80h.
0	Reserved

Notes on Pre-Allocated Memory for Graphics

These register bits control the use of memory from main memory space as graphics local memory. The memory for TSEG is pre-allocated first and then the graphics local memory is pre-allocated. An example of this theft mechanism is:

TOUD equals 62.5 MB = 03E7FFFFh
TSEG selected as 512 KB in size,
Graphics local memory selected as 1 MB in size
General System RAM available in system = 62.5 MB
    General system RAM range00000000h to 03E7FFFFh
    TSEG address range03F80000h to 03FFFFFFh
    TSEG pre-allocated from03F80000h to 03FFFFFFh
    Graphics local memory pre-allocated from03E80000h to 03F7FFFFh

VGA Memory and I/O Space Decode Priority

1. Integrated Graphics Device (IGD), Device 2.
2. PCI-to-PCI bridge, Device 1.
3. Hub Interface.

VGA Memory Space Decode to IGD

IF IGE = 1 AND IVD = 0 AND Device 2 Mem_Access_En = 1 AND Device 2 in powered up D0 state AND MSRb1 = 1
AND →

Additional qualification within IGD decode (comprehends MDA requirements)

Mem Access→ GR06(3:2)	A0000h–AFFFFh	B0000h–B7FFFh	B8000h–BFFFFh
00	IGD	IGD	IGD
01	IGD	PCI-to-PCI Bridge or Hub Interface	PCI-to-PCI Bridge or Hub Interface
10	PCI-to-PCI Bridge or Hub Interface	IGD	PCI-to-PCI Bridge or Hub Interface
11	PCI-to-PCI Bridge or Hub Interface	PCI-to-PCI Bridge or Hub Interface	IGD

ELSE VGA Mem space legacy decode:

IF Device 1 Mem_Access_En = 1.

VGA Mem Range xA0000h – xBFFFFh
MDA Mem Range xB0000h – xB7FFFh

VGA_en	MDAP	Range	Destination	Exceptions/Notes
0	0	VGA, MDA	Hub Interface	
0	1	Illegal	Illegal	Illegal
1	0	VGA, MDA	AGP	
1	1	VGA, MDA	AGP, Hub Interface	

ELSE defaults to Hub Interface.

VGA IO space decode to IGD:

IF IGE = 1 AND IVD = 0 AND Device 2 IO_Access_En = 1 AND Device 2 in Powered up D0 state AND →

Additional qualification within IGD decode (comprehends MDA requirements).

IO Access → MSRb0	3CX	3DX	3B0h–3BBh	3BCh–3BFh
0	IGD	PCI-to-PCI Bridge or Hub Interface	IGD	PCI-to-PCI Bridge or Hub Interface
1	IGD	IGD	PCI-to-PCI Bridge or Hub Interface	PCI-to-PCI Bridge or Hub Interface

ELSE VGA IO space Legacy Decode:

IF Device 1 IO_Access_En = 1.

VGA I/O x3B0h – x3BBh and x3C0h – x3DFh
MDA I/O x3B4h, x3B5h, x3B8h, x3B9h, x3BAh, x3BFh

VGA_EN	MDAP	Range	Destination	Exceptions/Notes
0	0	VGA, MDA	Hub Interface	x3BCh – x3BFh goes to AGP if ISA enabled bit is not set in Device 1
0	1	Illegal	Illegal	Illegal
1	0	VGA	AGP	Non-VGA Ranges will also go to Hub Interface
1	1	VGA, MDA	AGP Hub Interface	x3BCh – x3BEh will also go to Hub Interface

ELSE defaults to Hub Interface.

3.5.16 CSABCONT—CSA Basic Control Register (Device 0)

Address Offset: 53h
Default: 00h
Access: R/W, RO
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**Device Not Present bit—R/W.** 0 = Device Not Enabled 1 = Device Enabled

3.5.17 FPLLCONT— Front Side Bus PLL Clock Control Register (Device 0)

Address Offset: 60h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

These register bits are used for changing DDR frequency initializing GMCH memory and I/O clocks WIO DLL delays, and initializing internal graphics controller's clocks and resets.

Bit	Descriptions
7:5	Reserved.
4	**Memory and Memory I/O DLL Clock Gate (DLLCKGATE)—R/W.** 0 = Writing a 0 will cleanly re-enable the memory and memory I/O clocks from the DLL outputs. 1 = Writing a 1 will cleanly disable the memory and memory IO clocks of the chipset core and DDR interface from the DLL outputs. **NOTE:** This bit should always be written to before writing to the FPLLSYNC bit.
3	**Graphics Activate (GFXACT)—R/W.** 1 = After propagating the internal graphics enable, writing a 1 to this bit will cause the internal graphics logic to come out of reset. After a 1 has been written, the GMCH will take the internal graphics logic out of reset. From then on, the internal graphics can only be put back into reset with a hardware reset.
2	**Propagate Internal Graphics Enable (PIGE)—R/W.** 0 = This bit should be set to 0 shortly after setting it to 1, though no action is taken on writing a 0. 1 = After writing a 0 to IGDIS (Dev 0, Offset 52, bit 3) to enable internal graphics, writing a 1 to this bit will propagate the IGDIS register to the chip which will make the configuration space for Device 1 (AGP Bridge) disappear and Device 2 (integrated graphics) appear. Propagating the IGE will also enable the graphics clock.
1	**FSB PLL Sync (FPLLSYNC)—R/W.** 0 = After writing a 1, writing a 0 will cause the FSB PLL to synchronize the memory and graphics core clocks to the processor clock. 1 = Writing a 1 will reset the memory and core graphics clock dividers in the FSB FPLL. This will also enable the output of the system memory frequency bits and the Graphics Clock Test Mode register to propagate to the chip and the FPLL.
0	**Graphics/Memory Clock Gate (GMCLKGATE)—R/W.** 0 = Writing a 0 restarts (enable) the clocks. 1 = Writing a 1 cleanly disables the graphics and memory clocks while still enabling the core clocks. The memory and graphics clocks can then be programmed with new speed information. **NOTE:** This bit should always be written to before writing to the FPLLSYNC bit.

3.5.18 PAM[0:6]—Programmable Attribute Map Registers (Device 0)

Address Offset: 90–96h (PAM0–PAM6)
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits each register

The GMCH allows programmable memory attributes on 13 legacy memory segments of various sizes in the 640-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to host initiator only access to the PAM areas. GMCH will forward to main memory for any AGP, PCI, or HI initiated accesses to the PAM areas. These attributes are:

RE **Read Enable.** When RE = 1, the host read accesses to the corresponding memory segment are claimed by the GMCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE **Write Enable.** When WE = 1, the host write accesses to the corresponding memory segment are claimed by the GMCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be read only, write only, read/write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is read only.

Each PAM register controls two regions, typically 16 KB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and defined in the following table.

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	Disabled. Main memory is disabled and all accesses are directed to the Hub Interface A. The GMCH does not respond as a PCI target for any read or write access to this area.
X	X	0	1	Read Only. Reads are forwarded to main memory and writes are forwarded to the Hub Interface A for termination. This write protects the corresponding memory segment. The GMCH will respond as an AGP or the Hub Interface target for read accesses but not for any write accesses.
X	X	1	0	Write Only. Writes are forwarded to DRAM and reads are forwarded to the Hub Interface for termination. The GMCH will respond as an AGP or Hub Interface target for write accesses but not for any read accesses.
X	X	1	1	Read/Write. This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the GMCH and forwarded to main memory. The GMCH will respond as an AGP or the Hub Interface target for both read and write accesses.

At the time that a HI or AGP access to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writable.

As an example, consider BIOS that is implemented on the expansion bus. During the initialization process, BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address that is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Figure 8 and Table 7 show the PAM registers and the associated attribute bits.

Figure 8. PAM Register Attributes

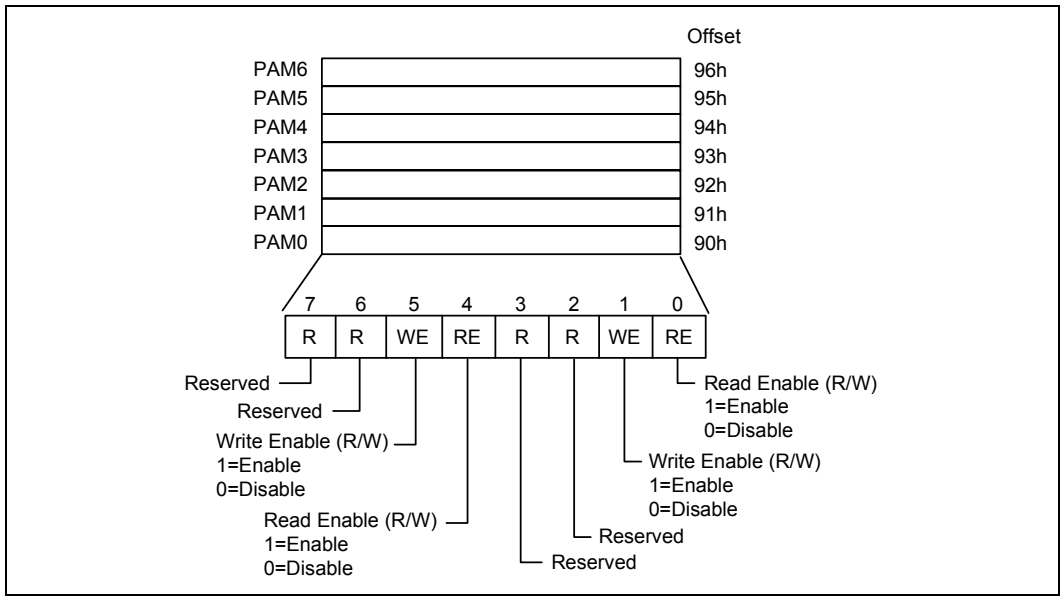


Table 7. PAM Register Attributes

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						90h
PAM0[7:6]	Reserved						90h
PAM0[5:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	90h
PAM1[1:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	91h
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	91h
PAM2[1:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	92h
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	92h
PAM3[1:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	93h
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	93h
PAM4[1:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	94h
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	94h
PAM5[1:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	95h
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	95h
PAM6[1:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	96h
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	96h

For details on overall system address mapping scheme see Chapter 4.

DOS Application Area (00000h–9FFFh)

The DOS area is 640 KB in size, and it is further divided into two parts. The 512-KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the GMCH, while the 128-KB address range from 080000 to 09FFFFh can be mapped to PCI_A or to main memory. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI_A) via the GMCH's FDHC configuration register.

Video Buffer Area (A0000h–BFFFFh)

Attribute bits do not control this 128-KB area. The host-initiated cycles in this region are always forwarded to either PCI_A or AGP unless this range is accessed in SMM mode. **Routing of accesses is controlled by the Legacy VGA control mechanism of the virtual PCI-to-PCI bridge device in the GMCH.**

This area can be programmed as SMM area via the SMRAM register. When used as a SMM space, this range cannot be accessed from the HI or AGP.

Expansion Area (C0000h–DFFFFh)

This 128 KB area is divided into eight, 16-KB segments, which can be assigned with different attributes via PAM control register as defined by Table 7.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four 16-KB segments that can be assigned with different attributes via the PAM Control register as defined by Table 7.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-KB segment that can be assigned with different attributes via PAM control register as defined by Table 7.

3.5.19 FDHC—Fixed Memory(ISA) Hole Control Register (Device 0)

Address Offset: 97h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This 8-bit register controls a fixed SDRAM hole from 15–16 MB.

Bit	Descriptions
7	**Hole Enable (HEN)—R/W.** This field enables a memory hole in SDRAM space. The SDRAM that lies "behind" this space is not remapped. 0 =Disable. No memory hole. 1 =Enable. Memory hole from 15 MB to 16 MB.
6:0	Reserved.

3.5.20 SMRAM—System Management RAM Control Register (Device 0)

Address Offset: 9Dh
Default Value: 02h
Access: R/W, RO, Lock
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The open, close, and lock bits function only when the G_SMRAME bit is set to 1. Also, the open bit must be reset before the lock bit is set.

Bit	Descriptions
7	Reserved.
6	**SMM Space Open (D_OPEN)—R/W.** When D_OPEN=1 and D_LCK=0, the SMM space SDRAM is made visible, even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	**SMM Space Closed (D_CLS)—R/W.** When D_CLS = 1, SMM space SDRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space SDRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	**SMM Space Locked (D_LCK)—R/W.** When D_LCK is set to 1, then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRARE)—R/W/L.** If set to 1, Compatible SMRAM functions are enabled, providing 128 KB of SDRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has to be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG)—RO.** This field indicates the location of SMM space. SMM SDRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to HI. Since the GMCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

3.5.21 ESMRAMC—Extended System Management RAM Control (Device 0)

Address Offset: 9Eh
Default Value: 38h
Access: R/W, R/WC, RO, Lock
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Descriptions
7	**Enable High SMRAM (H_SMRAME)—R/W/L.** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME (this bit) is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to SDRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	**Invalid SMRAM Access (E_SMERR)—R/WC.** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. **NOTE:** Software must write a 1 to this bit to clear it.
5	**SMRAM Cacheable (SM_CACHE)—RO.** Hardwired to 1.
4	**L1 Cache Enable for SMRAM (SM_L1)—RO.** Hardwired to 1.
3	**L2 Cache Enable for SMRAM (SM_L2)—RO.** Hardwired to 1.
2:1	**TSEG Size (TSEG_SZ)—R/W.** This field selects the size of the TSEG memory block, if enabled. Memory from the top of SDRAM space (TOUD +TSEG_SZ) to TOUD is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to HI when the TSEG memory block is enabled. 00 =Reserved 01 =Reserved 10=(TOUD + 512 KB) to TOUD 11 =(TOUD + 1 MB) to TOUD
0	**TSEG Enable (T_EN)—R/W/L.** This bit enables SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

3.5.22 ACAPID—AGP Capability Identifier Register (Device 0)

Address Offset: A0h–A3h
Default Value: 00300002h
Access: RO
Size: 32 bits

This register provides standard identifier for AGP capability.

Bit	Descriptions
31:24	Reserved.
23:20	**Major AGP Revision Number (MAJREV)—RO.** These bits provide a major revision number of AGP specification to which this version of GMCH conforms. This field is hardwired to value of 0011b (i.e., implying Rev 3.x).
19:16	**Minor AGP Revision Number (MINREV)—RO.** These bits provide a minor revision number of AGP specification to which this version of GMCH conforms. This number is hardwired to value of 0000 which implies that the revision is x.0. Together with major revision number this field identifies the GMCH as an AGP Rev 3.0 compliant device.
15:8	**Next Capability Pointer (NCAPTR)—RO.** AGP capability is the first and the last capability described via the capability pointer mechanism and therefore these bits are hardwired to 0 to indicate the end of the capability linked list.
7:0	**AGP Capability ID (CAPID)—RO.** This field identifies the linked list item as containing AGP registers. This field has a value of 0000_0010b assigned by the PCI SIG.

3.5.23 AGPSTAT—AGP Status Register (Device 0)

Address Offset: A4–A7h
Default Value: 1F004217h in AGP 2.0 mode
1F004A13h in AGP 3.0 mode
Access: RO
Size: 32 bits

This register reports AGP device capability/status.

Bit	Descriptions
31:24	**Request Queue (RQ)—RO.** Hardwired to 1Fh to indicate that a maximum of 32 outstanding AGP command requests can be handled by the GMCH. This field contains the maximum number of AGP command requests the GMCH is configured to manage.
23:16	Reserved.
15:13	**ARQSZ—RO.** This field is LOG2 of the optimum asynchronous request size in bytes minus 4 to be used with the target. The master should attempt to issue a group of sequential back-to-back asynchronous requests that total to this size and for which the group is naturally aligned. Optimum_request_size = 2 ^ (ARQSZ+4). Hardwired to 010 to indicate 64 B
12:10	**CAL_Cycle—RO.** This field specifies the required period for GMCH initiated bus cycle for calibrating I/O buffers. Hardwired to 010, indicating 64 ms.
9	**Side Band Addressing Support (SBA)—RO.** Hardwired to 1, indicating that the GMCH supports side band addressing.
8:6	Reserved.
5	**Greater Than Four Gigabyte Support (GT4GIG)—RO.** Hardwired to 0, indicating that the GMCH does not support addresses greater than 4 GB.

Bit	Descriptions
4	**Fast Write Support (FW)—RO.** Hardwired to 1, indicating that the GMCH supports Fast Writes from the processor to the AGP master.
3	**AGP 3.0 mode (AGP 30_MOD—RO.** This bit is set by the hardware on the assertion of PWROK based on the AGP 3.0 detection via the Vref comparator on the GVREF pin. In AGP 2.0 mode, GVREF is driven to 0.75 V, while in AGP 3.0 mode, GVREF is driven to 0.35 V. Note that the output of the Vref comparator is used “live” prior to the assertion of PWROK and used to select the appropriate pull-up, pull-down or termination on the I/O buffer depending on the mode selected. 0 = AGP 2.0 (1.5 V signaling) mode. 1 = AGP 3.0 signaling mode.
2:0	**Data Rate Support (RATE)—RO.** After reset, the GMCH reports its data transfer rate capability. AGP 2.0 Mode • **Bit 0 identifies if AGP device supports 1X data transfer mode,** • **Bit 1 identifies if AGP device supports 2X data transfer mode, (unsupported)** • **Bit 2 identifies if AGP device supports 4X data transfer.** AGP 3.0 Mode • **Bit 0 identifies if AGP device supports 4X data transfer mode,** • **Bit 1 identifies if AGP device supports 8X data transfer mode,** • **Bit 2 is reserved.** **NOTES:** 1. In AGP 3.0 mode (AGP_MODE=1) these bits are 011 indicating that both 4X and 8X modes are supported. 2. In AGP 2.0 mode these bits are 111 indicating that 4X, 2X, and 1X modes are supported; however, in the 82865G GMCH 2X is not supported.

3.5.24 AGPCMD—AGP Command Register (Device 0)

Address Offset: A8–ABh
Default Value: 00000000h in AGP 2.0 mode
00000A00h in AGP 3.0 mode
Access: RO, R/W
Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Descriptions
31:13	Reserved.
12:10	**PCAL_Cycle—R/W.** This filed is programmed with the period for GMCH-initiated bus cycle for calibrating I/O buffers for both master and target. This value is updated with the smaller of the value in CAL_CYCLE from Master's and Target's AGPSTAT.CAL_CYCLE. PCAL_CYCLE is set to 111 by software only if both the Target and Master have AGPSTAT.CAL_CYCLE = 111. 000 = 4 ms 001 = 16 ms 010 = 64 ms (Default). 011 = 256 ms 100–110 = Reserved 111 = Calibration Cycle Not Needed
9	**Side Band AddressingEnable (SBAEN)—R/W.** This bit is ignored in AGP 3.0 mode to allow legacy 2.0 software to work. (When AGP 3.0 is detected, sideband addressing mechanism is automatically enabled by the hardware.) 0 = Disable. 1 = Enable. Side band addressing mechanism is enabled.
8	**AGP Enable (AGPEN)—R/W.** 0 = Disable. GMCH ignores all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced, even if this bit is reset to 0. If this bit transitions from 1 to 0 on a clock edge in the middle of an SBA command being delivered in 1X mode, the command will be issued. 1 = Enable. GMCH responds to AGP operations delivered via PIPE#, or to operations delivered via SBA if the AGP Side Band Enable bit is also set to 1.
7:6	Reserved.
5	**Greater Than Four Gigabyte Enable (GT4GIGE)—RO.** Hardwired to 0 indicating that the GMCH, as an AGP target, does not support addressing greater than 4 GB.
4	**Fast Write Enable (FWEN)—R/W.** 0 = Disable. When this bit is cleared, or when the data rate bits are set to 1X mode, the memory write transactions from the GMCH to the AGP master use standard PCI protocol. 1 = Enable. The GMCH uses the Fast Write protocol for memory write transactions from the GMCH to the AGP master. Fast Writes will occur at the data transfer rate selected by the data rate bits (2:0) in this register.
3	Reserved.
2:0	**Data Rate Enable (DRATE)—R/W.** The setting of these bits determines the AGP data transfer rate. One (and only one) bit in this field must be set to indicate the desired data transfer rate. The same bit must be set on both master and target. **AGP 2.0** 001= 1X Transfer Mode (for AGP 2.0 signaling) 010= 2X Transfer Mode (NOT SUPPORTED) 100= 4X Transfer Mode (for AGP 2.0 signaling) **AGP 3.0** 001= 4X transfer mode (for AGP 3.0 signaling) 010= 8X Transfer mode (for AGP 3.0 signaling) 100= Reserved

3.5.25 AGPCTRL—AGP Control Register (Device 0)

Address Offset: B0–B3h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides for additional control of the AGP interface.

Bit	Descriptions
31:8	Reserved.
7	**GTLB Enable (GTLBEN)— R/W.** 0 = Disable (default). The GTLB is flushed by clearing the valid bits associated with each entry. In this mode of operation: — All accesses that require translation bypass the GTLB — All requests that are positively decoded to the graphics aperture force the GMCH to access the translation table in main memory before completing the request — Valid translation table entry fetches will not be cached in the GTLB — Invalid translation table entry fetches will still be cached in the GTLB (ejecting the least recently used entry). 1 = Enable. Normal operations of the Graphics Translation Lookaside Buffer are enabled. **NOTE:** This bit can be changed dynamically (i.e., while an access to GTLB occurs); however, the completion of the configuration write that asserts or deasserts this bit will be delayed pending a complete flush of all dirty entries from the write buffer. This delay will be incurred because this bit is used as a mechanism to signal the chipset that the graphics aperture translation table is about to be modified or has completed modifications. In the first case, all dirty entries need to be flushed before the translation table is changed. In the second case, all dirty entries need to be flushed because one of them is likely to be a translation table entry which must be made visible to the GTLB by flushing it to memory.
6:1	Reserved.
0	**4X Override (OVER4X)—R/W.** This back-door register bit allows the BIOS to force 1X mode for AGP 2.0 and 4X mode for AGP 3.0. Note that this bit must be set by the BIOS before AGP configuration. 0 = No override 1 = The RATE[2:0] bit in the AGPSTS register will be read as a 001.

3.5.26 APSIZE—Aperture Size Register (Device 0)

Address Offset: B4h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register determines the effective size of the graphics aperture used for a particular GMCH configuration. This register can be updated by the GMCH-specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated, then a default value will select an aperture of maximum size (i.e., 256 MB). The size of the table that will correspond to a 256-MB aperture is not practical for most applications; therefore, these bits must be programmed to a smaller practical value that will force adequate address range to be requested via APBASE register from the PCI configuration software.

Bit	Descriptions
7:6	Reserved.
5:0	**Graphics Aperture Size (APSIZE)—R/W.** Each bit in APSIZE[5:0] operates on similarly ordered bits in APBASE[27:22] of the Aperture Base configuration register. When a particular bit of this field is 0, it forces the similarly ordered bit in APBASE[27:22] to behave as hardwired to 0. When a particular bit of this field is set to 1, it allows the corresponding bit of the APBASE[27:22] to be read/write accessible. The default value (APSIZE[5:0]=000000b) forces the default APBASE[27:22] to read as 000000b (i.e., all bits respond as hardwired to 0). This provides the maximum aperture size of 256 MB. As another example, programming APSIZE[5:0] to 111000b hardwires APBASE[24:22] to 000b and enables APBASE[27:25] to be read/write programmable. 000000 = 256-MB aperture size 100000 = 128-MB aperture size 110000 = 64-MB aperture size 111000 = 32-MB aperture size 111100 = 16-MB aperture size 111110 = 8-MB aperture size 111111 = 4-MB aperture size

3.5.27 ATTBASE—Aperture Translation Table Register (Device 0)

Address Offset: B8-BBh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table Base located in the main memory. This value is used by the GMCH's graphics aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical main memory address. The ATTBASE register may be dynamically changed.

Bit	Descriptions
31:12	**Aperture Translation Table Base (TTABLE)—R/W.** This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory. Note that it should be modified only when the GTLB has been disabled.
11:0	Reserved.

3.5.28 AMTT—AGP MTT Control Register (Device 0)

Address Offset: BCh
Default Value: 10h
Access: RO, R/W
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the GMCH's arbiter allows AGP/PCI master to perform multiple back-to-back transactions. The GMCH's AMTT mechanism is used to optimize the performance of the AGP master (using PCI semantics) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the Processor-AGP/PCI transactions as well and it assures the processor of a fair share of the AGP/PCI interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8-clock granularity. For example, if the AMTT is programmed to 18h, then the selected value corresponds to the time period of 24 AGP (66 MHz) clocks. Set by BIOS.

Bit	Descriptions
7:3	**Multi-Transaction Timer Count Value (MTTC)—R/W.** The number programmed into these bits represents the time slice (measured in eight, 66 MHz clock granularity) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent.
2:0	Reserved.

3.5.29 LPTT—AGP Low Priority Transaction Timer Register (Device 0)

Address Offset: BDh
Default Value: 10h
Access: RO, R/W
Size: 8 bits

LPTT is an 8-bit register similar in function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms.

The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires, the AGP arbiter may grant the bus to another agent if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8-clock granularity. For example, if the LPTT is programmed to 10h, the selected value corresponds to the time period of 16 AGP (66 MHz) clocks.

Bit	Descriptions
7:3	**Low Priority Transaction Timer Count Value (LPTTC)—R/W.** The number of clocks programmed in these bits represents the time slice (measured in eight 66 MHz clock granularity) allotted to the current low priority AGP transaction data transfer state.
2:0	Reserved.

3.5.30 TOUD—Top of Used DRAM Register (Device 0)

Address Offset: C4–C5h
Default Value: 0400h
Access: RO, R/W
Size: 16 bits

Bit	Descriptions
15:3	**Top of Usable DRAM (TOUD)—R/W.** This register contains bits 31:19 of the maximum system memory address that is usable by the operating system. Address bits 31:19 imply a memory granularity of 512 KB. Configuration software should set this value to either the maximum amount of usable memory (minus TSEG, graphics stolen memory, and CSA stolen memory) in the system or to the minimum address allocated for PCI memory or the graphics aperture (minus TSEG, graphics stolen memory), whichever is smaller. Address bits 18:0 are assumed to be 0000h for the purposes of address comparison. This register must be set to at least 0400h for a minimum of 64 MB of system memory. To calculate the value of TOUD, configuration software should set this value to the **smaller** of the following 2 cases: • **The maximum amount of usable memory in the system minus optional TSEG, optional graphics stolen memory.** • **The address allocated for PCI memory or the graphics aperture minus optional TSEG, optional graphics stolen memory.** **Programming Example**: • **DRB7 is set to 4 GB.** • **TSEG is enabled and TSEG size is set to 1 MB.** • **Internal Graphics is enabled and Graphics Mode Select is set to 32 MB.** • **BIOS knows the OS requires 1 GB of PCI space.** • **BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20-MB range at the very top of addressable memory space is lost to APIC.** According to the above equation, TOUD is originally calculated to: • **4 GB (DRB7) – 1 MB (TSEG) – 32 MB (graphics) = FDF0_0000h** The system memory requirements are: • **4 GB (max addressable space) – 1 GB (PCI space) – 33 MB (TSEG, graphics) – 20 MB (lost memory) = BCB0_0000h** Since BCB0_0000h (PCI and other system memory requirements) is less than FDF0_0000h, TOUD should be programmed to BCB0_0000h. **NOTE:** Even if the OS does not need any PCI space, TOUD should never be programmed above FEC0_0000h. If TOUD is programmed above this, address ranges that are reserved will become accessible to applications.
2:0	Reserved.

3.5.31 GMCHCFG—GMCH Configuration Register (Device 0)

Address Offset: C6–C7h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

Bit	Descriptions
15:13	**Number of Stop Grant Cycles (NSG)—R/W.** This field contains the number of Stop Grant transactions expected on the FSB bus before a Stop Grant Acknowledge packet is sent to the ICH5. This field is programmed by the BIOS after it has enumerated the processors and before it has enabled Stop Clock generation in the ICH5. Once this field has been set, it should not be modified. Note that each enabled thread within each processor will generate Stop Grant Acknowledge transactions. 000 = HI Stop Grant sent after 1 FSB Stop Grant 001 = HI Stop Grant sent after 2 FSB Stop Grants 010–111= Reserved
12	Reserved
11:10	**System Memory Frequency Select (SMFREQ)—R/W.** Default = 00. The DDR memory frequency is determined by the following table and partly determined by the FSB frequency. FSBFREQ[1:0] =00 SMFREQ[11:10]=01 System Memory DDR set to 266 MHz FSBFREQ[1:0] =01 SMFREQ[11:10]=00 System Memory DDR set to 266 MHz FSBFREQ[1:0] =01 SMFREQ[11:10]=01 System Memory DDR set to 333 MHz FSBFREQ[1:0] =10 SMFREQ[11:10]=01 System Memory DDR set to 333 (320) MHz FSBFREQ[1:0] =10 SMFREQ[11:10]=10 System Memory DDR set to 400 MHz All others are Reserved Note that Memory I/O Clock always runs at 2x the frequency of the memory clock. When writing a new value to this register, software must perform a clock synchronization sequence to apply the new timings. The new value does not get applied until this is completed.
9:6	Reserved
5	**MDA Present (MDAP)—R/W.** This bit works with the VGA Enable bits in the BCTRL1 register of Device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if Device 1's VGA Enable bit is not set. If Device 1's VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are forwarded to HI. If the VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are treated just like any other I/O accesses. That is, the cycles are forwarded to AGP if the address is within the corresponding IOBASE and IOLIMIT and ISA enable bit is not set; otherwise, they are forwarded to HI. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the hub interface, even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGA MDA Behavior** 0 0 All references to MDA and VGA go to HI. 0 1 Illegal combination (DO NOT USE). 1 0 All references to VGA go to Device 1. MDA-only references (I/O address 3BFh and aliases) will go to HI. 1 1 VGA references go to AGP/PCI; MDA references go to HI.
4	Reserved

Bit	Descriptions
3	**AGP Mode (AGP/DVO#)—RO.** This bit reflects the GPAR/ADD_DETECT# strap value. This strap bit determines the function of the AGP I/O pins. Note that the strap value is sampled on the assertion of PWROK. 0 = 2xDVO 1 = AGP When the strap is sampled low, this bit will be a 0 and DVO mode will be selected. When the strap is sampled high, this bit will be a 1 and AGP mode will be selected. In addition, this bit is forced to 1 if the AGP 3.0 detect bit (AGPSTAT.3) is 1. This is shown in the following table: **AGP 30_MOD bit** / **ADD_DETECT Strap** / **Resulting AGP/DVO#** 0 / 0 / 0 0 / 1 / 1 1 / x / 1 **NOTE:** When this bit is set to 0 (DVO Mode), AGP is disabled (configuration cycles fall-through to HI) and the Next Pointer field in CAPREG in Device 0 will be hardwired to all 0s.
2	**FSB IOQ Depth (IOQD)—RO.** This bit reflects the HA7# strap value. It indicates the depth of the FSB IOQ. When the strap is sampled low, this bit will be a 0 and the FSB IOQ depth is set to 1. When the strap is sampled high, this bit will be a 1 and the FSB IOQ depth is set to the maximum (12 on the bus, 12 on the GMCH). 0 = 1 deep 1 = 12 on the bus, 12 on the GMCH
1:0	**FSB Frequency Select (FSBFREQ)—RO.** The default value of this bit is set by the strap assigned to the BSEL[1:0] pins and is latched at the rising edge of PWROK. 00 = Core Frequency is 100 MHz and the FSB frequency is 400 MHz 01 = Core Frequency is 133 MHz and the FSB frequency is 533 MHz 10 = Core Frequency is 200 MHz and the FSB frequency is 800 MHz 11 = Reserved

3.5.32 ERRSTS—Error Status Register (Device 0)

Address Offset: C8–C9h
Default Value: 0000h
Access: R/WC
Size: 16 bits

This register is used to report various error conditions via the SERR HI messaging mechanism. A SERR HI message is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated.

Note: Software must write a 1 to clear bits that are set.

Bit	Descriptions
15:10	Reserved
9	**Non-DRAM Lock Error (NDLOCK)—R/WC.** 0 = No Lock operation detected. 1 = GMCH has detected a lock operation to memory space that did not map into SDRAM.
8	**Software Generated SMI Flag—R/WC.** 0 = Source of an SMI was **not** the Device 2 Software SMI Trigger. 1 = Source of an SMI was the Device 2 Software SMI Trigger.
7:6	Reserved
5	**GMCH Detects Unimplemented HI Special Cycle (HIAUSC)—R/WC.** 0 = No unimplemented Special Cycle on HI detected. 1 = GMCH detects an Unimplemented Special Cycle on HI.
4	**AGP Access Outside of Graphics Aperture Flag (OOGF)—R/WC.** 0 = No AGP access outside of the graphics aperture range. 1 = AGP access occurred to an address that is outside of the graphics aperture range.
3	**Invalid AGP Access Flag (IAAF)—R/WC.** 0 = No invalid AGP Access Flag. 1 = AGP access was attempted outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of memory.
2	**Invalid Graphics Aperture Translation Table Entry (ITTEF)—R/WC.** 0 = No Invalid Graphics Aperture Translation Table Entry. 1 = Invalid translation table entry was returned in response to an AGP access to the graphics aperture.
1	**GMCH Detects Unsupported AGP Command—R/WC.** 0 = No unsupported AGP Command received. 1 = Bogus or unsupported command is received by the AGP target in the GMCH.
0	Reserved

3.5.33 ERRCMD—Error Command Register (Device 0)

Address Offset: CA–CBh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the GMCH responses to various system errors. Since the GMCH does not have a SERR# signal, SERR messages are passed from the GMCH to the ICH5 over HI. When a bit in this register is set, a SERR message will be generated on HI when the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Descriptions
15:10	Reserved
9	**SERR on Non-DRAM Lock (LCKERR)—R/W.** 0 = Disable 1 = Enable. The GMCH generates a HI SERR special cycle when a processor lock cycle is detected that does not hit system memory.
8:7	Reserved
6	**SERR on Target Abort on HI Exception (TAHLA)—R/W.** 0 = Reporting of this condition is disabled. 1 = GMCH generates a SERR special cycle over HI when an GMCH originated HI cycle is completed with a target abort completion packet or special cycle.
5	**SERR on Detecting HI Unimplemented Special Cycle (HIAUSCERR)—R/W.** 0 = GMCH does not generate a SERR message for this event. SERR messaging for Device 0 is globally enabled in the PCICMD register. 1 = GMCH generates a SERR message over HI when an Unimplemented Special Cycle is received on the HI.
4	**SERR on AGP Access Outside of Graphics Aperture (OOGF)—R/W.** 0 = Reporting of this condition is disabled. 1 = Enable. GMCH generates a SERR special cycle over HI when an AGP access occurs to an address outside of the graphics aperture.
3	**SERR on Invalid AGP Access (IAAF)—R/W.** 0 = Invalid AGP Access condition is not reported. 1 = GMCH generates a SERR special cycle over HI when an AGP access occurs to an address outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of memory.
2	**SERR on Invalid Translation Table Entry (ITTEF)—R/W.** 0 = Reporting of this condition is disabled. 1 = GMCH generates a SERR special cycle over HI when an invalid translation table entry was returned in response to an AGP access to the graphics aperture.
1	**SERR on GMCH Detects Unsupported AGP Command—R/W.** 0 = GMCH Detects Unsupported AGP command will **not** generate a SERR. 1 = GMCH generates a SERR when an unsupported AGP command is detected.
0	Reserved

3.5.34 SKPD—Scratchpad Data Register (Device 0)

Address Offset: DE–DFh
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Descriptions
15:0	**Scratchpad (SCRTCH)—R/W.** These bits are R/W storage bits that have no effect on the GMCH functionality.

3.5.35 CAPREG—Capability Identification Register (Device 0)

Address Offset: E4h–E9h
Default: 00000106A009h
Access: RO
Size 48 bits

The Capability Identification register uniquely identifies chipset capabilities as defined in the table below.

Bit	Descriptions
47:28	Reserved.
27:24	**CAPREG Version—RO.** This field has the value 0001b to identify the first revision of the CAPREG definition.
23:16	**Cap_length—RO.** This field has the value 06h indicating the structure length.
15:8	**Next_Pointer—RO.** This field has the value A0h pointing to the next capabilities register, AGP Capability Identifier register (ACAPID). If AGP is disabled, this field has the value 00h signifying the end of the capabilities linked list.
7:0	**CAP_ID—RO.** This field has the value 09h to identify the CAP_ID assigned by the PCI SIG for Vendor Dependent CAP_PTR.

3.6 PCI-to-AGP Bridge Configuration Register (Device 1)

This section contains the PCI-to-AGP bridge PCI configuration registers listed in order of ascending offset address. The register address map is shown in Table 8.

Table 8. PCI-to-AGP Bridge PCI Configuration Register Address Map (Device 1)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2571h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, R/W
06–07h	PCISTS1	PCI Status	00A0h	RO, R/WC
08h	RID1	Revision Identification	See register description	RO
09h	—	Reserved	—	—
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT1	Master Latency Timer	00h	RO, R/W
0Eh	HDR1	Header Type	01h	RO
0F–17h	—	Reserved	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	R/W
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	SMLT1	Secondary Bus Master Latency Timer	00h	RO, R/W
1Ch	IOBASE1	I/O Base Address	F0h	RO, R/W
1Dh	IOLIMIT1	I/O Limit Address	00h	RO, R/W
1E–1Fh	SSTS1	Secondary Status	02A0h	RO, R/WC
20–21h	MBASE1	Memory Base Address	FFF0h	RO, R/W
22–23h	MLIMIT1	Memory Limit Address	0000h	RO, R/W
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28–3Dh	—	Reserved	—	—
3Eh	BCTRL1	Bridge Control	00h	RO, R/W
3Fh	—	Reserved	—	—
40h	ERRCMD1	Error Command	00h	RO, R/W
41–FFh	—	Reserved	—	—

3.6.1 VID1—Vendor Identification Register (Device 1)

Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification register, uniquely identify any PCI device.

Bit	Descriptions
15:0	**Vendor Identification Device 1 (VID1)—RO.** This register field contains the PCI standard identification for Intel, 8086h.

3.6.2 DID1—Device Identification Register (Device 1)

Address Offset: 02–03h
Default Value: 2571h
Access: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Device Identification Number (DID)—RO.** A 16-bit value assigned to the GMCH device 1.

3.6.3 PCICMD1—PCI Command Register (Device 1)

Address Offset: 04–05h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back Enable (FB2B)—RO.** Hardwired to 0.
8	**SERR Message Enable (SERRE)—R/W.** This bit is a global enable bit for Device 1 SERR messaging. The GMCH communicates the SERR# condition by sending a SERR message to the ICH5. 0 = Disable. SERR message is not generated by the GMCH for Device 1. 1 = Enable. GMCH is enabled to generate SERR messages over HI for specific Device 1 error conditions that are individually enabled in the BCTRL1 register. The error status is reported in the PCISTS1 register.
7	**Address/Data Stepping (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5	Reserved.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.
2	**Bus Master Enable (BME)—R/W.** 0 = Disable. AGP Master initiated Frame# cycles will be ignored by the GMCH. The result is a master abort. Ignoring incoming cycles on the secondary side of the PCI-to-PCI bridge effectively disabled the bus master on the primary side. (default) 1 = Enable. AGP master initiated Frame# cycles will be accepted by the GMCH if they hit a valid address decode range. This bit has no affect on AGP Master originated SBA or PIPE# cycles.
1	**Memory Access Enable (MAE)—R/W.** 0 = Disable. All of Device 1's memory space is disabled. 1 = Enable. Enables the memory and pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	**IO Access Enable (IOAE)—R/W.** 0 = Disable. All of Device 1's I/O space is disabled. 1 = Enable. This bit must be set to1 to enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

3.6.4 PCISTS1—PCI Status Register (Device 1)

Address Offset: 06–07h
Default Value: 00A0h
Access: RO, R/WC
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the virtual PCI-to-PCI bridge in the GMCH.

Bit	Descriptions
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0. Parity is not supported on the primary side of this device.
14	**Signaled System Error (SSE)—R/WC.** 0 = Software clears this bit by writing a 1 to it. 1 = GMCH Device 1 generated a SERR message over HI for any enabled Device 1 error condition. Device 1 error conditions are enabled in the ERRCMD, PCICMD1 and BCTRL1 registers. Device 1 error flags are read/reset from the ERRSTS and SSTS1 register.
13	**Received Master Abort Status (RMAS)—RO.** Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	**Received Target Abort Status (RTAS)—RO.** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	**DEVSEL# Timing (DEVT)—RO.** The GMCH does not support subtractive decoding devices on bus 0. Therefore, this field is hardwired to 00 indicating that Device 1 uses the fastest possible decode.
8	**Data Parity Detected (DPD)—RO.** Hardwired to 0. Parity is not supported on the primary side of this device.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. The AGP/PCI_B interface always supports fast back-to-back writes.
6	Reserved.
5	**66/60 MHz capability (CAP66)—RO.** Hardwired to 1. The AGP/PCI bus is 66 MHz capable.
4:0	Reserved.

3.6.5 RID1—Revision Identification Register (Device 1)

Address Offset: 08h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH Device 1.

Bit	Descriptions
7:0	**Revision Identification Number (RID)—RO.** This is an 8-bit value that indicates the revision identification number for the GMCH Device 1. It is always the same as the value in RID. 02h = A-2 Stepping

3.6.6 SUBC1—Sub-Class Code Register (Device 1)

Address Offset: 0Ah
Default Value: 04h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the GMCH Device 1.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of bridge for the Device 1 of the GMCH. 04h = PCI-to-PCI bridge.

3.6.7 BCC1—Base Class Code Register (Device 1)

Address Offset: 0Bh
Default Value: 06h
Access: RO
Size: 8 bits

This register contains the Base Class Code of the GMCH Device 1.

Bit	Descriptions
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the Base Class Code for the GMCH Device 1. 06h = Bridge device.

3.6.8 MLT1—Master Latency Timer Register (Device 1)

Address Offset: 0Dh
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as read/write to prevent standard PCI-to-PCI bridge configuration software from getting "confused."

Bit	Descriptions
7:3	**Scratchpad MLT (NA7.3)—R/W.** These bits return the value with which they are written; however, they have no internal function and are implemented as a scratchpad to avoid confusing software.
2:0	Reserved.

3.6.9 HDR1—Header Type Register (Device 1)

Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**Header Type Register (HDR)—RO.** This read only field always returns 01 to indicate that GMCH Device 1 is a single function device with bridge header layout.

3.6.10 PBUSN1—Primary Bus Number Register (Device 1)

Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that virtual PCI-to-PCI bridge is connected to bus 0.

Bit	Descriptions
7:0	**Primary Bus Number (PBUSN)—RO.** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

3.6.11 SBUSN1—Secondary Bus Number Register (Device 1)

Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI bridge (i.e., to PCI_B/AGP). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI_B/AGP.

Bit	Descriptions
7:0	**Secondary Bus Number (SBUSN)—RO.** This field is programmed by configuration software with the bus number assigned to PCI_B.

3.6.12 SUBUSN1—Subordinate Bus Number Register (Device 1)

Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI_B/AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI_B/AGP.

Bit	Descriptions
7:0	**Subordinate Bus Number (BUSN)—R/W.** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 1 bridge. When only a single PCI device resides on the AGP/PCI_B segment, this register will contain the same value as the SBUSN1 register.

3.6.13 SMLT1—Secondary Bus Master Latency Timer Register (Device 1)

Address Offset: 1Bh
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register control the bus tenure of the GMCH on AGP/PCI the same way Device 0 MLT controls the access to the PCI_A bus.

Bit	Descriptions
7:3	**Secondary MLT Counter Value (MLT)—R/W.** Programmable, default = 0 (SMLT disabled)
2:0	Reserved.

3.6.14 IOBASE1—I/O Base Address Register (Device 1)

Address Offset: 1Ch
Default Value: F0h
Access: RO, R/W
Size: 8 bits

This register controls the processor-to-PCI_B/AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Descriptions
7:4	**I/O Address Base (IOBASE)—R/W.** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to AGP/PCI_B.
3:0	Reserved.

3.6.15 IOLIMIT1—I/O Limit Address Register (Device 1)

Address Offset: 1Dh
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the processor-to-PCI_B/AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Descriptions
7:4	**I/O Address Limit (IOLIMIT)—R/W.** This field corresponds to A[15:12] of the I/O address limit of Device 1. Devices between this upper limit and IOBASE1 will be passed to AGP/PCI_B.
3:0	Reserved.

3.6.16 SSTS1—Secondary Status Register (Device 1)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: RO, R/WC
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI_B/AGP side) of the virtual PCI-to-PCI bridge in the GMCH.

Bit	Descriptions
15	**Detected Parity Error (DPE)—R/WC.** 0 = No parity error detected. 1 = GMCH detected a parity error in the address or data phase of PCI_B/AGP bus transactions. **NOTE:** Software clears this bit by writing a 1 to it.
14	**Received System Error (RSE)—RO.** Hardwired to 0. GMCH does not have a SERR# signal pin on the AGP interface.
13	**Received Master Abort Status (RMAS)—R/WC.** 0 = No master abort termination. 1 = GMCH terminated a Host-to-PCI_B/AGP with an unexpected master abort. **NOTE:** Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS)—R/WC.** 0 = No target abort termination. 1 = GMCH-initiated transaction on PCI_B/AGP is terminated with a target abort. **NOTE:** Software clears this bit by writing a 1 to it.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. GMCH does not generate target abort on PCI_B/AGP.
10:9	**DEVSEL# Timing (DEVT)—RO.** This 2-bit field indicates the timing of the DEVSEL# signal when the GMCH responds as a target on PCI_B/AGP. This field is hardwired to 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Master Data Parity Error Detected (DPD)—RO.** Hardwired to 0. GMCH does not implement G_PERR# signal on PCI_B.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. GMCH as a target supports fast back-to-back transactions on PCI_B/AGP.
6	Reserved.
5	**66/60 MHz capability (CAP66)—RO.** Hardwired to 1 to indicate that the AGP/PCI_B bus is capable of 66 MHz operation.
4:0	Reserved.

3.6.17 MBASE1—Memory Base Address Register (Device 1)

Address Offset: 20–21h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-PCI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Descriptions
15:4	**Memory Address Base (MBASE)— R/W.** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed by the Device 1 bridge to AGP/PCI_B.
3:0	Reserved.

3.6.18 MLIMIT1—Memory Limit Address Register (Device 1)

Address Offset: 22–23h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-PCI_B non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI_B/AGP address ranges (typically, where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically, graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved Processor-AGP memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the GMCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Descriptions
15:4	**Memory Address Limit (MLIMIT)—R/W.** This field corresponds to A[31:20] of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the Device 1 bridge to AGP/PCI_B.
3:0	Reserved.

3.6.19 PMBASE1—Prefetchable Memory Base Address Register (Device 1)

Address Offset: 24–25h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-PCI_B prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeros when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Descriptions
15:4	**Prefetchable Memory Address Base (PMBASE)—R/W.** This field corresponds to A[31:20] of the lower limit of the address range passed by bridge Device 1 across AGP/PCI_B.
3:0	Reserved.

3.6.20 PMLIMIT1—Prefetchable Memory Limit Address Register (Device 1)

Address Offset: 26–27h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-PCI_B prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Descriptions
15:4	**Prefetchable Memory Address Limit (PMLIMIT)—R/W.** This field corresponds to A[31:20] of the upper limit of the address range passed by bridge Device 1 across AGP/PCI_B.
3:0	Reserved.

3.6.21 BCTRL1—Bridge Control Register (Device 1)

Address Offset: 3Eh
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL1 provides additional control for the secondary interface (i.e., PCI_B/AGP) as well as some bits that affect the overall behavior of the virtual PCI-to-PCI bridge in the GMCH (e.g., VGA compatible address ranges mapping).

Bit	Descriptions
7	**Fast Back-to-Back Enable (FB2BEN)—RO.** Hardwired to 0. GMCH does not generate fast back-to-back cycles as a master on AGP.
6	**Secondary Bus Reset (SRESET)—RO.** Hardwired to 0. GMCH does not support generation of reset via this bit on the AGP.
5	**Master Abort Mode (MAMODE)—RO.** Hardwired to 0. Thus, when acting as a master on AGP/PCI_B, the GMCH will discard writes and return all 1s during reads when a master abort occurs.
4	Reserved.
3	**VGA Enable (VGAEN)—R/W.** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. This bit works in conjunction with the GMCHCFG[MDAP] bit (offset C6h) as described in Table 9. 0 = Disable 1 = Enable
2	**ISA Enable (ISAEN)—R/W.** This bit modifies the response by the GMCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions are mapped to PCI_B/AGP. (default) 1 = The GMCH does not forward to PCI_B/AGP any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI_B/AGP these cycles are forwarded to HI where they can be subtractively or positively claimed by the ISA bridge.
1	**SERR Enable (SERREN)—RO.** Hardwired to 0. This bit normally controls forwarding SERR# on the secondary interface to the primary interface. The GMCH does not support the SERR# signal on the AGP/PCI_B bus.
0	**Parity Error Response Enable (PEREN)—R/W.** This bit controls the GMCH's response to data phase parity errors on PCI_B/AGP. G_PERR# is not implemented by the GMCH. 0 = Disable. Address and data parity errors on PCI_B/AGP are not reported via the GMCH HI SERR messaging mechanism. Other types of error conditions can still be signaled via SERR messaging independent of this bit's state. 1 = Enable. Address and data parity errors detected on PCI_B are reported via the HI SERR messaging mechanism, if further enabled by SERRE1.

The bit field definitions for VGAEN and MDAP are detailed in Table 9.

Table 9. VGAEN and MDAP Field Definitions

VGAEN	MDAP	Description
0	0	All References to MDA and VGA space are routed to HI.
0	1	Illegal combination.
1	0	All VGA references are routed to this bus. MDA references are routed to HI.
1	1	All VGA references are routed to this bus. MDA references are routed to HI.

3.6.22 ERRCMD1—Error Command Register (Device 1)

Address Offset: 40h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

Bit	Descriptions
7:1	Reserved.
0	**SERR on Receiving Target Abort (SERTA)—R/W.** 0 = The GMCH does not assert a SERR message upon receipt of a target abort on PCI_B. SERR messaging for Device 1 is globally enabled in the PCICMD1 register. 1 = The GMCH generates a SERR message over HI upon receiving a target abort on PCI_B.

3.7 Integrated Graphics Device Registers (Device 2)

Function 0 can be VGA compatible or not; this is selected through GC[bit 1] (offset 52, Device 0). This section contains the Integrated Graphics Device PCI configuration registers listed in order of ascending offset address. The register address map is shown in Table 10.

Table 10. Integrated Graphics Device PCI Register Address Map (Device 2)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2572h	RO
04–05h	PCICMD2	PCI Command	0000h	RO,R/W
06–07h	PCISTS2	PCI Status	0090h	RO,R/WC
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	00h	RO
0Fh	—	Intel Reserved	—	—
10–13h	GMADR	Graphics Memory Range Address	00000008h	R/W,RO
14–17h	MMADR	Memory-Mapped Range Address	00000000h	R/W,RO
18–1Bh	IOBAR	IO Decode	00000000h	R/W
1C–2Bh	—	Reserved	—	—
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35–3Bh	—	Reserved	—	—
3Ch	INTRLINE	Interrupt Line	00h	R/W, RO
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–CFh	—	Intel Reserved	00h	—
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0021h	RO
D4–D5h	PMCS	Power Management Control	0000h	R/W,RO
D6–DFh	—	Intel Reserved	—	—
E0–E1h	SWSMI	Software SMI Interface	0000h	R/W
E2–FFh	—	Intel Reserved	—	—

3.7.1 VID2—Vendor Identification Register (Device 2)

Address Offset: 00h–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification register, uniquely identify any PCI device.

Bit	Description
15:0	**Vendor Identification Number—RO.** This is a 16-bit value assigned to Intel.

3.7.2 DID2—Device Identification Register (Device 2)

Address Offset: 02h–03h
Default Value: 2572h
Access: RO
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Description
15:0	**Device Identification Number—RO.** This is a 16-bit value assigned to the GMCH IGD.

3.7.3 PCICMD2—PCI Command Register (Device 2)

Address Offset: 04h–05h
Default: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Description
15:10	Reserved.
9	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 0.
8	**SERR# Enable (SERRE) —RO.** Hardwired to 0.
7	**Address/Data Stepping—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	**Video Palette Snooping (VPS)—RO.** Hardwired to 0 to disable snooping.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0. The IGD ignores Special cycles.
2	**Bus Master Enable (BME)—R/W.** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	**Memory Access Enable (MAE)—R/W.** This bit controls the IGD's response to memory space accesses. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE)—R/W.** This bit controls the IGD's response to I/O space accesses. 0 = Disable (default). 1 = Enable.

3.7.4 PCISTS2—PCI Status Register (Device 2)

Address Offset: 06h–07h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Description
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0. The IGD does not detect parity.
14	**Signaled System Error (SSE)—RO**. Hardwired to 0. The IGD never asserts SERR#.
13	**Received Master Abort Status (RMAS)—RO**. Hardwired to 0. The IGD never gets a Master Abort.
12	**Received Target Abort Status (RTAS)—RO**. Hardwired to 0. The IGD never gets a Target Abort.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The IGD does not use target abort semantics.
10:9	**DEVSEL# Timing (DEVT) —RO.** Hardwired to 00; Not applicable.
8	**Data Parity Detected (DPD) —RO**. Hardwired to 0. Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection).
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	**User Defined Format (UDF)—RO.** Hardwired to 0.
5	**66 MHz PCI Capable (66C).—RO.** Hardwired to 0; Not applicable.
4	**CAP LIST—RO.** Hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration space containing a pointer to the location of the first item in the list.
3:0	Reserved.

3.7.5 RID2—Revision Identification Register (Device 2)

Address Offset: 08h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the IGD.

Bit	Description
7:0	**Revision Identification Number—RO.** This is an 8-bit value that indicates the revision identification number for the IGD. 02h = A-2 Stepping

3.7.6 CC—Class Code Register (Device 2)

Address Offset: 09h–0Bh
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
23:16	**Base Class Code (BASEC)—RO.** 03 = Display controller
15:8	**Sub-Class Code (SCC)—RO.** 00h = VGA compatible 80h = Non-VGA based on device 0 GCBIT 1 as well as Device 0 GC Register Bits 6:4
7:0	**Programming Interface (PI)—RO.** 00h = Display controller.

3.7.7 CLS—Cache Line Size Register (Device 2)

Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Description
7:0	**Cache Line Size (CLS)—RO.** Hardwired to 00h. The IGD, as a PCI compliant master, does not use the memory write and Invalidate command and, in general, does not perform operations based on cache line size.

3.7.8 MLT2—Master Latency Timer Register (Device 2)

Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Description
7:0	**Master Latency Timer Count Value—RO.** Hardwired to 00h.

3.7.9 HDR2—Header Type Register (Device 2)

Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Description
7:0	**Header Code (H)—RO.** This is an 8-bit value that indicates the Header Code for the IGD. 00h = Single function device with a type 0 configuration space format.

3.7.10 GMADR—Graphics Memory Range Address Register (Device 2)

Address Offset: 10–13h
Default Value: 00000008h
Access: R/W, RO
Size: 32 bits

This register requests allocation for the IGD graphics memory. The allocation is for 128 MB and the base address is defined by bits [31:27].

Bit	Description
31:27	**Memory Base Address—R/W.** Set by the OS, these bits correspond to address signals [31:26].
26	**128MB Address Mask—RO.** Hardwired to 0 to indicate 128-MB address space.
25:4	**Address Mask—RO.** Hardwired to 0s to indicate (at least) a 32-MB address range.
3	**Prefetchable Memory—RO.** Hardwired to 1 to enable prefetching.
2:1	**Memory Type—RO.** Hardwired to 00 to indicate 32-bit address.
0	**Memory/IO Space—RO.** Hardwired to 0 to indicate memory space.

3.7.11 MMADR—Memory-Mapped Range Address Register (Device 2)

Address Offset: 14–17h
Default Value: 00000000h
Access: R/W, RO
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Description
31:19	**Memory Base Address—R/W.** Set by the OS, these bits correspond to address signals [31:19].
18:4	**Address Mask—RO.** Hardwired to 0s to indicate 512-KB address range.
3	**Prefetchable Memory—RO.** Hardwired to 0 to prevent prefetching.
2:1	**Memory Type—RO.** Hardwired to 00 to indicate 32-bit address.
0	**Memory / IO Space—RO.** Hardwired to 0 to indicate memory space.

3.7.12 IOBAR—I/O Decode Register (Device 2)

Address Offset: 18–1Bh
Default Value: 00000001h
Access: R/W, RO
Size: 32 bits

This register provides the base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O base to be located anywhere in 16-bit I/O address space. Bits 2:1 are fixed and return 0s; bit 0 is hardwired to 1 indicating that 8 bytes of I/O space are decoded.

Access to the 8 bytes of I/O space is allowed in power management (PM) state D0 when the I/O Enable bit (PCICMD2 bit 0) is set. Access is disallowed in PM states D1–D3 if:

- the I/O Enable bit is 0
- Device 2 is turned off
- Internal graphics is disabled thru the fuse mechanisms.

Note that access to the IOBAR register is independent of VGA functionality in Device 2. Also, note that this mechanism is available only through function 0 of Device 2.

If accesses to the IOBAR is allowed, the GMCH claims all 8-, 16- or 32-bit I/O cycles from the processor that falls within the 8 bytes claimed.

Bit	Description
31:16	Reserved. Read as 0.
15:3	**I/O Base Address—R/W.** This field is set by the OS. These bits correspond to address signals 15:3. They provide the 16-bit I/O base address for the I/O registers.
2:1	**Memory Type—RO.** Hardwired to 00 to indicate 32-bit address.
0	**I/O Space—RO.** Hardwired to 1 to indicate I/O space.

3.7.13 SVID2—Subsystem Vendor Identification Register (Device 2)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bit

Bit	Description
15:0	**Subsystem Vendor ID—R/WO.** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a Reset.

3.7.14 SID2—Subsystem Identification Register (Device 2)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Description
15:0	**Subsystem Identification—R/WO.** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a Reset.

3.7.15 ROMADR—Video BIOS ROM Base Address Registers (Device 2)

Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore, this register is hardwired to zeros.

Bit	Description
31:18	**ROM Base Address—RO.** Hardwired to 0s.
17:11	**Address Mask—RO.** Hardwired to 0s to indicate 256-KB address range.
10:1	Reserved. Hardwired to 0s.
0	**ROM BIOS Enable—RO.** 0 = ROM not accessible.

3.7.16 CAPPOINT—Capabilities Pointer Register (Device 2)

Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer Value—RO.** This field contains an offset into the function's PCI configuration space for the first item in the New Capabilities Linked List, the ACPI registers at address D0h.

3.7.17 INTRLINE—Interrupt Line Register (Device 2)

Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Connection—R/W.** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to. This register is needed for Plug-N-Play software. Settings of this register field has **no** effect on GMCH operation as there is **no** hardware functionality associated with this register, other than the hardware implementation of the R/W register itself.

3.7.18 INTRPIN—Interrupt Pin Register (Device 2)

Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin—RO.** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h = INTA#.

3.7.19 MINGNT—Minimum Grant Register (Device 2)

Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Description
7:0	**Minimum Grant Value—RO.** Hardwired to 00h. The IGD does not burst as a PCI compliant master.

3.7.20 MAXLAT—Maximum Latency Register (Device 2)

Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Description
7:0	**Maximum Latency Value—RO.** Hardwired to 00h. The IGD has no specific requirements for how often it needs to access the PCI bus.

3.7.21 PMCAPID—Power Management Capabilities Identification Register (Device 2)

Address Offset: D0h–D1h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Description
15:8	**NEXT_PTR—RO.** This field contains a pointer to next item in the capabilities list. This is the final capability in the list and must be set to 00h.
7:0	**CAP_ID—RO.** SIG defines this ID as 01h for power management.

3.7.22 PMCAP—Power Management Capabilities Register (Device 2)

Address Offset: D2h–D3h
Default Value: 0021h
Access: RO
Size: 16 bits

Bit	Description
15:11	**PME Support—RO.** Hardwired to 0s. This field indicates the power states in which the IGD may assert PME#. It is hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	**D2—RO.** Hardwired to 0. The D2 power management state is not supported.
9	**D1—RO.** Hardwired to 0. The D1 power management state is not supported.
8:6	Reserved.
5	**Device Specific Initialization (DSI)—RO.** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	**Auxiliary Power Source—RO.** Hardwired to 0.
3	**PME Clock—RO.** Hardwired to 0. IGD does not support PME# generation.
2:0	**Version—RO.** Hardwired to 001b to indicate there are 4 bytes of power management registers implemented.

3.7.23 PMCS—Power Management Control/Status Register (Device 2)

Address Offset: D4h–D5h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

Bit	Description
15	**PME_Status—RO.** Hardwired to 0. IGD does not support PME# generation from D3 (cold).
14:13	**Data Scale (Reserved)—RO.** Hardwired to 00. The IGD does not support data register.
12:9	**Data_Select (Reserved)—RO.** Hardwired to 0h. The IGD does not support data register.
8	**PME_En—RO.** Hardwired to 0. PME# assertion from D3 (cold) is disabled.
7:2	Reserved.
1:0	**PowerState—R/W.** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 (Default) 01 = D1 (Not Supported– Writes will be blocked and will return the previous value.) 10 = D2 (Not Supported– Writes will be blocked and will return the previous value.) 11 = D3

3.7.24 SWSMI—Software SMI Interface Register (Device 2)

Address Offset: E0h–E1h
Default Value: 0000h
Size: 16 bits
Access: R/W

Bit	Description
15:1	**SMI Message Passing Field—R/W.** These bits are R/W bits that are used to pass messages between Graphics software and the System BIOS. These bits have no functional impact on the GMCH. (default = 0s)
0	**Software SMI Trigger—R/W.** When this bit transitions from 0 to 1, the GMCH will generate an SMI message over HI. The SMI handler (software) must clear this bit by writing a 0 to it. (default = 0).

3.8 PCI-to-CSA Bridge Registers (Device 3)

This device is the virtual PCI-to-CSA bridge. This section contains the PCI configuration registers listed in order of ascending offset address. Table 11 provides the register address map for this device.

Table 11. PCI-to-CSA Bridge Configuration Register Address Map (Device 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID3	Vendor Identification	8086h	RO
02–03h	DID3	Device Identification	2573h	RO
04–05h	PCICMD3	PCI Command	0000h	RO,R/W
06–07h	PCISTS3	PCI Status	00A0h	RO,R/WC
08h	RID3	Revision Identification	See register description	RO
09	—	Reserved	—	—
0Ah	SUBC3	Sub-Class Code	04h	RO
0Bh	BCC3	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT3	Master Latency Timer	00h	RO,R/W
0Eh	HDR3	Header Type	01h	RO
0F–17h	—	Reserved	—	—
18h	PBUSN3	Primary Bus Number	00h	R/W
19h	SBUSN3	Secondary Bus Number	00h	R/W
1Ah	SUBUSN3	Subordinate Bus Number	00h	R/W
1Bh	SMLT3	Secondary Bus Master Latency Timer	00h	RO,R/W
1Ch	IOBASE3	I/O Base Address	F0h	RO,R/W
1Dh	IOLIMIT3	I/O Limit Address	00h	RO,R/W
1E–1Fh	SSTS3	Secondary Status	02A0h	RO,R/WC
20–21h	MBASE3	Memory Base Address	FFF0h	RO,R/W
22–23h	MLIMIT3	Memory Limit Address	0000h	RO,R/W
24–25h	PMBASE3	Prefetchable Memory Base Limit Address	FFF0h	RO,R/W
26–27h	PMLIMIT3	Prefetchable Memory Limit Address	0000h	RO,R/W
28–3Dh	—	Reserved	—	—
3Eh	BCTRL3	Bridge Control	00h	RO,R/W
3Fh	—	Reserved	—	—
40h	ERRCMD3	Error Command	00h	RO,R/W
41–4Fh	—	Reserved	—	—
50–53h	CSACNTRL	CSA Control	0E04 2802h	RO,R/W
54–FFh	—	Intel Reserved	—	—

3.8.1 VID3—Vendor Identification Register (Device 3)

Address Offset: 00h–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification register, uniquely identify any PCI device.

Bit	Description
15:0	**Vendor Identification Number—RO.** This is a 16-bit value assigned to Intel.

3.8.2 DID3—Device Identification Register (Device 3)

Address Offset: 02h–03h
Default Value: 2573h
Access: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Description
15:0	**Device Identification Number—RO.** This is a 16-bit value assigned to the GMCH Device 3.

3.8.3 PCICMD3—PCI Command Register (Device 3)

Address Offset: 04h–05h
Default: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Description
15:10	Reserved.
9	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 0.
8	**SERR# Enable (SERRE)** —R/W. This bit is a global enable bit for Device 3 SERR messaging. The GMCH communicates the SERR# condition by sending a SERR message to the ICH5. 0 = Disable. The SERR message is not generated by the GMCH for Device 3. 1 = Enable. The GMCH is enabled to generate SERR messages over HI for specific Device 3 error conditions that are individually enabled in the BCTRL3 register. The error status is reported in the PCISTS3 register.
7	**Address/Data Stepping (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)** —**RO.** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5	Reserved.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.
2	**Bus Master Enable (BME)—R/W.** This bit is not functional. It is a R/W bit for compatibility with compliance testing software.
1	**Memory Access Enable (MAE)—R/W.** This bit must be set to 1 to enable the memory and pre-fetchable memory address ranges defined in the MBASE3, MLIMIT3, PMBASE3, and PMLIMIT3 registers. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE)—R/W.** This bit must be set to 1 to enable the I/O address range defined in the IOBASE3 and IOLIMIT3 registers 0 = Disable (default). 1 = Enable.

3.8.4 PCISTS3—PCI Status Register (Device 3)

Address Offset: 06h–07h
Default Value: 00A0h
Access: RO, R/WC
Size: 16 bits

PCISTS3 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the virtual PCI-to-CSA bridge in the GMCH.

Note: For R/WC bits, software must write a 1 to clear bits that are set.

Bit	Description
15	**Detected Parity Error (DPE)—RO**. Hardwired to 0. Parity is not supported on the primary side of this device.
14	**Signaled System Error (SSE)—R/WC**. 0 = No SERR message generated by GMCH Device 3 over HI. 1 = GMCH Device 3 generated a SERR message over HI for any enabled Device 3 error condition. Device 3 error conditions are enabled in the ERRCMD, PCICMD3, and BCTRL3 registers. Device 3 error flags are read/reset from the ERRSTS and SSTS3 register.
13	**Received Master Abort Status (RMAS)—RO**. Hardwired to 0. The concept of a master abort does not exist on the primary side of this device.
12	**Received Target Abort Status (RTAS)—RO**. Hardwired to 0. The concept of a target abort does not exist on the primary side of this device.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	**DEVSEL# Timing (DEVT)—RO.** The Hardwired to 00b. GMCH does not support subtractive decoding devices on bus 0. The value 00b indicates that Device 3 uses the fastest possible decode.
8	**Data Parity Detected (DPD)—RO**. Hardwired to 0. Parity Error Response is hardwired to disabled (and the GMCH does not support any parity detection on the primary side of this device).
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. The interface always supports fast back-to-back writes.
6	Reserved.
5	**66/60 MHz PCI Capable (CAP66)—RO.** Hardwired to 1. CSA is 66 MHz capable.
4:0	Reserved.

3.8.5 RID3—Revision Identification Register (Device 3)

Address Offset: 08h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH Device 3.

Bit	Description
7:0	**Revision Identification Number—RO.** This is an 8-bit value that indicates the revision identification number for the GMCH Device 3. It is always the same as the value in the RID register. 02h = A-2 Stepping

3.8.6 SUBC3—Class Code Register (Device 3)

Address Offset: 0Ah
Default Value: 04h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the GMCH Device 3.

Bit	Description
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of Bridge for the GMCH Device 3. 04h = PCI-to-PCI bridge.

3.8.7 BCC3—Base Class Code Register (Device 3)

Address Offset: 0Bh
Default Value: 06h
Access: RO
Size: 8 bits

This register contains the Base Class Code of the GMCH Device 3.

Bit	Description
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the Base Class Code for the GMCH Device 3. 06h = Bridge device.

3.8.8 MLT3—Master Latency Timer Register (Device 3)

Address Offset: 0Dh
Default Value: 00h
Access: RO, RW
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-to-PCI bridge configuration software from getting "confused."

Bit	Description
7:3	**Scratchpad MLT (NA7:3)—R/W.** These bits return the value that was last written; however, they have no internal function and are implemented as a Scratchpad to avoid confusing software.
2:0	Reserved.

3.8.9 HDR3—Header Type Register (Device 3)

Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Description
7:0	**Header Type Register (HDR)—RO.** 01h = GMCH Device 3 is a single function device with bridge header layout.

3.8.10 PBUSN3—Primary Bus Number Register (Device 3)

Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that virtual PCI-to-PCI bridge is connected to bus 0.

Bit	Description
7:0	**Primary Bus Number (BUSN)—RO.** Configuration software typcially programs this field with the number of the bus on the primary side of the bridge. Since Device 3 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 00h.

3.8.11 SBUSN3—Secondary Bus Number Register (Device 3)

Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI bridge (i.e., CSA). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to CSA.

Bit	Description
7:0	**Secondary Bus Number (BUSN)—R/W.** This field is programmed by configuration software with the bus number assigned to CSA.

3.8.12 SMLT3—Secondary Bus Master Latency Timer Register (Device 3)

Address Offset: 1Bh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Description
7:0	Reserved.

3.8.13 IOBASE3—I/O Base Address Register (Device 3)

Address Offset: 1Ch
Default Value: F0h
Access: RO, R/W
Size: 8 bits

This register controls the processor-to-CSA I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Description
7:4	**I/O Address Base (IOBASE)— R/W.** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to CSA.
3:0	Reserved.

3.8.14 IOLIMIT3—I/O Limit Address Register (Device 3)

Address Offset: 1Dh
Default Value: 00h
Access: RO, RW
Size: 8 bits

This register controls the processor-to-CSA I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Description
7:4	**I/O Address Limit (IOLIMIT)—R/W.** This field corresponds to A[15:12] of the I/O address limit of Device 3. Devices between this upper limit and IOBASE3 will be passed to CSA.
3:0	Reserved.

3.8.15 SSTS3—Secondary Status Register (Device 3)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: RO, RWC
Size: 16 bits

SSTS3 is a 16 bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., CSA side) of the virtual PCI-to-PCI bridge in the GMCH.

Note: For R/WC bits, software must write a 1 to clear bits that are set.

Bit	Description
15	**Detected Parity Error (DPE)— RO.** Hardwired to 0. Parity is not supported on the CSA interface.
14	**Received System Error (RSE)—R/WC.** 0 = No system error signalled by CSA device. 1 = CSA device signals a system error to the GMCH.
13	**Received Master Abort Status (RMAS) —R/WC.** 0 = No master abort by GMCH to terminate a Host-to-CSA transaction. 1 = GMCH terminated a Host-to-CSA transaction with an unexpected master abort.
12	**Received Target Abort Status (RTAS) —R/WC.** 0 = No target abort for GMCH-initiated transaction on CSA. 1 = GMCH-initiated transaction on CSA is terminated with a target abort.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0. The GMCH does not generate a target abort on CSA.
10:9	**DEVSEL# Timing (DEVT) —RO.** Hardwired to 01b. This 2-bit field indicates the timing of the DEVSEL# signal when the GMCH responds as a target on CSA. The 01b value (medium timing) indicates the time when a valid DEVSEL# can be sampled by initiator of the PCI cycle.
8	**Master Data Parity Detected (DPD)—RO.** Hardwired to 0. GMCH does not implement G_PERR# signal on CSA.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. GMCH, as a target, supports fast back-to-back transactions on CSA.
6	Reserved.
5	**66/60 MHz PCI Capable (CAP66)—RO.** Hardwired to 1. CSA is 66 MHz capable.
4:0	Reserved.

3.8.16 MBASE3—Memory Base Address Register (Device 3)

Address Offset: 20–21h
Default Value: FFF0h
Access: RO, RW
Size: 16 bits

This register controls the processor-to-CSA non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The Upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to 1-MB boundary.

Bit	Description
15:4	**Memory Address Limit (MLIMIT)— R/W.** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed by Device 3 bridge to CSA.
3:0	Reserved.

3.8.17 MLIMIT3—Memory Limit Address Register (Device 3)

Address Offset: 22–23h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the processor-to-CSA non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory ranges covered by the MBASE and MLIMIT registers are used to map non-prefetchable CSA address ranges (typically, where control/status memory-mapped I/O data structures of the graphics controller will reside) and the PMBASE and PMLIMIT registers are used to map prefetchable address ranges (typically, graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved Processor-CSA memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the GMCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Description
15:4	**Memory Address Limit (MLIMIT)—R/W.** This field corresponds to A[31:20] of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the Device 3 bridge to CSA.
3:0	Reserved.

3.8.18 PMBASE3—Prefetchable Memory Base Address Register (Device 3)

Address Offset: 24–25h
Default Value: FFF0h
Access: R/W, RO
Size: 16 bits

This register controls the processor-to-CSA prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom four bits of this register are read only and return 0s when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Prefetchable Memory Address Base (PMBASE)—R/W.** This field corresponds to A[31:20] of the lower limit of the address range passed by bridge Device 3 across CSA.
3:0	Reserved.

3.8.19 PMLIMIT3—Prefetchable Memory Limit Address Register (Device 3)

Address Offset: 26–27h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This register controls the processor to CSA prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read only and return 0s when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Description
15:4	**Prefetchable Memory Address Limit (PMLIMIT)—R/W.** This field corresponds to A[31:20] of the upper limit of the address range passed by bridge Device 3 across CSA.
3:0	Reserved.

3.8.20 BCTRL3—Bridge Control Register (Device 3)

Address Offset: 3Eh
Default Value: 00h
Access: R/W, RO
Size: 8 bits

Bit	Description
7	**Fast Back-to-Back Enable (FB2BEN)—RO.** Hardwired to 0. The GMCH does not generate fast back-to-back cycles as a master on AGP.
6	**Secondary Bus reset (SREST)—RO.** Hardwired to 0. The GMCH does not support generation of reset via this bit on the AGP.
5	**Master Abort Mode (MAMODE)—RO.** Hardwired to 0. This means that when acting as a master on CSA, the GMCH will discard writes and return all 1s during reads when a master abort occurs.
4	Reserved.
3	**VGA Enable (VGAEN)—R/W.** This bit control the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. This bit works in conjunction with the GMCHCFG[MDAP] bit (Device 0, offset C6h) as described in Table 12. 0 = Disable 1 = Enable
2	**ISA Enable (ISAEN)—R/W.** This bit modifies the response by the GMCH to an I/O access issued by the processor that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = Disable (default). All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions are mapped to CSA. 1 = Enable. The GMCH does not forward to CSA any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to CSA, these cycles are forwarded to HI where they can be subtractively or positively claimed by the ISA bridge.
1	**SERR Enable (SERREN)—RO.** Hardwired to 0. This bit normally controls forwarding SERR# on the secondary interface to the primary interface. However, the GMCH does not support the SERR# signal on the CSA Bus.
0	**Parity Error Response Enable (PEREN)—RO.** Hardwired to 0.

The bit field definitions for VGAEN and MDAP are detailed in Table 12.

Table 12. VGAEN and MDAP Definitions

VGAEN	MDAP	Description
0	0	All References to MDA and VGA space are routed to HI.
0	1	Illegal combination.
1	0	All VGA references are routed to this bus. MDA references are routed to HI.
1	1	All VGA references are routed to this bus. MDA references are routed to HI.

3.8.21 ERRCMD3—Error Command Register (Device 3)

Address Offset: 40h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**SERR on Receiving Target Abort (SERTA)—R/W.** 0 = The GMCH does not assert a SERR message upon receipt of a target abort on CSA. 1 = The GMCH generates a SERR message over CSA upon receiving a target abort on CSA. SERR messaging for Device 3 is globally enabled in the PCICMD3 register.

3.8.22 CSACNTRL—CSA Control Register (Device 3)

Address Offset: 50–53h
Default Value: 0E042802h
Access: R/W, RO
Size: 32 bits

Bit	Description
31:29	**First Subordinate CSA (CSA_SUB_FIRST)—R/W.** This field stores the lowest subordinate CI hub number.
28	Reserved.
27:25	**Last Subordinate CSA (CSA_SUB_LAST)—R/W.** This field stores the highest subordinate CSA hub number.
24:16	Reserved.
15:14	**CSA Width (CSA_WIDTH)—R/W.** This field describes the used width of the data bus. 00 = 8 bit 01 = Reserved 10 = Reserved 11 = Reserved
13:0	Intel Reserved.

3.9 Overflow Configuration Registers (Device 6)

Device 6 is the Overflow Device for Device 0. The registers in this section are arranged in ascending order of the address offset. Table 13 provides the configuration register address map.

Table 13. Overflow Device Configuration Register Address Map (Device 6)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID6	Vendor Identification	8086h	RO
02–03h	DID6	Device Identification	2576h	RO
04–05h	PCICMD6	PCI Command	0000h	RO, R/W
06–07h	PCISTS6	PCI Status	0080h	RO
08h	RID6	Revision Identification	See register description	RO
09h	—	Reserved	—	—
0Ah	SUBC6	Sub-Class Code	80h	RO
0Bh	BCC6	Base Class Code	08h	RO
0Ch–0Dh	—	Reserved	—	—
0Eh	HDR6	Header Type	00h	RO
0Fh	—	Reserved	—	—
10–13h	BAR6	Base Address	00000000h	RO
14–2Bh	—	Reserved	—	—
2C–2Dh	SVID6	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID6	Subsystem Identification	0000h	R/WO
30–E6h	—	Reserved	—	—
E7–FFh	—	Intel Reserved	—	—

3.9.1 VID6—Vendor Identification Register (Device 6)

Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

The VID register contains the vendor identification number. This 16-bit register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Vendor Identification (VID)—RO.** This register field contains the PCI standard identification for Intel, 8086h.

3.9.2 DID6—Device Identification Register (Device 6)

Address Offset: 02–03h
Default Value: 2576h
Access: RO
Size: 16 bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Descriptions
15:0	**Device Identification Number (DID)—RO.** This is a 16-bit value assigned to the GMCH Host-to-HI Bridge, Function 0.

3.9.3 PCICMD6—PCI Command Register (Device 6)

Address Offset: 04–05h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Since GMCH Device 0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back Enable (FB2B)—RO.** Hardwired to 0.
8	**SERR Enable (SERRE)—RO.** Hardwired to 0.
7	**Address/Data Stepping Enable (ADSTEP)—RO.** Hardwired to 0.
6	**Parity Error Enable (PERRE)—RO.** Hardwired to 0.
5	**VGA Palette Snoop Enable (VGASNOOP)—RO.** Hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE)—RO.** Hardwired to 0.
3	**Special Cycle Enable (SCE)—RO.** Hardwired to 0.
2	**Bus Master Enable (BME)—RO.** Hardwired to 0.
1	**Memory Access Enable (MAE) —R/W.** Set this bit to 1 to enables Device 6 memory space accesses. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE) —R/W.** This bit must be set to 1 to enable the I/O address range defined in the IOBASE3 and IOLIMIT3 registers. 0 = Disable (default). 1 = Enable.

3.9.4 PCISTS6—PCI Status Register (Device 6)

Address Offset: 06–07h
Default Value: 0080h
Access: RO
Size: 16 bits

PCISTS6 is a 16-bit status register that reports the occurrence of error events on Device 6, Function 0's PCI interface. Since GMCH Device 6 does not physically reside on PCI_0, many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE)—RO.** Hardwired to 0.
14	**Signaled System Error (SSE)—RO.** Hardwired to 0.
13	**Received Master Abort Status (RMAS)—RO.** Hardwired to 0.
12	**Received Target Abort Status (RTAS)—RO.** Hardwired to 0.
11	**Signaled Target Abort Status (STAS)—RO.** Hardwired to 0.
10:9	**DEVSEL Timing (DEVT)—RO.** Hardwired to 00b. Device 6 does not physically connect to PCI_A. These bits are set to 00b (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the GMCH.
8	**Master Data Parity Error Detected (DPD)—RO.** Hardwired to 0.
7	**Fast Back-to-Back (FB2B)—RO.** Hardwired to 1. This indicates fast back-to-back capability; thus, the optimum setting for PCI_A is not limited by the GMCH.
6:0	Reserved.

3.9.5 RID6—Revision Identification Register (Device 6)

Address Offset: 08h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH Device 0.

Bit	Descriptions
7:0	**Revision Identification Number (RID)—RO.** This is an 8-bit value that indicates the revision identification number for the GMCH Device 6. This value is the same as the RID register. 02h = A-2 Stepping

3.9.6 SUBC6—Sub-Class Code Register (Device 6)

Address Offset: 0Ah
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Sub-Class Code for the GMCH Device 0.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)—RO.** This is an 8-bit value that indicates the category of Device for the GMCH Device 6. 80h = Other system peripherals.

3.9.7 BCC6—Base Class Code Register (Device 6)

Address Offset: 0Bh
Default Value: 08h
Access: RO
Size: 8 bits

This register contains the Base Class Code for the GMCH Device 0.

Bit	Descriptions
7:0	**Base Class Code (BASEC)—RO.** This is an 8-bit value that indicates the category of Device for the GMCH Device 6. 08h = Other system peripherals.

3.9.8 HDR6—Header Type Register (Device 6)

Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Descriptions
7:0	**PCI Header (HDR)—RO.** This field indicates a single function device with standard header layout.

3.9.9 BAR6—Memory Delays Base Address Register (Device 6)

Address Offset: 10–13h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register is a standard PCI scheme to claim a memory-mapped address range. This memory-mapped address range can be enabled once the relevant enable bit in the PCI command register is set to 1.

Bit	Descriptions
31:12	**Memory base Address—R/W.** Set by the OS, these bits correspond to address signals [31:13].
11:4	**Address Mask—RO.** Hardwired to 00h to indicate 4-KB address range is reserved for memory-mapped address space.
3	**Prefetchable—RO.** This read only bit indicates the prefetchability of the requested memory address range. 0 = Not prefetchable. The memory range is not prefetchable and may have read side effects. 1 = Prefetchable. The memory address range is prefetchable (i.e., has no read side effects and returns all bytes on reads regardless of byte enables) and byte merging of write transactions is allowed.
2:1	**Memory Type (TYPE)—RO.** Hardwired to 00b to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	**Memory Space Indicator (MSPACE)—RO.** Hardwired to 0 to identify memory space.

3.9.10 SVID6—Subsystem Vendor Identification Register (Device 6)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)—R/WO.** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

3.9.11 SID6—Subsystem Identification Register (Device 6)

Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)—R/WO.** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

3.10 Device 6 Memory-Mapped I/O Register Space

The DRAM timing and delay registers are located in the memory-mapped register (MMR) space of Device 6. Table 14 provides the register address map for this set of registers.

Note: All accesses to these memory-mapped registers must be made as a single DWord (4 bytes) or less. Access must be aligned on a natural boundary.

Table 14. Device 6 Memory-Mapped I/O Register Address Map

Byte Address Offset	Register Symbol	Register Name	Default Value	Access
0000h	DRB0	DRAM Row 0 Boundary	01h	RW
0001h	DRB1	DRAM Row 1 Boundary	01h	RW
0002h	DRB2	DRAM Row 2 Boundary	01h	RW
0003h	DRB3	DRAM Row 3 Boundary	01h	RW
0004h	DRB4	DRAM Row 4 Boundary	01h	RW
0005h	DRB5	DRAM Row 5 Boundary	01h	RW
0006h	DRB6	DRAM Row 6 Boundary	01h	RW
0007h	DRB7	DRAM Row 7 Boundary	01h	RW
0008–000Bh	—	Intel Reserved	—	—
0010h	DRA0,1	DRAM Row 0,1 Attribute	00h	RW
0011h	DRA2,3	DRAM Row 2,3 Attribute	00h	RW
0012h	DRA4,5	DRAM Row 4,5 Attribute	00h	RW
0013h	DRA6,7	DRAM Row 6,7 Attribute	00h	RW
0014–005Fh	—	Intel Reserved	—	—
0060–0063h	DRT	DRAM Timing	0000 0000h	RW
0064–0067h	—	Intel Reserved	—	—
0068–006Bh	DRC	DRAM Controller Mode	0001 0001h	RW
006C–FFFFh	—	Intel Reserved	—	—

3.10.1 DRB[0:7]—DRAM Row Boundary Register (Device 6, MMR)

Address Offset: 0000h–0007h (DRB0–DRB7)
Default Value: 00h
Access: R/W
Size: 8 bits each register

The DRAM row Boundary registers define the upper boundary address of each DRAM row. Each row has its own single-byte DRB register. The granularity of these registers is 64 MB. For example, a value of 1 in DRB0 indicates that 64 MB of DRAM has been populated in the first row. When in either of the two dual-channel modes, the granularity of these registers is still 64 MB. In this case, the lowest order bit in each register is always programmed to 0 yielding a minimum granularity of 128 MB. Bit 7 of each of these registers is reserved and must be programmed to 0.

The remaining 7 bits of each of these registers are compared against address lines 31:26 to determine which row is being addressed by the current cycle. In either of the dual-channel modes, the GMCH supports a total of 4 rows of memory (only DRB0:3 are used). When in either of the dual-channel modes and four rows populated with 512-Mb technology, x8 devices, the largest memory size of 4 GB is supported. In this case, DRB3 is programmed to 40h. In the dual-channel modes, DRB[7:4] must be programmed to the same value as DRB3. In single-channel mode, all eight DRB registers are used. In this case, DRB[3:0] are used for the rows in channel A and DRB[7:4] are used for rows populated in channel B. If only channel A is populated, then only DRB[3:0] are used. DRB[7:4] are programmed to the same value as DBR3. If only channel B is populated, then DRB[7:4] are used and DRB[3:0] are programmed to 00h. When both channels are populated but not identically, all of the DRB registers are used. This configuration is referred to as "virtual single-channel mode."

Row0: 0000h
Row1: 0001h
Row2: 0002h
Row3: 0003h
Row4: 0004h
Row5: 0005h
Row6: 0006h
Row7: 0007h
0008h, reserved
0009h, reserved
000Ah, reserved
000Bh, reserved
000Ch, reserved
000Dh, reserved
000Eh, reserved
000Fh, reserved

DRB0 = Total memory in Row0 (in 64-MB increments)
DRB1 = Total memory in Row0 + Row1 (in 64-MB increments)
DRB2 = Total memory in Row0 + Row1 + Row2 (in 64-MB increments)
DRB3 = Total memory in Row0 + Row1 + Row2 + Row3 (in 64-MB increments)
DRB4 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 (in 64-MB increments)
DRB5 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 (in 64-MB increments)
DRB6 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 + Row6 (in 64-MB increments)
DRB7 = Total memory in Row0 + Row1 + Row2 + Row3 + Row4 + Row5 + Row6 + Row7 (in 64-MB increments)

Each row is represented by a byte. Each byte has the following format:

Bit	Description
7	Reserved.
6:0	**DRAM Row Boundary Address—R/W.** This 7-bit value defines the upper and lower addresses for each SDRAM row. This 7-bit value is compared against address lines 0,31:26 (0 concatenated with the address bits 31:26) to determine which row the incoming address is directed. Default= 0000001b

3.10.2 DRA—DRAM Row Attribute Register (Device 6, MMR)

Address Offset: 0010h–0013h
Default Value: 00h
Access: RO, R/W
Size: 8 bits each register

The DRAM Row Attribute registers define the page sizes to be used when accessing different rows or pairs of rows. The minimum page size of 4 KB occurs when in single-channel mode and either 128-Mb, x16 devices are populated or 256-Mb, x16 devices are populated. The maximum page size of 32 KB occurs when in dual-channel mode and 512-MB, x8 devices are populated. Each nibble of information in the DRA registers describes the page size of a row or pair of rows. When in either of the dual-channel modes, only registers 10h and 11h are used. The page size programmed reflects the page size for the pair of DIMMS installed. When in single-channel mode, registers 10h and 11h are used to specify page sizes for channel A and registers 12h and 13h are used to specify page sizes for channel B. **If the associated row is not populated, the field must be left at the default value.**

Row0, 1:0010h
Row2, 3:0011h
Row4, 5:0012h
Row6, 7:0013h

7	6 4	3	2 0
Rsvd	Row Attribute for Row 1	Rsvd	Row Attribute for Row 0

7	6 4	3	2 0
Rsvd	Row Attribute for Row 3	Rsvd	Row Attribute for Row 2

7	6 4	3	2 0
Rsvd	Row Attribute for Row 5	Rsvd	Row Attribute for Row 4

7	6 4	3	2 0
Rsvd	Row Attribute for Row 7	Rsvd	Row Attribute for Row 6

Bit	Description
7	Reserved.
6:4	**Row Attribute for Odd-Numbered Row—R/W.** This field defines the page size of the corresponding row. If the associated row is not populated, this field must be left at the default value. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB Others = Reserved
3	Reserved.
2:0	**Row Attribute for Even-Numbered Row—R/W.** This field defines the page size of the corresponding row. If the associated row is not populated, this field must be left at the default value. 000 = 4 KB 001 = 8 KB 010 = 16 KB 011 = 32 KB Others = Reserved

3.10.3 DRT—DRAM Timing Register (Device 6, MMR)

Address Offset: 0060h–0063h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register controls the timing of micro-commands. When in virtual single-channel mode, the timing fields specified here apply even if two back-to-back cycles are to different physical channels. That is, the controller acts as if the two cycles are to the same physical channel.

Bit	Description
31:11	Reserved
10	**Activate to Precharge Delay (t_{RAS}) Max—R/W.** These bits control the number of DRAM clocks for t_{RAS} maximum. 0 = 120 µs 1 = 70 µs **NOTE:** DDR333 SDRAM require a shorter T_{RAS} (max) of 70 µs.
9:7	**Activate to Precharge delay (t_{RAS}), Min—R/W.** These bits control the number of DRAM clocks for t_{RAS} minimum. 000 = 10 DRAM clocks 001 = 9 DRAM clocks 010 = 8 DRAM clocks 011 = 7 DRAM clocks 100 = 6 DRAM clocks 101 = 5 DRAM clocks others = Reserved
6:5	**CAS# Latency (t_{CL})—R/W.** 00 = 2.5 DRAM clocks 01 = 2 DRAM clocks 10 = 3 DRAM clocks 11 = Reserved
4	Reserved
3:2	**DRAM RAS# to CAS# Delay (t_{RCD})—R/W.** This bit controls the number of clocks inserted between an activate command and a read or write command to that bank. 00 = 4 DRAM clocks 01 = 3 DRAM clocks 10 = 2 DRAM clocks 11 = Reserved
1:0	**DRAM RAS# Precharge (t_{RP})—R/W.** This bit controls the number of clocks that are inserted between a precharge command and an activate command to the same bank. 00 = 4 DRAM clocks (DDR 333) 01 = 3 DRAM clocks 10 = 2 DRAM clocks 11 = Reserved

3.10.4 DRC—DRAM Controller Mode Register (Device 6, MMR)

Address Offset: 0068h–006Bh
Default Value: 00000001h
Access: R/W, RO
Size: 32 bits

Bit	Description
31:30	Reserved.
29	**Initialization Complete (IC)—R/W.** This bit is used for communication of the software state between the memory controller and the BIOS. 1 = BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28:23	Reserved.
22:21	**Number of Channels (CHAN)—R/W.** The GMCH memory controller supports three modes of operation. When programmed for single-channel mode, there are three options: channel A is populated, channel B is populated, or both are populated but not identically. When both channels have DIMMs installed and they are not identical (from channel to channel), the controller operates in a mode that is referred to as virtual single-channel. In this mode, the two physical channels are not in lock step but act as one logical channel. To operate in either dual-channel mode, the two channels must be populated identically. 00 = Single-channel or virtual single-channel 01 = Dual-channel, linear organization 10 = Dual-channel, tiled organization 11 = Reserved
20:11	Reserved
10:8	**Refresh Mode Select (RMS)—R/W.** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Reserved 001 = Refresh enabled. Refresh interval 15.6 µsec 010 = Refresh enabled. Refresh interval 7.8 µsec 011 = Refresh enabled. Refresh interval 64 µsec 111 = Refresh enabled. Refresh interval 64 clocks (fast refresh mode) Other = Reserved
7	Reserved.

Bit	Description
6:4	**Mode Select (SMS)—R/W.** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. Note that FCSEN (fast CS#) must be set to 0 while SMS cycles are performed. It is expected that BIOS may program FCSEN to possible 1 only after initialization. 000 =Post Reset state – When the GMCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the GMCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During suspend (S3, S4), GMCH internal signal triggers SDRAM controller to flush pending commands and enter all rows into Self-Refresh mode. As part of resume sequence, the GMCH will be reset – which clears this bit field to 000 and maintains CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. 001 =NOP Command Enable – All processor cycles to DRAM result in a NOP command on the DRAM interface. 010 =All Banks Pre-charge Enable – All processor cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011 =Mode Register Set Enable – All processor cycles to DRAM result in a “mode register” set command on the SDRAM interface. Host address lines are mapped to SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to memory address SMA[5:1]. 100 =Extended Mode Register Set Enable – All processor cycles to SDRAM result in an “extended mode register set” command on the SDRAM interface. Host address lines are mapped to SDRAM address lines in order to specify the command sent. Host address lines are mapped to SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to memory address SMA[5:1]. 101 =Reserved 110 =CBR Refresh Enable – In this mode all processor cycles to SDRAM result in a CBR cycle on the SDRAM interface 111 =Normal operation
3:2	Reserved
1:0	**DRAM Type (DT)—RO.** This field is used to select between supported SDRAM types. 00 = Reserved 01 = Dual Data Rate SDRAM Other = Reserved.

This page is intentionally left blank.

System Address Map 4

The processor in an 865G chipset system supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1-MB region that is divided into regions that can be individually controlled with programmable attributes (e.g., disable, read/write, write only, or read only). Attribute programming is described in Chapter 3. This section focuses on how the memory space is partitioned and the use of the separate memory regions.

The Pentium 4 processor family supports addressing of memory ranges larger than 4 GB. The GMCH claims any processor access over 4 GB and terminates the transaction without forwarding it to the hub interface or AGP (discarding the data terminates writes). For reads, the GMCH returns all zeros on the host bus. Note that the 865G chipset platform does not support the PCI Dual Address Cycle Mechanism; therefore, it does not allow addressing of greater than 4 GB on either the hub interface or AGP interface.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the hub interface/PCI. The exception to this rule is VGA ranges that may be mapped to AGP or to the IGD. In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the hub interface/PCI, while cycle descriptions referencing AGP are related to the AGP bus.

The 865G chipset memory map includes a number of programmable ranges.

Note: All of these ranges must be unique and non-overlapping. There are no hardware interlocks to prevent problems in the case of overlapping ranges. Accesses to overlapped ranges may produce indeterminate results.

4.1 System Memory Address Ranges

The GMCH provides a maximum system memory address decode space of 4 GB. The GMCH does not remap APIC memory space. The GMCH does not limit system memory space in hardware. **It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, AGP, High BIOS, and APIC memory space can be allocated.** Figure 9 provides a simplified system memory address map. Figure 10 provides additional details on mapping specific memory regions as defined and supported by the GMCH.

Figure 9. Memory System Address Map

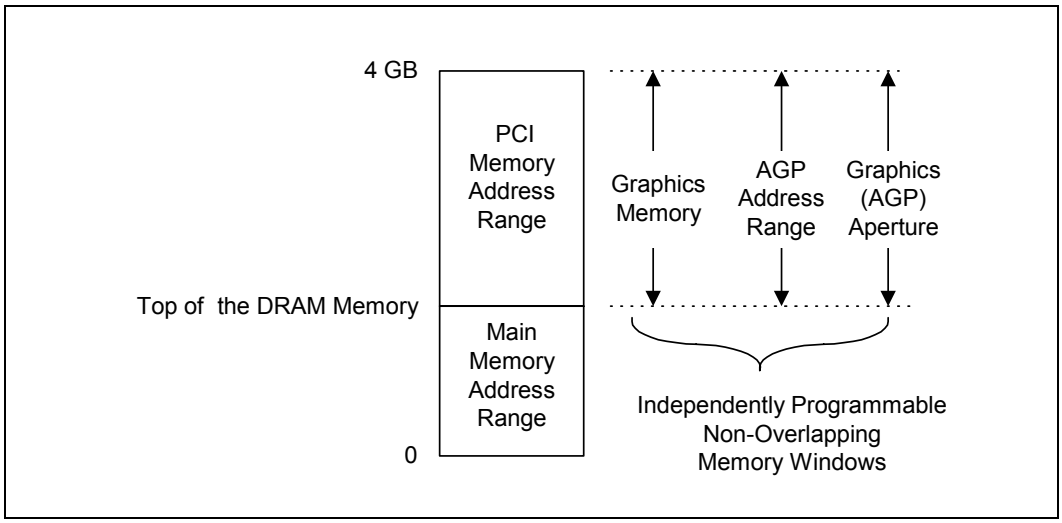
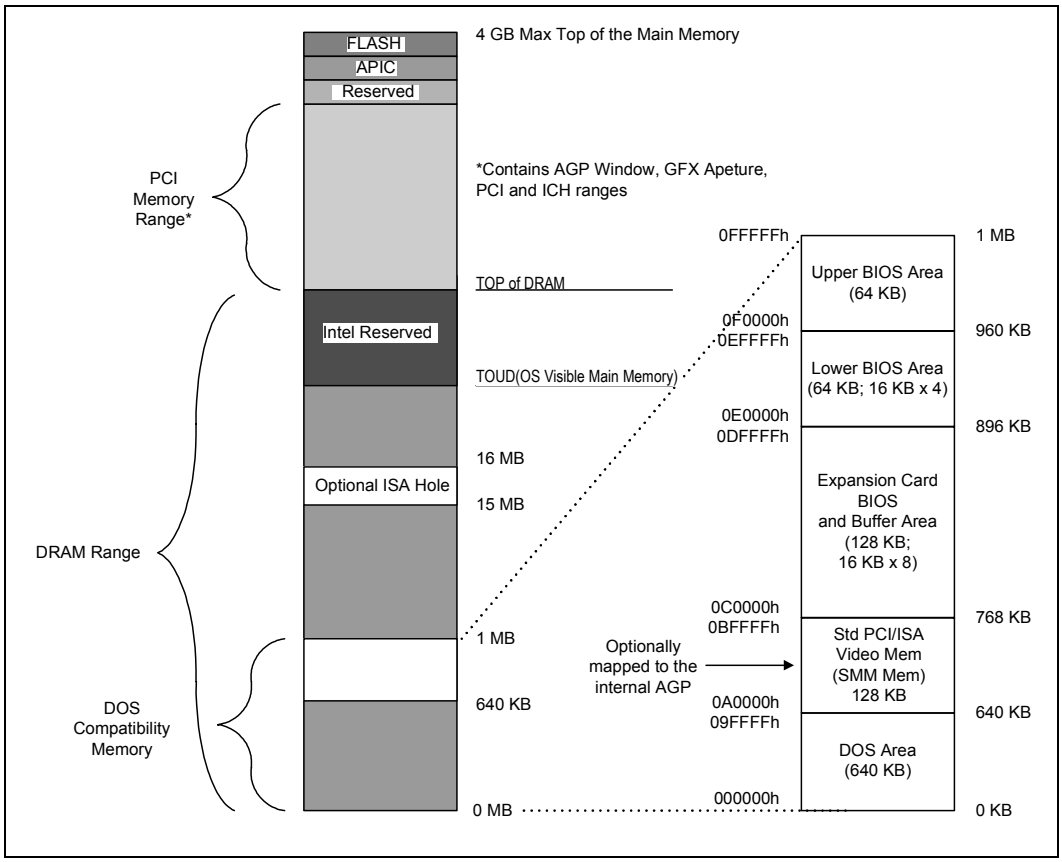


Figure 10. Detailed Memory System Address Map



4.2 Compatibility Area

This area is divided into the following address regions:

- 0–640 KB MS-DOS Area.
- 640–768 KB Video Buffer Area.
- 768–896 KB in 16-KB sections (total of 8 sections) – Expansion Area.
- 896–960 KB in 16-KB sections (total of 4 sections) – Extended System BIOS Area.
- 960 KB–1 MB Memory (BIOS Area) – System BIOS Area.

There are fifteen memory segments in the compatibility area (see Table 15). Thirteen of the memory ranges can be enabled or disabled independently for both read and write cycles.

Table 15. Memory Segments and Their Attributes

Memory Segments	Attributes	Comments
000000h–09FFFFh	Fixed: always mapped to main SDRAM	0 to 640 KB – DOS Region
0A0000h–0BFFFFh	Mapped to hub interface, AGP, or IGD: configurable as SMM space	Video Buffer (physical SDRAM configurable as SMM space)
0C0000h–0C3FFFh	WE RE	Add-on BIOS
0C4000h–0C7FFFh	WE RE	Add-on BIOS
0C8000h–0CBFFFh	WE RE	Add-on BIOS
0CC000h–0CFFFFh	WE RE	Add-on BIOS
0D0000h–0D3FFFh	WE RE	Add-on BIOS
0D4000h–0D7FFFh	WE RE	Add-on BIOS
0D8000h–0DBFFFh	WE RE	Add-on BIOS
0DC000h–0DFFFFh	WE RE	Add-on BIOS
0E0000h–0E3FFFh	WE RE	BIOS Extension
0E4000h–0E7FFFh	WE RE	BIOS Extension
0E8000h–0EBFFFh	WE RE	BIOS Extension
0EC000h–0EFFFFh	WE RE	BIOS Extension
0F0000h–0FFFFFh	WE RE	BIOS Area

DOS Area (00000h–9FFFFh)

The DOS area is 640 KB in size and is always mapped to the main memory controlled by the GMCH.

Legacy VGA Ranges (A0000h–BFFFFh)

The legacy 128-KB VGA memory range A0000h–BFFFFh (Frame Buffer) can be mapped to IGD (Device 2), to AGP/PCI_B (Device 1), and/or to the hub interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and AGP/PCI_B. Subsequent decoding of regions mapped to AGP/PCI_B or the hub interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (A0000h–BFFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system SDRAM at this address. Non-SMM-mode processor accesses to this range are considered to be to the video buffer area as described above. AGP and HI originated cycles to enabled SMM space are not allowed and are considered to be to the video buffer area.

Monochrome Adapter (MDA) Range (B0000h–B7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, AGP/PCI_B, and the hub interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the GMCH must decode cycles in the MDA range and forward them either to IGD, AGP/PCI_B, or to the hub interface. This capability is controlled by VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the GMCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to the either the IGD, AGP/PCI_B, and/or the hub interface.

Expansion Area (C0000h–DFFFFh)

This 128-KB ISA Expansion region is divided into eight, 16-KB segments. Each segment can be assigned one of four read/write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main system memory or to hub interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single, 64-KB segment. This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the hub interface. By manipulating the read/write attributes, the GMCH can “shadow” BIOS into the main system memory. When disabled, this segment is not remapped.

4.3 Extended Memory Area

This memory area covers the 1 MB to 4 GB–1 (100000h–FFFFFFFFh) address range and is divided into the following regions:

- Main system SDRAM memory from 1 MB to the Top of Memory; maximum of 4-GB SDRAM.
- AGP or PCI Memory space from the Top of Memory to 4 GB, with two specific ranges:
  - APIC Configuration Space from FEC0_0000h (4 GB–20 MB) to FECF_FFFFh and FEE0_0000h to FEEF_FFFFh
  - High BIOS area from 4 GB to 4 GB – 2 MB

Main System Memory Address Range (0010_0000h to Top of Main Memory)

The address range from 1 MB to the top of system memory is mapped to system memory address range controlled by the GMCH. The Top of Main Memory (TOMM) is limited to 4-GB SDRAM. All accesses to addresses within this range will be forwarded by the GMCH to system memory unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to the hub interface.

The GMCH provides a maximum system memory address decode space of 4 GB. The GMCH does not remap APIC memory space. The GMCH does not limit system memory address space in hardware.

4.3.1 15 MB–16 MB Window

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the hub interface. The range of physical SDRAM memory disabled by opening the hole is not remapped to the Top of the memory – that physical SDRAM space is not accessible. This 15-MB–16-MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. There is no inherent BIOS request for the 15-MB–16-MB hole.

4.3.2 Pre-Allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within the system memory address range (< TOSM) are created for SMM-mode and legacy VGA graphics compatibility. For VGA graphics compatibility, pre-allocated memory is only required in non-local memory configurations. **It is the responsibility of BIOS to properly initialize these regions**. Table 16 details the location and attributes of the regions. Enabling/Disabling these ranges are described in the GMCH Control (GC) Register in Device 0.

Table 16. Pre-Allocated Memory

Memory Segments	Attributes	Comments
00000000h–03E7FFFFh	R/W	Available System Memory 62.5 MB
03E80000h–03EFFFFFh	SMM Mode Only - processor Reads	TSEG Address Range
03E80000h–03EFFFFFh	SMM Mode Only - processor Reads	TSEG Pre-allocated Memory
03F00000h– 03FFFFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 512 K or 8 MB) when IGD is enabled.

Extended SMRAM Address Range (HSEG and TSEG)

The HSEG and TSEG SMM transaction address spaces reside in this extended memory area.

HSEG

SMM-mode processor accesses to enabled HSEG are remapped to 000A0000h–000BFFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode write back cycles that are remapped to SMM space to maintain cache coherency. AGP and HI originated cycles to enabled SMM space are not allowed. Physical SDRAM behind the HSEG transaction address is not remapped and is not accessible.

TSEG

TSEG can be up to 1 MB in size and is the first block after the top of usable physical memory. SMM-mode processor accesses to enabled TSEG access the physical SDRAM at the same address. Non-SMM-mode processor accesses to enabled TSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode write back cycles that are directed to the physical SMM space to maintain cache coherency. AGP and HI originated cycles to enabled SMM space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM processor accesses and all other accesses in this range are forwarded to the hub interface. When SMM is enabled, the amount of memory available to the system is equal to the amount of physical SDRAM minus the value in the TSEG register.

PCI Memory Address Range (Top of Main Memory to 4 GB)

The address range from the top of main SDRAM to 4 GB (top of physical memory space supported by the GMCH) is normally mapped via the hub interface to PCI.

As a memory controller hub, there is one exception to this rule.

- Addresses decoded to MMIO for DRAM RCOMP configuration registers.

As an internal graphics configuration, there are two exceptions to this rule. Both of these exception cases are forwarded to the IGD.

- Addresses decoded to graphics configuration registers.
- Addresses decoded to the memory-mapped range of the Internal Graphics Device (IGD).

As an AGP configuration, there are two exceptions to this rule.

- Addresses decoded to the AGP memory window defined by the MBASE, MLIMIT, PMBASE, and PMLIMIT registers are mapped to AGP.
- Addresses decoded to the graphics aperture range defined by the APBASE and APSIZE registers are mapped to the main SDRAM.

Caution: There are two sub-ranges within the PCI memory address range defined as APIC configuration space and High BIOS address range. As an Internal Graphics Device, the memory-mapped range of the Internal Graphics Device **Must Not** overlap with these two ranges. Similarly, as an AGP device, the AGP memory window and graphics aperture window **Must Not** overlap with these two ranges. These ranges are described in detail in the following paragraphs.

APIC Configuration Space (FEC0_0000h–FECF_FFFFh, FEE0_0000h–FEEF_FFFFh)

This range is reserved for APIC configuration space that includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_0FFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0_0000h (4 GB–20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH5 portion of the chipset or as a stand-alone component.

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC is located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is the I/O APIC unit number 0 through F(hex). This address range will be normally mapped to the hub interface.

Note: There is no provision to support an I/O APIC device on AGP.

The address range between the APIC configuration space and the High BIOS (FED0_0000h to FFDF_FFFFh) is always mapped to the hub interface.

High BIOS Area (FFE0_0000h–FFFF_FFFFh)

The top 2 MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to the hub interface so that the upper subset of this region aliases to 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that the full 2 MB must be considered.

4.4 AGP Memory Address Ranges

The GMCH can be programmed to direct memory accesses to the AGP bus interface when addresses are within either of two ranges specified via registers in GMCH's Device 1 configuration space. The first range is controlled via the Memory Base (MBASE) and Memory Limit (MLIMIT) registers. The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address. For the purpose of address decoding, the GMCH assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFFh. This forces each memory address range to be aligned to 1-MB boundary and to have a size granularity of 1 MB.

The GMCH positively decodes memory accesses to AGP memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the AGP device. Normally, these ranges reside above the top of main memory and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOUD) so they do not steal any physical SDRAM memory space.

It is essential to support a separate Prefetchable range in order to apply the USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the GMCH Device 1 memory range registers described above are used to allocate memory address space for any devices on AGP that require such a window. These devices include the AGP device, PCI-66 MHz/1.5 V agents, and multifunctional AGP devices where one or more functions are implemented as PCI devices.

The PCICMD1 register can override the routing of memory accesses to AGP. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

Functional Description 5

This chapter describes the GMCH interfaces and functional units including the processor system bus interface, the AGP interface, system memory controller, integrated graphics device, DVO interfaces, display interfaces, power management, and clocking.

5.1 Processor Front Side Bus (FSB)

The GMCH supports a single Pentium 4 processor with 512-KB L2 cache on 0.13 micron process in a 478-pin package or the Pentium 4 processor on 90 nm process. The GMCH supports FSB frequencies of 400 MHz, 533 MHz, and 800 MHz using a scalable FSB VTT voltage and on-die termination. It supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to AGP/PCI_B, Hub Interface, or the GMCH configuration space. Host-initiated memory cycles are decoded to AGP/PCI_B, Hub Interface or system memory. All memory accesses from the host interface that hit the graphics aperture are translated using an AGP address translation table. AGP/PCI_B device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from AGP/PCI_B using PCI semantics and from the hub interface to system memory will be snooped on the host bus.

The GMCH supports the Pentium 4 processor subset of the Enhanced Mode Scalable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. At 100/133/200 MHz bus clock the address signals are double pumped to run at 200/266/400 MHz and a new address can be generated every other bus clock. At 100/133/200 MHz bus clock the data signals are quad pumped to run at 400/533/800 MHz and an entire 64-B cache line can be transferred in two bus clocks.

The GMCH integrates AGTL+ termination resistors on die. The GMCH has an IOQ depth of 12. The GMCH supports one outstanding deferred transaction on the FSB.

5.1.1 FSB Dynamic Bus Inversion

The GMCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the GMCH. DINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

DINV[3:0]#	Data Bits
DINV0#	HD[15:0]#
DINV1#	HD[31:16]#
DINV2#	HD[47:32]#
DINV3#	HD[63:48]#

When the processor or the GMCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding DINVx# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the GMCH receives data, it monitors DINV[3:0]# to determine if the corresponding data segment should be inverted.

5.1.2 FSB Interrupt Overview

Pentium 4 processors support FSB interrupt delivery. They do **not** support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the FSB as "Interrupt Message Transactions." In the 865G chipset platform FSB interrupts may originate from the processor on the system bus, or from a downstream device on the hub interface, or AGP. In the later case the GMCH drives the "Interrupt Message Transaction" onto the system bus.

In the 865G chipset environment the ICH5 contains IOxAPICs, and its interrupts are generated as upstream HI memory writes. Furthermore, PCI 2.3 defines MSIs (Message Signaled Interrupts) that are also in the form of memory writes. A PCI 2.3 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC which in turn generates an interrupt as an upstream hub interface memory write. Alternatively, the MSI may be directed directly to the FSB. The target of an MSI is dependent on the address of the interrupt memory write. The GMCH forwards inbound HI and AGP/PCI (PCI semantic only) memory writes to address 0FEEx_xxxxh to the FSB as "Interrupt Message Transactions."

5.1.2.1 Upstream Interrupt Messages

The GMCH accepts message-based interrupts from PCI (**PCI semantics only**) hub interface and forwards them to the FSB as Interrupt Message Transactions. The interrupt messages presented to the GMCH are in the form of memory writes to address 0FEEx_xxxxh. At the HI or PCI interface, the memory write interrupt message is treated like any other memory write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the memory write from PCI or hub interface to address 0FEEx_xxxxh is decoded as a cycle that needs to be propagated by the GMCH to the FSB as an Interrupt Message Transaction.

5.2 System Memory Controller

The GMCH can be configured to support DDR266/333/400 MHz memory in single- or dual-channel mode. This includes support for:

- Up to 4 GB of 266/333/400 MHz DDR SDRAM
- DDR266, DDR333, and DDR400 unbuffered 184-pin DDR SDRAM DIMMs
- Up to 2 DIMMs per-channel, single-sided and/or double-sided
- Byte masking on writes through data masking.

Table 17. System Memory Capacity

DRAM Technology	Smallest Increments	Largest Increments	Maximum Capacity (4 DS DIMMs)
128 Mb	64 MB	256 MB	1024 MB
256 Mb	128 MB	512 MB	2048 MB
512 Mb	256 MB	1024 MB	4096 MB

NOTE: The *Smallest Increments* column also represents the smallest possible single DIMM capacity.

DIMM population guidelines are shown in Figure 11 and Chapter 13.

Figure 11. Single-Channel Mode Operation

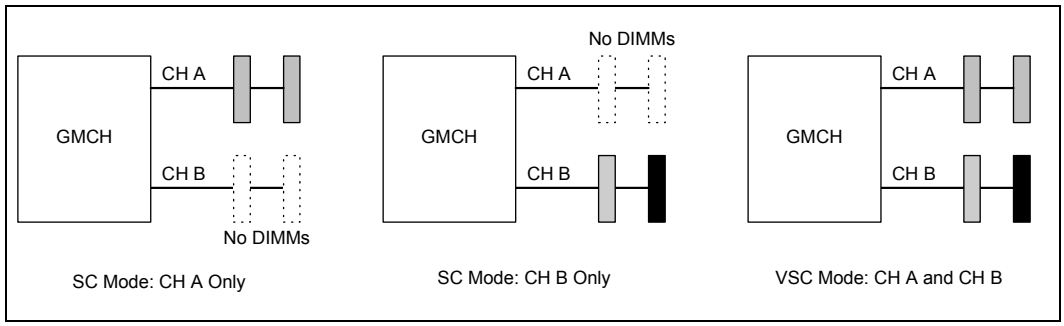
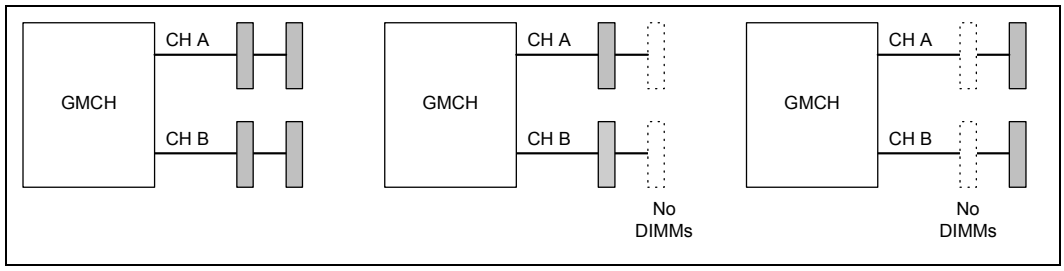


Figure 12. Dual-Channel Mode Operation



5.2.1 DRAM Technologies and Organization

Supported DRAM technologies and organizations include:

- All standard 128-Mb, 256-Mb and 512-Mb technologies and addressing are supported for x16 and x8 devices.
- All supported devices have 4 banks.
- The GMCH supports page sizes. Page size is individually selected for every row
  - 4 KB, 8 KB, 16 KB for single-channel mode.
  - 8 KB,16 KB, and 32 KB in dual-channel mode
- The DRAM sub-system supports a single or dual-channel, 64 b wide per channel
- There can be a maximum of four rows populated (two double-sided DIMMs) per channel.
- Mixed mode DDR DS-DIMMs (x8 and x16 on same DIMM) are not supported
- By using 512-Mb technology, the largest memory capacity is 2 GB per channel (64M x 8b x 8 devices x 4 rows = 2 GB)
- By using 128-Mb technology, the smallest memory capacity is 64 MB per channel (8M x 16b x 4 devices x 1 rows = 64 MB)

5.2.2 Memory Operating Modes

The GMCH supports the following modes of operation

- Single-channel mode (SC).
  - Populate channel A only
  - Populate channel B Only
  - Populate both channel A and B.
- Dual-channel lock step mode (DS).
  - DS linear mode.
  - DS tiled mode. (internal graphics mode)

The GMCH supports a special mode of addressing – Dynamic Addressing mode. All the above-mentioned modes can be enabled with/without Dynamic addressing mode enabled. Table 18 summarizes the different operating modes GMCH memory controller can operate.

Table 18. GMCH Memory Controller Operating Modes

Mode Type		Dynamic Addressing Mode	Non-Dynamic Addressing Mode
SC Mode	Channel A Only	Yes(1)	Yes
	Channel B Only	Yes(1)	Yes
	Both Channel A and B	Yes(1)	Yes
DS Mode	Linear	Yes	Yes(1)
	Tiled	Yes	Yes(1)

NOTE:
1. Special cases – need to meet few requirements discussed in Section 5.2.2.1.

5.2.2.1 Dynamic Addressing Mode

When the GMCH is configured to operate in this mode, FSB-to-memory bus address mapping undergoes a significant change compared to that of in a Linear Operating mode (normal operating mode). In non-dynamic mode, the row selection (row indicates the side of a DIMM) via chip select signals is accomplished based on the size of the row. For example, for a 512-Mb, 16Mx8x4b has a row size of 512 MB selected by CS0# and only four open pages can be maintained for the full 512 MB. This lowers the memory performance (increases read latencies) if most of the memory cycles are targeted to that single row, resulting in opening and closing of accessed pages in that row.

Dynamic Addressing mode minimizes the overhead of opening/closing pages in memory banks allowing for row switching to be done less often.

5.2.3 Single-Channel (SC) Mode

If either only channel A or only channel B is populated, the GMCH is set to operate in single-channel mode. Data is accessed in chunks of 64 bits (8 B) from the memory channels. If both channels are populated with uneven memory (DIMMs), the GMCH defaults to virtual single-channel (VSC) mode. Even with similar memory configuration on both the channels, it is possible to force the GMCH to operate in single-channel mode, which by default is configured as Lock Step mode. The GMCH behaves identical in both single-channel and virtual single-channel modes (hereafter referred to as single-channel (SC) mode).

In this mode of operation, the populated DIMMs configuration can be identical or completely different. In addition, for SC mode, not all the slots need to be populated. For example, populating only one DIMM in channel A is a valid configuration for SC mode. Likewise, in VSC mode odd number of slots can be populated. For Dynamic Mode operation, the requirement is to have an even number of rows (side of the DIMM) populated. In SC, dynamic mode operation can be enabled with one single-sided (SS), two SS or two double-sided (DS). For VSC mode, both the channels need to have an identical row structure.

5.2.3.1 Linear Mode

This mode is the normal mode of operation for the GMCH with internal graphics device disabled.

5.2.3.2 Tiled Mode

This mode was specifically aimed at improving the performance of the Integrated Graphics Device.

5.2.4 Memory Address Translation and Decoding

The address translation and decoding for the GMCH is provided in Table 19 through Table 24. The supported DIMM configurations are listed in the following bullets. Refer to Section 5.2.5 for details about the configurations being double-sided versus single-sided.

- Technology 128 Mbit – 16Mx8 – page size of 8 KB – row size of 128 MB
- Technology 128 Mbit – 8Mx16 – page size of 4 KB – row size of 64 MB
- Technology 256 Mbit – 32Mx8 – page size of 8 KB – row size of 256 MB
- Technology 256 Mbit – 16Mx16 – page size of 4 KB – row size of 128 MB
- Technology 512 Mbit – 32Mx16 – page size of 8 KB – row size of 256 MB
- Technology 512 Mbit – 64Mx8 – page size of 16 KB – row size of 512 MB

Note: In Table 19 through Table 24 A0, A1, … refers to memory address MA0, MA1, ….
The table cell contents refers to host address signals HAx.

Table 19. DRAM Address Translation (Single-Channel Mode) (Non-Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	13	12		16	15	14	25	24	23	22	21	20	19	18	17
		4KB		Col		13	12			AP		11	10	9	8	7	6	5	4	3
128Mb	16Mx8	128MB	12x10x2	Row	26	14	13		16	15	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
256Mb	16Mx16	128MB	13x9x2	Row	26	13	12	26	16	15	14	25	24	23	22	21	20	19	18	17
		4KB		Col		13	12			AP		11	10	9	8	7	6	5	4	3
256Mb	32Mx8	256MB	13x10x2	Row	27	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	32Mx16	256MB	13x10x2	Row	27	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	64Mx8	512MB	13x11x2	Row	28	15	14	28	16	27	26	25	24	23	22	21	20	19	18	17
		16KB		Col		15	14		13	AP	12	11	10	9	8	7	6	5	4	3

Table 20. DRAM Address Translation (Dual-Channel Mode, Discrete) (Non-Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	14	13		16	15	26	25	24	23	22	21	20	19	18	17
		4KB		Col		14	13			AP		12	11	10	9	8	7	6	5	4
128Mb	16Mx8	128MB	12x10x2	Row	26	14	15		16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
256Mb	16Mx16	128MB	13x9x2	Row	26	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		4KB		Col		14	13			AP		12	11	10	9	8	7	6	5	4
256Mb	32Mx8	256MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
512Mb	32Mx16	256MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	4
512Mb	64Mx8	512MB	13x11x2	Row	28	16	15	28	29	27	26	25	24	23	22	21	20	19	18	17
		16KB		Col		16	15		14	AP	13	12	11	10	9	8	7	6	5	4

Table 21. DRAM Address Translation (Dual-Channel Mode, Internal Gfx) (Non-Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	14	13		16	15	26	25	24	23	22	21	20	19	18	17
		4KB		Col		14	13			AP		12	11	10	9	8	7	6	5	3
128Mb	16Mx8	128MB	12x10x2	Row	26	14	15		16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	3
256Mb	16Mx16	128MB	13x9x2	Row	26	14	13	27	16	15	26	25	24	23	22	21	20	19	18	17
		4KB		Col		14	13			AP		12	11	10	9	8	7	6	5	3
256Mb	32Mx8	256MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	3
512Mb	32Mx16	256MB	13x10x2	Row	27	14	15	28	16	27	26	25	24	23	22	21	20	19	18	17
		8KB		Col		14	15			AP	13	12	11	10	9	8	7	6	5	3
512Mb	64Mx8	512MB	13x11x2	Row	28	16	15	28	29	27	26	25	24	23	22	21	20	19	18	17
		16KB		Col		16	15		14	AP	13	12	11	10	9	8	7	6	5	3

Table 22. DRAM Address Translation (Single-Channel Mode) (Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	12	18		16	13	14	27	26	23	22	21	25	24	15	17
		4KB		Col		12	18			AP		11	10	9	8	7	6	5	4	3
128Mb	16Mx8	128MB	12x10x2	Row	26	18	13		16	14	26	28	27	23	22	21	25	24	15	17
		8KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
256Mb	16Mx16	128MB	13x9x2	Row	26	12	18	26	16	13	14	28	27	23	22	21	25	24	15	17
		4KB		Col		12	18			AP		11	10	9	8	7	6	5	4	3
256Mb	32Mx8	256MB	13x10x2	Row	27	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		8KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	32Mx16	256MB	13x10x2	Row	27	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		8KB		Col		18	13			AP	12	11	10	9	8	7	6	5	4	3
512Mb	64Mx8	512MB	13x11x2	Row	28	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		16KB		Col		14	18		13	AP	12	11	10	9	8	7	6	5	4	3

Table 23. DRAM Address Translation (Dual-Channel Mode, Discrete) (Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	18	13		16	14	26	28	27	23	22	21	25	24	15	17
		4KB		Col		18	13			AP		12	11	10	9	8	7	6	5	4
128Mb	16Mx8	128MB	12x10x2	Row	26	14	18		16	27	26	25	24	23	22	21	29	28	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
256Mb	16Mx16	128MB	13x9x2	Row	26	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		4KB		Col		18	13			AP		12	11	10	9	8	7	6	5	4
256Mb	32Mx8	256MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
512Mb	32Mx16	256MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	4
512Mb	64Mx8	512MB	13x11x2	Row	28	18	15	28	29	27	26	31	30	23	22	21	25	24	15	17
		16KB		Col		18	15		14	AP	13	12	11	10	9	8	7	6	5	4

Table 24. RAM Address Translation (Dual-Channel Mode, Internal Gfx) (Dynamic Mode)

Tech.	Config.	Row size Page size	Row / Column / Bank		Addr	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
128Mb	8Mx16	64MB	12x9x2	Row	25	18	13		16	14	26	28	27	23	22	21	25	24	15	17
		4KB		Col		18	13			AP		12	11	10	9	8	7	6	5	3
128Mb	16Mx8	128MB	12x10x2	Row	26	14	18		16	27	26	25	24	23	22	21	29	28	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	3
256Mb	16Mx16	128MB	13x9x2	Row	26	18	13	27	16	14	26	25	24	23	22	21	29	28	15	17
		4KB		Col		18	13			AP		12	11	10	9	8	7	6	5	3
256Mb	32Mx8	256MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	3
512Mb	32Mx16	256MB	13x10x2	Row	27	14	18	28	16	27	26	25	24	23	22	21	30	29	15	17
		8KB		Col		14	18			AP	13	12	11	10	9	8	7	6	5	3
512Mb	64Mx8	512MB	13x11x2	Row	28	18	15	28	29	27	26	31	30	23	22	21	25	24	16	17
		16KB		Col		18	15		14	AP	13	12	11	10	9	8	7	6	5	3

5.2.5 Memory Organization and Configuration

In the following discussion the term “row” refers to a set of memory devices that are simultaneously selected by a chip select signal. The GMCH supports a maximum of four rows of memory. For the purposes of this discussion, a “side” of a DIMM is equivalent to a “row” of SDRAM devices.

The memory bank address lines and the address lines allow the GMCH to support 64-bit wide x8 and x16 DIMMs using 128-Mb, 256-Mb, and 512-Mb SDRAM technology.

For the DDR SDRAM interface, Table 25 lists the supported configurations. Note that the GMCH supports configurations defined in the JEDEC DDR DIMM specification only (A, B, C). Non-JEDEC standard DIMMs (e.g., double-sided x16 DDR SDRAM DIMMs) are not supported. For additional information on DIMM configurations, refer to the *JEDEC DDR DIMM specification*.

Table 25. Supported DDR DIMM Configurations

Density	128 Mbit		256 Mbit		512 Mbit	
Device Width	x8	x16	x8	x16	x8	x16
Single / Double	SS/DS	SS/DS	SS/DS	SS/DS	SS/DS	SS/DS
184 pin DDR DIMMs	128/256 MB	64 MB/NA	256/512 MB	128 MB/NA	512/1024 MB	256 MB/NA

5.2.6 Configuration Mechanism for DIMMS

Detection of the type of SDRAM installed on the DIMM is supported via the Serial Presence Detect (SPD) mechanism as defined in the JEDEC DIMM specification. This uses the SCL, SDA, and SA[2:0] pins on the DIMMs to detect the type and size of the installed DIMMs. No special programmable modes are provided on the GMCH for detecting the size and type of memory installed. Type and size detection must be accomplished via the serial presence detection pins and is required to configure the GMCH.

5.2.6.1 Memory Detection and Initialization

Before any cycles to the memory interface can be supported, the GMCH SDRAM registers must be initialized. The GMCH must be configured for operation with the installed memory types. Detection of memory type and size is accomplished via the System Management Bus (SMBus) interface on the ICH5. This two-wire bus is used to extract the SDRAM type and size information from the Serial Presence Detect port on the SDRAM DIMMs. SDRAM DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data), and SA[2:0]. Devices on the SMBus bus have a 7-bit address. For the SDRAM DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected to the System Management Bus on the ICH5. Thus, data is read from the Serial Presence Detect port on the DIMMs via a series of I/O cycles to the ICH5. BIOS needs to determine the size and type of memory used for each of the rows of memory to properly configure the GMCH memory interface.

5.2.6.2 SMBus Configuration and Access of the Serial Presence Detect Ports

For more details, refer to the *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet*.

5.2.6.3 Memory Register Programming

This section provides an overview of how the required information for programming the SDRAM registers is obtained from the Serial Presence Detect ports on the DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, SMA and SMD Buffer Strength, Row Type (on a row-by-row basis), SDRAM Timings, Row Sizes, and Row Page Sizes. Table 26 lists a subset of the data available through the on board Serial Presence Detect ROM on each DIMM.

Table 26. Data Bytes on DIMM Used for Programming DRAM Registers

Byte	Function
2	Memory type (DDR SDRAM)
3	Number of row addresses, not counting bank addresses
4	number of column addresses
5	Number of banks of SDRAM (single- or double-sided DIMM)
11	ECC, non-ECC (865G chipset GMCH does not support ECC)
12	Refresh rate
17	Number of banks on each device

Table 26 is only a subset of the defined SPD bytes on the DIMMs. These bytes collectively provide enough data for programming the GMCH SDRAM registers.

5.2.7 Memory Thermal Management

The GMCH provides a thermal management method that selectively reduces reads and writes to DRAM when the access rate crosses the allowed thermal threshold.

Read and write thermal management operate independently, and have their own 64-bit register to control operation. Memory reads typically causes power dissipation in the DRAM chips while memory writes typically causes power dissipation in the GMCH.

5.2.7.1 Determining When to Thermal Manage

Thermal management may be enabled by one of two mechanisms:

- Software forcing throttling via the SRT (SWT) bit.
- Counter Mechanism.

5.3 Accelerated Graphics Port (AGP)

The GMCH supports AGP 3.0 with limited AGP 2.0 compatibility. The electrical characteristics are supported for AGP 3.0 (0.8 V swing) and the AGP 2.0 (1.5 V swing). The GMCH may be operated in 1X and 4X for AGP 2.0 mode at 1.5 V; 3.3 V electrical characteristics are not supported.

The GMCH has a 32 deep AGP request queue. The GMCH integrates two fully-associative 10 entry Translation Look-aside Buffer. This 20 entry buffer is used for both reads and writes.

The GMCH multiplexes an AGP interface with two DVO ports. When an external AGP device is utilized, the multiplexed DVO ports are not available as the GMCH's IGD will be disabled. For more information on the multiplexed DVO interface, see Section 5.5.2.

See the AGP Revision 3.0 specification for additional details about the AGP interface.

5.3.1 GMCH AGP Support

Table 27. AGP Support Matrix

Parameter	AGP 3.0	AGP 2.0	Comments
Data Rate	4X or 8X	4X, or 1X	GMCH does not Support AGP 2X
Electricals	0.8 V swing, parallel terminated	1.5 V swing serial terminated	
Signal Polarity	Most control signals active high	Most control signals active low	This change was necessary to eliminate current flow in the idle state. Parallel termination has a large current flow for a high level.
Hi / Low priority commands	Only low priority (renamed Async)	High and low priority commands supported.	High priority does not have a good usage model.
Strobe Protocol	Strobe First – Strobe Second Protocol	Strobe – Strobe# protocol.	
Long transactions	Removed	Supported	
PIPE# support	No	Yes	SBA required for AGP 3.0
Calibration Cycle	Required	No	New to AGP 3.0.
Dynamic Bus Inversion	Yes	No	New to AGP 3.0
Coherency	Required for AGP accesses outside of the aperture, and for FRAME-based accesses	Required only for FRAME-based accesses.	

5.3.2 Selecting between AGP 3.0 and AGP 2.0

The GMCH supports both AGP 3.0 and limited AGP 2.0, allowing a “Universal AGP 3.0 motherboard” implementation. Whether AGP 2.0 or AGP 3.0 mode is used is determined by the graphics card installed. An AGP 2.0 card will put the system into AGP 2.0. An AGP 3.0 card will put the system into AGP 3.0 mode. The mode is selected during RESET by a hardware mechanism which is described in Section 5.3.3.1. The mode determines the electrical mode and can not be dynamically changed once the system powers up.

5.3.3 AGP 3.0 Downshift (4X Data Rate) Mode

AGP 3.0 supports both an 8X data rate and a 4X data rate. The purpose of the 4X data rate is to allow a fallback mode when board routing or other reasons make the 8X data rate marginal. Some AGP4X graphics cards currently fall back to a 2X data rate when board layout or other issues arise. This is referred as “downshift” mode. Since AGP 2X is not supported, any card falling back to 2X will be running in a non supported mode. When in AGP 3.0 mode in the 4X data rate, all of the AGP 3.0 protocols are used.

Table 28. AGP 3.0 Downshift Mode Parameters

Parameter	AGP 2.0 Signaling (All Data Rates)	AGP 3.0 Signaling (4X Data Rate)	AGP 3.0 Signaling (8X Data Rate)
Data rate	1X, 4X	4X	8X
VREF level	0.75 V	0.35 V	0.35 V
Signaling	2.0 (1.5 V)	3.0 signaling (0.8 V swing)	3.0 signaling (0.8 V swing)
Polarity of GREQ, GGNT, GDEVSEL, GFRAME, GIRDT, GTRDY, GSTOP, RBF, WBF	Active low	Active high	Active high
Polarity of SBA	normal (111 = idle)	inverted (000 = idle)	inverted (000 = idle)
GCBE polarity	GC/BE#	GC#/BE	GC#/BE
Strobe definition	Strobe Strobe#	StrobeFirst StrobeSecond	StrobeFirst StrobeSecond
DBI used?	No	Disabled on xmit	Yes
PIPE# allowed	Yes	No	No
Commands supported	AGP 2.0 commands	AGP 3.0 commands	AGP 3.0 commands
Isoch supported	No	(Not supported)	No
Calibration cycles included	No	Yes	Yes

5.3.3.1 Mechanism for Detecting AGP 2.0, AGP 3.0, or Intel® DVO

Two new signals are provided in the AGP 3.0 specification to allow for detection of an AGP 3.0 capable graphics card by the motherboard and an AGP 3.0 capable motherboard by the graphics card respectively.

The signals are:

- GC_DET#: Pulled low by an AGP 3.0 graphics card; left floating by an AGP 2.0 graphics card.
- MB_DET#: Pulled low by an AGP 3.0 motherboard; left floating by an AGP 2.0 motherboard.

The 3.0 capable motherboard uses GC_DET# to determine whether to generate VREF of 0.75 V (floating GC_DET# for 2.0 graphics card), or 0.35 V (GC_DET# low) to the graphics card. This is sent to the graphics card via the VREFCG pin on the AGP connector.

Similarly, the 3.0 capable graphics card uses MB_DET# to determine whether to generate VREF of 0.75 V (floating MB_DET# on 2.0 motherboard), or 0.35 V (MB_DET# low) to the motherboard. The card could also use this pin as a strap to determine 2.0 or 3.0 mode. Note, however, that VREFGC is not used by the GMCH. Instead, VREFCG is used to account for the DVO ADD card, where VREFGC is not connected.

The GMCH detects whether the graphics card connected is AGP 2.0 or AGP 3.0 via the voltage level driven into the GVREF pin (0.35 V{< 0.55 V} = AGP 3.0; 0.75 V{>0.55 V} = AGP 2.0). GVREF is driven by VREFCG on the motherboard.

An ADD card pulls the GPAR/ADD_DETECT# pin low and leaves GC_DET# pin unconnected. Since GC_DET# is unconnected, the VREF generator generates an AGP 2.0 compliant voltage, 0.75 V to the GVREF pin. This is detected by the VREF voltage comparator, which drives a “live” AGP 3.0 mode detect signal to GPAR (and other AGP I/O buffers), as well as the pull-up/pull-

down controlling logic on the AGP I/O buffers, selecting the weak pull-up on GPAR. On the assertion of PWROK, a 0 is detected on the GPAR pin and is latched into the GMCHCFG.3 strap bit to select DVO over AGP. At the assertion of PWROK, the AGP 3.0 detect signal (value 0) is also latched into the AGPSTAT.3 strap bit. Note that a 0 in AGP 3.0 detect is meaningless when DVO is selected.

An AGP 2.0 card tri-states GPAR and leaves the GC_DET# pin unconnected. GVREF = 0.75 V and GPAR is weakly pulled high during assertion of PWROK; a 1 is latched into GMCHCFG.3 strap bit to select AGP. AGP 3.0 detect value latched on the assertion of PWROK = 0 indicating AGP 2.0 mode.

An AGP 3.0 card terminates GPAR low, and pulls GC_DET# low, causing the VREF generator to drive 0.35 V to GVREF. Note that during the assertion of PWROK, GPAR = 0 and AGP 3.0 detect = 1. To work correctly when AGP 3.0 detect = 1, AGP must be selected over DVO (i.e., when AGP 3.0 detect = 1, AGP/DVO# strap value must also be 1, regardless of the value on GPAR).

Table 29. Pin and Strap Values Selecting Intel® DVO, AGP 2.0, and AGP 3.0

Card Plugged Into AGP Connector	Pull-up/ Termination on GPAR Pin Prior to Assertion of PWROK	GPAR/ ADD_DETECT# value on PWROK Assertion	AGP 3.0 Detect Value on PWROK Assertion	GMCHCFG.3 Strap Bit (AGP/DVO#)	AGPSTAT.3 Strap Bit (AGP 3.0 Detect)
ADD card	pull-up	0	0 (0.75 V)	0	0
AGP 2.0 card	pull-up	1	0 (0.75 V)	1	0
AGP 3.0 card (1)	termination to ground	0	1 (0.35 V)	1	1

NOTE:
1. Difference between GPAR/ADD_DETECT# and GMCHCFG.3 value.

5.3.4 AGP Target Operations

As an initiator, the GMCH does not initiate cycles using AGP enhanced protocols. The GMCH supports AGP target interface to main memory only. The GMCH supports interleaved AGP and PCI transactions. AGP 2.0 and AGP 3.0 support different command types, as indicated in Table 30.

Table 30. AGP 3.0 Commands Compared to AGP 2.0

GC/BE[3:0]# (GC#/BE[3:0]) Encoding	APG 2.0 Command	AGP 3.0 Command
0000	Read (Low Priority)	Read (Asynchronous)
0001	Read (High Priority)	Reserved
0010	Reserved	Reserved
0011	Reserved	ISOCH Read (NOT SUPPORTED)
0100	Write (Low Priority)	Write (Asynchronous)
0101	Write (High Priority)	Reserved
0110	Reserved	ISOCH Write, Unfenced (NOT SUPPORTED)
0111	Reserved	ISOCH Write, Fenced (NOT SUPPORTED)
1000	Long Read (Low Priority)	Reserved
1001	Long Read (High Priority)	Reserved
1010	Flush (Low Priority)	Flush
1011	Reserved	Reserved)
1100	Fence (Low Priority)	Fence (for reads and writes)
1101	Reserved (was DAC cycle)	Reserved (was DAC cycle)
1110	Reserved	Isoch Align (NOT SUPPORTED)
1111	Reserved	Reserved

5.3.5 AGP Transaction Ordering

High priority reads and writes are not checked for conflicts between themselves or normal priority reads and writes. AGP commands (delivered via PIPE# or SBA, not FRAME#) snoop the global SDRAM write buffer.

Table 31. Supported Data Rates

Data Rate	Signaling Level		
	0.8 V	1.5 V	3.3 V
PCI-66	Yes	Yes	No
1X AGP	Yes	Yes	No
2X AGP	No	See Note	No
4X AGP	Yes	Yes	No
8X AGP	Yes	No	No

NOTE: AGP 2X is **not** supported on the GMCH.

5.3.6 Support for PCI-66 Devices

The GMCH's AGP interface may be used as a PCI-66 MHz interface with the following restrictions:

1. Support for 1.5 V operation only.
2. Support for only one device. The GMCH does not provide arbitration or electrical support for more than one PCI-66 device.
3. The PCI-66 device must meet the AGP 2.0 electrical specification.
4. The GMCH does not provide full PCI-to-PCI bridge support between AGP/PCI and hub interface. Traffic between AGP and hub interface is limited to hub interface-to-AGP memory writes.
5. LOCK# signal is not present. Neither inbound nor outbound locks are supported.
6. SERR# / PERR# signals are not present.
7. 16-clock Subsequent Data Latency timer (instead of 8).

5.3.7 8X AGP Protocol

The GMCH supports 1X and 4X AGP operation in 2.0 mode, and 4X and 8X in 3.0 mode. Bit 3 of the AGP status register is set to 0 in AGP 2.0 mode, and 1 in APG 3.0 mode. The GMCH indicates that it supports 8X data transfers in AGP 3.0 mode through RATE[1] of the AGP status register. When DATA_RATE[1] of the AGP Command Register is set to 1 during system initialization, the GMCH will perform AGP read and write data transactions using 8X protocol. This bit is set once during initialization and the data transfer rate cannot be changed dynamically.

The 8X data transfer protocol provides 2.1 GB/s transfer rates. In 8X mode, 32 bytes of data are transferred during each 66 MHz clock period. The minimum throttleable block size remains four, 66 MHz clocks, which means 128 bytes of data is transferred per block.

5.3.7.1 Fast Writes

The Fast Write (FW) transaction is from the core logic to the AGP master acting as a PCI target. This type of access is required to pass data/control directly to the AGP master instead of placing the data into main memory and then having the AGP master read the data. For 1X transactions, the protocol simply follows the PCI bus specification. However, for higher speed transactions (4X or 8X), FW transactions follow a combination for PCI and AGP bus protocols for data movement.

The GMCH only supports the AGP 1.5 V connector, which permits a 1.5 V AGP add-in card to be supported by the system.

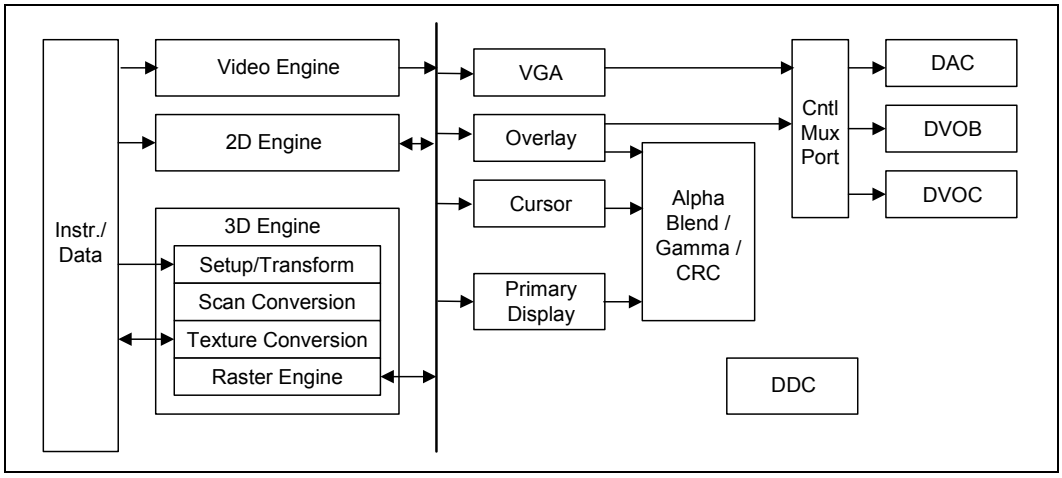
5.3.7.2 PCI Semantic Transactions on AGP

The GMCH accepts and generates PCI semantic transactions on the AGP bus. The GMCH guarantees that PCI semantic accesses to SDRAM are kept coherent with the processor caches by generating snoops to the processor bus.

5.4 Integrated Graphics Controller

The GMCH provides a highly integrated graphics accelerator and chipset while allowing a flexible integrated system graphics solution.

Figure 13. GMCH Graphics Block Diagram



High bandwidth access to data is provided through the graphics and system memory ports. The GMCH can access graphics data located in system memory at 2.1 GB/s – 6.4 GB/s (depending on memory configuration). The GMCH uses Intel's Direct Memory Execution model to fetch textures from system memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

The GMCH is able to drive an integrated DAC, and/or two DVO ports (multiplexed with AGP) capable of driving an ADD card. The DAC is capable of driving a standard progressive scan analog monitor with resolutions up to 2048x1536 @ 75Hz. The DVO ports are capable of driving a variety of TV-Out, TMDS, and LVDS transmitters.

As seen in Figure 13, the Internal Graphics Device contains several types of components. The major components in the IGD are the engines, planes, pipes and ports. The GMCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines. The IGD's 2D and 3D engines are fed with data through the memory controller. The output of the engines are surfaces sent to memory, which are then retrieved and processed by the GMCH's planes.

The GMCH contains a variety of planes, such as display, overlay, cursor, and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The GMCH has a single display pipe, which means that the GMCH can only support a single display stream. A port is the destination for the result of the pipe. The GMCH contains three display ports, 1 analog (DAC), and two digital (DVO ports B and C). The ports will be explained in more detail in Section 5.5.

The entire IGD is fed with data from its memory controller. The GMCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR266), the rest of the IGD will also be affected.

5.4.1 3D Engine

The 3D engine of the GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports perspective-correct texture mapping, multitextures, bump-mapping, cubic environment maps, bilinear, trilinear and anisotropic MIP mapped filtering, Gouraud shading, alpha-blending, vertex and per pixel fog and Z/W buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will significantly outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

5.4.1.1 Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, GMCH maintains sub-pixel accuracy.

3D Primitives and Data Formats Support

The 3D primitives rendered by GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans and polygons. In addition to this, GMCH supports the Microsoft DirectX* Flexible Vertex Format (FVF), which enables the application to specify a variable length of parameter list obviating the need for sending unused information to the hardware. Strips, Fans, and Indexed Vertices, as well as FVF, improves delivered vertex rate to the setup engine significantly.

Pixel Accurate "Fast" Scissoring and Clipping Operation

The GMCH supports 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the scissor rectangle, avoiding processing pixels that fall outside the rectangle. GMCH's clipping and scissoring in hardware reduce the need for software to clip objects, and thus improves performance. During the setup stage, the GMCH clips objects to the scissor window.

A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle needs to be pixel accurate, and independent of line and point width. The GMCH supports a single scissor box rectangle that can be enabled or disabled. The rectangle is defined as an Inclusive box. Inclusive is defined as "draw the pixel if it is inside the scissor rectangle".

Depth-Bias

The GMCH supports source depth biasing in the setup engine, the depth bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The depth bias value is added to the z or w value of the vertices. This is used for coplanar polygon priority. If two polygons are to be rendered that are coplanar, due to the inherent precision differences induced by unique x, y and z values, there is no guarantee which polygon will be closer or farther. By using depth bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

Backface Culling

As part of the setup, the GMCH discards polygons from further processing, if they are facing away from or towards the user's viewpoint. This operation, referred to as "Back Face Culling" is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive. This can be enabled or disabled by the driver. This is referred to as "Back Face Culling."

5.4.1.2 Scan Converter

The Scan Converter takes the vertex and edge information that is used to identify all pixels that are affected by features being rendered. It works on a per-polygon basis.

Pixel Rasterization Rules

The GMCH supports both OpenGL and D3D pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry is used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

5.4.1.3 2D Functionality

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

5.4.1.4 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear and bilinear interpolation), and YUV-to-RGB conversions.

Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

Texture Formats and Storage

The GMCH supports up to 32 bits of color for textures.

Texture Decompression

DirectX supports Texture Compression to reduce the bandwidth required to deliver textures. As the textures' average sizes gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism to compress textures. Supported Texture decompression formats include DXT1, DXT2, DXT3, DXT4, DXT5, and FXT1.

Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For "linear" texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns that occur as a result of the fact that there is very small number of pixels available on screen to contain the data of a high resolution texture map. More subtle effects are observed in animation, where very small primitives blink in and out of view.

Texture Map Filtering

Many texture mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. (A texel is defined as a texture map element). Textures need not be square. Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The GMCH supports 7 types of texture filtering:

1. Nearest (aka Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present).
2. Linear (aka Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel are used. (This is used if only one LOD is present).
3. Nearest MIP Nearest (aka Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel are used.
4. Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel are used (four texels). This is also referred to as Bilinear MIP Mapping.
5. Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel are selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.

6. Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used to minimize the visibility of LOD transitions across the polygon.
7. Anisotropic MIP Nearest (Anisotropic Filtering): This is used if many LODs are present. The nearest LOD-1 level will be determined for each of four sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.

Both D3D (DirectX 6.0) and OGL (Revision1.1) allow support for all these filtering modes.

Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP Maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

Bi-Cubic Filter (4x4 Programmable Texture Filter)

A bi-cubic texture filter can be selected instead of the bilinear filter. The implementation is of a 4x4 separable filter with loadable coefficients. A 4x4 filter can be used for providing high-quality up/down scaling of rendered 2D or 3D rendered images.

Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing the processor load. There are several methods to generate environment maps (e.g., spherical, circular, and cubic). The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping requires a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

5.4.1.5 Raster Engine

The Raster Engine is where the color data (e.g., fogging, specular RGB, texture map blending, etc.) is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the Texture Engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted that will determine whether the Frame and Depth Buffers will be updated with the new pixel values.

Texture Map Blending

Multiple textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports using a texture coordinate set to access multiple texture maps. State variables in multiple texture are bound to texture coordinates, texture map or texture blending.

Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated "specular RGB" attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices which apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, RGB values from the output of the map blending are added to values for R_S, G_S, B_S on a component by component basis.

Color Shading Modes

The raster engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (red, green, blue), Specular (R, G, B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex's attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

OpenGL and D3D use a different vertex to select the flat shaded color. This vertex is defined as the "provoking vertex". In the case of strips/fans, after the first triangle, attributes on every vertex that define a primitive is used to select the flat color of the primitive. A state variable is used to select the "flat color" prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (red, green, blue). Specular (RGB), fog, and alpha to the pixel, where each vertex color has a different value.

All the attributes can be selected independently to one of the shading mode by setting the appropriate value state variables.

Color Dithering

Color Dithering helps to hide color quantization errors. Color Dithering takes advantage of the human eye's propensity to "average" the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5- or 6- bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed on the components.

Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects (e.g., low visibility conditions in flight simulator-type games). It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (less polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating

the color of an object with the fog color as a function of distance. The greater the distance, the higher the density (lower visibility for distant objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (e.g., a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit.

Alpha Blending (Frame Buffer)

Alpha Blending adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color ($R_SG_SB_S$) and alpha (A_S) component with a destination pixel color ($R_DG_DB_D$) and alpha (A_D) component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.

DXn and OGL Logic Ops

Both APIs provide a mode to use bitwise ops in place of alpha blending. This is used for rubber-banding (i.e., draw a rubber band outline over the scene using an XOR operation). Drawing it again restores the original image without having to do a potentially expensive redraw.

Color Buffer Formats: 8-, 16-, or 32-bits per pixel (Destination Alpha)

The Raster Engine supports 8-bit, 16-bit, and 32-bit Color Buffer Formats. The 8-bit format is used to support planar YUV420 format, which is used only in motion compensation and arithmetic stretch format. The bit format of Color and Z will be allowed to mix.

The GMCH supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer of the GMCH contains at least two hardware buffers—the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing. This also speeds up the display process over a single buffer. Additionally, triple back buffering is also supported. The Instruction set of the GMCH provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

Depth Buffer

The Raster Engine is able to read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values as opposed to only 64 K with a 16-bit Z-buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when w (or eye-relative z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, allowing applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point.

The GMCH supports a flexible format for the floating-point W buffer, wherein the number of exponent bits is programmable. This allows the driver to determine variable precision as a function of the dynamic range of the W (screen-space Z) parameter.

The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

Stencil Buffer

The Raster Engine provides 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects (e.g., decals, outlining, shadows, and constructive solid geometry rendering).

Projective Textures

The GMCH supports two, simultaneous projective textures at full rate processing, and four textures at half rate. These textures require three floating point texture coordinates to be included in the FVF format. Projective textures enable special effects (e.g., projecting spot light textures obliquely onto walls, etc.).

5.4.2 2D Engine

The GMCH contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions (e.g., Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs make use of the 3D renderer.

GMCH VGA Registers

The 2D registers are a combination of registers defined by IBM when the Video Graphics Array (VGA) was first introduced and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

Logical 128-bit Fixed BLT and 256-bit Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between:

- cacheable and system memory and frame buffer memory
- frame buffer memory and frame buffer memory
- within system memory.

Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers, move the data specified to the destination. Transparent transfers, compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT and STRBLT operations, permitting software to set up instruction buffers and use batch processing. The GMCH can perform hardware clipping during BLTs.

5.4.3 Video Engine

Hardware Motion Compensation

The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward, or bidirectionally) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements motion compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The motion compensation functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally supports the following input formats:

- YUV420 planar

Sub-Picture Support

Sub-picture is used for two purposes; one is Subtitles for movie captions, etc., which are superimposed on a main picture, and another is for Menus to provide some visual operation environments for the user of the player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called “Subtitle” because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications; for example, as Subtitles in different languages or other information to be displayed.

There are two kinds of Menus, the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can use four methods when dealing with sub-pictures. The flexibility enables the GMCH to work with all sub-picture formats.

5.4.4 Planes

A plane consists of a rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

5.4.4.1 Cursor Plane

The cursor plane is one of the simplest display planes. With a few exceptions, this plane has a fixed size of 64x64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.

5.4.4.2 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external video capture device) or data delivered by the processor, with the graphics data on the screen. The source data can be mirrored horizontally, vertically, or both.

Source/Destination Color Keying/ChromaKeying

Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color keying/ChromaKeying can be used to handle occluded portions of the overlay window on a pixel by pixel basis that is actually an underlay. Destination ChromaKeying would only be used for YUV passthrough to TV. Destination color keying supports a specific color (8- or 15-bit) mode as well as 32-bit alpha blending.

Source color keying/ChromaKeying is used to handle transparency based on the overlay window on a pixel-by-pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

Gamma Correction

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

YUV-to-RGB Conversion

The format conversion can be bypassed in the case of RGB source data. The format conversion assumes that the YUV data is input in the 4:4:4 format and uses the full range scale.

Maximum Resolution and Frequency

The maximum frequency supported by the overlay logic is 170 MHz. The maximum resolution is dependent on a number of variables.

Deinterlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.

Dynamic Bob and Weave. Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to deinterlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as Weaving. This is the best solution for images with little motion; however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or “Bob” interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion; however, it will have reduced spatial resolution in areas that have no motion and introduces *jaggies*. In absence of any other deinterlacing, these form the baseline and are supported by the GMCH.

Scaling Filter and Control

The scaling filter has three vertical taps and five horizontal taps. Arbitrary scaling (per pixel granularity) for any video source (YUV422 or YUV420) format is supported.

The overlay logic can scale an input image up to 1600X1200 with no major degradation in the filter used as long as the maximum frequency limitation is met. Display resolution and refresh rate combinations, where the dot clock is greater than the maximum frequency, require the overlay to use pixel replication.

5.4.5 Pipes

The display consists of a single pipe. The pipe can operate in a single-wide or "double-wide" mode at 2X graphics core clock though, it is effectively limited by its display port (350 MHz maximum). The primary display plane and the cursor plane provides a "double wide" mode to feed the pipe.

Clock Generator Units (DPLL)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25–350 MHz. Accuracy for VESA timing modes is required to be within ± 0.5%.

The DPLL can take a reference frequency from the external reference input (e.g., DREFCLK) for the TV clock input (DVOBC_CLKIN).

5.5 Display Interfaces

The GMCH has three display ports; one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure, and/or determine the capabilities of an external device.

The GMCH has one dedicated display port, the analog port. DVO B and DVO C are multiplexed with the AGP interface and are not available if an external AGP graphics device is in use. When a system uses an AGP connector, DVO ports B and C can be used via an ADD (AGP Digital Display) card. Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

The GMCH's analog port uses an integrated 350 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

The GMCH's DVO ports are each capable of driving a 165 MHz pixel clock. Each port is capable of driving a digital display up to 1600x1200 @ 60Hz. When in dual-channel mode, the GMCH can drive a flat panel up to 2048x1536 @ 60Hz or dCRT/HDTV up to 1920x1080 @ 85Hz.

The GMCH is compliant with *Digital Visual Interface (DVI) Specification, Revision 1.0*. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

Table 32. Display Port Characteristics

Parameter		Analog	Digital Port B	Digital Port C
Interface Protocol		RGB DAC	DVO 2.0	DVO 2.0
SIGNALS	HSYNC	Yes Enable/Polarity		
	VSYNC	Yes Enable/Polarity		
	BLANK	No	Yes(1)	Yes(1)
	STALL	No	Yes	Yes
	Field	No	Yes	Yes
	Display_Enable	No		Yes(1)
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1		
Pixel Aspect Ratio		Square(1)		
Voltage		RGB 0.7 V p-p	1.5 V	1.5 V
Clock		NA	Differential	
Max Rate		350 Mpixel	165/330 Mpixel	
Format		Analog RGB	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1/DDC2B	DDC2B	
External Device		No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-I	DVI/CVBS/S-Video/Component/SCART	

NOTE:
1. Single signal software selectable between display enable and Blank#.

5.5.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT-based monitor with a VGA connector. Display devices (e.g., LCD panels with analog inputs) may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 33. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	3.3 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. GMCH's integrated 350 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 75 Hz. Three 8-bit DACs provide the RED, GREEN, and BLUE signals to the monitor.

Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support is included.

VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDCA_CLK and DDCA_DATA to communicate with the analog monitor. The GMCH generates these signals at 2.6 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals. This allows higher speed transactions (up to 400 kHz) on theses lines than previous software centric 'bit-bashing' techniques.

5.5.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two DVO ports that are multiplexed on the AGP interface. When an external AGP graphics accelerator is not present, the GMCH can use the multiplexed DVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD card that is designed to plug in to a 1.5 V AGP connector.

5.5.2.1 Digital Display Channels – Intel® DVOB and Intel® DVOC

The GMCH has the capability to support digital display devices through two DVO ports multiplexed with the AGP signals. When an external graphics accelerator is used via AGP, these DVO ports are not available. Refer to Section 2.5.6 for a detailed description of the shared DVO signals.

The shared DVO ports each support a pixel clock up to 165 MHz and can support a variety of transmission devices. When using a 24-bit external transmitter, it will be possible to pair the two DVO ports in dual-channel mode to support a single digital display with higher resolutions and refresh rates. In this mode, the GMCH is capable of driving a pixel clock up to 330 MHz.

The GMCH multiplexes an ADD_DETECT signal with the GPAR signal on the AGP bus. This signal acts as a strap and indicates whether the interface is in AGP or DVO mode. The GMCH has an internal pull-up on this signal that will naturally pull it high. If an ADD card is present, the signal will be pulled low on the ADD card and the AGP/DVO multiplex select bit in the GMCHCFG register will be toggled to DVO mode. Motherboards that do not use an AGP connector should have a pull-down resistor on ADD_DETECT if they have digital display devices connected to the AGP/DVO interface.

5.5.2.1.1 ADD Card

When an 865G chipset platform uses an AGP connector, the multiplexed DVO ports may be used via an ADD card. The ADD card will be designed to fit a standard 1.5 V AGP connector.

5.5.2.1.2 TMDS Capabilities

The GMCH is compliant with *Digital Visual Interface (DVI) Specification, Revision 1.0*. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT). When combining the two multiplexed DVO ports, the GMCH can drive a flat panel up to 2048x1536 or a dCRT/HDTV up to 1920x1080. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH, however, provides unscaled mode where the display is centered on the panel.

5.5.2.1.3 LVDS Capabilities

The GMCH can use the multiplexed DVO ports to drive an LVDS transmitter. The flat panel is a fixed resolution display. While the GMCH supports panel fitting in the transmitter, receiver, or an external device, it has no native panel fitting capabilities. The GMCH, however, provides unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the DVOB (or C)_STL pin, which is multiplexed with DVOB (or C)_FLD.

5.5.2.1.4 TV-Out Capabilities

While traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For this reason, the GMCH considers a TV-Output to be a digital display. GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH generates the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed DVO interface is 1.5 V, care should be taken to ensure that the TV encoder is operational at that signaling voltage.

A NTSC/PAL/SECAM display on the TV-Out port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided.

The TV-Out interface on the GMCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on DVOBC_CLKINT# that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required. Data is driven to the encoder across 12 data lines, along with a clock pair and sync signals. The encoder can expect a continuous flow of data from GMCH because data will not be throttled.

Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation is that the overlay source data is in the YUV format and bypasses the conversion to RBG as it is sent to the TV port directly.

Sync Lock Support

Sync lock to the TV is accomplished using the external encoders PLL combined with the display phase detector mechanism. The availability of this feature is determined by which external encoder is in use.

Analog Content Protection

Analog content protection is provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

Connectors

Target TV connectors support includes the CVBS, S-Video, Component, and SCART connectors. The external TV encoder in use will determine the method of support.

5.5.2.1.5 DDC (Display Data Channel)

The multiplexed digital display interface uses the MDVI_CLK and MDVI_DATA signals to interrogate the panel. The GMCH supports the DDC2B protocol to initiate the transfer of EDID data. The multiplexed digital display interface uses the M_I^2C bus to interrogate the external transmitter. A third set of signals (MDDC_CLK and MDDC_DATA) is available for a variety of purposes. They can be used as a second DDC pair when two TMDS transmitters are used, or as a second I^2C pair if there are multiple devices (e.g., PROM and DVO device) that need I^2C and there is a speed or addressing conflict.

The GMCH implements a hardware GMBus controller that can be used to control these signals. This allows higher speed transactions (up to 400 kHz) on theses lines than was allowed with previous software centric ‘bit-bashing’ techniques.

5.5.2.1.6 Optional High-Speed (Dual-Channel) Interface

The multiplexed digital display ports can operate in either two 12-bit port modes or one 24-bit mode. The 24-bit mode uses the 12-bit DVOC data pins combined with the DVOB data pins to make a 24-bit bus. This doubles the transfer rate capabilities of the port. In the single port case, horizontal periods have a granularity of a single pixel clock; in the double case, horizontal periods have a granularity of two pixel clocks. In both cases, data is transferred on both edges of the differential clock. The GMCH can output the data in a high-low fashion, with the lower 12 bits of the pixel on DVOC and the upper 12 bits of data on DVOB. In this manner, the GMCH transfers an entire pixel per clock edge (2 pixels per clock). In addition to this, the GMCH also can transfer dual-channel data in odd-even format. In this mode, the GMCH transfers all odd pixels on one DVO, and all even pixels on the other DVO. In this format, each DVO will see both the high and low half of the pixel, but will only see half of the pixels transferred. As in high-low mode, 2 full pixels are transferred per clock period. This ordering can be modified through DVO control registers.

5.5.2.1.7 Intel® DVO Modes

In single-channel mode, the order of pixel transmission (high-low vs. low-high) can be adjusted via the data ordering bit of that DVO's control register. As mentioned above, when in dual-channel mode, the GMCH can transmit data in a high-low or odd-even format. In high-low mode, software can choose which half goes to which port. A 0 = DVOB Lo/DVOC Hi, and a 1 = DVOB Hi/ DVOC Lo. In odd/even mode, the odd pixels will always go out to DVOC and even pixels will always go out to DVOB. Which DVO port is even and which is odd **cannot** be switched, but the data order bit can be used to change the active data order within the even and odd pixels. The GMCH considers the first pixel to be pixel zero and will send it out to DVOB.

5.5.3 Synchronous Display

Microsoft Windows* Me, Windows* 2000, and Windows* XP operating systems have enabled support for multi-monitor display. Synchronous mode displays the same information on multiple displays.

Since the GMCH has several display ports available for its single pipe, it can support a synchronous display on 2 or 3 displays, unless one of the displays is a TV. No synchronous display is available when a TV is in use. The GMCH cannot drive multiple displays concurrently (different data or timings). In addition, the GMCH cannot operate in parallel with an external AGP device. The GMCH can, however, work in conjunction with a PCI graphics adapter.

5.6 Power Management

The GMCH power management support includes:

- ACPI supported
- System States: S0, S1 (desktop), S3, S4, S5, C0, C1, C2 (desktop)
- Graphics States: D0, D3
- Monitor States: D0, D1, D2, D3

5.6.1 Supported ACPI States

GMCH supports the following ACPI States:

- Graphics
  - D0 — Full on, display active.
  - D3 Hot — GMCH power on. Display off. Configuration registers, state, and main memory contents retained.
  - D3 Cold — Power off.
- Processor
  - C0 — Full On.
  - C1 — Auto Halt.
  - C2-Desktop — Stop Grant. Clk to processor still running. Clock stopped to processor core.

- System
  - G0/S0 Full On.
  - G1/S1 Stop Grant, Desktop S1, same as C2.
  - G1/S2 Not supported.
  - G1/S3 Suspend to RAM (STR). Power and context lost to chipset.
  - G1/S4 Suspend to Disk (STD). All power lost (except wakeup logic on ICH5).
  - G2/S5 Soft off. Requires total system reboot.
  - G3 Mechanical Off. All power lost (except real time clock).

5.7 Thermal Management

The GMCH implements the following thermal management mechanisms. The mechanisms will manage the read and write cycles of the system memory interface, thus, ensuring that the temperature can return to the normal operating range.

Hardware-Based Thermal Management

The number of hexwords transferred over the DRAM interface are tracked per row. The tracking mechanism takes into account that the DRAM devices consume different levels of power based on cycle type (i.e., page hit/miss/empty). If the programmed threshold is exceeded during a monitoring window, the activity on the DRAM interface is reduced. This helps in lowering the power and temperature.

Software-Based Thermal Management

This is used when the external thermal sensor in the system interrupts the processor to engage a software routine for thermal management.

5.7.1 External Thermal Sensor Interface Overview

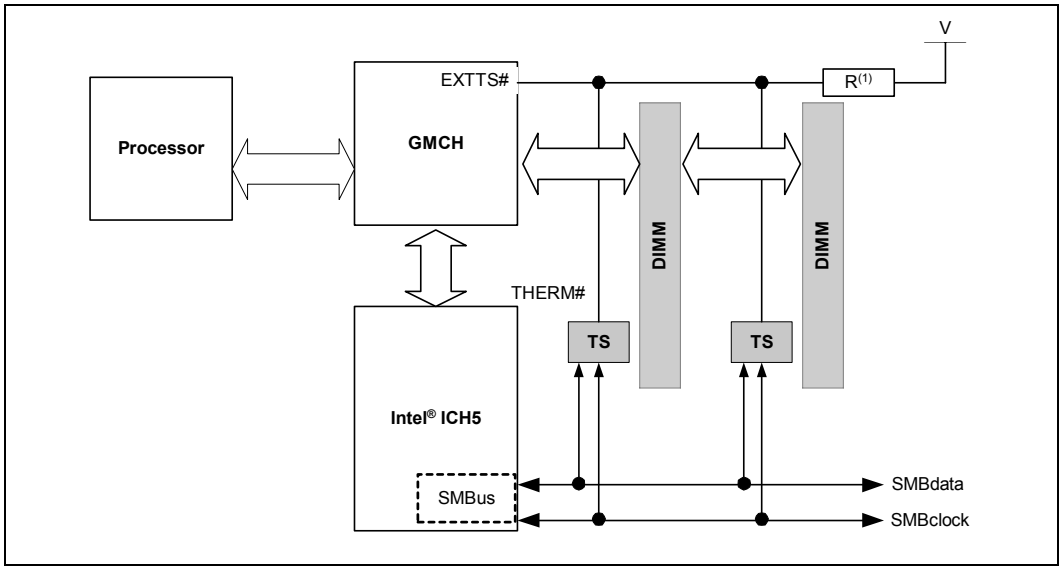
An external thermal sensor with a serial interface (e.g., the National Semiconductor LM77, LM87, or other) may be placed next to DDR DIMM (or any other appropriate platform location), or a remote thermal diode may be placed next to the DIMM (or any other appropriate platform location) and connected to the external thermal sensor.

The external sensor can be connected to the ICH5 via the SMBus interface to allow programming and setup by BIOS software over the serial interface. The external sensor's output should include an active-low open-drain signal indicating an over-temp condition (e.g., LM77 T_CRIT# or INT# in comparator mode). The sensor's output remains asserted for as long as the over-temp condition exists and deasserts when the temperature has returned to within normal operating range. This external sensor output will be connected to the GMCH input (EXTTS#) and will trigger a preset interrupt and/or read-throttle on a level-sensitive basis.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-OR'd together to allow signaling from multiple sensors that are physically separated. Software can, if necessary, distinguish which DIMM(s) is the source of the over-temp through the serial interface. However, since the DIMMs are located on the same memory bus data lines, any GMCH-base read throttle will apply equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain thermal trip output is discouraged; however, it may be possible depending on the size of the pull-up and the voltage of the sensor.

Figure 14. Platform External Sensor



NOTE:
1. External pull-up R is associated with the voltage rail of the GMCH input.

5.7.1.1 External Thermal Sensor Usage Model

There are several possible usage models for an external thermal sensor:

- External sensor(s) used for characterization only, not for normal production
- Sensor on the DIMMs for temperature in OEM platform and use the results to permanently set read throttle values in the BIOS
- Sensor on the GMCH for temperature in OEM platform and use the results to permanently set write throttle values in the BIOS
- External sensor(s) used for dynamic temperature feedback control in production releases
- Sensor on DIMMs, which can be used to dynamically control read throttling
- Sensor on GMCH, which can be used to dynamically control write throttling

The advantage of the characterization model is the Bill-Of-Material (BOM) cost, whereas the potential advantage of the dynamic model is that retail customers may be able to experience higher peak performance since the throttle values are not forced to encompass worse case environmental conditions.

Characterization tools (e.g., CTMI and Maxband) can be made to work either with external or internal sensors.

5.8 Clocking

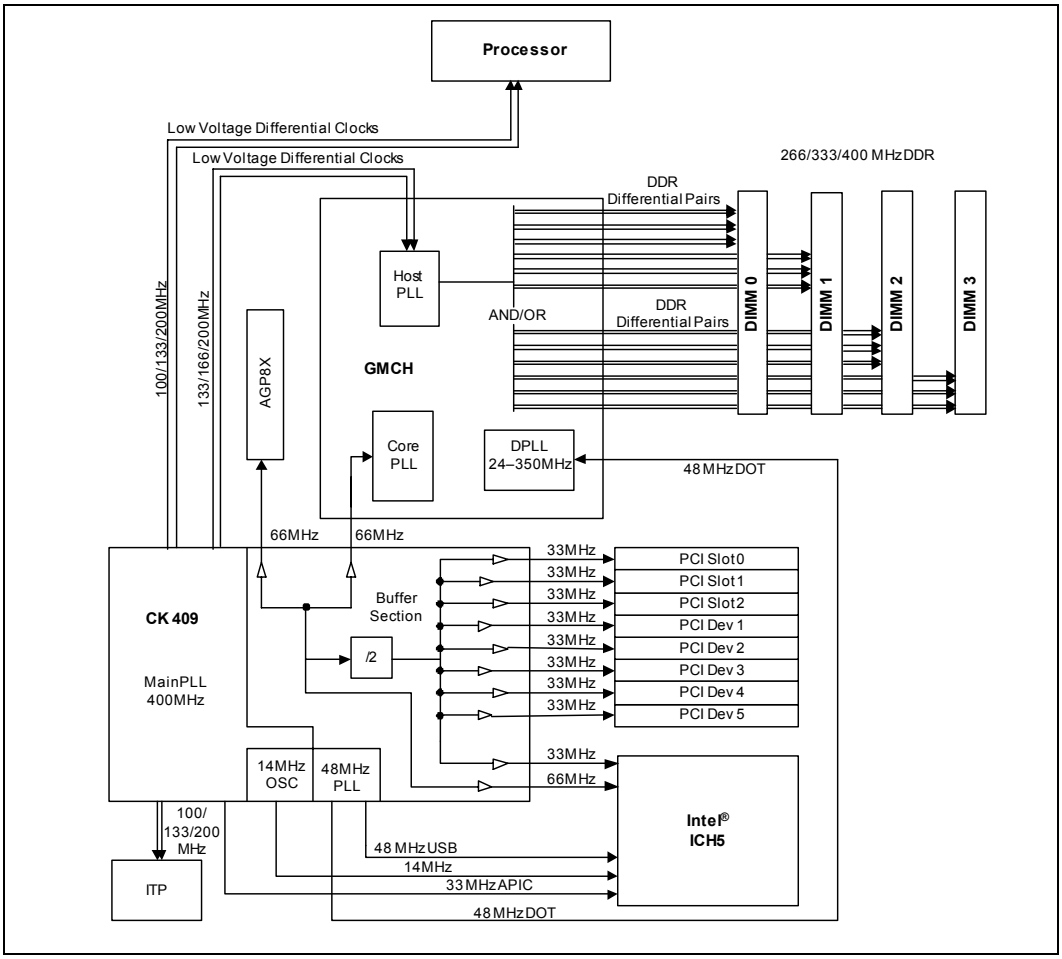
The GMCH has the following clocks:

- 100/133/200 spread spectrum, Low voltage (0.7 V) Differential HCLKP/HCLKN for FSB
- 66.667 MHz, spread spectrum, 3.3 V GCLKIN for Hub Interface and AGP
- 48 MHz, non-spread spectrum, 3.3 V DREFCLK for the Display frequency syntheses
- 12 pairs SDRAM output clocks (SCMCLK_x[5:0] and SCMDCLK_x[5:0]# for both channels A and B)
- Up to 85 MHz, 1.5 V DVOBC_CLKINT for TV-Out mode only.

The GMCH has inputs for a low voltage, differential pair of clocks called HCLKP and HCLKN. These pins receive a host clock from the external clock synthesizer. This clock is used by the host interface and system memory logic (Host Clock Domain). The graphics engine also uses this clock. AGP and hub interface are synchronous to each other and are driven from the 66 MHz clock.

The Graphics core and display interfaces are asynchronous to the rest of the GMCH.

Figure 15. Intel® 865G Chipset System Clocking Block Diagram



This page is intentionally left blank.

Electrical Characteristics 6

This chapter contains the maximum ratings, thermal characteristics, power characteristics, and DC characteristics for the GMCH.

6.1 Absolute Maximum Ratings

Table 34 lists the GMCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the DC characteristics tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 34. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	1.5 V Core Supply	-0.3	1.75	V
VCC_AGP	1.5 V AGP Supply (AGP mode)	-0.3	1.75	V
VCCA_AGP	1.5 V Analog AGP Supply	-0.3	1.75	V
VTT	VTT Supply	-0.3	1.75	V
VCC_DDR	2.6 V DDR System Memory Interface Supply	-0.5	3	V
VCCA_DDR	1.5 V Analog Supply for System Memory DLLs	-0.3	1.75	V
VCC_DAC	3.3 V DAC Supply	-0.3	3.6	V
VCCA_DAC	1.5 V DAC Analog Supply	-0.3	1.65	V
VCCA_DPLL	1.5 V Display PLL Analog Supply	-0.3	1.75	V
VCCA_FSB	1.5 V Host PLL Analog Supply	-0.3	1.75	V

6.2 Thermal Characteristics

Refer to the *Intel® 865G*/865GV/*865PE/865P Chipset Thermal Design Guide* for thermal characteristics.

6.3 Power Characteristics

Table 35. Power Characteristics

Symbol	Parameter	Max	Unit	Notes
I_{VCC}	1.5 V Core Supply Current (integrated graphics)	4.38	A	1,2,3
I_{VCC}	1.5 V Core Supply Current (discrete graphics)	2.88	A	1,2
I_{VCC_AGP}	1.5 V AGP Supply Current (AGP mode)	0.37	A	2
I_{VCC_AGP}	1.5 V AGP Supply Current (DVO mode)	0.18	A	2
I_{VCCA_AGP}	1.5 V Analog AGP Supply Current	0.01	A	
I_{VTT}	VTT Supply Current	1.6	A	
I_{VCC_DDR}	2.6 V DDR System Memory Interface Supply Current	5.7	A	
I_{VCCA_DDR}	1.5 V Analog Supply Current for System Memory DLLs	1.2	A	
I_{VCC_DAC}	3.3 V DAC Supply Current	0.2	A	
I_{VCCA_DAC}	1.5 V DAC Analog Supply Current	0.07	A	
I_{VCCA_DPLL}	1.5 V Display PLL Analog Supply Current	0.01	A	
I_{VCCA_FSB}	1.5 V Host PLL Analog Supply Current	0.05	A	
$I_{VCC\_SUS\_2.6}$	2.6 V Standby Supply Current	0.25	A	

NOTES:
1. The hub interface and CSA interface supply currents are included in the 1.5 V VCC core supply current.
2. VCC and VCC_AGP current levels may happen simultaneously and can be summed into one 1.5 V supply.
3. This specification applies to the GMCH using integrated graphics.

6.4 Signal Groups

The signal description includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates most AGTL+ termination resistors.

AGP AGP interface signals. These signals are compatible with *AGP 2.0 1.5 V and AGP 3.0 0.8V Signaling Environment DC and AC Specifications*. The buffers are not 3.3 V tolerant. (DVO signals use the same buffers as AGP)

HI15 Hub Interface 1.5 V CMOS buffers.

SSTL_2 Stub Series Terminated Logic 2.6 V compatible signals. DDR system memory 2.6 V CMOS buffers.

Miscellaneous 2.6 V and 3.3 V Miscellaneous buffers.

Table 36. Signal Groups (Sheet 1 of 2)

Signal Group	Signal Type	Signals	Notes[1]
AGP Interface Signal Groups (only AGP 3.0 naming convention listed)			
(a)	AGP I/O	GADSTBF[1:0], GADSTBS[1:0], GFRAME, GIRDY, GTRDY, GSTOP, GDEVSEL, GAD[31:0], GCBE[3:0], GPAR/ADD_DETECT, DBI_HI, DBI_LO	
(b)	AGP Input	GSBA[7:0]#, GRBF, GWBF, GSBSTBF, GSBSTBS, GREQ	
(c)	AGP Output	GST[2:0], GGNT	
(d)	AGP Miscellaneous	GVREF, GRCOMP/DVOBCRCOMP, GVSWING	
Hub Interface Signal Groups			
(e)	HI15 I/O	HI[10:0], HISTRS, HISTRF	
(f)	Hub Interface Miscellaneous	HI_SWING, HI_VREF, HI_RCOMP	
CSA Interface Signal Groups			
(e)	HI15 I/O	CI[10:0], CISTRS, CISTRF	
(f)	CSA Interface Miscellaneous	CI_SWING, CI_VREF, CI_RCOMP	
Host Interface Signal Groups			
(g)	AGTL+ I/O	ADS#, BNR#, DBSY#, DINV[3:0]#, DRDY#, HA[31:3]#, HADSTB[1:0] #, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HIT#, HITM#, HREQ[4:0]#, PROCHOT#	
(h)	AGTL+ Input	HLOCK#	
(i)	AGTL+ Output	BPRI#, BREQ0#, CPURST#, DEFER#, HTRDY#, RS[2:0]#	
(j)	CMOS Host Clock Input	HCLKP, HCLKN	
(k)	Host Miscellaneous	HDVREF[2:0], HDRCOMP, HDSWING	
DDR Interface Signal Groups			
(l)	DDR SSTL_2 I/O	SDQ_A[63:0], SDQ_B[63:0], SDQS_A[7:0], SDQS_B[7:0]	
(m)	DDR SSTL_2 Output	SDM_A[7:0], SDM_B[7:0], SCMDCLK_A[5:0], SCMDCLK_B[5:0], SCMDCLK_A[5:0]#, SCMDCLK_B[5:0]#, SMAA_A[12:0], SMAA_B[12:0], SMAB_A[5:1], SMAB_B[5:1], SBA_A[1:0], SBA_B[1:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SCS_A[3:0]#, SCS_B[3:0]#, SCKE_A[3:0], SCKE_B[3:0]	
(v)	DDR RCOMP	SMXRCOMP, SMYRCOMP	
(n)	DDR Miscellaneous[2]	SMXRCOMPVOL, SMXRCOMPVOH, SMYRCOMPVOL, SMYRCOMPVOH, SMVREF_A, SMVREF_B	

Table 36. Signal Groups (Sheet 2 of 2)

Signal Group	Signal Type	Signals	Notes[1]
DAC Signal Groups			
(o)	Display Output	VSYNC, HSYNC	
(p)	Display Analog Outputs	RED, GREEN, BLUE, RED#, GREEN#, BLUE#	
(q)	Display Miscellaneous	REFSET	
DVO Signal Groups			
(r)	DVOx Input	DVOBC_CLKINT, DVOx_FLD/STL, DVOBC_INTR#	
(s)	DVOx Output	DVOx_CLK, DVOx_CLK#, DVOx_D[11:0], DVOx_HSYNC, DVOx_VSYNC, DVOx_BLANK#	
Reset and Miscellaneous Signal Groups			
(t)	2.6 V Miscellaneous Input (3.3 V tolerant) LVTTL	RSTIN#, PWROK, EXTTS#	
(o)	3.3 V Miscellaneous I/O	DDCA_CLK, DDCA_DATA	
(w)	FSB Select Input	BSEL[0:1]	
(x)	Clocks LVTTL	GCLKIN, DREFCLK	

NOTES:
1. For details on BSEL[1:0] pin electrical requirements, see the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide*.
2. For additional details on SMXRCOMP, SMYRCOMP, SMXRCOMPVOL, SMXRCOMPVOH, SMYRCOMPVOL, SMYRCOMPVOH pin electrical requirements, see the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide*.

6.5 DC Parameters

All DC operating conditions are specified at the pin unless otherwise specified.

Table 37. DC Operating Characteristics (Sheet 1 of 2)

Signal Name	Parameter	Min	Nom	Max	Unit
I/O Buffer Supply Voltage					
VCC	Core Voltage	1.425	1.5	1.575	V
VCC_AGP	AGP I/O Voltage	1.425	1.5	1.575	V
VCCA_AGP	AGP Analog Supply Voltage	1.425	1.5	1.575	V
VTT (Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process)	Host AGTL+ Termination Voltage	1.35	1.45	1.55	V
VTT (Intel® Pentium® 4 processor on 90 nm process	Host AGTL+ Termination Voltage	1.14	1.225	1.31	V
VCC_DDR	DDR I/O Supply Voltage	2.5	2.6	2.7	V
VCCA_DDR	DDR Supply Voltage	1.425	1.5	1.575	V
VCC_DAC	3.3 V DAC Supply Voltage	3.135	3.3	3.465	V
VCCA_DAC	DAC Supply Voltage	1.425	1.5	1.6	V
VCCA_DPLL	Display PLL Analog Voltage	1.425	1.5	1.575	V
VCCA_FSB	Host PLL Analog Voltage	1.425	1.5	1.575	V
Reference Voltages					
GVREF (2.0)	AGP 2.0 Reference Voltage	1/2 * VCC_AGP_min – 2%	1/2 * VCC_AGP	1/2 * VCC_AGP_max + 2%	V
GVREF (3.0)[4]	AGP 3.0 Reference Voltage	0.2333 * VCC_AGP_min – 0.01	0.2333 * VCC_AGP	0.2333 * VCC_AGP_max + 0.01	V
GVSWING (3.0)[5]	AGP 3.0 Swing Voltage	0.5333 * VCC_AGP_min – 0.05	0.5333 * VCC_AGP	0.5333 * VCC_AGP_max + 0.05	V
HI_VREF[6,7]	Hub Interface Reference Voltage	0.343	0.35	0.357	V
HI_SWING[6,8]	Hub Interface Compensation Reference Voltage	0.784	0.8	0.816	V
CI_VREF[9,10]	CSA Interface Reference Voltage	0.343	0.35	0.357	V
CI_SWING[9,11]	CSA Interface Compensation Reference Voltage	0.784	0.8	0.816	V
Vsh[1]	GMCH VTT/processor Shared Voltage	(VTT_min + VccCPU_min)/2	(VTT + VccCPU)/2	(VTT_max + VccCPU_max)/2	V

Table 37. DC Operating Characteristics (Sheet 2 of 2)

Signal Name	Parameter	Min	Nom	Max	Unit
HDVREF[2]	Host Reference Voltage	0.63 x Vsh_min – 2%	0.63 x Vsh	0.63 x Vsh_max + 2%	V
HDSWING/ HASWING	Host Compensation Reference Voltage	1/4 x VTT_min – 2%	1/4 x VTT	1/4 x VTT_max + 2%	V
SMXRCOMPVOL[3]/ SMYRCOMPVOL	DDR RCOMP VOL	VCC_DDR_min * (1/4.112) – 2%	VCC_DDR * (1/4.112)	VCC_DDR_max * (1/4.112) + 2%	V
SMXRCOMPVOH[3]/ SMYRCOMPVOH	DDR RCOMP VOH	VCC_DDR_min * (3.112/4.112) - 2%	VCC_DDR * (3.112/4.112)	VCC_DDR_max * (3.112/4.112) + 2%	V
SMVREF	DDR Reference Voltage	0.49 x VCC_DDR_min	0.5 x VCC_DDR	0.51 x VCC_DDR_max	V

NOTES:
1. Refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet* VCC values used to calculate Vsh. For values pertaining to the Pentium 4 processor on 90 nm process, contact your Intel field representative.
2. HDVREF is generically referred to as GTLREF throughout the rest of this chapter.
3. SMXRCOMPVOL/SMYRCOMPVOL and SMXRCOMPVOH/SMYRCOMPVOH have maximum input leakage current of 1 mA.
4. Measured at receiver pad.
5. Standard 50 Ω load to ground.
6. HI_REF and HI_SWING are derived from VCC (nominal VCC = 1.5 V) that is the nominal core voltage for the GMCH. Voltage supply tolerance for a particular interface driver voltage must be within a 5% range of nominal.
7. Nominal value of HI_REF is 0.350 V. The specification is at nominal VCC. Note that HI_REF varies linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the HI_REF specification in addition to the 2% variation of HI_REF in the table.
8. Nominal value of HI_SWING is 0.800 V. The specification is at nominal VCC. Note that HI_SWING varies linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the HI_SWING specification in addition to the 2% variation of HI_SWING in the table.
9. CI_REF and CI_SWING are derived from VCC (nominal VCC = 1.5 V) that is the nominal core voltage for the GMCH. Voltage supply tolerance for a particular interface driver voltage must be within a 5% range of nominal.
10. Nominal value of CI_VREF is 0.350 V. The specification is at nominal VCC. Note that CI_VREF varies linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the CI_VREF specification in addition to the 2% variation of CI_REF in the table.
11. Nominal value of CI_SWING is 0.800 V. The specification is at nominal VCC. Note that CI_SWING varies linearly with VCC; thus, VCC variation (± 5%) must be accounted for in the CI_SWING specification in addition to the 2% variation of CI_SWING in the table.
12. For AC noise components >20 MHz, the maximum allowable noise component at the GMCH is ±180 mV at VCC_nom, +180/-105 mV at VCC_min, and +105/-180 mV at VCC_max. For AC noise components <20 MHz, the sum of the DC voltage and AC noise component must be within the specified DC minimum/ maximum operating range.

Table 38. DC Characteristics (Sheet 1 of 3)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
1.5 V AGP 2.0 (1.5 V signaling) and DVO Interface[6]							
V_{IL_AGP}	(a,b,r)	AGP/DVO Input Low Voltage	–0.5		AGP_VREF – 0.15	V	
V_{IH_AGP}	(a,b,r)	AGP/DVO Input High Voltage	AGP_VREF + 0.15		VCC_AGP + 0.5	V	
V_{OL_AGP}	(a,c,s)	AGP/DVO Output Low Voltage			0.225	V	
V_{OH_AGP}	(a,c,s)	AGP/DVO Output High Voltage	1.275			V	
I_{OL_AGP}	(a,c,s)	AGP/DVO Output Low Current			6.65	mA	@ 0.1* VCC_AGP
I_{OH_AGP}	(a,c,s)	AGP/DVO Output High Current	–4.7			mA	@ 0.85* VCC_AGP
I_{LEAK_AGP}	(a,b,r)	AGP/DVO Input Leakage Current			±25	µA	0<Vin< VCC_AGP
C_{IN_AGP}	(a,b,r)	AGP/DVO Input Capacitance			4	pF	F_C=1 MHz
1.5 V AGP 3.0 (0.8 V signaling) and DVO Interface[6]							
V_{IL_AGP}	(a,b,r)	AGP/DVO Input Low Voltage	–0.3		AGP_VREF – 0.1	V	
V_{IH_AGP}	(a,b,r)	AGP/DVO Input High Voltage	AGP_VREF + 0.10		VCC_AGP	V	
V_{OL_AGP}	(a,c,s)	AGP/DVO Output Low Voltage			0.05	V	I_{out} = 1500 µA
V_{OH_AGP}	(a,c,s)	AGP/DVO Output High Voltage	0.5333 * VCC_AGP_min – 0.05	0.5333 * VCC_AGP	0.5333 * VCC_AGP_ max + 0.05	V	Standard 50 Ω load to ground.
I_{OH_AGP}	(a,c,s)	AGP/DVO Output High Current	14.54		17.78	mA	
I_{LEAK_AGP}	(a,b,r)	AGP/DVO Input Leakage Current			±25	µA	
C_{IN_AGP}	(a,b,r)	AGP/DVO Input Capacitance	1		2.5	pF	F_C=1 MHz
1.5 V Hub Interface[7]							
V_{IL_HI}	(e)	Hub Interface Input Low Voltage	–0.3		HI_VREF – 0.1	V	
V_{IH_HI}	(e)	Hub Interface Input High Voltage	HI_VREF + 0.1		1.2	V	
V_{OL_HI}	(e)	Hub Interface Output Low Voltage			0.05	V	I_{OL}= 1 mA
V_{OH_HI}	(e)	Hub Interface Output High Voltage	0.6		1.2	V	$I_{OUT} = 0.8/R_{TT}$, R_{TT} = 60 Ω
I_{LEAK_HI}	(e)	Hub Interface Input Leakage Current			± 50	µA	
C_{IN_HI}	(e)	Hub Interface Input Capacitance			5	pF	F_C=1 MHz

Table 38. DC Characteristics (Sheet 2 of 3)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
1.5 V CSA Interface[8]							
V_{IL_CI}	(e)	CSA Interface Input Low Voltage	–0.3		CI_VREF – 0.1	V	
V_{IH_CI}	(e)	CSA Interface Input High Voltage	CI_VREF + 0.1		1.2	V	
V_{OL_CI}	(e)	CSA Interface Output Low Voltage			0.05	V	I_{OL}= 1 mA
V_{OH_CI}	(e)	CSA Interface Output High Voltage	0.6		1.2	V	$I_{OUT} = 0.8/R_{TT}$, R_{TT} = 60 Ω
I_{LEAK_CI}	(e)	CSA Interface Input Leakage Current			± 50	µA	
C_{IN_CI}	(e)	CSA Interface Input Capacitance			5	pF	F_C=1 MHz
VTT DC Characteristics							
V_{IL_AGTL+}	(g,h)	Host AGTL+ Input Low Voltage			HDVREF –(0.04*Vsh)	V	
V_{IH_AGTL+}	(g,h)	Host AGTL+ Input High Voltage	HDVREF + (0.04*Vsh)			V	
V_{OL_AGTL+}	(g,i)	Host AGTL+ Output Low Voltage		1/4* Vsh		V	
V_{OH_AGTL+}	(g,i)	Host AGTL+ Output High Voltage	(Vsh-0.1) * 0.95		Vsh	V	
I_{OL_AGTL+}	(g,i)	Host AGTL+ Output Low Current			0.75 * Vshmax / Rttmin	mA	Rtt_{min}=57 Ω
I_{LEAK_AGTL+}	(g,h)	Host AGTL+ Input Leakage Current			± 25	µA	V_{OL}<Vpad<VTT
C_{PAD_AGTL+}	(g,h)	Host AGTL+ Input Capacitance	1		3.3	pF	F_C=1 MHz
2.6 V DDR System Memory							
$V_{IL\_DDR(DC)}$	(l)	DDR Input Low Voltage	–0.1 * VCC_DDR		SMVREF – 0.15	V	
$V_{IH\_DDR(DC)}$	(l)	DDR Input High Voltage	SMVREF + 0.15		VCC_DDR	V	
$V_{IL\_DDR(AC)}$	(l)	DDR Input Low Voltage	–0.1 * VCC_DDR		SMVREF– 0.31	V	
$V_{IH\_DDR(AC)}$	(l)	DDR Input High Voltage	SMVREF + 0.31		VCC_DDR	V	
V_{OL_DDR}	(l,m,v)	DDR Output Low Voltage			0.600	V	With 50 Ω termination to DDR VTT.
V_{OH_DDR}	(l,m,v)	DDR Output High Voltage	VCC_DDR – 0.600			V	With 50 Ω termination to DDR VTT.
I_{OL_DDR}	(l,m)	DDR Output Low Current			25	mA	With 50 Ω termination to DDR VTT.
I_{OH_DDR}	(l,m)	DDR Output High Current	–25			mA	With 50 Ω termination to DDR VTT.
$I_{OL\_DDR\ RCOMP}$	(v)	DDR RCOMP Output Low Current			50	mA	
$I_{OH\_DDR\ RCOMP}$	(v)	DDR RCOMP Output High Current	–50			mA	
I_{Leak_DDR}	(l)	Input Leakage Current			±15	µA	
C_{IN_DDR}	(l)	DDR Input /Output Pin Capacitance			5.5	pF	F_C=1 MHz

Table 38. DC Characteristics (Sheet 3 of 3)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
2.6 V Miscellaneous Signals (3.3 V tolerant)							
V_{IL}	(t)	2.6 V Input Low Voltage			0.4	V	
V_{IH}	(t)	2.6 V Input High Voltage	VCC_DDR – 0.4		VCC_DAC	V	
I_{LEAK}	(t)	2.6 V Input Leakage Current			±50	µA	
C_{IN}	(t)	2.6 V Input Capacitance			5.5	pF	
3.3 V Miscellaneous Signals							
V_{IL}	(o)	3.3V Input Low Voltage			0.4	V	
V_{IH}	(o)	3.3 V Input High Voltage	VCC_DAC – 0.4		VCC_DAC	V	
V_{OL}	(o)	3.3 V Output Low Voltage			0.2	V	
V_{OH}	(o)	3.3 V Output High Voltage	VCC_DAC – 0.2			V	
I_{OL}	(o)	3.3 V Output Low Current			50	mA	@V_{OL} max
I_{OH}	(o)	3.3 V Output High Current	–50			mA	@V_{OH} min
I_{LEAK}	(o)	3.3 V Input Leakage Current			±50	µA	
C_{IN}	(o)	3.3 V Input Capacitance			5.5	pF	
FSB Select Signals							
V_{IL}	(w)	Input Low Voltage			0.4	V	
V_{IH}	(w)	Input High Voltage	0.8			V	
Clocks							
V_{IL}	(x)	Input Low Voltage			0.4	V	
V_{IH}	(x)	Input High Voltage	VCC_DDR – 0.4		VCC_DAC	V	1
I_{LEAK}	(x)	Input Leakage Current			100	µA	
C_{IN}	(x)	Input Capacitance			5.5	pF	
$V_{CROSS(abs)}$	(j)	Absolute Crossing Voltage	0.250	NA	0.550	V	2,3
$V_{CROSS(rel)}$	(j)	Relative Crossing Voltage	0.250 + 0.5 (V_{Havg} – 0.700)		0.550 + 0.5(V_{Havg} – 0.700)	V	3,4,5

NOTES:
1. Absolute max overshoot = 4.5 V
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of HCLKP equals the falling edge of HCLKN.
3. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
4. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
5. VHavg can be measured directly using “Vtop” on Agilent* oscilloscopes and “High” on Tektronix oscilloscopes.
6. Maximum leakage current specification for the GVREF pin is 65 uA. The Maximum leakage current specification for the GVSWING pin is 50 µA. Refer to *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for the resistor divider circuit details that take this specification into account.
7. Maximum leakage current specification for HI_VREF and HI_SWING pins is 50 µA. Refer to 865G/*865GV*/865PE/865P Chipset Platform Design Guide for the resistor divider circuit details that take this specification into account.
8. Maximum leakage current specification for CI_VREF and CI_SWING pins is 50 µA. Refer to 865G/*865GV*/865PE Chipset Platform Design Guide for the resistor divider circuit details that take this specification into account.

6.6 DAC

The GMCH DAC (digital-to-analog converter) consists of three, identical 8-bit DACs to provide red, green, and blue color components.

6.6.1 DAC DC Characteristics

Table 39. DAC DC Characteristics

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	8			Bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1, 2, 4, white video level voltage
Min Luminance		0.000		V	1, 3, 4, black video level voltage
LSB Current		73.2		µA	4, 5
Integral Linearity (INL)	–1.0		+1.0	LSB	1
Differential Linearity (DNL)	–1.0		+1.0	LSB	1
Video channel-channel voltage amplitude mismatch			6	%	6
Monotonicity	Guaranteed				

NOTES:
1. Measured at each R,G,B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude.
3. Min steady-state amplitude.
4. Defined for a double 75 Ω termination.
5. Set by external reference resistor value.
6. Max full-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).

6.6.2 DAC Reference and Output Specifications

Table 40. DAC Reference and Output Specifications

Parameter	Min	Typical	Max	Units	Notes[1]
Reference resistor	124	127	130	Ω	1% tolerance, 1/16 Ω

NOTE:
1. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for details on video filter implementation.

6.6.3 DAC AC Characteristics

Table 41. DAC AC Characteristics

Parameter	Min	Typical	Max	Units	Notes
Pixel Clock Frequency			350	MHz	
R,G,B Video Rise Time	0.57		1.43	ns	(10–90% of black-to-white transition, @ 350 MHz pixel clock)
R,G,B Video Fall Time	0.57		1.43	ns	(90–10% of white-to-black transition, @ 350 MHz pixel clock)
Settling Time			0.86	ns	@ 350 MHz pixel clock
Video channel-to-channel output skew			0.714	ns	@ 350 MHz pixel clock
Overshoot/ Undershoot	–0.084		+0.084	V	Full-scale voltage step of 0.7 V
Noise Injection Ratio			0.5	%	
VCCA_DAC DC to 10 MHz 10 MHz to Pixel Clock Frequency	 VCCA_DAC – 0.3% VCCA_DAC – 0.9%	 VCCA_DAC VCCA_DAC	 VCCA_DAC + 0.3% VCCA_DAC + 0.9%	 V V	(1) DAC Supply Voltage

NOTES:
1. Any deviation from this specification should be validated. Refer to the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide* for the VCCA_DAC filter circuit implementation.

This page is intentionally left blank.

Ballout and Package Information 7

This chapter provides the GMCH ballout and package information.

7.1 GMCH Ballout

The ballout footprint is shown in Figure 16 and Figure 17. These figures represent the ballout arranged by ball number. Table 42 provides the ballout arranged alphabetically by signal name.

Note: The following notes apply to the ballout.

1. For the multiplexed AGP and DVO signals, only the AGP signal names are listed in this chapter. Refer to Section 2.5.7 for the DVO-to-AGP signal mapping.
2. For AGP signals, only the AGP 3.0 signal name is listed. For the corresponding AGP 2.0 signal name, refer to Chapter 2.
3. NC = No Connect.
4. RSVD = These reserved balls should not be connected and should be allowed to float.
5. Shaded cells in Figure 16 and Figure 17 do not have a ball.

Figure 16. Intel® 82865G GMCH Ballout Diagram (Top View—Left Side)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AR	NC		NC	VSS	VCC_DDR		VSS		VSS		VSS		VSS		VCC_DDR	VSS		
AP		RSVD	SDQ_A26	SMAB_A3	SMAB_A4	SDM_A3	SDQ_A25	SDQ_A24	SDQ_A23	SMAA_A8	SDQ_A22	SMAA_A9	SDQS_A2	SDQ_A16	SDQ_A20	SCKE_A3	SDQ_A11	SDQ_A14
AN	RSVD	SDQ_A31		VSS	SMAA_A3	VSS	SDQ_A29	VSS	SDQ_A19	VSS	SMAA_A7	VSS	SMAA_A11	VSS	SMAA_A12	VSS	SCKE_A1	VSS
AM	VSS	SMAB_A2	SDQ_A27		SDQ_A30	SDQS_A3	VSS	SDQ_A28	VSS	SMAB_A5	VSS	SDM_A2	VSS	SDQ_A17	VSS	SCKE_A2	VSS	SDQ_A15
AL	VCCA_DDR	SMAB_A1	SMAA_A1	VSS		SMAA_A4	SMAB_B3	SMAA_A6	SMAB_B4	SMAA_A5	SMAA_B6	SDQ_A18	SMAA_B8	SDQ_A21	SMAA_B11	SCKE_A0	SDQ_B20	SDQ_A10
AK		SCMD CLK_A3#	SCMD CLK_A3	SCMD CLK_A0	SCMD CLK_A0#		SMAA_A2	VSS	SMAA_B4	VSS	SDQ_B24	VSS	SDQ_B19	VSS	SDQ_B21	VSS	SCKE_B0	VSS
AJ	VSS	SMAA_A0	SMAA_ A10	VSS	SMAA_B1	SCMDCLK_ B3		SDM_B3	SDQ_B29	SDQ_B28		SDQ_B22		SMAA_B9		SMAA_B12		SDQ_B15
AH		SBA_A1	VSS	SDQ_A32	SDQ_A36	VSS	SCMD CLK_B3#		SDQS_B3	SDQ_B25		VSS		VSS		VSS		VSS
AG	VSS	SDQ_A33	SDQ_A37	VSS	SMAA_B0	SCMD CLK_B0#	SCMD CLK_B0	VSS	SDQ_B26	VSS	SMAA_B5	VSS	SDQ_B18	VSS	SDQS_B2	VSS	SCKE_B2	VSS
AF		SDQS_A4	VSS	SDQ_A34	SDM_A4	VSS	SMAA_ B10	SDQ_B31	SDQ_B27		VSS	VSS	NC	VSS	SMAA_B7	VSS	SCKE_B1	VSS
AE	VSS	SDQ_A38	SBA_A0	VSS	SDQ_B36	SDQ_B32			SMAB_B1	VSS	VSS	SMAA_B3	SMAB_B5	SDQ_B23	SDM_B2	SDQ_B17	SDQ_B16	SCKE_B3
AD		SDQ_A39	VSS	SDQ_A35	SDQ_A44	VSS	SDQS_B4	VSS	SMAA_B2	SMAB_B2	SDQ_B30							
AC	VSS	SDQ_A40	SAS_A#	VSS	SDM_B4	SDQ_B34			SDQ_B33	VCCA_ DDR	VCCA_ DDR							
AB		SWE_A#	VSS	SDQ_A45	SDQ_A41	VSS	SDQ_B37	VSS	VSS	VSS	VCCA_ DDR							
AA	VCC_DDR	SCS_A0#	SMYRCO MP	VSS	SDQ_B44	SDQ_B40			SDQ_B39	SDQ_B38	SBA_B1							
Y	VSS	SCAS_A#	VSS	SCS_A2#	SCS_A1#	VSS	SDQ_B35	VSS	VSS	VSS	SBA_B0					VCC	VCC	VCC
W		SCS_A3#	SDM_A5	VSS	SCAS_B#	SDQ_B41			SWE_B#	SRAS_B#	SCS_B3#					VCC	VCC	VSS
V		SDQS_A5	VSS	SDQ_A42	SDQ_A43	VSS	SDQ_B45	VSS	VSS	VSS	SCS_B2#					VCC	VSS	VCC
U		SDQ_A46	SDQ_A47	VSS	SDM_B5	SDQS_B5			SDQ_B42	SCS_B0#	SDQ_B46					VCC	VSS	VSS
T	VSS	SDQ_A48	VSS	SDQ_A49	SDQ_A52	VSS	SCS_B1#	VSS	VSS	VSS	SDQ_B43					VCC	VCC	VCC
R	VCC_DDR	SMYRCOM PVOH	SMYRCO MPVOL	VSS	SDQ_B52	SDQ_B49			SDQ_B47	SDQ_B53	NC							
P		SDQ_A53	VSS	SCMD CLK_A5#	SCMDC LK_A5	VSS	SDQ_B48	VSS	VSS	VSS	SDQ_B54							
N	VSS	SCMD CLK_A2#	SCMD CLK_A2	VSS	SCMD CLK_B5	SCMD CLK_B5#			SCMD CLK_B2	SCMD CLK_B2#	SDQ_B60							
M		SDM_A6	VSS	SDQS_A6	NC	VSS	SDM_B6	VSS	VSS	VSS	SDQ_B61							
L	VSS	SDQ_A54	SDQ_A55	SDQ_B55	VSS	SDQ_B51			SDQS_B6	VSS	VSS	VSS	HA5#	HREQ2#	DEFER#	PROCHOT#	HDSTBP1#	HD21#
K		SDQ_A50	VSS	SDQ_A51	SDQ_A60	SDQ_B56	VSS	SDQ_B50	VSS		VSS	HA26#	HA8#	VSS	HIT#	VSS	HDSTBNB_1	VSS
J	VSS	SDQ_A61	SDQ_A56	VSS	SDM_B7	SDQS_B7	SDQ_B62	VSS	HA21#	HA30#	HA11#	HA15#	HREQ1#	VSS	HREQ4#	VSS	HD28#	VSS
H		SDQ_A57	VSS	SDM_A7	SDQS_A7	VSS	SDQ_B57		HA25#	VSS		VSS		VSS		VSS		VSS
G	VSS	SDQ_A62	SDQ_B59	SDQ_B63	VSS	HA29#		VSS	HA22#	HA31#		DRDY#		RS0#		HD16#		HD23#
F		SDQ_A63	SDQ_A59	SDQ_B58	HA28#		HA23#	HA19#	ADS#	VSS	HA16#	VSS	HDVREF	VSS	HD24#	VSS	HD19#	VSS
E	VCC_DDR	SMVREF_A	SDQ_A58	HA27#		HA13#	HA6#	HA24#	DBSY#	NC	HLOCK#	HDRCOMP	HITM#	HD1#	HD27#	HD9#	HD18#	HD8#
D	VSS	HA17#	VSS		VSS	HA4#	VSS	HADSTB1#	VSS	HA3#	VSS	HTRDY#	VSS	HD5#	VSS	HD3#	VSS	HD15#
C	NC	HA20#		HA18#	HA10#	HA9#	HREQ3#	VSS	RS1#	VSS	HD SWING	VSS	NC	VSS	HD7#	VSS	HDSTBNB_0	VSS
B		NC	HA14#	HA7#	HA12#	HADSTB0#	HREQ0#	BNR#	RS2#	BPRI#	NC	BREQ0#	HD0#	HD4#	HD2#	HD6#	HDSTBP0#	HD12#
A	NC		NC	VSS	VCCA_FSB		VSS		VSS		VSS		VSS		VTT	VSS		
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18

Figure 17. Intel® 82865G GMCH Ballout Diagram (Top View—Right Side)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	VSS	VCC_DDR		VSS		VSS		VSS		VCC_DDR		VCC_DDR	VCC_DDR	NC		RSVD	AR
SCMD CLK_A1	SDM_A1	SDQS_A1	SDQ_A8	SDQ_A7	SDM_A0	SDQ_A1	SDQ_A0	SMVREF_B	EXTTS#	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	NC		AP
SCMD CLK_A1#	VSS	SDQ_A13	VSS	SDQ_A3	VSS	SDQS_A0	VSS	SMXRCOMPVOH	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR		VCC_DDR	NC	AN
VSS	SCMD CLK_A4	VSS	SDQ_A9	VSS	SDQ_A2	VSS	SDQ_A4	VSS	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR		VCC_DDR	VCC_DDR	VCC_DDR	AM
SDQ_B11	SCMD CLK_A4#	SCMD CLK_B4#	SDQ_A12	SDQ_B9	SDQ_A6	SDQ_B2	SDQ_A5	SMXRCOMPVOL	SDQ_B4	VCC_DDR	VCC_DDR		HI7	HI5	HI6	VSS	AL
SDQ_B10	VSS	SCMD CLK_B4	VSS	SDQ_B12	VSS	SDQ_B6	VSS	SMX RCOMP	VSS	CI0		HI4	RSTIN#	VSS	HI2		AK
	SDQ_B14		SDQ_B13		NC		SDQ_B0	VSS	RSVD		CISTRF	CISTRS	VSS	HI10	HI8	VSS	AJ
	VSS		VSS		VSS		VSS	CI9		CI1	VSS	HISTRF	HISTRS	VSS	HI9		AH
SCMD CLK_B1#	VSS	SDM_B1	VSS	SDQS_B1	SDQ_B7	SDM_B0	TESTIN#	RSVD	VSS	CI7	CI10	HI3	VSS	HI1	CI_RCOMP	VCCA_AGP	AG
SCMD CLK_B1	VSS	SDQS_B0	VSS	NC	SDQ_B5	VSS		VSS	CI6	CI3	VSS	HI0	CI_VREF	VSS	CI_SWING		AF
SDQ_B8	SDQ_B3	SDQ_B1	PWROK	VSS	VSS	VSS	VSS	CI8			GAD0	GAD3	VSS	HI_SWING	HI_VREF	VSS	AE
						CI2	VSS	VSS	VSS	CI4	VSS	GAD2	HI_RCOMP	VSS	GVREF		AD
						GAD1	CI5	GAD5			GADSTBF0	GADSTBS0	VSS	GVSWING	GRCOMP/ DVOBRCOMP	VSS	AC
						GAD6	VSS	VSS	VSS	GAD7	VSS	GTRDY	GDEVSEL	VSS	GPAR/ ADD_DETECT		AB
						GAD12	GAD4	GAD8			GAD9	GAD10	VSS	GC#/BE2	GAD16	VSS	AA
VCC	VCC					VCCA_AGP	VSS	VSS	VSS	GC#/BE0	VSS	GAD20	GAD17	VSS	GAD18	VCC_AGP	Y
VSS	VCC					GSTOP	GAD11	GAD14			GAD13	GC#/BE1	VSS	GAD22	GAD19		W
VSS	VCC					GIRDY	VSS	VSS	VSS	GAD15	VSS	GADSTBS1	GADSTBF1	VSS	GAD21		V
VCC	VCC					GSBSTBF	GSBA5#	GSBA4#			GFRAME	GSBA6#	VSS	GAD23	GC#/BE3		U
VCC	VCC					GSBSTBS	VSS	VSS	VSS	GSBA7#	VSS	GAD26	GAD25	VSS	GAD24	VSS	T
						VCC	GRBF	GWBF			GSBA0#	GSBA3#	VSS	GSBA2#	GAD27	VSS	R
						VCC	VCC	VSS	VSS	GSBA1#	VSS	GAD29	GAD30	VSS	GAD28		P
						VCC	VCC	VCC			GREQ	GST1	VSS	GST0	GST2	VSS	N
						VCC	VCC	VCC	VCC	GGNT	VSS	DBI_LO	DBI_HI	VSS	GAD31		M
DINV1#	HD33#	HD41#	DINV2#	BSEL0	BSEL1	VCC	VCC	VCC		VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	L
HD31#	VSS	HD38#	VSS	HD43#	VSS	VSS		VCC	VCC	VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP		K
HD20#	VSS	HD32#	VSS	HD34#	VSS	HD44#	VSS	VCC	VCC	VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	J
	VSS		VSS		VSS		HD45#	VSS	VSS	BLUE	GREEN	VSS	GCLKIN	DDCA_DATA	VSS		H
	HD22#		HD29#		HD39#		HD40#	HDSTBP2#	HD46#		BLUE#	GREEN#	DREFCLK	HSYNC	VCC_DAC	VCC_DAC	G
HD17#	VSS	HD25#	VSS	HD35#	VSS	HD36#	VSS	HDSTBN2#	VSS	VTT		VSS	RED	VSS	DDCA_CLK	VSS	F
HD30#	HD14#	HD26#	HD49#	HD37#	HDSTBN3#	HD42#	HD58#	HD47#	CPURST#	VTT	VTT		RED#	VSS	VSYNC	VSS	E
VSS	HD11#	VSS	HD53#	VSS	HDSTBP3#	VSS	HD56#	VSS	HD62#	VTT	VTT	VTT		VSSA_DAC	REFSET	VSS	D
DINV0#	VSS	DINV3#	VSS	HD54#	VSS	HD57#	VSS	HD60#	VSS	HCLKN	VTT	VTT	VSS		VCCA_DAC	NC	C
HD13#	HD10#	HD52#	HD50#	HD48#	HD51#	HD55#	HD59#	HD61#	HD63#	HCLKP	VTT	VTT	VCCA_FSB	VCCA_DPLL	NC		B
	VSS	VTT		VSS		VSS		VSS		VSS	VTT	VTT	VTT	NC			A
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

This page is intentionally left blank.

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
ADS#	F27
BLUE	H7
BLUE#	G6
BNR#	B28
BPRI#	B26
BREQ0#	B24
BSEL0	L13
BSEL1	L12
CI_RCOMP	AG2
CI_SWING	AF2
CI_VREF	AF4
CI0	AK7
CI1	AH7
CI10	AG6
CI2	AD11
CI3	AF7
CI4	AD7
CI5	AC10
CI6	AF8
CI7	AG7
CI8	AE9
CI9	AH9
CISTRF	AJ6
CISTRS	AJ5
CPURST#	E8
DBI_HI	M4
DBI_LO	M5
DBSY#	E27
DDCA_CLK	F2
DDCA_DATA	H3
DEFER#	L21
DINV0#	C17
DINV1#	L17
DINV2#	L14
DINV3#	C15
DRDY#	G24
DREFCLK	G4
EXTTS#	AP8
GAD0	AE6
GAD1	AC11

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
GAD2	AD5
GAD3	AE5
GAD4	AA10
GAD5	AC9
GAD6	AB11
GAD7	AB7
GAD8	AA9
GAD9	AA6
GAD10	AA5
GAD11	W10
GAD12	AA11
GAD13	W6
GAD14	W9
GAD15	V7
GAD16	AA2
GAD17	Y4
GAD18	Y2
GAD19	W2
GAD20	Y5
GAD21	V2
GAD22	W3
GAD23	U3
GAD24	T2
GAD25	T4
GAD26	T5
GAD27	R2
GAD28	P2
GAD29	P5
GAD30	P4
GAD31	M2
GADSTBF0	AC6
GADSTBF1	V4
GADSTBS0	AC5
GADSTBS1	V5
GC#/BE0	Y7
GC#/BE1	W5
GC#/BE2	AA3
GC#/BE3	U2
GCLKIN	H4
GDEVSEL	AB4

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
GFRAME	U6
GGNT	M7
GIRDY	V11
GPAR/ADD_DETECT	AB2
GRBF	R10
GRCOMP/ DVOBRCOMP	AC2
GREEN	H6
GREEN#	G5
GREQ	N6
GSBA0#	R6
GSBA1#	P7
GSBA2#	R3
GSBA3#	R5
GSBA4#	U9
GSBA5#	U10
GSBA6#	U5
GSBA7#	T7
GSBSTBF	U11
GSBSTBS	T11
GST0	N3
GST1	N5
GST2	N2
GSTOP	W11
GTRDY	AB5
GVREF	AD2
GVSWING	AC3
GWBF	R9
HA3#	D26
HA4#	D30
HA5#	L23
HA6#	E29
HA7#	B32
HA8#	K23
HA9#	C30
HA10#	C31
HA11#	J25
HA12#	B31
HA13#	E30
HA14#	B33

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
HA15#	J24
HA16#	F25
HA17#	D34
HA18#	C32
HA19#	F28
HA20#	C34
HA21#	J27
HA22#	G27
HA23#	F29
HA24#	E28
HA25#	H27
HA26#	K24
HA27#	E32
HA28#	F31
HA29#	G30
HA30#	J26
HA31#	G26
HADSTB0#	B30
HADSTB1#	D28
HCLKN	C7
HCLKP	B7
HD0#	B23
HD1#	E22
HD2#	B21
HD3#	D20
HD4#	B22
HD5#	D22
HD6#	B20
HD7#	C21
HD8#	E18
HD9#	E20
HD10#	B16
HD11#	D16
HD12#	B18
HD13#	B17
HD14#	E16
HD15#	D18
HD16#	G20
HD17#	F17
HD18#	E19

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
HD19#	F19
HD20#	J17
HD21#	L18
HD22#	G16
HD23#	G18
HD24#	F21
HD25#	F15
HD26#	E15
HD27#	E21
HD28#	J19
HD29#	G14
HD30#	E17
HD31#	K17
HD32#	J15
HD33#	L16
HD34#	J13
HD35#	F13
HD36#	F11
HD37#	E13
HD38#	K15
HD39#	G12
HD40#	G10
HD41#	L15
HD42#	E11
HD43#	K13
HD44#	J11
HD45#	H10
HD46#	G8
HD47#	E9
HD48#	B13
HD49#	E14
HD50#	B14
HD51#	B12
HD52#	B15
HD53#	D14
HD54#	C13
HD55#	B11
HD56#	D10
HD57#	C11
HD58#	E10

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
HD59#	B10
HD60#	C9
HD61#	B9
HD62#	D8
HD63#	B8
HDRCOMP	E24
HDSTBN0#	C19
HDSTBN1#	K19
HDSTBN2#	F9
HDSTBN3#	E12
HDSTBP0#	B19
HDSTBP1#	L19
HDSTBP2#	G9
HDSTBP3#	D12
HDSWING	C25
HDVREF	F23
HI_RCOMP	AD4
HI_SWING	AE3
HI_VREF	AE2
HI0	AF5
HI1	AG3
HI2	AK2
HI3	AG5
HI4	AK5
HI5	AL3
HI6	AL2
HI7	AL4
HI8	AJ2
HI9	AH2
HI10	AJ3
HISTRF	AH5
HISTRS	AH4
HIT#	K21
HITM#	E23
HLOCK#	E25
HREQ0#	B29
HREQ1#	J23
HREQ2#	L22
HREQ3#	C29
HREQ4#	J21

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
HSYNC	G3
HTRDY#	D24
NC	A3
NC	A33
NC	A35
NC	AF13
NC	AF23
NC	AJ12
NC	AN1
NC	AP2
NC	AR3
NC	AR33
NC	AR35
NC	B2
NC	B25
NC	B34
NC	C1
NC	C23
NC	C35
NC	E26
NC	M31
NC	R25
PROCHOT#	L20
PWROK	AE14
RED	F4
RED#	E4
REFSET	D2
RS0#	G22
RS1#	C27
RS2#	B27
RSTIN#	AK4
RSVD	AJ8
RSVD	AR1
RSVD	AP34
RSVD	AG9
RSVD	AN35
TESTIN#	AG10
SBA_A0	AE33
SBA_A1	AH34
SBA_B0	Y25

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SBA_B1	AA25
SCAS_A#	Y34
SCAS_B#	W31
SCKE_A0	AL20
SCKE_A1	AN19
SCKE_A2	AM20
SCKE_A3	AP20
SCKE_B0	AK19
SCKE_B1	AF19
SCKE_B2	AG19
SCKE_B3	AE18
SCMDCLK_A0	AK32
SCMDCLK_A0#	AK31
SCMDCLK_A1	AP17
SCMDCLK_A1#	AN17
SCMDCLK_A2	N33
SCMDCLK_A2#	N34
SCMDCLK_A3	AK33
SCMDCLK_A3#	AK34
SCMDCLK_A4	AM16
SCMDCLK_A4#	AL16
SCMDCLK_A5	P31
SCMDCLK_A5#	P32
SCMDCLK_B0	AG29
SCMDCLK_B0#	AG30
SCMDCLK_B1	AF17
SCMDCLK_B1#	AG17
SCMDCLK_B2	N27
SCMDCLK_B2#	N26
SCMDCLK_B3	AJ30
SCMDCLK_B3#	AH29
SCMDCLK_B4	AK15
SCMDCLK_B4#	AL15
SCMDCLK_B5	N31
SCMDCLK_B5#	N30
SCS_A0#	AA34
SCS_A1#	Y31
SCS_A2#	Y32
SCS_A3#	W34
SCS_B0#	U26

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SCS_B1#	T29
SCS_B2#	V25
SCS_B3#	W25
SDM_A0	AP12
SDM_A1	AP16
SDM_A2	AM24
SDM_A3	AP30
SDM_A4	AF31
SDM_A5	W33
SDM_A6	M34
SDM_A7	H32
SDM_B0	AG11
SDM_B1	AG15
SDM_B2	AE21
SDM_B3	AJ28
SDM_B4	AC31
SDM_B5	U31
SDM_B6	M29
SDM_B7	J31
SDQ_A_17	AM22
SDQ_A0	AP10
SDQ_A1	AP11
SDQ_A2	AM12
SDQ_A3	AN13
SDQ_A4	AM10
SDQ_A5	AL10
SDQ_A6	AL12
SDQ_A7	AP13
SDQ_A8	AP14
SDQ_A9	AM14
SDQ_A10	AL18
SDQ_A11	AP19
SDQ_A12	AL14
SDQ_A13	AN15
SDQ_A14	AP18
SDQ_A15	AM18
SDQ_A16	AP22
SDQ_A18	AL24
SDQ_A19	AN27
SDQ_A20	AP21

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SDQ_A21	AL22
SDQ_A22	AP25
SDQ_A23	AP27
SDQ_A24	AP28
SDQ_A25	AP29
SDQ_A26	AP33
SDQ_A27	AM33
SDQ_A28	AM28
SDQ_A29	AN29
SDQ_A30	AM31
SDQ_A31	AN34
SDQ_A32	AH32
SDQ_A33	AG34
SDQ_A34	AF32
SDQ_A35	AD32
SDQ_A36	AH31
SDQ_A37	AG33
SDQ_A38	AE34
SDQ_A39	AD34
SDQ_A40	AC34
SDQ_A41	AB31
SDQ_A42	V32
SDQ_A43	V31
SDQ_A44	AD31
SDQ_A45	AB32
SDQ_A46	U34
SDQ_A47	U33
SDQ_A48	T34
SDQ_A49	T32
SDQ_A50	K34
SDQ_A51	K32
SDQ_A52	T31
SDQ_A53	P34
SDQ_A54	L34
SDQ_A55	L33
SDQ_A56	J33
SDQ_A57	H34
SDQ_A58	E33
SDQ_A59	F33
SDQ_A60	K31

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SDQ_A61	J34
SDQ_A62	G34
SDQ_A63	F34
SDQ_B0	AJ10
SDQ_B1	AE15
SDQ_B2	AL11
SDQ_B3	AE16
SDQ_B4	AL8
SDQ_B5	AF12
SDQ_B6	AK11
SDQ_B7	AG12
SDQ_B8	AE17
SDQ_B9	AL13
SDQ_B10	AK17
SDQ_B11	AL17
SDQ_B12	AK13
SDQ_B13	AJ14
SDQ_B14	AJ16
SDQ_B15	AJ18
SDQ_B16	AE19
SDQ_B17	AE20
SDQ_B18	AG23
SDQ_B19	AK23
SDQ_B20	AL19
SDQ_B21	AK21
SDQ_B22	AJ24
SDQ_B23	AE22
SDQ_B24	AK25
SDQ_B25	AH26
SDQ_B26	AG27
SDQ_B27	AF27
SDQ_B28	AJ26
SDQ_B29	AJ27
SDQ_B30	AD25
SDQ_B31	AF28
SDQ_B32	AE30
SDQ_B33	AC27
SDQ_B34	AC30
SDQ_B35	Y29
SDQ_B36	AE31

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SDQ_B37	AB29
SDQ_B38	AA26
SDQ_B39	AA27
SDQ_B40	AA30
SDQ_B41	W30
SDQ_B42	U27
SDQ_B43	T25
SDQ_B44	AA31
SDQ_B45	V29
SDQ_B46	U25
SDQ_B47	R27
SDQ_B48	P29
SDQ_B49	R30
SDQ_B50	K28
SDQ_B51	L30
SDQ_B52	R31
SDQ_B53	R26
SDQ_B54	P25
SDQ_B55	L32
SDQ_B56	K30
SDQ_B57	H29
SDQ_B58	F32
SDQ_B59	G33
SDQ_B60	N25
SDQ_B61	M25
SDQ_B62	J29
SDQ_B63	G32
SDQS_A0	AN11
SDQS_A1	AP15
SDQS_A2	AP23
SDQS_A3	AM30
SDQS_A4	AF34
SDQS_A5	V34
SDQS_A6	M32
SDQS_A7	H31
SDQS_B0	AF15
SDQS_B1	AG13
SDQS_B2	AG21
SDQS_B3	AH27
SDQS_B4	AD29

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SDQS_B5	U30
SDQS_B6	L27
SDQS_B7	J30
SMAA_A0	AJ34
SMAA_A1	AL33
SMAA_A2	AK29
SMAA_A3	AN31
SMAA_A4	AL30
SMAA_A5	AL26
SMAA_A6	AL28
SMAA_A7	AN25
SMAA_A8	AP26
SMAA_A9	AP24
SMAA_A10	AJ33
SMAA_A11	AN23
SMAA_A12	AN21
SMAA_B0	AG31
SMAA_B1	AJ31
SMAA_B2	AD27
SMAA_B3	AE24
SMAA_B4	AK27
SMAA_B5	AG25
SMAA_B6	AL25
SMAA_B7	AF21
SMAA_B8	AL23
SMAA_B9	AJ22
SMAA_B10	AF29
SMAA_B11	AL21
SMAA_B12	AJ20
SMAB_A1	AL34
SMAB_A2	AM34
SMAB_A3	AP32
SMAB_A4	AP31
SMAB_A5	AM26
SMAB_B1	AE27
SMAB_B2	AD26
SMAB_B3	AL29
SMAB_B4	AL27
SMAB_B5	AE23
SMVREF_A	E34

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
SMVREF_B	AP9
SMXRCOMP	AK9
SMXRCOMPVOH	AN9
SMXRCOMPVOL	AL9
SMYRCOMP	AA33
SMYRCOMPVOH	R34
SMYRCOMPVOL	R33
SRAS_A#	AC33
SRAS_B#	W26
SWE_A#	AB34
SWE_B#	W27
VCC	J6
VCC	J7
VCC	J8
VCC	J9
VCC	K6
VCC	K7
VCC	K8
VCC	K9
VCC	L10
VCC	L11
VCC	L6
VCC	L7
VCC	L9
VCC	M10
VCC	M11
VCC	M8
VCC	M9
VCC	N10
VCC	N11
VCC	N9
VCC	P10
VCC	P11
VCC	R11
VCC	T16
VCC	T17
VCC	T18
VCC	T19
VCC	T20
VCC	U16

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VCC	U17
VCC	U20
VCC	V16
VCC	V18
VCC	V20
VCC	W16
VCC	W19
VCC	W20
VCC	Y16
VCC	Y17
VCC	Y18
VCC	Y19
VCC	Y20
VCC_AGP	J1
VCC_AGP	J2
VCC_AGP	J3
VCC_AGP	J4
VCC_AGP	J5
VCC_AGP	K2
VCC_AGP	K3
VCC_AGP	K4
VCC_AGP	K5
VCC_AGP	L1
VCC_AGP	L2
VCC_AGP	L3
VCC_AGP	L4
VCC_AGP	L5
VCC_AGP	Y1
VCC_DAC	G1
VCC_DAC	G2
VCC_DDR	AA35
VCC_DDR	AL6
VCC_DDR	AL7
VCC_DDR	AM1
VCC_DDR	AM2
VCC_DDR	AM3
VCC_DDR	AM5
VCC_DDR	AM6
VCC_DDR	AM7
VCC_DDR	AM8

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VCC_DDR	AN2
VCC_DDR	AN4
VCC_DDR	AN5
VCC_DDR	AN6
VCC_DDR	AN7
VCC_DDR	AN8
VCC_DDR	AP3
VCC_DDR	AP4
VCC_DDR	AP5
VCC_DDR	AP6
VCC_DDR	AP7
VCC_DDR	AR15
VCC_DDR	AR21
VCC_DDR	AR31
VCC_DDR	AR4
VCC_DDR	AR5
VCC_DDR	AR7
VCC_DDR	E35
VCC_DDR	R35
VCCA_AGP	AG1
VCCA_AGP	Y11
VCCA_DAC	C2
VCCA_DDR	AC26
VCCA_DDR	AL35
VCCA_DDR	AB25
VCCA_DDR	AC25
VCCA_DPLL	B3
VCCA_FSB	A31
VCCA_FSB	B4
VSS	AF24
VSS	AF25
VSS	AF3
VSS	AF30
VSS	AF33
VSS	AF6
VSS	AF9
VSS	AG14
VSS	AG16
VSS	AG18
VSS	AG20

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	AG22
VSS	AG24
VSS	AG26
VSS	AG28
VSS	AG32
VSS	AG35
VSS	AG4
VSS	AG8
VSS	AH10
VSS	AH12
VSS	AH14
VSS	AH16
VSS	AH18
VSS	AN30
VSS	AN32
VSS	AR11
VSS	AR13
VSS	AR16
VSS	AR20
VSS	AR23
VSS	AR25
VSS	AR27
VSS	AR29
VSS	AR32
VSS	AR9
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20
VSS	C22
VSS	C24
VSS	C26
VSS	C28
VSS	C4
VSS	C8
VSS	D1
VSS	D11
VSS	D13

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	D15
VSS	D17
VSS	D19
VSS	K29
VSS	K33
VSS	L24
VSS	L25
VSS	L26
VSS	L31
VSS	L35
VSS	M26
VSS	M27
VSS	M28
VSS	M3
VSS	M30
VSS	M33
VSS	M6
VSS	N1
VSS	N32
VSS	N35
VSS	N4
VSS	P26
VSS	P27
VSS	P28
VSS	P3
VSS	P30
VSS	P33
VSS	P6
VSS	P8
VSS	P9
VSS	R1
VSS	R32
VSS	R4
VSS	T1
VSS	T10
VSS	A11
VSS	A13
VSS	A16
VSS	A20
VSS	A23

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	A25
VSS	A27
VSS	A29
VSS	A32
VSS	A7
VSS	A9
VSS	AA1
VSS	AA32
VSS	AA4
VSS	AB10
VSS	AB26
VSS	AB27
VSS	AB28
VSS	AB3
VSS	AB30
VSS	AB33
VSS	AB6
VSS	AB8
VSS	AB9
VSS	AH20
VSS	AH22
VSS	AH24
VSS	AH3
VSS	AH30
VSS	AH33
VSS	AH6
VSS	AJ1
VSS	AJ32
VSS	AJ35
VSS	AJ4
VSS	AJ9
VSS	AK10
VSS	AK12
VSS	AK14
VSS	AK16
VSS	AK18
VSS	AK20
VSS	AK22
VSS	AK24
VSS	AK26

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	AK28
VSS	AK3
VSS	AK8
VSS	D21
VSS	D23
VSS	D25
VSS	D27
VSS	D29
VSS	D31
VSS	D33
VSS	D35
VSS	D9
VSS	E1
VSS	E3
VSS	F1
VSS	F10
VSS	F12
VSS	F14
VSS	F16
VSS	F18
VSS	F20
VSS	F22
VSS	F24
VSS	F26
VSS	F3
VSS	F5
VSS	F8
VSS	G28
VSS	G31
VSS	G35
VSS	H12
VSS	H14
VSS	H16
VSS	T26
VSS	T27
VSS	T28
VSS	T3
VSS	T30
VSS	T33
VSS	T35

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	T6
VSS	T8
VSS	T9
VSS	U18
VSS	U19
VSS	U32
VSS	U4
VSS	V10
VSS	V17
VSS	V19
VSS	V26
VSS	V27
VSS	V28
VSS	V3
VSS	V30
VSS	V33
VSS	V6
VSS	V8
VSS	V9
VSS	W17
VSS	W18
VSS	W32
VSS	W4
VSS	Y10
VSS	Y26
VSS	AC1
VSS	AC32
VSS	AC35
VSS	AC4
VSS	AD10
VSS	AD28
VSS	AD3
VSS	AD30
VSS	AD33
VSS	AD6
VSS	AD8
VSS	AD9
VSS	AE1
VSS	AE10
VSS	AE11

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	AE12
VSS	AE13
VSS	AE25
VSS	AE26
VSS	AE32
VSS	AE35
VSS	AE4
VSS	AF11
VSS	AF14
VSS	AF16
VSS	AF18
VSS	AF20
VSS	AF22
VSS	AL1
VSS	AL32
VSS	AM11
VSS	AM13
VSS	AM15
VSS	AM17
VSS	AM19
VSS	AM21
VSS	AM23
VSS	AM25
VSS	AM27
VSS	AM29
VSS	AM35
VSS	AM9
VSS	AN10
VSS	AN12
VSS	AN14
VSS	AN16

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	AN18
VSS	AN20
VSS	AN22
VSS	AN24
VSS	AN26
VSS	AN28
VSS	H18
VSS	H2
VSS	H20
VSS	H22
VSS	H24
VSS	H26
VSS	H30
VSS	H33
VSS	H5
VSS	H8
VSS	H9
VSS	J10
VSS	J12
VSS	J14
VSS	J16
VSS	J18
VSS	J20
VSS	J22
VSS	J28
VSS	J32
VSS	J35
VSS	K11
VSS	K12
VSS	K14
VSS	K16

Table 42. Intel® 82865G Ball List by Signal Name

Signal Name	Ball #
VSS	K18
VSS	K20
VSS	K22
VSS	K25
VSS	K27
VSS	Y27
VSS	Y28
VSS	Y3
VSS	Y30
VSS	Y33
VSS	Y35
VSS	Y6
VSS	Y8
VSS	Y9
VSSA_DAC	D3
VSYNC	E2
VTT	A15
VTT	A21
VTT	A4
VTT	A5
VTT	A6
VTT	B5
VTT	B6
VTT	C5
VTT	C6
VTT	D5
VTT	D6
VTT	D7
VTT	E6
VTT	E7
VTT	F7

7.2 GMCH Package Information

The GMCH is in a 37.5 mm x 37.5 mm Flip Chip Ball Grid Array (FC-BGA) package with 932 solder balls. Figure 18 and Figure 19 show the package dimensions.

Figure 18. Intel® 82865G GMCH Package Dimensions (Top and Side Views)

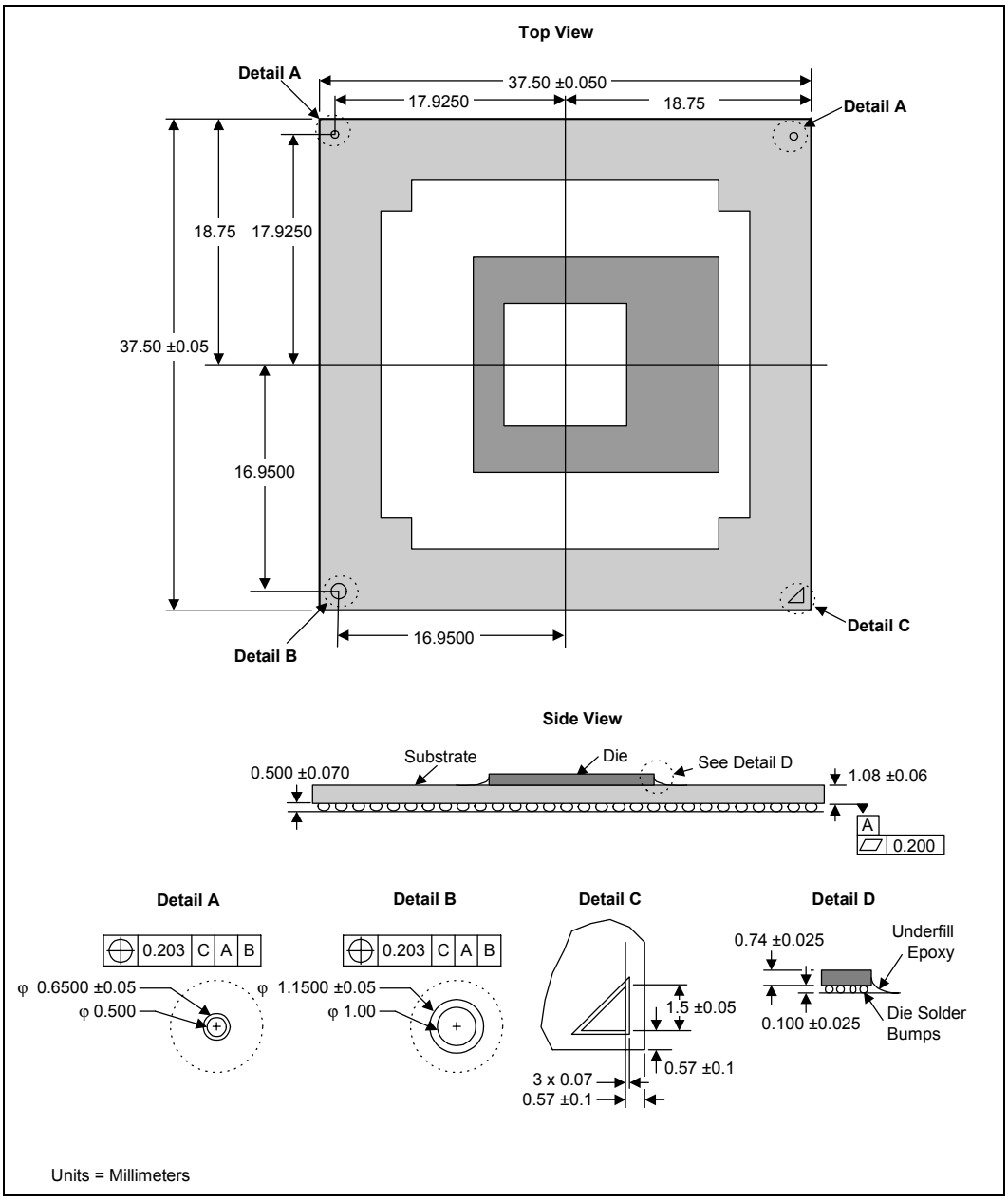
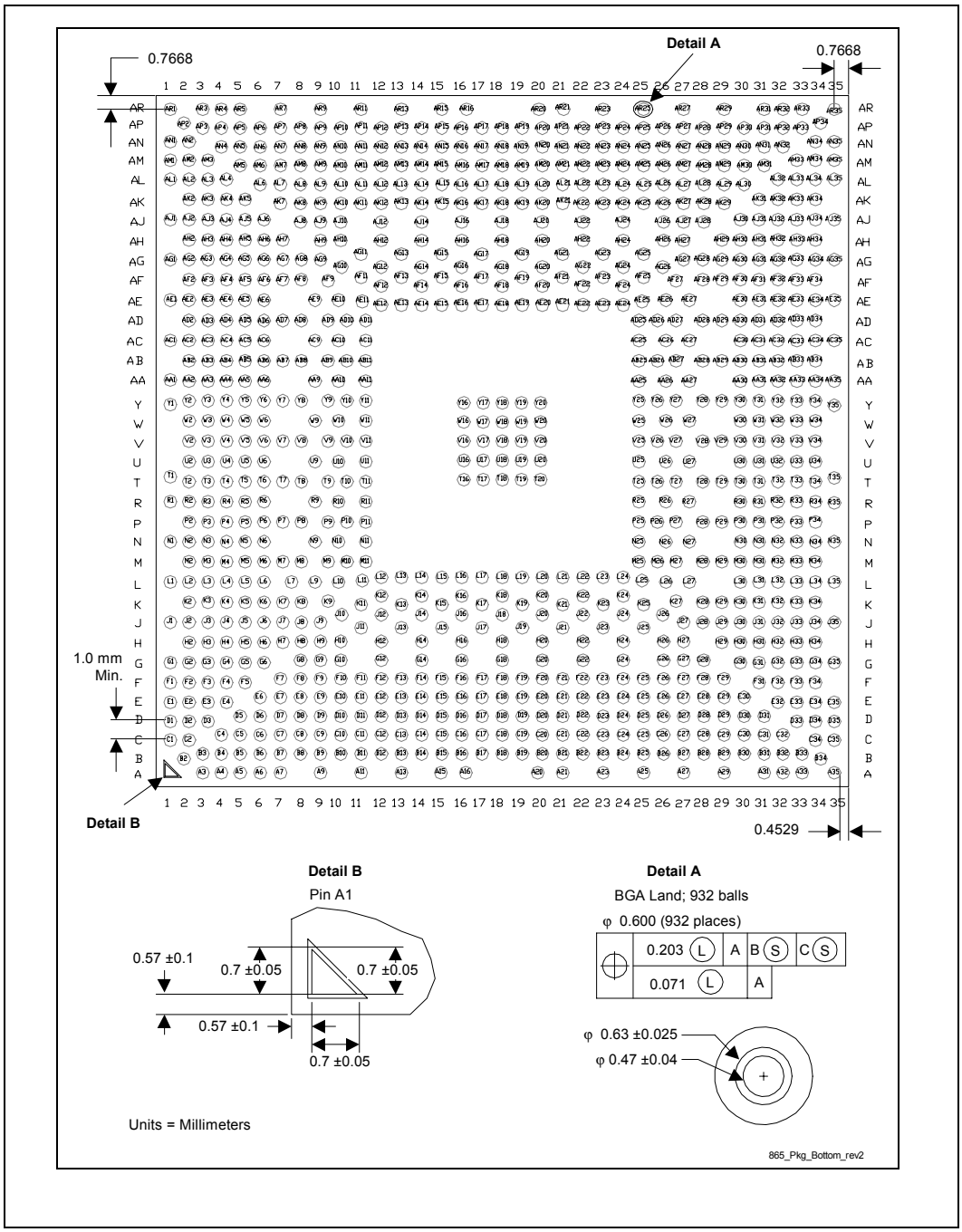


Figure 19. Intel® 82865G GMCH Package Dimensions (Bottom View)



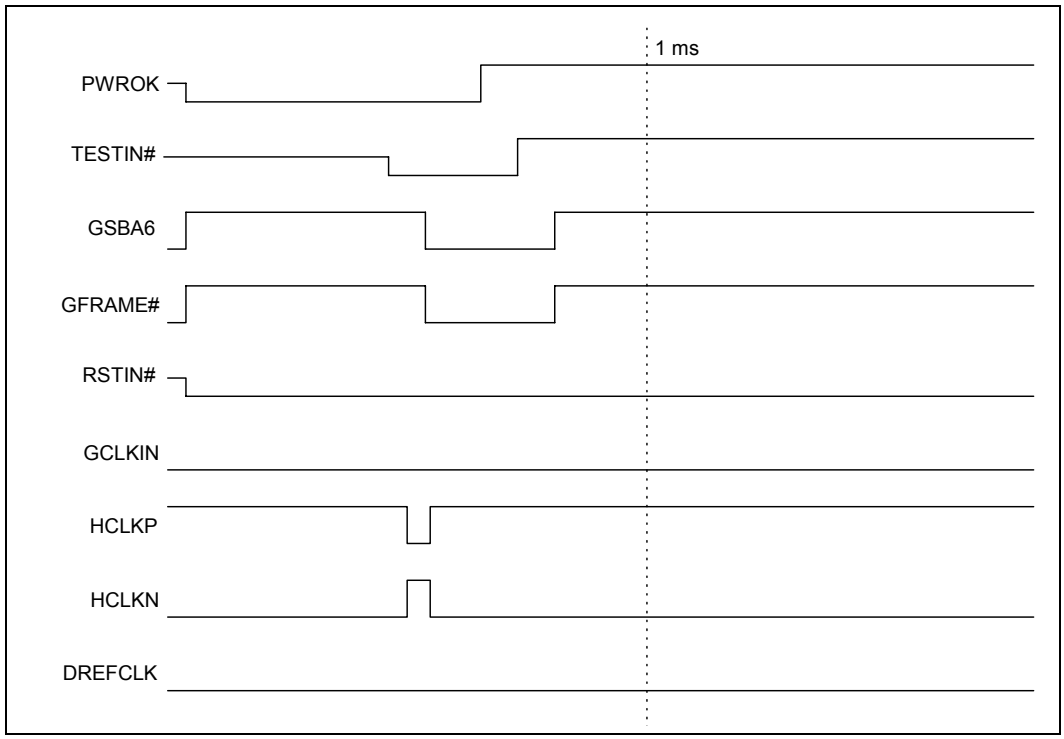
Testability 8

In the GMCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates, each with one input pin connected to it.

8.1 XOR Test Mode Initialization

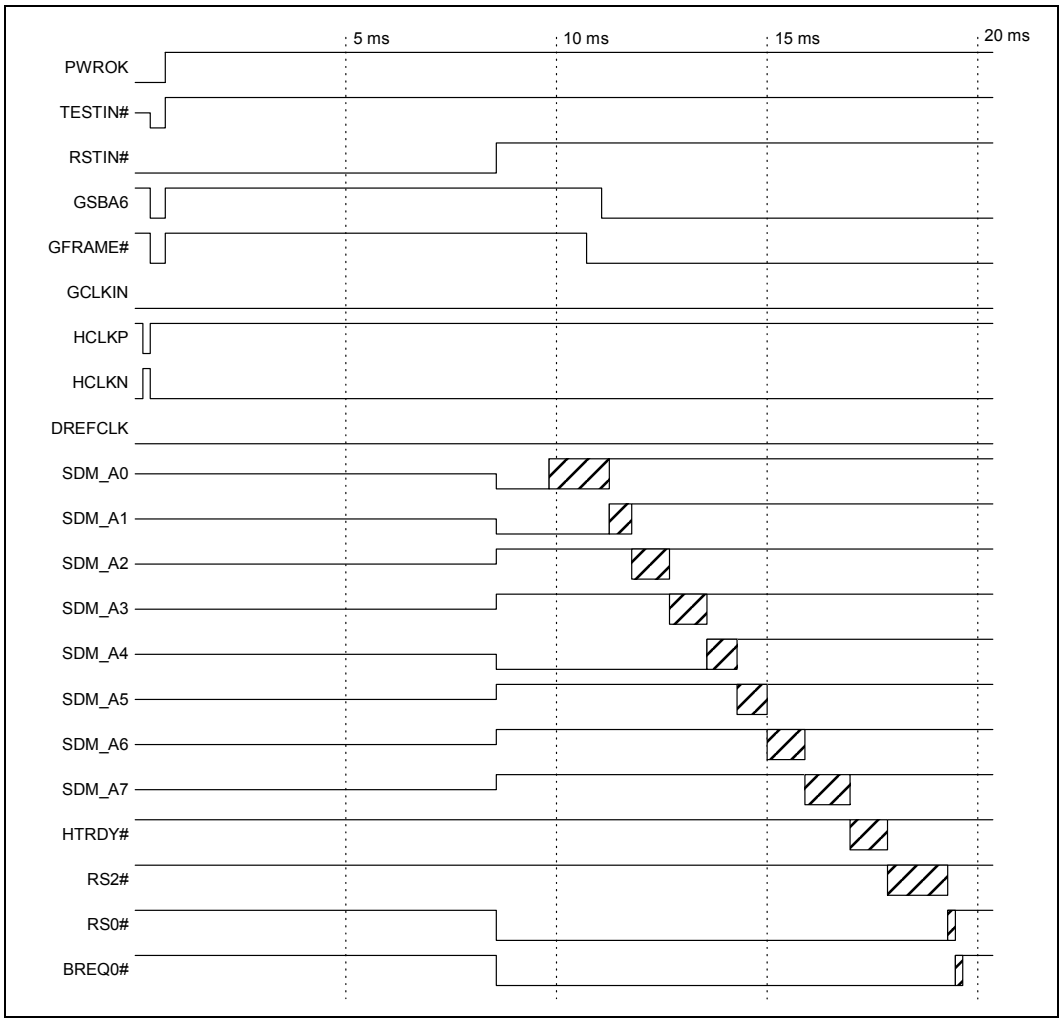
XOR test mode can be entered by driving GSBA6#, GSBA7#, TESTIN#, PWROK low, and RSTIN# low, then driving PWROK high, then RSTIN# high. XOR test mode via TESTIN# does not require a clock. But toggling of HCLKP and HCLKN as shown in Figure 20 is required for deterministic XOR operation when in AGP 2.0 mode. If the component is in AGP 3.0 mode, GSBA6#, GSBA7#, and GC#/BE1 must be driven high.

Figure 20. XOR Toggling of HCLKP and HCLKN



Pin testing will not start until RSTIN# is deasserted. Figure 21 shows chains that are tested sequentially. Note that for the GMCH, sequential testing is not required. All chains can be tested in parallel for test time reduction.

Figure 21. XOR Testing Chains Tested Sequentially



8.2 XOR Chain Definition

The GMCH has 10 XOR chains. The XOR chain outputs are driven out on the output pins as shown in Table 43. During fullwidth testing, XOR chain outputs will be visible on both pins (For example, xor_out0 will be visible on SDM_A0 and SDM_B0). During channel shared mode on the tester, outputs will be visible on their respective channels. (For example, in channel A mode, xor_out0 will be visible on SDM_A0 and the same will be visible on SDM_B0 in channel B mode.)

Table 43. XOR Chain Outputs

XOR Chain	DDR Output Pin Channel A	DDR Output Pin Channel B
xor_out0	SDM_A0	SDM_B0
xor_out1	SDM_A1	SDM_B1
xor_out2	SDM_A2	SDM_B2
xor_out3	SDM_A3	SDM_B3
xor_out4	SDM_A4	SDM_B4
xor_out5	SDM_A5	SDM_B5
xor_out6	SDM_A6	SDM_B6
xor_out7	SDM_A7	SDM_B7
xor_out8	HTRDY#	BPRI#
xor_out9	RS2#	DEFER#
xor_out10	RS0#	RS1#
xor_out11	BREQ0#	CPURST#

The following tables show the XOR chain pin mappings and their monitors for the GMCH.

Note: Notes for Table 44 through Table 54.

1. Only AGP differential strobes are on different chains but in the same channel group. Other interface strobes are on the same chain since they are not required to be in opposite polarity all the time. All XOR chains can be run in parallel, except chains with AGP strobes (chains 0 and 1, chains 0 and 2, and chains 2 and 4).
2. The channel A and channel B output pins for each chain show the same output.
3. For the multiplexed AGP and DVO signals, only the AGP signal names are listed. Refer to Section 2.5.7 for the DVO-to-AGP signal mapping.
4. For AGP signals, only the AGP 3.0 signal name is listed. For the corresponding AGP 2.0 signal name, refer to Chapter 2.

Table 44. XOR Chain 0 (60 Inputs) Output Pins: SDM_A0, SDM_B0

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
CI7	AG7	GAD3	AE5	GST0	N3
CI1	AH7	GC#/BE0	Y7	GIRDY	V11
CI2	AD11	GADSTB0	AC6	GC#/BE2	AA3
CI8	AE9	GAD12	AA11	GC#/BE3	U2
CI9	AH9	GAD7	AB7	GST2	N2
CI0	AK7	GSTOP	W11	DBI_HI	M4
CISTRF	AJ6	GAD11	W10	GREQ	N6
CISTRS	AJ5	GAD10	AA5	GSBA2#	R3
CI6	AF8	GAD9	AA6	GSBSTBF	U11
CI3	AF7	GAD15	V7	GSBA7#	T7
CI4	AD7	GAD13	W6	GSBA0#	R6
CI5	AC10	GAD14	W9	GSBA5#	U10
CI10	AG6	GTRDY	AB5	GSBA3#	R5
GAD1	AC11	GPAR	AB2	GSBA4#	U9
GAD5	AC9	GC#/BE1	W5	GSBA1#	P7
GAD0	AE6	GFRAME	U6	GSBA6#	U5
GAD6	AB11	DBI_LO	M5	DDCA_CLK	F2
GAD2	AD5	GDEVSEL	AB4	DDCA_DATA	H3
GAD4	AA10	GRBF	R10	VSYNC	E2
GAD8	AA9	GWBF	R9	RSVD	AJ8
Output Pins					
SDM_A0	AP12				
SDM_B0	AG11				

Table 45. XOR Chain 1 (33 Inputs) Output Pins: SDM_A1, SDM_B1

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HI7	AL4	HI8	AJ2	GAD23	U3
HI4	AK5	HI9	AH2	GAD25	T4
HI3	AG5	GST1	N5	GAD27	R2
HI5	AL3	GAD20	Y5	GAD24	T2
HISTRF	AH5	GAD16	AA2	GAD21	V2
HI10	AJ3	GAD17	Y4	GAD28	P2
HISTRS	AH4	GAD19	W2	GAD30	P4
HI2	AK2	GAD18	Y2	GAD31	M2
HI0	AF5	GADSTBF1	V5	GAD29	P5
HI6	AL2	GAD22	W3	GGNT	M7
HI1	AG3	GAD26	T5	EXTTS#	AP8
Output Pins					
SDM_A1	AP16				
SDM_B1	AG15				

Table 46. XOR Chain 2 (44 Inputs) Output Pins: SDM_A2, SDM_B2

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
GADSTBS0	AC5	HD19#	F19	HDSTBN0#	C19
GSBSTBS	T11	HD27#	E21	HD6#	B20
HD29#	G14	HD24#	F21	HD9#	E20
HD25#	F15	HD21#	L18	HD12#	B18
HD26#	E15	HD28#	J19	HD3#	D20
HD31#	K17	HD16#	G20	HD2#	B21
HD22#	G16	HD18#	E19	HD0#	B23
HD17#	F17	DINV0#	C17	HD4#	B22
HD30#	E17	HD8#	E18	HD5#	D22
HD20#	J17	HD11#	D16	HD7#	C21
DINVB_1	L17	HD14#	E16	HD1#	E22
HD23#	G18	HD10#	B16	PROCHOT#	L20
HDSTBP1#	L19	HD15#	D18	HITM#	E23
HDSTBN1#	K19	HD13#	B17	BSEL0	L13
		HDSTBP0#	B19	HLOCK#	E25
Output Pins					
SDM_A2	AM24				
SDM_B2	AE21				

Table 47. XOR Chain 3 (41 Inputs) Output Pins: SDM_A3, SDM_B3

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
BNR#	B28	HA12#	B31	HA19#	F28
BSEL1	L12	HA9#	C30	HA18#	C32
HIT#	K21			HA22#	G27
DRDY#	G24	HA4#	D30	HA24#	E28
DBSY#	E27	HA10#	C31	HA23#	F29
ADS#	F27	HA15#	J24	HADSTB1#	D28
HREQ4#	J21	HA8#	K23	HA17#	D34
HA16#	F25	HA13#	E30	HA25#	H27
HREQ3#	C29	HA6#	E29	HA20#	C34
HREQ0#	B29	HA5#	L23	HA30#	J26
HA3#	D26	HA11#	J25	HA21#	J27
HREQ1#	J23	HREQ2#	L22	HA27#	E32
HA7#	B32	HA31#	G26	HA29#	G30
HA14#	B33	HA26#	K24	HA28#	F31
Output Pins					
SDM_A3	AP30				
SDM_B3	AJ28				

Table 48. XOR Chain 4 (40 Inputs) Output Pins: SDM_A4, SDM_B4

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HD45#	H10	HD43#	K13	HD57#	C11
HD46#	G8	HD33#	L16	HDSTBP3#	D12
HD40#	G10	HD41#	L15	HDSTBN3#	E12
HD47#	E9	HD35#	F13	HD51#	B12
HD39#	G12	HD32#	J15	HD49#	E14
HD36#	F11	HD37#	E13	HD55#	B11
HD44#	J11	HD58#	E10	HD54#	C13
HD42#	E11	HD56#	D10	HD53#	D14
DINV2#	L14	HD62#	D8	HD50#	B14
HDSTBP2#	G9	HD61#	B9	HD48#	B13
HDSTBN2#	F9	HD63#	B8	HD52#	B15
HD34#	J13	HD59#	B10	DINV3#	C15
HD38#	K15	HD60#	C9	GADSTBF1	V4
Output Pins				HSYNC	G3
SDM_A1	AF31				
SDM_B1	AC31				

Table 49. XOR Chain 5 (44 Inputs) Output Pins: SDM_A5, SDM_B5

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A58	E33	SDQ_A53	P34	SDQ_A41	AB31
SDQ_A59	F33	SDQ_A48	T34	SDQ_A44	AD31
SDQ_A62	G34	SDQ_A52	T31	SDQS_A4	AF34
SDQ_A63	F34	SDQ_A49	T32	SDQ_A35	AD32
SDQS_A7	H31	SCMDCLK_A5#	P32	SDQ_A38	AE34
SDQ_A61	J34	SCMDCLK_A5	P31	SDQ_A39	AD34
SDQ_A57	H34	SCMDCLK_A2#	N34	SDQ_A34	AF32
SDQ_A56	J33	SCMDCLK_A2	N33	SDQ_A33	AG34
SDQ_A60	K31	SDQS_A5	V34	SDQ_A37	AG33
SDQ_A51	K32	SDQ_A42	V32	SDQ_A36	AH31
SDQ_A50	K34	SDQ_A46	U34	SDQ_A32	AH32
SDQ_A55	L33	SDQ_A47	U33	SCMDCLK_A0	AK32
SDQS_A6	M32	SDQ_A43	V31	SCMDCLK_A0#	AK31
SDQ_A54	L34	SDQ_A40	AC34	SCMDCLK_A3#	AK34
		SDQ_A45	AB32	SCMDCLK_A3	AK33
Output Pins					
SDM_A1	W33				
SDM_B1	U31				

Table 50. XOR Chain 6 (40 Inputs) Output Pins: SDM_A6, SDM_B6

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A30	AM31	SDQ_A19	AN27	SDQ_A8	AP14
SDQS_A3	AM30	SDQ_A23	AP27	SDQ_A6	AL12
SDQ_A27	AM33	SDQ_A22	AP25	SDQ_A2	AM12
SDQ_A31	AN34	SDQ_A16	AP22	SDQ_A3	AN13
SDQ_A29	AN29	SDQ_A20	AP21	SDQS_A0	AN11
SDQ_A26	AP33	SDQ_A10	AL18	SDQ_A5	AL10
SDQ_A25	AP29	SDQ_A15	AM18	SDQ_A7	AP13
SDQ_A24	AP28	SDQ_A14	AP18	SDQ_A4	AM10
SDQ_A28	AM28	SDQS_A1	AP15	SCMDCLK_A1	AP17
SDQS_A2	AP23	SDQ_A11	AP19	SCMDCLK_A1#	AN17
SDQ_A21	AL22	SDQ_A13	AN15	SDQ_A1	AP11
SDQ_A17	AM22	SDQ_A9	AM14	SCMDCLK_A4#	AL16
SDQ_A18	AL24	SDQ_A12	AL14	SCMDCLK_A4	AM16
				SDQ_A0	AP10
Output Pins					
SDM_A6	M34				
SDM_B6	M29				

Table 51. XOR Chain 7 (45 Inputs) Output Pins: SDM_A7, SDM_B7

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HADSTB1#	D28	SDQS_B6	L27	SDQ_B41	W30
SDQ_B57	H29	SDQ_B48	P29	SDQS_B5	U30
SDQ_B61	M25	SDQ_B49	R30	SDQ_B37	AB29
SDQ_B58	F32	SDQ_B52	R31	SDQ_B36	AE31
SDQ_B63	G32	SCMDCLK_B5	N31	SDQ_B35	Y29
SDQ_B60	N25	SCMDCLK_B5#	N30	SDQ_B32	AE30
SDQS_B7	J30	SCMDCLK_B2#	N26	SDQ_B34	AC30
SDQ_B62	J29	SCMDCLK_B2	N27	SDQ_B38	AA26
SDQ_B59	G33	SDQ_B43	T25	SDQ_B33	AC27
SDQ_B56	K30	SDQ_B46	U25	SDQ_B39	AA27
SDQ_B51	L30	SDQ_B42	U27	SDQS_B4	AD29
SDQ_B54	P25	SDQ_B47	R27	SCMDCLK_B0	AG29
SDQ_B55	L32	SDQ_B45	V29	SCMDCLK_B0#	AG30
SDQ_B53	R26	SDQ_B40	AA30	SCMDCLK_B3	AJ30
SDQ_B50	K28	SDQ_B44	AA31	SCMDCLK_B3#	AH29
Output Pins					
SDM_A7	H32				
SDM_B7	J31				

Table 52. XOR Chain 8 (40 Inputs) Output Pins: SDM_A8, SDM_B8

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_B30	AD25	SDQ_B21	AK21	SDQ_B8	AE17
SDQ_B26	AG27	SDQ_B17	AE20	SCMDCLK_B4#	AL15
SDQ_B29	AJ27	SDQS_B2	AG21	SCMDCLK_B4	AK15
SDQ_B27	AF27	SDQ_B16	AE19	SCMDCLK_B1#	AG17
SDQ_B31	AF28	SDQ_B20	AL19	SCMDCLK_B1	AF17
SDQ_B25	AH26	SDQ_B10	AK17	SDQ_B1	AE15
SDQS_B3	AH27	SDQ_B14	AJ16	SDQ_B3	AE16
SDQ_B28	AJ26	SDQ_B15	AJ18	SDQ_B7	AG12
SDQ_B24	AK25	SDQ_B11	AL17	SDQ_B2	AL11
SDQ_B23	AE22	SDQ_B13	AJ14	SDQ_B6	AK11
SDQ_B18	AG23	SDQ_B12	AK13	SDQ_B5	AF12
SDQ_B19	AK23	SDQ_B9	AL13	SDQ_B0	AJ10
SDQ_B22	AJ24	SDQS_B1	AG13	SDQ_B4	AL8
				SDQS_B0	AF15
Output Pins					
HTRDY#	D24				
BPRI#	B26				

Table 53. XOR Chain 9 (62 Inputs) Output Pins: RS2#, DEFER#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SCAS_A#	Y34	SMAA_B0	AG31	SMAA_B7	AF21
SWE_A#	AB34	SMAB_A1	AL34	SMAA_B9	AJ22
SCS_B3#	W25	SMAA_A6	AL28	SMAA_B11	AL21
SBA_B1	AA25	SMAA_B6	AL25	SMAA_B4	AK27
SBA_A1	AH34	SMAB_A3	AP32	SMAA_B5	AG25
SCS_A1#	Y31	SMAB_A2	AM34	SCKE_A3	AP20
SCS_A2#	Y32	SMAA_A3	AN31	SCKE_A0	AL20
SCS_A3#	W34	SMAA_B3	AE24	SMAA_A11	AN23
SRAS_A#	AC33	SMAA_B1	AJ31	SMAA_A12	AN21
SBA_A0	AE33	SMAB_B3	AL29	SCKE_A2	AM20
SCS_A0#	AA34	SMAA_A4	AL30	SCKE_A1	AN19
SMAA_B2	AD27	SMAB_B4	AL27	SCKE_B0	AK19
SRAS_B#	W26	SMAB_B2	AD26	SCKE_B3	AE18
SMAA_B10	AF29	SMAB_A4	AP31	SCKE_B2	AG19
SBA_B0	Y25	SMAB_A5	AM26	SMAA_B12	AJ20
SMAA_A10	AJ33	SMAA_A9	AP24	SCKE_B1	AF19
SMAB_B1	AE27	SMAB_B5	AE23	SCS_B1#	T29
SMAA_A0	AJ34	SMAA_A8	AP26	SCS_B0#	U26
SMAA_A1	AL33	SMAA_A5	AL26	SCS_B2#	V25
SMAA_A2	AK29	SMAA_A7	AN25	SWE_B#	W27
		SMAA_B8	AL23	SCAS_B#	W31
Output Pins					
RS2#	B27				
DEFER#	L21				

Table 54. XOR Excluded Pins

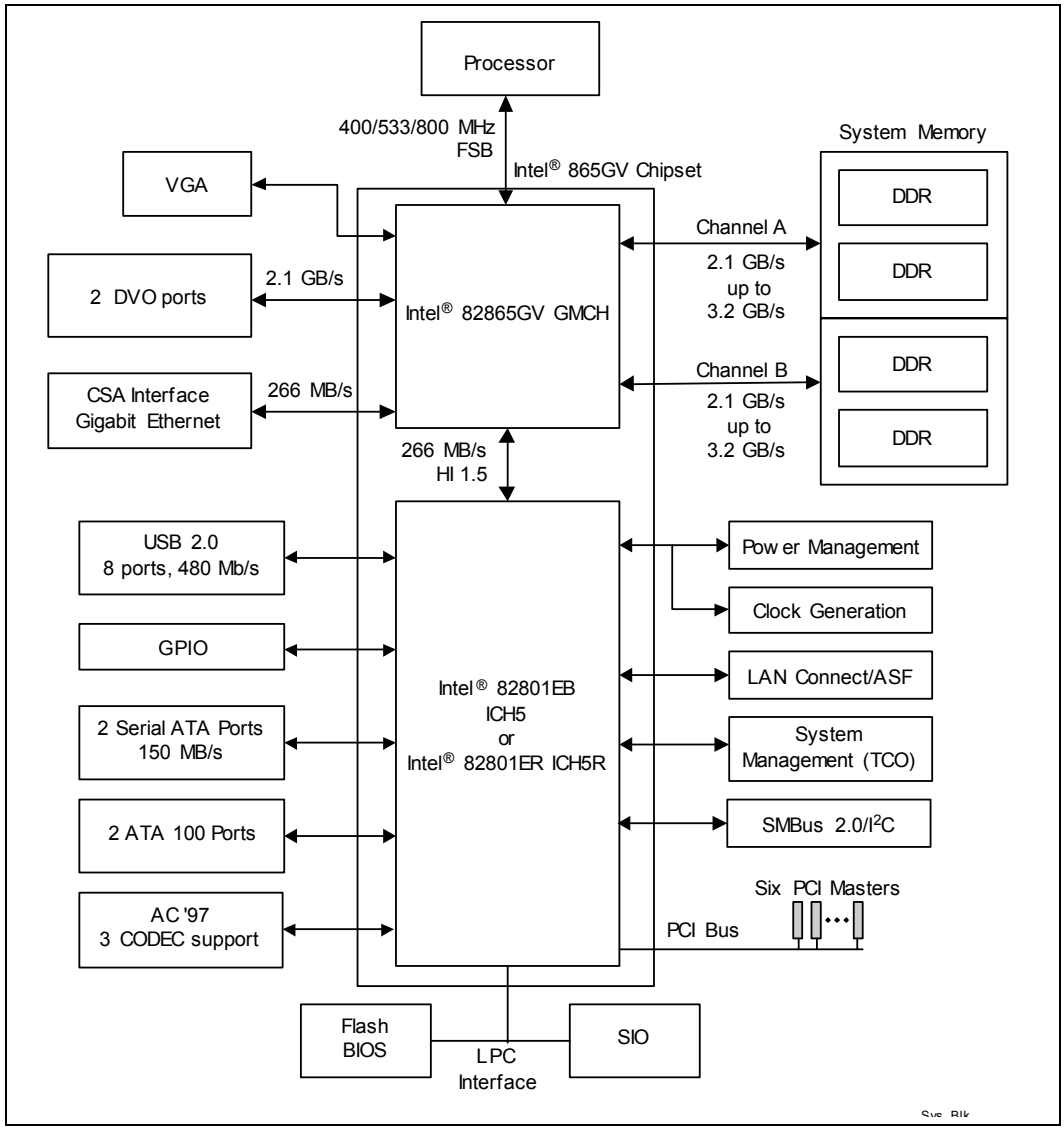
Signal Name	Ball Number	Signal Name	Ball Number
BLUE	H7	SDM_A0	AP12
BLUE#	G6	SDM_A1	AP16
BPRI#	B26	SDM_A2	AM24
BREQ0#	B24	SDM_A3	AP30
CPURST#	E8	SDM_A4	AF31
DEFER#	L21	SDM_A5	W33
DREFCLK	G4	SDM_A6	M34
GCLKIN	H4	SDM_A7	H32
GRCOMP	AC2	SDM_B0	AG11
GREEN	H6	SDM_B1	AG15
GREEN#	G5	SDM_B2	AE21
GVREF	AD2	SDM_B3	AJ28
GVSWING	AC3	SDM_B4	AC31
HCLKN	C7	SDM_B5	U31
HCLKP	B7	SDM_B6	M29
HDRCOMP	E24	SDM_B7	J31
HDSWING	C25	SMVREF_A0	E34
HDVREF	F23	SMVREF_B0	AP9
HTRDY#	D24	SMXRCOMP	AK9
HI_COMP	AD4	SMXRCOMPVOH	AN9
HI_VREF	AE2	SMXRCOMPVOL	AL9
HI_SWING	AE3	SMYRCOMP	AA33
PWROK	AE14	SMYRCOMPVOH	R34
RED	F4	SMYRCOMPVOL	R33
RED#	E4	Reserved	AG9
REFSET	D2	TESTIN#	AG10
RS0#	G22	CI_RCOMP	AG2
RS1#	C27	CI_VREF	AF4
RS2#	B27	CI_VSWING	AF2
RSTIN#	AK4		

Intel® 82865GV GMCH 9

Chapter 1 through Chapter 8 of this datasheet described the 82865G component. The first 8 chapters also apply to the 82865GV, with the differences noted in this chapter. This chapter describes the differences between the 82865G and the 82865GV components. Figure 22 shows an example block diagram of an 865GV chipset-based platform.

The information in Chapter 9 through Chapter 11apply to the 82865GV component, unless otherwise noted.

Figure 22. Intel® 865GV Chipset System Block Diagram



9.1 No AGP Interface

The 82865GV does not have an AGP interface. References to AGP or AGP/PCI_B in this document only apply to the 82865G component. For example, Chapter 2 describes how the 82865G DVO signals are multiplexed with the AGP signals. For the 82865GV, the DVO signals are **not** multiplexed. In addition, AGP related registers are **not** in the 82865GV component.

9.2 Intel® 82865G / 82865GV Signal Differences

The 82865G and 82865GV signals are the same, except for the following:

- ADD_DETECT signal functionality is slightly different between the two components.
- There are no AGP signals on the 82865GV. The 82865GV DVO signals are not multiplexed.

Section 2.5.7, *Intel® DVO Signals Name to AGP Signal Name Pin Mapping* does not apply to the 82865GV.

In Section 2.5.5, replace the ADD_DETECT signal description with the following:

Signal Name	Type	Description
GPAR/ ADD_DETECT	I/O AGP	**PAR:** Same as PCI. Not used on AGP transactions but used during PCI transactions as defined by the *PCI Local Bus Specification, Revision 2.1.* **ADD_DETECT:** This signal acts as a strap and indicates whether the interface is in DVO mode. The 82865GV GMCH has an internal pull-up on this signal that will naturally pull it high. If an Intel® DVO is used, the signal should be pulled low and the DVO select bit in the GMCHCFG register will be set to DVO mode. Motherboards that use this interface in a DVO down scenario should have a pull-down resistor on ADD_DETECT.

9.2.1 Functional Straps

In Section 2.11.1, *Functional Straps*, replace the PSBSEL signal description with the following:

Signal Name	Type	Description
GPAR/ ADD_DETECT	DVO	**Operating Mode Select Strap:** This strap selects the operating mode of the Intel® DVO signals • 0 (low voltage) = ADD Card (2X DVO) • 1 (high voltage) = Reserved The ADD_DETECT strap is flow-through while RSTIN# is asserted and latched on the deasserting edge of RSTIN#. RSTIN# is used to make sure that the card is not driving the GPAR/ADD_DETECT signal when it is latched.

9.3 Intel® 82865G / 82865GV Register Differences

Chapter 3 describes the registers for the 82865G GMCH. This section describes the changes to Chapter 3 for the 82865GV GMCH. The differences are in the Device 0 and Device 1 register sets. The Device 2 registers are the same for the 82865G and 82865GV.

9.3.1 DRAM Controller/Host-Hub Interface Device Registers (Device 0)

9.3.1.1 Device 0 Registers Not in 82865GV

The following registers are not in the 82865GV and the address locations are Intel Reserved.

APBASE — Aperture Base Configuration Register (Device 0)

Address Offset: 10–13h
Size: 32 bits

AGPM — AGP Miscellaneous Configuration Register (Device 0)

Address Offset 51h
Size: 8 bits

ACAPID — AGP Capability Identifier Register (Device 0)

Address Offset A0–A3h
Size: 32 bits

AGPSTAT — AGP Status Register (Device 0)

Address Offset A4–A7h
Size: 32 bits

AGPCMD — AGP Command Register (Device 0)

Address Offset A8–ABh
Size: 32 bits

AGPCTRL — AGP Control Register (Device 0)

Address Offset B0–B3h
Size: 32 bits

APSIZE — Aperture Size Register (Device 0)

Address Offset B4h
Size: 8 bits

ATTBASE — Aperture Translation Table Register (Device 0)

Address Offset B8–BBh
Size: 32 bits

AMTT — AGP MTT Control Register (Device 0)

Address Offset BC–BFh
Size: 8 bits

LPTT — AGP Low Priority Transaction Timer Register (Device 0)

Address Offset BDh
Size: 8 bits

9.3.1.2 Device 0 Register Bit Differences

The registers described in this section are in both the 82865G and 82865GV. However, some of the register bits have different functions/operations between the two components. Only the bits that are different are shown in this section. The remaining register bits are the same for both the 82865G and 82865GV and are described in Chapter 3.

GC—Graphics Control Register (Device 0)

Address Offset 52h
Default Value 0000_0000b
Access RO, R/W. R/W/L
Size: 8 bits

Bits	Description
3	**Integrated Graphics Disable (IGDIS) — RO.** The GMCH's Device 1 is disabled such that all configuration cycles to Device 1 flow through to the hub interface. Also, the Next_Pointer field in the CAPREG register (Device 0, Offset E4h) is RO at 00h. This enables internal graphics capability. 0 = Enable. Internal Graphics is enabled (default)

GMCHCFG—GMCH Configuration Register (Device 0)

Address Offset	C6–C7h
Default Value	0000h
Access	R/W, RO
Size:	16 bits

Bits	Description
3	**AGP Mode (AGP/DVO#)—RO.** This bit reflects the ADD_DETECT strap value. This strap bit determines the function of the AGP I/O signal. 0 = 2xDVO 1 = no DVO mode, internal graphics only. When the strap is sampled low, this bit is 0 and Intel® DVO mode is selected. When the strap is sampled high, this bit is 1 and DVO mode is not selected, and the internal graphics device is running. Note that when this bit is set to 0 (DVO mode), Device 1 is disabled (configuration cycles fall-through to the hub interface) and the Next Pointer field in CAPREG will be hardwired to 0s.

ERRSTS—Error Status Register (Device 0)

Address Offset	C8–C9h
Default Value	0000h
Access	R/WC
Size:	16 bits

Bits	Description
4:0	Intel Reserved

ERRCMD—Error Command Register (Device 0)

Address Offset	CA–CBh
Default Value	0000h
Access	RO, R/W
Size:	16 bits

Bits	Description
4:0	Intel Reserved

CAPREG—Capability Identification Register (Device 0)

Address Offset	E4h–E8h
Default Value	000001060009h
Access	RO
Size:	40 bits

Bits	Description
15:8	**Next_Pointer.** This field has the value A0h pointing to the next capabilities register, AGP Capability Identifier Register (ACAPID). Since AGP is disabled (IGDIS = 0), this becomes the last pointer in the device, and it is set to 00h signifying the end of the capabilities linked list.

9.3.2 Host-to-AGP Bridge Registers (Device 1)

Device 1 does not exist on the 82865GV component. The Device 1 registers described in Chapter 3 are not in the 82865GV. For the 82865GV, these register address locations are Intel Reserved.

9.4 Synchronous Display Differences

The synchronous display is different between the 82865G and 82865GV. For the 82865GV, replace Section 5.5.3, *Synchronous Display* with the following:

Synchronous Display

Microsoft Windows* 98 and Windows* 2000/XP have enabled support for multi-monitor display. Synchronous mode will display the same information on multiple displays.

Since the 82865GV GMCH has several display ports available for its single pipe, it can support synchronous display on two displays unless one of the displays is a TV. No synchronous display is available when a TV is in use. The GMCH does not support two synchronous digital displays. The 82865GV GMCH cannot drive multiple displays concurrently (different data or timings). Since the 82865GV GMCH does not support AGP, it is incapable of operating in parallel with an external AGP device. The 82865GV GMCH can, however, work in conjunction with a PCI graphics adapter.

Intel® 82865GV GMCH Ballout 10

The chapter provides the ballout for the 82865GV component only. Table 55 provides the 82865GV ballout arranged alphabetically by signal name. The differences between the ballout list in this chapter and the ballout list in Chapter 7 is that the AGP signals have been replaced with their corresponding DVO signal names. Since not all 82865G AGP signals are multiplexed, the remaining non-multiplexed 82865G AGP signals are shown in Table 55 as TESTP[153:140].

The ballout footprint is shown in Figure 23 and Figure 24. These figures represent the ballout arranged by ball number. Table 55 provides the ballout arranged alphabetically by signal name.

Note: The following notes apply to the ballout.

1. NC = No Connect
2. RSVD = These reserved balls should not be connected and should be allowed to float.
3. Shaded cells in Figure 23 and Figure 24 do not have a ball.

Figure 23. Intel® 82865GV GMCH Ballout Diagram (Top View—Left Side)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AR	NC		NC	VSS	VCC_DDR		VSS		VSS		VSS		VSS		VCC_DDR	VSS		
AP		RSVD	SDQ_A26	SMAB_A3	SMAB_A4	SDM_A3	SDQ_A25	SDQ_A24	SDQ_A23	SMAA_A8	SDQ_A22	SMAA_A9	SDQS_A2	SDQ_A16	SDQ_A20	SCKE_A3	SDQ_A11	SDQ_A14
AN	RSVD	SDQ_A31		VSS	SMAA_A3	VSS	SDQ_A29	VSS	SDQ_A19	VSS	SMAA_A7	VSS	SMAA_A11	VSS	SMAA_A12	VSS	SCKE_A1	VSS
AM	VSS	SMAB_A2	SDQ_A27		SDQ_A30	SDQS_A3	VSS	SDQ_A28	VSS	SMAB_A5	VSS	SDM_A2	VSS	SDQ_A17	VSS	SCKE_A2	VSS	SDQ_A15
AL	VCCA_DDR	SMAB_A1	SMAA_A1	VSS		SMAA_A4	SMAB_B3	SMAA_A6	SMAB_B4	SMAA_A5	SMAA_B6	SDQ_A18	SMAA_B8	SDQ_A21	SMAA_B11	SCKE_A0	SDQ_B20	SDQ_A10
AK		SCMD CLK_A3#	SCMD CLK_A3	SCMD CLK_A0	SCMD CLK_A0#		SMAA_A2	VSS	SMAA_B4	VSS	SDQ_B24	VSS	SDQ_B19	VSS	SDQ_B21	VSS	SCKE_B0	VSS
AJ	VSS	SMAA_A0	SMAA_ A10	VSS	SMAA_B1	SCMDCLK_ B3		SDM_B3	SDQ_B29	SDQ_B28		SDQ_B22		SMAA_B9		SMAA_B12		SDQ_B15
AH		SBA_A1	VSS	SDQ_A32	SDQ_A36	VSS	SCMD CLK_B3#		SDQS_B3	SDQ_B25		VSS		VSS		VSS		VSS
AG	VSS	SDQ_A33	SDQ_A37	VSS	SMAA_B0	SCMD CLK_B0#	SCMD CLK_B0	VSS	SDQ_B26	VSS	SMAA_B5	VSS	SDQ_B18	VSS	SDQS_B2	VSS	SCKE_B2	VSS
AF		SDQS_A4	VSS	SDQ_A34	SDM_A4	VSS	SMAA_ B10	SDQ_B31	SDQ_B27		VSS	VSS	NC	VSS	SMAA_B7	VSS	SCKE_B1	VSS
AE	VSS	SDQ_A38	SBA_A0	VSS	SDQ_B36	SDQ_B32			SMAB_B1	VSS	VSS	SMAA_B3	SMAB_B5	SDQ_B23	SDM_B2	SDQ_B17	SDQ_B16	SCKE_B3
AD		SDQ_A39	VSS	SDQ_A35	SDQ_A44	VSS	SDQS_B4	VSS	SMAA_B2	SMAB_B2	SDQ_B30							
AC	VSS	SDQ_A40	SAS_A#	VSS	SDM_B4	SDQ_B34			SDQ_B33	VCCA_ DDR	VCCA_ DDR							
AB		SWE_A#	VSS	SDQ_A45	SDQ_A41	VSS	SDQ_B37	VSS	VSS	VSS	VCCA_ DDR							
AA	VCC_DDR	SCS_A0#	SMYRCO MP	VSS	SDQ_B44	SDQ_B40			SDQ_B39	SDQ_B38	SBA_B1							
Y	VSS	SCAS_A#	VSS	SCS_A2#	SCS_A1#	VSS	SDQ_B35	VSS	VSS	VSS	SBA_B0					VCC	VCC	VCC
W		SCS_A3#	SDM_A5	VSS	SCAS_B#	SDQ_B41			SWE_B#	SRAS_B#	SCS_B3#					VCC	VCC	VSS
V		SDQS_A5	VSS	SDQ_A42	SDQ_A43	VSS	SDQ_B45	VSS	VSS	VSS	SCS_B2#					VCC	VSS	VCC
U		SDQ_A46	SDQ_A47	VSS	SDM_B5	SDQS_B5			SDQ_B42	SCS_B0#	SDQ_B46					VCC	VSS	VSS
T	VSS	SDQ_A48	VSS	SDQ_A49	SDQ_A52	VSS	SCS_B1#	VSS	VSS	VSS	SDQ_B43					VCC	VCC	VCC
R	VCC_DDR	SMYRCOM PVOH	SMYRCO MPVOL	VSS	SDQ_B52	SDQ_B49			SDQ_B47	SDQ_B53	NC							
P		SDQ_A53	VSS	SCMD CLK_A5#	SCMDC LK_A5	VSS	SDQ_B48	VSS	VSS	VSS	SDQ_B54							
N	VSS	SCMD CLK_A2#	SCMD CLK_A2	VSS	SCMD CLK_B5	SCMD CLK_B5#			SCMD CLK_B2	SCMD CLK_B2#	SDQ_B60							
M		SDM_A6	VSS	SDQS_A6	NC	VSS	SDM_B6	VSS	VSS	VSS	SDQ_B61							
L	VSS	SDQ_A54	SDQ_A55	SDQ_B55	VSS	SDQ_B51			SDQS_B6	VSS	VSS	VSS	HA5#	HREQ2#	DEFER#	PROCHOT#	HDSTBP1#	HD21#
K		SDQ_A50	VSS	SDQ_A51	SDQ_A60	SDQ_B56	VSS	SDQ_B50	VSS		VSS	HA26#	HA8#	VSS	HIT#	VSS	HDSTBNB_1	VSS
J	VSS	SDQ_A61	SDQ_A56	VSS	SDM_B7	SDQS_B7	SDQ_B62	VSS	HA21#	HA30#	HA11#	HA15#	HREQ1#	VSS	HREQ4#	VSS	HD28#	VSS
H		SDQ_A57	VSS	SDM_A7	SDQS_A7	VSS	SDQ_B57		HA25#	VSS		VSS		VSS		VSS		VSS
G	VSS	SDQ_A62	SDQ_B59	SDQ_B63	VSS	HA29#		VSS	HA22#	HA31#		DRDY#		RS0#		HD16#		HD23#
F		SDQ_A63	SDQ_A59	SDQ_B58	HA28#		HA23#	HA19#	ADS#	VSS	HA16#	VSS	HDVREF	VSS	HD24#	VSS	HD19#	VSS
E	VCC_DDR	SMVREF_A	SDQ_A58	HA27#		HA13#	HA6#	HA24#	DBSY#	NC	HLOCK#	HDRCOMP	HITM#	HD1#	HD27#	HD9#	HD18#	HD8#
D	VSS	HA17#	VSS		VSS	HA4#	VSS	HADSTB1#	VSS	HA3#	VSS	HTRDY#	VSS	HD5#	VSS	HD3#	VSS	HD15#
C	NC	HA20#		HA18#	HA10#	HA9#	HREQ3#	VSS	RS1#	VSS	HD SWING	VSS	NC	VSS	HD7#	VSS	HDSTBNB_0	VSS
B		NC	HA14#	HA7#	HA12#	HADSTB0#	HREQ0#	BNR#	RS2#	BPRI#	NC	BREQ0#	HD0#	HD4#	HD2#	HD6#	HDSTBP0#	HD12#
A	NC		NC	VSS	VCCA_FSB		VSS		VSS		VSS		VSS		VTT	VSS		
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18

Figure 24. Intel® 82865GV GMCH Ballout Diagram (Top View—Right Side)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	VSS	VCC_DDR		VSS		VSS		VSS		VCC_DDR		VCC_DDR	VCC_DDR	NC		RSVD	AR
SCMD CLK_A1	SDM_A1	SDQS_A1	SDQ_A8	SDQ_A7	SDM_A0	SDQ_A1	SDQ_A0	SMVREF_B	EXTTS#	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	NC		AP
SCMD CLK_A1#	VSS	SDQ_A13	VSS	SDQ_A3	VSS	SDQS_A0	VSS	SMXRCOMPVOH	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR		VCC_DDR	NC	AN
VSS	SCMD CLK_A4	VSS	SDQ_A9	VSS	SDQ_A2	VSS	SDQ_A4	VSS	VCC_DDR	VCC_DDR	VCC_DDR	VCC_DDR		VCC_DDR	VCC_DDR	VCC_DDR	AM
SDQ_B11	SCMD CLK_A4#	SCMD CLK_B4#	SDQ_A12	SDQ_B9	SDQ_A6	SDQ_B2	SDQ_A5	SMXRCOMPVOL	SDQ_B4	VCC_DDR	VCC_DDR		HI7	HI5	HI6	VSS	AL
SDQ_B10	VSS	SCMD CLK_B4	VSS	SDQ_B12	VSS	SDQ_B6	VSS	SMX RCOMP	VSS	CI0		HI4	RSTIN#	VSS	HI2		AK
	SDQ_B14		SDQ_B13		NC		SDQ_B0	VSS	RSVD		CISTRF	CISTRS	VSS	HI10	HI8	VSS	AJ
	VSS		VSS		VSS		VSS	CI9		CI1	VSS	HISTRF	HISTRS	VSS	HI9		AH
SCMD CLK_B1#	VSS	SDM_B1	VSS	SDQS_B1	SDQ_B7	SDM_B0	TESTIN#	RSVD	VSS	CI7	CI10	HI3	VSS	HI1	CI_RCOMP	VCCA_AGP	AG
SCMD CLK_B1	VSS	SDQS_B0	VSS	NC	SDQ_B5	VSS		VSS	CI6	CI3	VSS	HI0	CI_VREF	VSS	CI_SWING		AF
SDQ_B8	SDQ_B3	SDQ_B1	PWROK	VSS	VSS	VSS	VSS	CI8			DVOB_HSYNC	DVOB_D0	VSS	HI_SWING	HI_VREF	VSS	AE
						CI2	VSS	VSS	VSS	CI4	VSS	DVOB_D1	HI_RCOMP	VSS	GVREF		AD
						DVOB_VSYNC	CI5	DVOB_D2			DVOB_CLK	DVOB_CLK#	VSS	TESTP141	DVOB CRCOMP	VSS	AC
						DVOB_D5	VSS	VSS	VSS	DVOB_D4	VSS	MDVI_CLK	MI2CDATA	VSS	TESTP144		AB
						DVOB_D10	DVOB_D3	DVOB_D6			DVOB_D9	DVOB_D8	VSS	TESTP140	DVOC_VSYNC	VSS	AA
VCC	VCC					VCCA_AGP	VSS	VSS	VSS	DVOB_D7	VSS	DVOC_D1	DVOC_HSYNC	VSS	DVOC_BLANK#	VCC_AGP	Y
VSS	VCC					MDDC_CLK	DVOB_D11	DVOB_FLDSTL			DVOBC_CLKINT	DVOB_BLANK#	VSS	DVOC_D3	DVOC_D0		W
VSS	VCC					MI2CCLK	VSS	VSS	VSS	MDDC_DATA	VSS	DVOC_CLK#	DVOC_CLK	VSS	DVOC_D2		V
VCC	VCC					TESTP145	ADDID5	ADDID4			MDVI_DATA	ADDID6	VSS	DVOC_D4	DVOC_D5		U
VCC	VCC					TESTP146	VSS	VSS	VSS	ADDID7	VSS	DVOC_D9	DVOC_D6	VSS	DVOC_D7	VSS	T
						VCC	TESTP147	TESTP148			ADDID0	ADDID3	VSS	ADDID2	DVOC_D8	VSS	R
						VCC	VCC	VSS	VSS	ADDID1	VSS	DVOC_D10	DVOBC_INTR#	VSS	DVOC_D11		P
						VCC	VCC	VCC			TESTP142	TESTP150	VSS	TESTP149	TESTP151	VSS	N
						VCC	VCC	VCC	VCC	TESTP143	VSS	TESTP153	TESTP152	VSS	DVOC_FLDSTL		M
DINV1#	HD33#	HD41#	DINV2#	BSEL0	BSEL1	VCC	VCC	VCC		VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	L
HD31#	VSS	HD38#	VSS	HD43#	VSS	VSS		VCC	VCC	VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP		K
HD20#	VSS	HD32#	VSS	HD34#	VSS	HD44#	VSS	VCC	VCC	VCC	VCC	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	VCC_AGP	J
	VSS		VSS		VSS		HD45#	VSS	VSS	BLUE	GREEN	VSS	GCLKIN	DDCA_DATA	VSS		H
	HD22#		HD29#		HD39#		HD40#	HDSTBP2#	HD46#		BLUE#	GREEN#	DREFCLK	HSYNC	VCC_DAC	VCC_DAC	G
HD17#	VSS	HD25#	VSS	HD35#	VSS	HD36#	VSS	HDSTBN2#	VSS	VTT		VSS	RED	VSS	DDCA_CLK	VSS	F
HD30#	HD14#	HD26#	HD49#	HD37#	HDSTBN3#	HD42#	HD58#	HD47#	CPURST#	VTT	VTT		RED#	VSS	VSYNC	VSS	E
VSS	HD11#	VSS	HD53#	VSS	HDSTBP3#	VSS	HD56#	VSS	HD62#	VTT	VTT	VTT		VSSA_DAC	REFSET	VSS	D
DINV0#	VSS	DINV3#	VSS	HD54#	VSS	HD57#	VSS	HD60#	VSS	HCLKN	VTT	VTT	VSS		VCCA_DAC	NC	C
HD13#	HD10#	HD52#	HD50#	HD48#	HD51#	HD55#	HD59#	HD61#	HD63#	HCLKP	VTT	VTT	VCCA_FSB	VCCA_DPLL	NC		B
	VSS	VTT		VSS		VSS		VSS		VSS	VTT	VTT	VTT	NC			A
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

This page is intentionally left blank.

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
ADDID0	R6
ADDID1	P7
ADDID2	R3
ADDID3	R5
ADDID4	U9
ADDID5	U10
ADDID6	U5
ADDID7	T7
ADS#	F27
BLUE	H7
BLUE#	G6
BNR#	B28
BPRI#	B26
BREQ0#	B24
BSEL0	L13
BSEL1	L12
CI_RCOMP	AG2
CI_SWING	AF2
CI_VREF	AF4
CI0	AK7
CI1	AH7
CI10	AG6
CI2	AD11
CI3	AF7
CI4	AD7
CI5	AC10
CI6	AF8
CI7	AG7
CI8	AE9
CI9	AH9
CISTRF	AJ6
CISTRS	AJ5
CPURST#	E8
DBSY#	E27
DDCA_CLK	F2
DDCA_DATA	H3
DEFER#	L21
DINV0#	C17
DINV1#	L17
DINV2#	L14

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
DINV3#	C15
DRDY#	G24
DREFCLK	G4
DVOB_BLANK#	W5
DVOBC_CLKINT	W6
DVOBC_INTR#	P4
DVOB_CLK	AC6
DVOB_CLK#	AC5
DVOBCRCOMP	AC2
DVOB_D0	AE5
DVOB_D1	AD5
DVOB_D2	AC9
DVOB_D3	AA10
DVOB_D4	AB7
DVOB_D5	AB11
DVOB_D6	AA9
DVOB_D7	Y7
DVOB_D8	AA5
DVOB_D9	AA6
DVOB_D10	AA11
DVOB_D11	W10
DVOB_FLDSTL	W9
DVOB_HSYNC	AE6
DVOB_VSYNC	AC11
DVOC_BLANK#	Y2
DVOC_CLK	V4
DVOC_CLK#	V5
DVOC_D0	W2
DVOC_D1	Y5
DVOC_D2	V2
DVOC_D3	W3
DVOC_D4	U3
DVOC_D5	U2
DVOC_D6	T4
DVOC_D7	T2
DVOC_D8	R2
DVOC_D9	T5
DVOC_D10	P5
DVOC_D11	P2
DVOC_FLDSTL	M2

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
DVOC_HSYNC	Y4
DVOC_VSYNC	AA2
EXTTS#	AP8
GCLKIN	H4
GREEN	H6
GREEN#	G5
GVREF	AD2
HA3#	D26
HA4#	D30
HA5#	L23
HA6#	E29
HA7#	B32
HA8#	K23
HA9#	C30
HA10#	C31
HA11#	J25
HA12#	B31
HA13#	E30
HA14#	B33
HA15#	J24
HA16#	F25
HA17#	D34
HA18#	C32
HA19#	F28
HA20#	C34
HA21#	J27
HA22#	G27
HA23#	F29
HA24#	E28
HA25#	H27
HA26#	K24
HA27#	E32
HA28#	F31
HA29#	G30
HA30#	J26
HA31#	G26
HADSTB0#	B30
HADSTB1#	D28
HCLKN	C7
HCLKP	B7

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
HD0#	B23
HD1#	E22
HD2#	B21
HD3#	D20
HD4#	B22
HD5#	D22
HD6#	B20
HD7#	C21
HD8#	E18
HD9#	E20
HD10#	B16
HD11#	D16
HD12#	B18
HD13#	B17
HD14#	E16
HD15#	D18
HD16#	G20
HD17#	F17
HD18#	E19
HD19#	F19
HD20#	J17
HD21#	L18
HD22#	G16
HD23#	G18
HD24#	F21
HD25#	F15
HD26#	E15
HD27#	E21
HD28#	J19
HD29#	G14
HD30#	E17
HD31#	K17
HD32#	J15
HD33#	L16
HD34#	J13
HD35#	F13
HD36#	F11
HD37#	E13
HD38#	K15
HD39#	G12

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
HD40#	G10
HD41#	L15
HD42#	E11
HD43#	K13
HD44#	J11
HD45#	H10
HD46#	G8
HD47#	E9
HD48#	B13
HD49#	E14
HD50#	B14
HD51#	B12
HD52#	B15
HD53#	D14
HD54#	C13
HD55#	B11
HD56#	D10
HD57#	C11
HD58#	E10
HD59#	B10
HD60#	C9
HD61#	B9
HD62#	D8
HD63#	B8
HDRCOMP	E24
HDSTBN0#	C19
HDSTBN1#	K19
HDSTBN2#	F9
HDSTBN3#	E12
HDSTBP0#	B19
HDSTBP1#	L19
HDSTBP2#	G9
HDSTBP3#	D12
HDSWING	C25
HDVREF	F23
HI_RCOMP	AD4
HI_SWING	AE3
HI_VREF	AE2
HI0	AF5
HI1	AG3

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
HI2	AK2
HI3	AG5
HI4	AK5
HI5	AL3
HI6	AL2
HI7	AL4
HI8	AJ2
HI9	AH2
HI10	AJ3
HISTRF	AH5
HISTRS	AH4
HIT#	K21
HITM#	E23
HLOCK#	E25
HREQ0#	B29
HREQ1#	J23
HREQ2#	L22
HREQ3#	C29
HREQ4#	J21
HSYNC	G3
HTRDY#	D24
MDDC_CLK	W11
MDDC_DATA	V7
MDVI_CLK	AB5
MDVI_DATA	U6
MI2CCLK	V11
MI2CDATA	AB4
NC	A3
NC	A33
NC	A35
NC	AF13
NC	AF23
NC	AJ12
NC	AN1
NC	AP2
NC	AR3
NC	AR33
NC	AR35
NC	B2
NC	B25

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
NC	B34
NC	C1
NC	C23
NC	C35
NC	E26
NC	M31
NC	R25
PROCHOT#	L20
PWROK	AE14
RED	F4
RED#	E4
REFSET	D2
RS0#	G22
RS1#	C27
RS2#	B27
RSTIN#	AK4
RSVD	AJ8
RSVD	AR1
RSVD	AP34
RSVD	AG9
RSVD	AN35
TESTIN#	AG10
SBA_A0	AE33
SBA_A1	AH34
SBA_B0	Y25
SBA_B1	AA25
SCAS_A#	Y34
SCAS_B#	W31
SCKE_A0	AL20
SCKE_A1	AN19
SCKE_A2	AM20
SCKE_A3	AP20
SCKE_B0	AK19
SCKE_B1	AF19
SCKE_B2	AG19
SCKE_B3	AE18
SCMDCLK_A0	AK32
SCMDCLK_A0#	AK31
SCMDCLK_A1	AP17
SCMDCLK_A1#	AN17

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SCMDCLK_A2	N33
SCMDCLK_A2#	N34
SCMDCLK_A3	AK33
SCMDCLK_A3#	AK34
SCMDCLK_A4	AM16
SCMDCLK_A4#	AL16
SCMDCLK_A5	P31
SCMDCLK_A5#	P32
SCMDCLK_B0	AG29
SCMDCLK_B0#	AG30
SCMDCLK_B1	AF17
SCMDCLK_B1#	AG17
SCMDCLK_B2	N27
SCMDCLK_B2#	N26
SCMDCLK_B3	AJ30
SCMDCLK_B3#	AH29
SCMDCLK_B4	AK15
SCMDCLK_B4#	AL15
SCMDCLK_B5	N31
SCMDCLK_B5#	N30
SCS_A0#	AA34
SCS_A1#	Y31
SCS_A2#	Y32
SCS_A3#	W34
SCS_B0#	U26
SCS_B1#	T29
SCS_B2#	V25
SCS_B3#	W25
SDM_A0	AP12
SDM_A1	AP16
SDM_A2	AM24
SDM_A3	AP30
SDM_A4	AF31
SDM_A5	W33
SDM_A6	M34
SDM_A7	H32
SDM_B0	AG11
SDM_B1	AG15
SDM_B2	AE21
SDM_B3	AJ28

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SDM_B4	AC31
SDM_B5	U31
SDM_B6	M29
SDM_B7	J31
SDQ_A_17	AM22
SDQ_A0	AP10
SDQ_A1	AP11
SDQ_A2	AM12
SDQ_A3	AN13
SDQ_A4	AM10
SDQ_A5	AL10
SDQ_A6	AL12
SDQ_A7	AP13
SDQ_A8	AP14
SDQ_A9	AM14
SDQ_A10	AL18
SDQ_A11	AP19
SDQ_A12	AL14
SDQ_A13	AN15
SDQ_A14	AP18
SDQ_A15	AM18
SDQ_A16	AP22
SDQ_A18	AL24
SDQ_A19	AN27
SDQ_A20	AP21
SDQ_A21	AL22
SDQ_A22	AP25
SDQ_A23	AP27
SDQ_A24	AP28
SDQ_A25	AP29
SDQ_A26	AP33
SDQ_A27	AM33
SDQ_A28	AM28
SDQ_A29	AN29
SDQ_A30	AM31
SDQ_A31	AN34
SDQ_A32	AH32
SDQ_A33	AG34
SDQ_A34	AF32
SDQ_A35	AD32

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SDQ_A36	AH31
SDQ_A37	AG33
SDQ_A38	AE34
SDQ_A39	AD34
SDQ_A40	AC34
SDQ_A41	AB31
SDQ_A42	V32
SDQ_A43	V31
SDQ_A44	AD31
SDQ_A45	AB32
SDQ_A46	U34
SDQ_A47	U33
SDQ_A48	T34
SDQ_A49	T32
SDQ_A50	K34
SDQ_A51	K32
SDQ_A52	T31
SDQ_A53	P34
SDQ_A54	L34
SDQ_A55	L33
SDQ_A56	J33
SDQ_A57	H34
SDQ_A58	E33
SDQ_A59	F33
SDQ_A60	K31
SDQ_A61	J34
SDQ_A62	G34
SDQ_A63	F34
SDQ_B0	AJ10
SDQ_B1	AE15
SDQ_B2	AL11
SDQ_B3	AE16
SDQ_B4	AL8
SDQ_B5	AF12
SDQ_B6	AK11
SDQ_B7	AG12
SDQ_B8	AE17
SDQ_B9	AL13
SDQ_B10	AK17
SDQ_B11	AL17

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SDQ_B12	AK13
SDQ_B13	AJ14
SDQ_B14	AJ16
SDQ_B15	AJ18
SDQ_B16	AE19
SDQ_B17	AE20
SDQ_B18	AG23
SDQ_B19	AK23
SDQ_B20	AL19
SDQ_B21	AK21
SDQ_B22	AJ24
SDQ_B23	AE22
SDQ_B24	AK25
SDQ_B25	AH26
SDQ_B26	AG27
SDQ_B27	AF27
SDQ_B28	AJ26
SDQ_B29	AJ27
SDQ_B30	AD25
SDQ_B31	AF28
SDQ_B32	AE30
SDQ_B33	AC27
SDQ_B34	AC30
SDQ_B35	Y29
SDQ_B36	AE31
SDQ_B37	AB29
SDQ_B38	AA26
SDQ_B39	AA27
SDQ_B40	AA30
SDQ_B41	W30
SDQ_B42	U27
SDQ_B43	T25
SDQ_B44	AA31
SDQ_B45	V29
SDQ_B46	U25
SDQ_B47	R27
SDQ_B48	P29
SDQ_B49	R30
SDQ_B50	K28
SDQ_B51	L30

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SDQ_B52	R31
SDQ_B53	R26
SDQ_B54	P25
SDQ_B55	L32
SDQ_B56	K30
SDQ_B57	H29
SDQ_B58	F32
SDQ_B59	G33
SDQ_B60	N25
SDQ_B61	M25
SDQ_B62	J29
SDQ_B63	G32
SDQS_A0	AN11
SDQS_A1	AP15
SDQS_A2	AP23
SDQS_A3	AM30
SDQS_A4	AF34
SDQS_A5	V34
SDQS_A6	M32
SDQS_A7	H31
SDQS_B0	AF15
SDQS_B1	AG13
SDQS_B2	AG21
SDQS_B3	AH27
SDQS_B4	AD29
SDQS_B5	U30
SDQS_B6	L27
SDQS_B7	J30
SMAA_A0	AJ34
SMAA_A1	AL33
SMAA_A2	AK29
SMAA_A3	AN31
SMAA_A4	AL30
SMAA_A5	AL26
SMAA_A6	AL28
SMAA_A7	AN25
SMAA_A8	AP26
SMAA_A9	AP24
SMAA_A10	AJ33
SMAA_A11	AN23

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
SMAA_A12	AN21
SMAA_B0	AG31
SMAA_B1	AJ31
SMAA_B2	AD27
SMAA_B3	AE24
SMAA_B4	AK27
SMAA_B5	AG25
SMAA_B6	AL25
SMAA_B7	AF21
SMAA_B8	AL23
SMAA_B9	AJ22
SMAA_B10	AF29
SMAA_B11	AL21
SMAA_B12	AJ20
SMAB_A1	AL34
SMAB_A2	AM34
SMAB_A3	AP32
SMAB_A4	AP31
SMAB_A5	AM26
SMAB_B1	AE27
SMAB_B2	AD26
SMAB_B3	AL29
SMAB_B4	AL27
SMAB_B5	AE23
SMVREF_A	E34
SMVREF_B	AP9
SMXRCOMP	AK9
SMXRCOMPVOH	AN9
SMXRCOMPVOL	AL9
SMYRCOMP	AA33
SMYRCOMPVOH	R34
SMYRCOMPVOL	R33
SRAS_A#	AC33
SRAS_B#	W26
SWE_A#	AB34
SWE_B#	W27
TESTP140	AA3
TESTP141	AC3
TESTP142	N6
TESTP143	M7

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
TESTP144	AB2
TESTP145	U11
TESTP146	T11
TESTP147	R10
TESTP148	R9
TESTP149	N3
TESTP150	N5
TESTP151	N2
TESTP152	M4
TESTP153	M5
VCC	J7
VCC	J6
VCC	J8
VCC	J9
VCC	K6
VCC	K7
VCC	K8
VCC	K9
VCC	L10
VCC	L11
VCC	L6
VCC	L7
VCC	L9
VCC	M10
VCC	M11
VCC	M8
VCC	M9
VCC	N10
VCC	N11
VCC	N9
VCC	P10
VCC	P11
VCC	R11
VCC	T16
VCC	T17
VCC	T18
VCC	T19
VCC	T20
VCC	U16
VCC	U17

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VCC	U20
VCC	V16
VCC	V18
VCC	V20
VCC	W16
VCC	W19
VCC	W20
VCC	Y16
VCC	Y17
VCC	Y18
VCC	Y19
VCC	Y20
VCC_AGP	J1
VCC_AGP	J2
VCC_AGP	J3
VCC_AGP	J4
VCC_AGP	J5
VCC_AGP	K2
VCC_AGP	K3
VCC_AGP	K4
VCC_AGP	K5
VCC_AGP	L1
VCC_AGP	L2
VCC_AGP	L3
VCC_AGP	L4
VCC_AGP	L5
VCC_AGP	Y1
VCC_DAC	G1
VCC_DAC	G2
VCC_DDR	AA35
VCC_DDR	AL6
VCC_DDR	AL7
VCC_DDR	AM1
VCC_DDR	AM2
VCC_DDR	AM3
VCC_DDR	AM5
VCC_DDR	AM6
VCC_DDR	AM7
VCC_DDR	AM8
VCC_DDR	AN2

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VCC_DDR	AN4
VCC_DDR	AN5
VCC_DDR	AN6
VCC_DDR	AN7
VCC_DDR	AN8
VCC_DDR	AP3
VCC_DDR	AP4
VCC_DDR	AP5
VCC_DDR	AP6
VCC_DDR	AP7
VCC_DDR	AR15
VCC_DDR	AR21
VCC_DDR	AR31
VCC_DDR	AR4
VCC_DDR	AR5
VCC_DDR	AR7
VCC_DDR	E35
VCC_DDR	R35
VCCA_AGP	AG1
VCCA_AGP	Y11
VCCA_DAC	C2
VCCA_DDR	AC26
VCCA_DDR	AL35
VCCA_DDR	AB25
VCCA_DDR	AC25
VCCA_DPLL	B3
VCCA_FSB	A31
VCCA_FSB	B4
VSS	AF24
VSS	AF25
VSS	AF3
VSS	AF30
VSS	AF33
VSS	AF6
VSS	AF9
VSS	AG14
VSS	AG16
VSS	AG18
VSS	AG20
VSS	AG22

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	AG24
VSS	AG26
VSS	AG28
VSS	AG32
VSS	AG35
VSS	AG4
VSS	AG8
VSS	AH10
VSS	AH12
VSS	AH14
VSS	AH16
VSS	AH18
VSS	AN30
VSS	AN32
VSS	AR11
VSS	AR13
VSS	AR16
VSS	AR20
VSS	AR23
VSS	AR25
VSS	AR27
VSS	AR29
VSS	AR32
VSS	AR9
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20
VSS	C22
VSS	C24
VSS	C26
VSS	C28
VSS	C4
VSS	C8
VSS	D1
VSS	D11
VSS	D13
VSS	D15

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	D17
VSS	D19
VSS	K29
VSS	K33
VSS	L24
VSS	L25
VSS	L26
VSS	L31
VSS	L35
VSS	M26
VSS	M27
VSS	M28
VSS	M3
VSS	M30
VSS	M33
VSS	M6
VSS	N1
VSS	N32
VSS	N35
VSS	N4
VSS	P26
VSS	P27
VSS	P28
VSS	P3
VSS	P30
VSS	P33
VSS	P6
VSS	P8
VSS	P9
VSS	R1
VSS	R32
VSS	R4
VSS	T1
VSS	T10
VSS	A11
VSS	A13
VSS	A16
VSS	A20
VSS	A23
VSS	A25

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	A27
VSS	A29
VSS	A32
VSS	A7
VSS	A9
VSS	AA1
VSS	AA32
VSS	AA4
VSS	AB10
VSS	AB26
VSS	AB27
VSS	AB28
VSS	AB3
VSS	AB30
VSS	AB33
VSS	AB6
VSS	AB8
VSS	AB9
VSS	AH20
VSS	AH22
VSS	AH24
VSS	AH3
VSS	AH30
VSS	AH33
VSS	AH6
VSS	AJ1
VSS	AJ32
VSS	AJ35
VSS	AJ4
VSS	AJ9
VSS	AK10
VSS	AK12
VSS	AK14
VSS	AK16
VSS	AK18
VSS	AK20
VSS	AK22
VSS	AK24
VSS	AK26
VSS	AK28

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	AK3
VSS	AK8
VSS	D21
VSS	D23
VSS	D25
VSS	D27
VSS	D29
VSS	D31
VSS	D33
VSS	D35
VSS	D9
VSS	E1
VSS	E3
VSS	F1
VSS	F10
VSS	F12
VSS	F14
VSS	F16
VSS	F18
VSS	F20
VSS	F22
VSS	F24
VSS	F26
VSS	F3
VSS	F5
VSS	F8
VSS	G28
VSS	G31
VSS	G35
VSS	H12
VSS	H14
VSS	H16
VSS	T26
VSS	T27
VSS	T28
VSS	T3
VSS	T30
VSS	T33
VSS	T35
VSS	T6

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	T8
VSS	T9
VSS	U18
VSS	U19
VSS	U32
VSS	U4
VSS	V10
VSS	V17
VSS	V19
VSS	V26
VSS	V27
VSS	V28
VSS	V3
VSS	V30
VSS	V33
VSS	V6
VSS	V8
VSS	V9
VSS	W17
VSS	W18
VSS	W32
VSS	W4
VSS	Y10
VSS	Y26
VSS	AC1
VSS	AC32
VSS	AC35
VSS	AC4
VSS	AD10
VSS	AD28
VSS	AD3
VSS	AD30
VSS	AD33
VSS	AD6
VSS	AD8
VSS	AD9
VSS	AE1
VSS	AE10
VSS	AE11
VSS	AE12

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	AE13
VSS	AE25
VSS	AE26
VSS	AE32
VSS	AE35
VSS	AE4
VSS	AF11
VSS	AF14
VSS	AF16
VSS	AF18
VSS	AF20
VSS	AF22
VSS	AL1
VSS	AL32
VSS	AM11
VSS	AM13
VSS	AM15
VSS	AM17
VSS	AM19
VSS	AM21
VSS	AM23
VSS	AM25
VSS	AM27
VSS	AM29
VSS	AM35
VSS	AM9
VSS	AN10
VSS	AN12
VSS	AN14
VSS	AN16
VSS	AN18
VSS	AN20
VSS	AN22
VSS	AN24
VSS	AN26
VSS	AN28
VSS	H18
VSS	H2
VSS	H20
VSS	H22

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	H24
VSS	H26
VSS	H30
VSS	H33

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	H5
VSS	H8
VSS	H9
VSS	J10
VSS	J12
VSS	J14
VSS	J16
VSS	J18
VSS	J20
VSS	J22
VSS	J28
VSS	J32
VSS	J35
VSS	K11
VSS	K12
VSS	K14
VSS	K16
VSS	K18
VSS	K20
VSS	K22
VSS	K25
VSS	K27
VSS	Y27
VSS	Y28

Table 55. Intel® 82865GV Ball List by Signal Name

Signal Name	Ball #
VSS	Y3
VSS	Y30
VSS	Y33
VSS	Y35
VSS	Y6
VSS	Y8
VSS	Y9
VSSA_DAC	D3
VSYNC	E2
VTT	A15
VTT	A21
VTT	A4
VTT	A5
VTT	A6
VTT	B5
VTT	B6
VTT	C5
VTT	C6
VTT	D5
VTT	D6
VTT	D7
VTT	E6
VTT	E7
VTT	F7

This page is intentionally left blank.

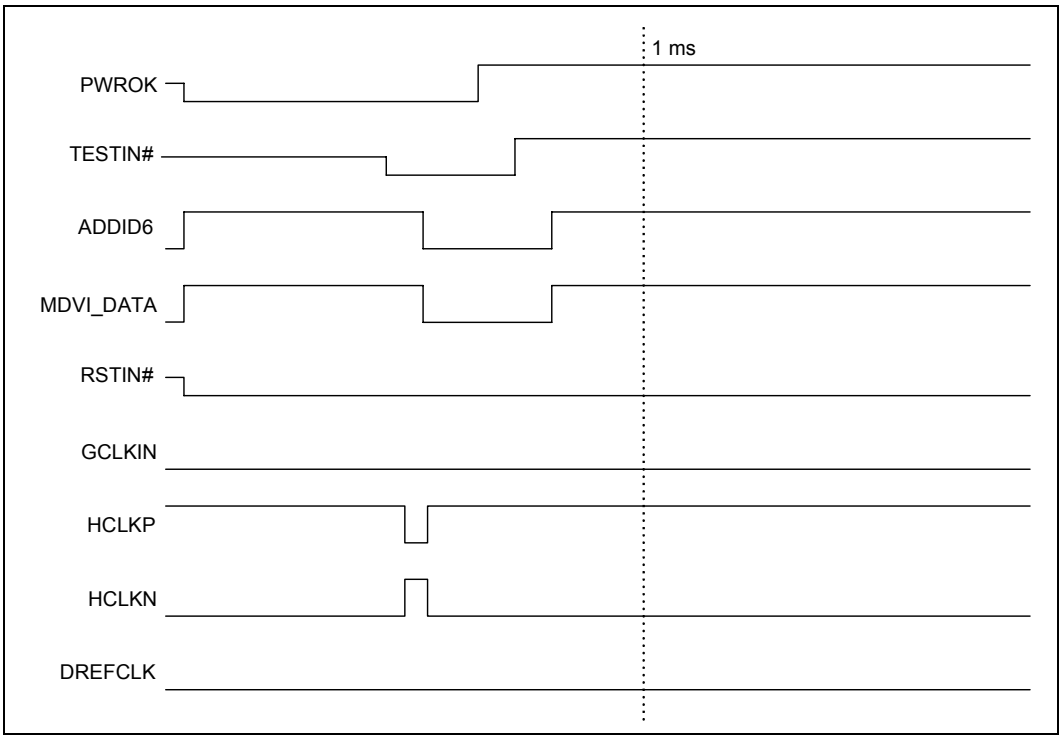
Intel® 82865GV GMCH Testability 11

The chapter provides the testability for the 82865GV component only. In the GMCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates, each with one input pin connected to it.

11.1 XOR Test Mode Initialization

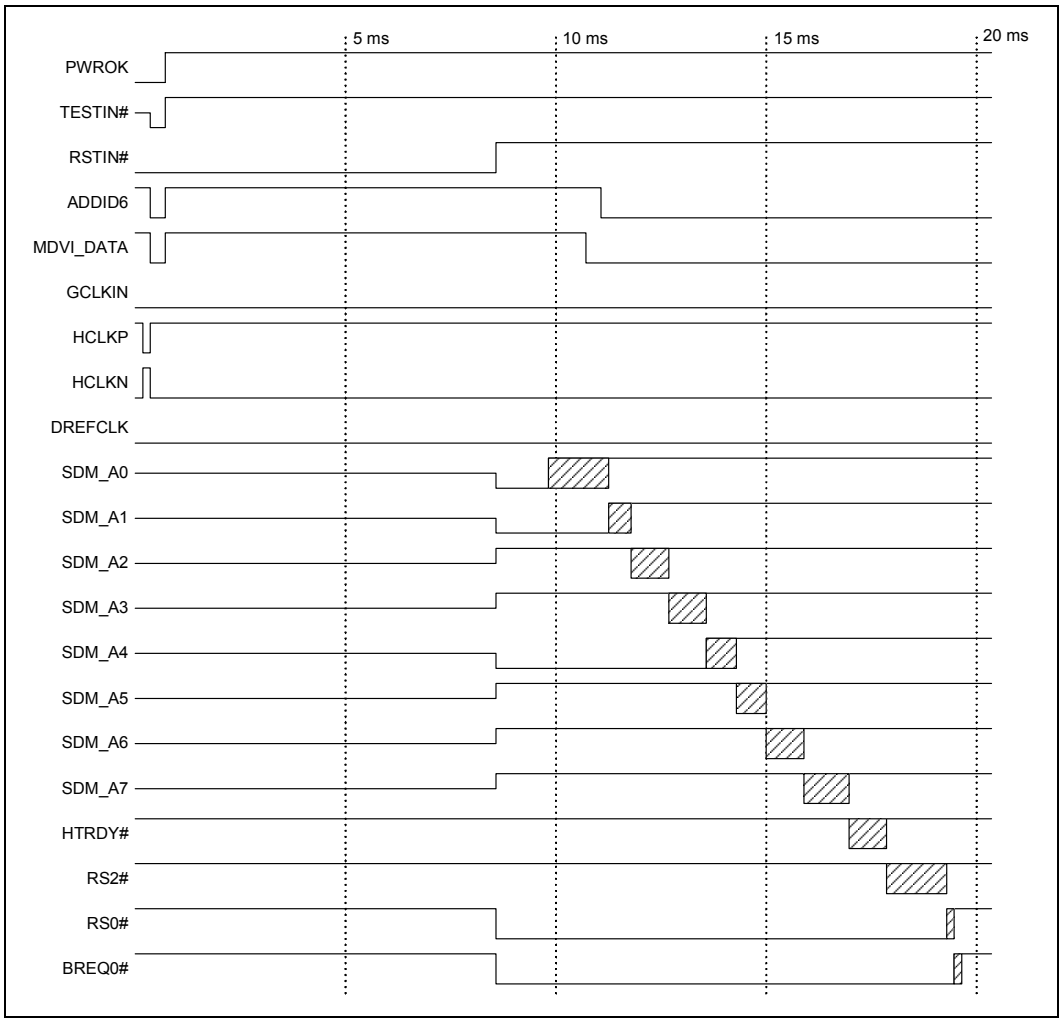
XOR test mode can be entered by driving ADDID6, ADDID7, TESTIN#, PWROK low, and RSTIN# low, then driving PWROK high, then RSTIN# high. XOR test mode via TESTIN# does not require a clock. But toggling of HCLKP and HCLKN as shown in Figure 25 is required for deterministic XOR operation when in AGP 2.0 mode. If the component is in AGP 3.0 mode, ADDID6, ADDID7, and DVOB_BLANK#must be driven high.

Figure 25. XOR Toggling of HCLKP and HCLKN



Pin testing will not start until RSTIN# is deasserted. Figure 26 shows chains that are tested sequentially. Note that for the GMCH, sequential testing is not required. All chains can be tested in parallel for test time reduction.

Figure 26. XOR Testing Chains Tested Sequentially



11.2 XOR Chain Definition

The GMCH has 10 XOR chains. The XOR chain outputs are driven out on the output pins as shown in Table 56. During fullwidth testing, XOR chain outputs will be visible on both pins (For example, xor_out0 will be visible on SDM_A0 and SDM_B0). During channel shared mode on the tester, outputs will be visible on their respective channels. (For example, in channel A mode, xor_out0 will be visible on SDM_A0 and the same will be visible on SDM_B0 in channel B mode.)

Table 56. XOR Chain Outputs

XOR Chain	DDR Output Pin Channel A	DDR Output Pin Channel B
xor_out0	SDM_A0	SDM_B0
xor_out1	SDM_A1	SDM_B1
xor_out2	SDM_A2	SDM_B2
xor_out3	SDM_A3	SDM_B3
xor_out4	SDM_A4	SDM_B4
xor_out5	SDM_A5	SDM_B5
xor_out6	SDM_A6	SDM_B6
xor_out7	SDM_A7	SDM_B7
xor_out8	HTRDY#	BPRI#
xor_out9	RS2#	DEFER#
xor_out10	RS0#	RS1#
xor_out11	BREQ0#	CPURST#

The following tables show the XOR chain pin mappings and their monitors for the GMCH.

Note: Notes for Table 57 through Table 67.

1. All XOR chains can be run in parallel, except chains 0 and 1, chains 0 and 2, and chains 2 and 4).
2. The channel A and channel B output pins for each chain show the same output.

Table 57. XOR Chain 0 (60 Inputs) Output Pins: SDM_A0, SDM_B0

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
CI7	AG7	DVOB_D0	AE5	TESTP149	N3
CI1	AH7	DVOB_D7	Y7	MI2CCLK	V11
CI2	AD11	DVOB_CLK	AC6	TESTP140	AA3
CI8	AE9	DVOB_D10	AA11	DVODC5	U2
CI9	AH9	DVOB_D4	AB7	TESTP151	N2
CI0	AK7	MDDC_CLK	W11	TESTP152	M4
CISTRF	AJ6	DVOB_D11	W10	TESTP142	N6
CISTRS	AJ5	DVOB_D8	AA5	ADDID2	R3
CI6	AF8	DVOB_D9	AA6	TESTP145	U11
CI3	AF7	MDDC_DATA	V7	ADDID7	T7
CI4	AD7	DVOBC_CLKINT	W6	ADDID0	R6
CI5	AC10	DVOB_FLDSTL	W9	ADDID5	U10
CI10	AG6	MDVI_CLK	AB5	ADDID3	R5
DVOB_VSYNC	AC11	TESTP144	AB2	ADDID4	U9
DVOB_D2	AC9	DVOB_BLANK#	W5	ADDID1	P7
DVOB_HSYNC	AE6	MDVI_DATA	U6	ADDID6	U5
DVOB_D5	AB11	TESTP153	M5	DDCA_CLK	F2
DVOB_D1	AD5	MI2CDATA	AB4	DDCA_DATA	H3
DVOB_D3	AA10	TESTP147	R10	VSYNC	E2
DVOB_D6	AA9	TESTP148	R9	RSVD	AJ8
Output Pins					
SDM_A0	AP12				
SDM_B0	AG11				

Table 58. XOR Chain 1 (33 Inputs) Output Pins: SDM_A1, SDM_B1

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HI7	AL4	HI8	AJ2	DVOC_D4	U3
HI4	AK5	HI9	AH2	DVOC_D6	T4
HI3	AG5	TESTP150	N5	DVOC_D8	R2
HI5	AL3	DVOC_D1	Y5	DVOC_D7	T2
HISTRF	AH5	DVOC_VSYNC	AA2	DVOC_D2	V2
HI10	AJ3	DVOC_HSYNC	Y4	DVOC_D11	P2
HISTRS	AH4	DVOC_D0	W2	DVOB_CINTR#	P4
HI2	AK2	DVOC_BLANK#	Y2	DVOC_FLDSTL	M2
HI0	AF5	DVOC_CLK#	V5	DVOC_D10	P5
HI6	AL2	DVOC_D3	W3	TESTP143	M7
HI1	AG3	DVOC_D9	T5	EXTTS#	AP8
Output Pins					
SDM_A1	AP16				
SDM_B1	AG15				

Table 59. XOR Chain 2 (44 Inputs) Output Pins: SDM_A2, SDM_B2

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
DVOB_CLK#	AC5	HD19#	F19	HDSTBN0#	C19
TESTP146	T11	HD27#	E21	HD6#	B20
HD29#	G14	HD24#	F21	HD9#	E20
HD25#	F15	HD21#	L18	HD12#	B18
HD26#	E15	HD28#	J19	HD3#	D20
HD31#	K17	HD16#	G20	HD2#	B21
HD22#	G16	HD18#	E19	HD0#	B23
HD17#	F17	DINV0#	C17	HD4#	B22
HD30#	E17	HD8#	E18	HD5#	D22
HD20#	J17	HD11#	D16	HD7#	C21
DINVB_1	L17	HD14#	E16	HD1#	E22
HD23#	G18	HD10#	B16	PROCHOT#	L20
HDSTBP1#	L19	HD15#	D18	HITM#	E23
HDSTBN1#	K19	HD13#	B17	BSEL0	L13
		HDSTBP0#	B19	HLOCK#	E25
Output Pins					
SDM_A2	AM24				
SDM_B2	AE21				

Table 60. XOR Chain 3 (41 Inputs) Output Pins: SDM_A3, SDM_B3

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
BNR#	B28	HA12#	B31	HA19#	F28
BSEL1	L12	HA9#	C30	HA18#	C32
HIT#	K21			HA22#	G27
DRDY#	G24	HA4#	D30	HA24#	E28
DBSY#	E27	HA10#	C31	HA23#	F29
ADS#	F27	HA15#	J24	HADSTB1#	D28
HREQ4#	J21	HA8#	K23	HA17#	D34
HA16#	F25	HA13#	E30	HA25#	H27
HREQ3#	C29	HA6#	E29	HA20#	C34
HREQ0#	B29	HA5#	L23	HA30#	J26
HA3#	D26	HA11#	J25	HA21#	J27
HREQ1#	J23	HREQ2#	L22	HA27#	E32
HA7#	B32	HA31#	G26	HA29#	G30
HA14#	B33	HA26#	K24	HA28#	F31
Output Pins					
SDM_A3	AP30				
SDM_B3	AJ28				

Table 61. XOR Chain 4 (40 Inputs) Output Pins: SDM_A4, SDM_B4

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HD45#	H10	HD43#	K13	HD57#	C11
HD46#	G8	HD33#	L16	HDSTBP3#	D12
HD40#	G10	HD41#	L15	HDSTBN3#	E12
HD47#	E9	HD35#	F13	HD51#	B12
HD39#	G12	HD32#	J15	HD49#	E14
HD36#	F11	HD37#	E13	HD55#	B11
HD44#	J11	HD58#	E10	HD54#	C13
HD42#	E11	HD56#	D10	HD53#	D14
DINV2#	L14	HD62#	D8	HD50#	B14
HDSTBP2#	G9	HD61#	B9	HD48#	B13
HDSTBN2#	F9	HD63#	B8	HD52#	B15
HD34#	J13	HD59#	B10	DINV3#	C15
HD38#	K15	HD60#	C9	DVOC_CLK	V4
Output Pins				HSYNC	G3
SDM_A1	AF31				
SDM_B1	AC31				

Table 62. XOR Chain 5 (44 Inputs) Output Pins: SDM_A5, SDM_B5

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A58	E33	SDQ_A53	P34	SDQ_A41	AB31
SDQ_A59	F33	SDQ_A48	T34	SDQ_A44	AD31
SDQ_A62	G34	SDQ_A52	T31	SDQS_A4	AF34
SDQ_A63	F34	SDQ_A49	T32	SDQ_A35	AD32
SDQS_A7	H31	SCMDCLK_A5#	P32	SDQ_A38	AE34
SDQ_A61	J34	SCMDCLK_A5	P31	SDQ_A39	AD34
SDQ_A57	H34	SCMDCLK_A2#	N34	SDQ_A34	AF32
SDQ_A56	J33	SCMDCLK_A2	N33	SDQ_A33	AG34
SDQ_A60	K31	SDQS_A5	V34	SDQ_A37	AG33
SDQ_A51	K32	SDQ_A42	V32	SDQ_A36	AH31
SDQ_A50	K34	SDQ_A46	U34	SDQ_A32	AH32
SDQ_A55	L33	SDQ_A47	U33	SCMDCLK_A0	AK32
SDQS_A6	M32	SDQ_A43	V31	SCMDCLK_A0#	AK31
SDQ_A54	L34	SDQ_A40	AC34	SCMDCLK_A3#	AK34
		SDQ_A45	AB32	SCMDCLK_A3	AK33
Output Pins					
SDM_A1	W33				
SDM_B1	U31				

Table 63. XOR Chain 6 (40 Inputs) Output Pins: SDM_A6, SDM_B6

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_A30	AM31	SDQ_A19	AN27	SDQ_A8	AP14
SDQS_A3	AM30	SDQ_A23	AP27	SDQ_A6	AL12
SDQ_A27	AM33	SDQ_A22	AP25	SDQ_A2	AM12
SDQ_A31	AN34	SDQ_A16	AP22	SDQ_A3	AN13
SDQ_A29	AN29	SDQ_A20	AP21	SDQS_A0	AN11
SDQ_A26	AP33	SDQ_A10	AL18	SDQ_A5	AL10
SDQ_A25	AP29	SDQ_A15	AM18	SDQ_A7	AP13
SDQ_A24	AP28	SDQ_A14	AP18	SDQ_A4	AM10
SDQ_A28	AM28	SDQS_A1	AP15	SCMDCLK_A1	AP17
SDQS_A2	AP23	SDQ_A11	AP19	SCMDCLK_A1#	AN17
SDQ_A21	AL22	SDQ_A13	AN15	SDQ_A1	AP11
SDQ_A17	AM22	SDQ_A9	AM14	SCMDCLK_A4#	AL16
SDQ_A18	AL24	SDQ_A12	AL14	SCMDCLK_A4	AM16
				SDQ_A0	AP10
Output Pins					
SDM_A6	M34				
SDM_B6	M29				

Table 64. XOR Chain 7 (45 Inputs) Output Pins: SDM_A7, SDM_B7

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
HADSTB1#	D28	SDQS_B6	L27	SDQ_B41	W30
SDQ_B57	H29	SDQ_B48	P29	SDQS_B5	U30
SDQ_B61	M25	SDQ_B49	R30	SDQ_B37	AB29
SDQ_B58	F32	SDQ_B52	R31	SDQ_B36	AE31
SDQ_B63	G32	SCMDCLK_B5	N31	SDQ_B35	Y29
SDQ_B60	N25	SCMDCLK_B5#	N30	SDQ_B32	AE30
SDQS_B7	J30	SCMDCLK_B2#	N26	SDQ_B34	AC30
SDQ_B62	J29	SCMDCLK_B2	N27	SDQ_B38	AA26
SDQ_B59	G33	SDQ_B43	T25	SDQ_B33	AC27
SDQ_B56	K30	SDQ_B46	U25	SDQ_B39	AA27
SDQ_B51	L30	SDQ_B42	U27	SDQS_B4	AD29
SDQ_B54	P25	SDQ_B47	R27	SCMDCLK_B0	AG29
SDQ_B55	L32	SDQ_B45	V29	SCMDCLK_B0#	AG30
SDQ_B53	R26	SDQ_B40	AA30	SCMDCLK_B3	AJ30
SDQ_B50	K28	SDQ_B44	AA31	SCMDCLK_B3#	AH29
Output Pins					
SDM_A7	H32				
SDM_B7	J31				

Table 65. XOR Chain 8 (40 Inputs) Output Pins: HTRDY#, BPRI#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SDQ_B30	AD25	SDQ_B21	AK21	SDQ_B8	AE17
SDQ_B26	AG27	SDQ_B17	AE20	SCMDCLK_B4#	AL15
SDQ_B29	AJ27	SDQS_B2	AG21	SCMDCLK_B4	AK15
SDQ_B27	AF27	SDQ_B16	AE19	SCMDCLK_B1#	AG17
SDQ_B31	AF28	SDQ_B20	AL19	SCMDCLK_B1	AF17
SDQ_B25	AH26	SDQ_B10	AK17	SDQ_B1	AE15
SDQS_B3	AH27	SDQ_B14	AJ16	SDQ_B3	AE16
SDQ_B28	AJ26	SDQ_B15	AJ18	SDQ_B7	AG12
SDQ_B24	AK25	SDQ_B11	AL17	SDQ_B2	AL11
SDQ_B23	AE22	SDQ_B13	AJ14	SDQ_B6	AK11
SDQ_B18	AG23	SDQ_B12	AK13	SDQ_B5	AF12
SDQ_B19	AK23	SDQ_B9	AL13	SDQ_B0	AJ10
SDQ_B22	AJ24	SDQS_B1	AG13	SDQ_B4	AL8
				SDQS_B0	AF15
Output Pins					
HTRDY#	D24				
BPRI#	B26				

Table 66. XOR Chain 9 (62 Inputs) Output Pins: RS2#, DEFER#

Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number
SCAS_A#	Y34	SMAA_B0	AG31	SMAA_B7	AF21
SWE_A#	AB34	SMAB_A1	AL34	SMAA_B9	AJ22
SCS_B3#	W25	SMAA_A6	AL28	SMAA_B11	AL21
SBA_B1	AA25	SMAA_B6	AL25	SMAA_B4	AK27
SBA_A1	AH34	SMAB_A3	AP32	SMAA_B5	AG25
SCS_A1#	Y31	SMAB_A2	AM34	SCKE_A3	AP20
SCS_A2#	Y32	SMAA_A3	AN31	SCKE_A0	AL20
SCS_A3#	W34	SMAA_B3	AE24	SMAA_A11	AN23
SRAS_A#	AC33	SMAA_B1	AJ31	SMAA_A12	AN21
SBA_A0	AE33	SMAB_B3	AL29	SCKE_A2	AM20
SCS_A0#	AA34	SMAA_A4	AL30	SCKE_A1	AN19
SMAA_B2	AD27	SMAB_B4	AL27	SCKE_B0	AK19
SRAS_B#	W26	SMAB_B2	AD26	SCKE_B3	AE18
SMAA_B10	AF29	SMAB_A4	AP31	SCKE_B2	AG19
SBA_B0	Y25	SMAB_A5	AM26	SMAA_B12	AJ20
SMAA_A10	AJ33	SMAA_A9	AP24	SCKE_B1	AF19
SMAB_B1	AE27	SMAB_B5	AE23	SCS_B1#	T29
SMAA_A0	AJ34	SMAA_A8	AP26	SCS_B0#	U26
SMAA_A1	AL33	SMAA_A5	AL26	SCS_B2#	V25
SMAA_A2	AK29	SMAA_A7	AN25	SWE_B#	W27
		SMAA_B8	AL23	SCAS_B#	W31
Output Pins					
RS2#	B27				
DEFER#	L21				

Table 67. XOR Excluded Pins

Signal Name	Ball Number	Signal Name	Ball Number
BLUE	H7	SDM_A0	AP12
BLUE#	G6	SDM_A1	AP16
BPRI#	B26	SDM_A2	AM24
BREQ0#	B24	SDM_A3	AP30
CPURST#	E8	SDM_A4	AF31
DEFER#	L21	SDM_A5	W33
DREFCLK	G4	SDM_A6	M34
GCLKIN	H4	SDM_A7	H32
DVOB_CROMP	AC2	SDM_B0	AG11
GREEN	H6	SDM_B1	AG15
GREEN#	G5	SDM_B2	AE21
GVREF	AD2	SDM_B3	AJ28
TESTP141	AC3	SDM_B4	AC31
HCLKN	C7	SDM_B5	U31
HCLKP	B7	SDM_B6	M29
HDRCOMP	E24	SDM_B7	J31
HDSWING	C25	SMVREF_A0	E34
HDVREF	F23	SMVREF_B0	AP9
HTRDY#	D24	SMXRCOMP	AK9
HI_COMP	AD4	SMXRCOMPVOH	AN9
HI_VREF	AE2	SMXRCOMPVOL	AL9
HI_SWING	AE3	SMYRCOMP	AA33
PWROK	AE14	SMYRCOMPVOH	R34
RED	F4	SMYRCOMPVOL	R33
RED#	E4	Reserved	AG9
REFSET	D2	TESTIN#	AG10
RS0#	G22	CI_RCOMP	AG2
RS1#	C27	CI_VREF	AF4
RS2#	B27	CI_VSWING	AF2
RSTIN#	AK4		