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PRELIMINARY SPECIFICATION

82C601
SINGLE CHIP PERIPHERAL CONTROLLER

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STK #10055-002

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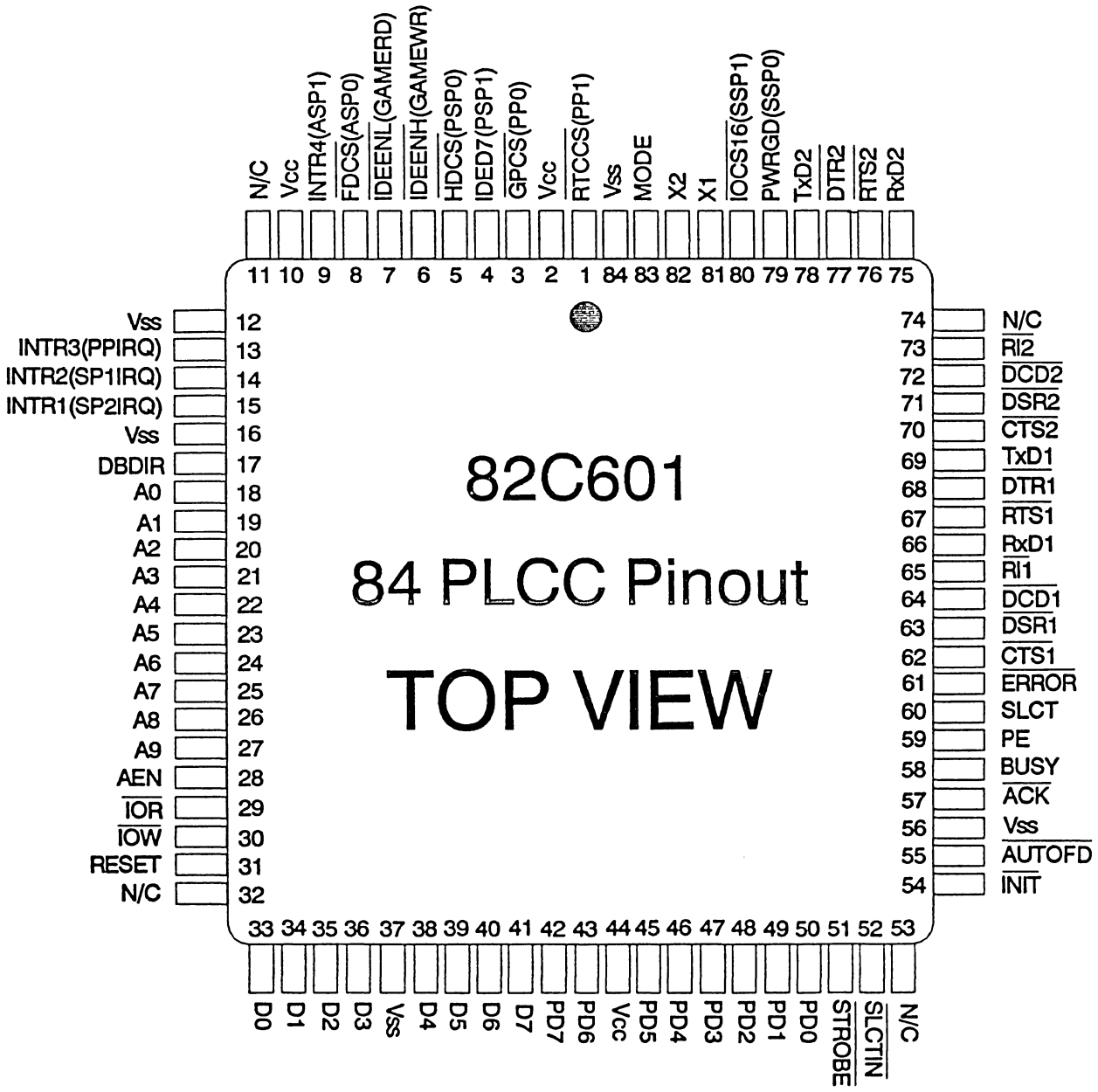
84 PLCC PINOUT



Features Highlights:

- O 100% Compatible to IBM PC-XT/AT
- O 2 x 16450 Compatible UARTs
- O 1 IBM PC-XT/AT Compatible Enhanced Parallel Port
- O ADAPTER mode functions:
  - o Game Port Decodes
  - o Select Pins for Serial and Parallel ports
- O MOTHER-BOARD mode functions:
  - o IDE Interface
  - o Real Time Clock Chip Select
  - o Programmable General Purpose Chip Select
  - o Power Saving Features and Power Down Modes
- O 16 mA Output Drivers
- O Schmitt Trigger Inputs on RESET
- O Internal Address Decoders
- O EISA Ready (MOTHER-BOARD mode)
  - o Relocatable Ports
  - o Relocatable IRQ
  - o Interrupt Sharing Capability
- O Low Power CMOS
- O 80 PFP or 84 PLCC packages

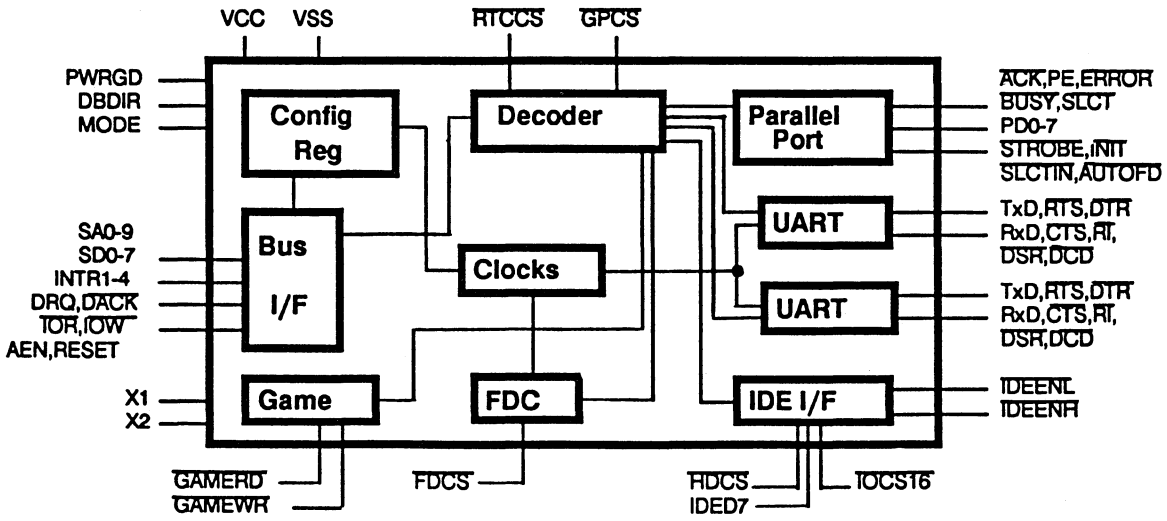


Figure 1. 82C601 Block Diagram

Functional Description:

82C601 is the second generation of our Multifunction Controller product line. The chip features 24 mA drivers for the output buffers, such as the host data bus and 16n mA drivers for the parallel port. It incorporates two 16450 compatible UARTs, one enhanced parallel port (with bidirectional capability), an IDE compatible hard disk interface and various chip selects (in the MOTHER-BOARD mode) or select pins and Game port decodes (in the ADAPTER mode). This chip supports 2 modes:

* ADAPTER mode where the base addresses for the ports are determined by the select pins (PSPs, SSPs, ASPs, and PPs); except for game port, it is fixed @ 200H-207H. -GAMERD and -GAMEWR outputs are provided to minimize external gate count.
* MOTHER-BOARD mode where all the ports are relocatable. An Integrated Drive Electronics interface, and various Chip Selects (Floppy Disk , Real Time Clock, and a General Purpose) have been added for this mode. Power management aspects of the 82C601in the MOTHER-BOARD mode includes modular power down for each port, oscillator disable, and chip power down through the PWRGD pin. When the chip is powered down (i.e. when PWRGD is inactive) the current draw should be minimal, all the inputs are disabled, and all outputs are tri-stated. The contents of all the registers are preserved, as long as power supply to the 82C601 is maintained.

The host interface is PC compatible, i.e. D0-D7, A0-A9, -IOR, -IOW, AEN, INTR1, INTR2, INTR3, INTR4, and RESET, and can be connected directly to the bus. The system bus interface buffers (D0-D7, INTR1-4) are capable of sinking 24 mA @ 0.5 V, the parallel port control signals are capable of sinking 16 mA @ 0.5 V.

Pin Description:

PLCC (PFP)	Symbol	Buffer Type	Description
Host Interface (27 pins)			
9 (79)	INTR4	T	Active high Interrupt Request , MOTHER-BOARD function. When the parallel port is assigned to be LPT1 (I/O address 3BCH) or LPT3 (I/O address 378H), INTR4 generates interrupt to the host, normally connected to IRQ7. If I/O address 278H is selected , then the parallel port is assigned to be LPT2, therefore it should use IRQ5. INTR4 originates from either the Secondary Serial Port or the Parallel Port Controller.
	(ASP1)	I	Alternate Serial Port select 1, ADAPTER mode function. ASP0 (pin 8/78) and ASP1 determines the Serial Port addresses.
13 (2)	INTR3	T	Active high Interrupt Request, MOTHER-BOARD function. In the MOTHER-BOARD mode, INTR3 originates from the Primary Serial Port or the Parallel Port Controller.
	(PPIRQ)	T	Active high Parallel Port Interrupt, ADAPTER mode. In the ADAPTER mode, this pin should be connected to IRQ5 when the parallel port is assigned to be LPT3 (I/O address 278H).

14 (3)	INTR2	T	Active high Interrupt Request, MOTHER-BOARD function. In the MOTHER-BOARD mode, INTR2 originates from the Primary Serial Port or the Secondary Serial Port.
	(SP1IRQ)	T	Active high Primary Serial Port Interrupt, ADAPTER function. In the ADAPTER mode, SP1IRQ is normally connected to IRQ4 for COM1/COM3.
15 (4)	INTR1	T	Active high Interrupt Request, MOTHER-BOARD function. In the MOTHER-BOARD mode, INTR1 originates from the Primary Serial Port or the Secondary Serial Port.
	(SP2IRQ)	T	Active high Secondary Serial Port Interrupt, ADAPTER function. In the ADAPTER mode, SP2IRQ is normally connected to IRQ3 for COM2/COM4.
17 (6)	DBDIR	O	Host Data Bus Buffer Direction, when low it indicates a read cycle. Active low indicates read cycles for 82C601 internal accesses, Serial Ports, Parallel Port, Real Time Clock, Floppy Disk Controller, low byte of IDE, and/or the General Purpose Port if selected.
18-27 (7-16)	A0-A9	I	Host Address bit 0-9. These addresss bits are latched internally at the beginning of -IOR or IOW.
28(17)	AEN	I	Active high Address Enable indicates DMA activities.
29(18)	-IOR	I	Active low I/O Read.
30(19)	-IOW	I	Active low I/O Write.
31 (20)	RESET	IS	Active high Reset, Schmitt-trigger input. RESET has to be valid for minimum of 1 microsecond.
33-36, 38-41	D0-D7 (21-24,26-29)	I/O1	Host Data bus, 24 mA drivers.

Parallel Port Controller (17 pins):

42,43, 45-50	PD7-PD0 (30,31,33-38)	I/O2	Parallel Port data bus. These outputs are capable of sinking 16 mA @ 0.5 V.
51(39)	-STROBE	O2	Active low Data Strobe output, 16 mA driver.
52(40)	-SLCTIN	O2	Active low Select Control output, 16 mA driver.
54(41)	-INIT	O2	Active low Initialize output, 16 mA driver.
55(42)	-AUTOFD	O2	Active low Auto Feed output, 16 mA driver.

57(44)	-ACK	I	Active low Acknowledge input.
58(45)	BUSY	I	Active high Busy input.
59(46)	PE	I	Active high Paper End input.
60(47)	SLCT	I	Active high device Selected input.
61(48)	-ERROR	I	Active low Error input.

Serial Port Interface (18 pins)

62,70 (49,57)	-CTS1,-CTS2	I	Active low Clear To Send input.
63,71 (50,58)	-DSR1,-DSR2	I	Active low Data Set Ready input.
64,72 (51,59)	-DCD1,-DCD2	I	Active low Data Carrier Detect input.
65,73 (52,60)	-RI1,-RI2	I	Active low Ring Indicator input.
66,75 (53,61)	RXD1,RXD2	I	Active high Receive Data input.
67,76 (54,62)	-RTS1,-RTS2	OL	Active low Request To Send output.
68,77 (55,62)	-DTR1,-DTR2	OL	Active low Data Terminal Ready output.
69,78 (56,64)	TXD1,TXD2	OL	Active high Transmit Data output.
67(81)	X1	I	Serial Port crystal input, normally 1.8432 MHz.
68(82)	X2	OL	Serial Port crystal output.

IDE Interface and Chip Selects (MOTHER-BOARD mode, 9 pins)
Configuration Selects (ADAPTER mode, 9 pins)

79 (65)	PWRGD	I	Active high Power Good indication, MOTHER-BOARD AT/XT mode. The 82C601 is fully functional when PWRGD is active; when PWRGD is inactive and Vcc is still valid, the 82C601 is isolated from the rest of the circuit. All

accesses are ignored, all inputs are disabled, and all outputs are tri-stated. However, register contents are preserved, and the current draw is minimal.

	(SSP0)	I	Secondary Serial Port Select 0, ADAPTER mode.

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80 (66)	-IOCS16	I	Active low 16 bit I/O indication, MOTHER-BOARD AT mode. The hard disk interface generates -IOCS16 to inform the host and the 82C601 that 16 bit I/O transfers are about to begin. -IOCS16 is active only when transferring data words in AT mode. Low = 16 bit, high = 8 bit. (AT mode).
	(-HDACK)	I	Active Low HDC DMA Acknowledge, MOTHER-BOARD XT mode.
	(SSP1)	I	Secondary Serial Port Select 1, ADAPTER MODE. SSP0 and SSP1 select the address assignment for the second serial port.

SSP1	SSP0	IRQ	Address
0	0	IRQ3	2F8H (COM2)
0	1	IRQ4	COM3, the address is assigned by AS1, AS0
1	0	IRQ3	COM4, the address is assigned by AS1, AS0
1	1	--	Disabled

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4 (74)	IDED7	I/O1	IDE Data Bit 7, MOTHER-BOARD AT mode, 24 mA driver. IDED7 transfers data @ I/O addresses 1F0H-1F7H (R/W), 3F6H (R/W), 3F7 (W). IDED7 should be connected to the IDE data bit 7. Normally, the 82C601 functions as a buffer, transferring data bit 7 between the IDE device and the host. Except during read of I/O address 3F7H, D7 is tri-stated, and data bits 0-6 are sourced by the hard disk interface.
	(RSVD)	N/A	Not Used in MOTHER-BOARD XT mode
	(PSP1)	I	Primary Serial Port Select 1, ADAPTER MODE. PSP0 and PSP1 select the address assignment for the primary serial port.

PSP1	PSP0	IRQ	Address
0	0	IRQ4	3F8H (COM1)
0	1	IRQ3	2F8H (COM2)
1	0	IRQ4	COM3, the address is assigned by AS1, AS0
1	1	--	Disabled

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5 (75)	-HDCS	O1	Active low Hard Disk Chip Select, MOTHER-BOARD AT/XT mode. -HDCS decodes the primary HDC; default is I/O address 1F0H-1F7H (AT mode, CR#0CH<6> = 0) or 320H-323H (XT mode, CR#0CH<6> = 1).
	(PSP0)	I	Primary Serial Port Select 0, ADAPTER MODE. PSP0 and PSP1 select the address assignment for the primary serial port.

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6 (76)	-IDEENH	O	Active low High Data Buffer Enable, MOTHER-BOARD AT mode -IDEENH is active only when -IOCS16 is active, I/O address 1F0H-1F7H, and AT mode is selected.
	(RSVD)	N/A	Not Used in MOTHER-BOARD XT mode.
	(-GAMEWR)	O	Active low Game Write strobe, ADAPTER mode. -GAMEWR decodes I/O address range 200H-207H and qualifies it with -IOW.

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7 (77)	-IDEENL	O	Active low Low Data Buffer Enable, MOTHER-BOARD AT/XT mode. -IDEENL is active when accessing I/O address 1F0H-1F7H and 3F6H-3F7H (AT mode) or 320H-323H (XT mode: 8 bit DMA or programmed I/O).

	(-GAMERD)	O	Active low Game Read strobe, ADAPTER mode. -GAMERD decodes I/O address range 200H-207H and qualifies it with -IOR.
1 (71)	-RTCCS	O	Active low Real Time Clock Chip Select, MOTHER-BOARD AT/XT mode. -RTCCS decodes I/O addresses 70H and 71H for the 146818 compatible RTC.
	(PP1)	I	Parallel Port Select 1, ADAPTER mode. PP0 and PP1 determine the base address for the parallel port controller.

PP1	PP0	IRQ	Address
0	0	IRQ7	3BCH (LPT1)
0	1	IRQ5	378H (LPT2)
1	0	IRQ7	278H (LPT3)
1	1	--	Disabled

3 (73)	-GPCS	O	Active low General Purpose Chip Select, MOTHER-BOARD AT/XT mode. -GPCS decodes the address specified in the Config. Reg. #09H and #0AH with the mask bit specified in the Config. Reg. 0AH.
	(OUT1)	O	OUT1 output from the Primary Serial Port, when CR#0BH<0> = 1.
	(PP0)	I	Parallel Port Select 0, ADAPTER mode. PP0 and PP1 determine the base address for the parallel port controller.
8 (78)	-FDCS	O1	Active low Floppy Disk Chip Select, MOTHER-BOARD AT/XT mode. -FDCCS decodes the the primary Floppy Disk @ address 3F0H-3F7H.
	(ASP0)	I	Alternate Serial Port select 0, ADAPTER mode.
9 (79)	ASP1	I	Alternate Serial Port select 1, ADAPTER mode. ASP0 and ASP1 select the base address pairs for the primary and secondary serial port when they are used as COM3, COM4 pair.

ASP1	ASP0	COM3	COM4
0	0	338H	238H
0	1	3E8H	2E8H
1	0	2E8H	2E0H
1	1	220H	228H

Miscellaneous (9 pins)

83 (69)	MODE	I	Mode Select. 0 = MOTHER-BOARD mode. MOTHER-BOARD mode allows you to configure the 82C601 and fully utilize the power management functions. 1 = ADAPTER mode. In the ADAPTER mode the port addresses are determined by the jumper selects, except for the game port, which is fixed at address 200H-207H.
2,10,44 (32,72,80)			Vcc (+5V)
12,16,37,56,84 (1,5,25,43,70)			Vss (ground)

Buffer Type:

I = TTL input
IS = Schmitt-trigger input
I/O1 = TTL input and output type 1, 24 mA, -8 mA
I/O2 = TTL input and output type 2, 16 mA, -200 uA
OL = Low TTL output, 4 mA, -1 mA
O = TTL output, 8mA, -1mA
T = 3-state TTL output, 24mA, -8 mA

TOP LEVEL LOGIC:

Power Up Conditions

Configuration Register default values

Upon power up the configuration registers are set to the default values, control signals are inactive, status registers reflect the status of the input pins, other registers are cleared to 00H, and unused bits are cleared to "0"s. All the control signals and the register contents are preserved as long as power is maintained.

The default values upon power up:

CR#00H = 0EH
CR#01H = 00H
CR#02H = 08H
CR#03H = XXH (Not Used)
CR#04H = FEH
CR#05H = BEH
CR#06H = 9EH
CR#07H = 00H (Not Used)
CR#08H = ECH
CR#09H = B0H
CR#0AH = 00H
CR#0BH = 00H
CR#0CH = 00H
CR#0DH = XXH (Not Used)
CR#0EH = 00H
CR#0FH = N/A

Configuration Register Definitions (MOTHER-BOARD mode only):

Configuration Register #00H (R/W)

Chip Selects and Enable.

b7: Valid Configuration indication.
0 = Invalid, default upon power up.
Invalid configuration, because Vcc to the 82C601 was removed; therefore the previous configuration is lost.
1 = Valid Configuration.

b6-5: Serial Port Oscillator Enable.
b6-b5
0 0 = Oscillator always ON, default.
0 1 = Oscillator is ON when PWRGD is active; otherwise it is OFF.
1 0 = Oscillator is ON when PWRGD is active; otherwise it is OFF.
1 1 = Oscillator always OFF.

b4: Reserved.

b3: Parallel Port Enable.
0 = Disabled.
1 = Enabled, default upon power up.

b2: Primary Serial Port Enable.
0 = Disabled.
1 = Enabled, default upon power up.
b1: Secondary Serial Port Enable.
0 = Disabled.
1 = Enabled, default upon power up.
b0: Reserved.

Configuration Register #01H (R/W)

Parallel Port mode.

b7: Reset Control.
0 = Normal reset.
Resets all serial port registers to the default values, except Tx, Rx, and Divisor register.
1 = Restricted reset.
None of the serial port registers is cleared.
b6: Extended or Compatible mode.
0 = Compatible/Printer mode, default.
1 = Extended/Bidirectional mode.
b5: Force -CTS1 active.
b4: Force -DSR1 active.
b3: Force -DCD1 active.
b2: Force -CTS2 active.
b1: Force -DSR2 active.
b0: Force -DCD2 active.
A "1" in any of bits 0-5 will force the appropriate inputs to active/low. The default is not forced, that is, the output is dependent on the programmed Modem Control register value.

Configuration Register #02H (R/W)

Parallel Port mode.

b7: Reserved =0.
b6: Primary Serial Port clock divider select.
0 = Divide by 2, default.
1 = Divide by 4.
b5: Primary Serial Port Receive clock source.
0 = Baud rate Generator, default.
1 = Divider output (see bit 6).
b4: Primary Serial Port Transmit clock source.
0 = Baud rate Generator, default.
1 = Divider output (see bit 6).
b3: 8250 or 16450 mode.
0 = 8250 mode.
1 = 16450 mode, default.
The difference between 8250 and 16450 mode is when there are multiple interrupts pending. In 8250 mode the 82C601 will bring the INTR line low momentarily, after each read of the interrupt status. Except after the last interrupt, in this case the INTR will remains inactive. In the 16450 mode, no low pulse will be generated. The INTR will become inactive (low), after the last interrupt status is read.
b2: Secondary Serial Port clock divider select.
0 = Divide by 2, default.

1 = Divide by 4.

b1: Secondary Serial Port Receive clock source.
0 = Baud rate Generator, default.
1 = Divider output (see bit 2).

b0: Secondary Serial Port Transmit clock source.
0 = Baud rate Generator, default.
1 = Divider output (see bit 2).

Configuration Register #04H (R/W)

Primary Serial Port Address.

b7-b1: The MSB of the Primary Serial Port address (bits 9-3).

b0: Reserved = 0.

Default upon power up is FEH: address 3F8H (COM1).

Configuration Register #05H (R/W)

Secondary Serial Port Address.

b7-b1: The MSB of the Secondary Serial Port address (bits 9-3).

b0: Reserved = 0.

Default upon power up is BEH: address 2F8H (COM2).

Configuration Register #06H (R/W)

Parallel Port Address.

b7-b0: The 8 most significant address bits of the Parallel Port.

Default upon power up is 9EH: address 278H (LPT2).

Configuration Register #08H (R/W)

Interrupt Request Source.

b7-b6: INTR1 Source.

b7	b6	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port.
1	1	Secondary Serial Port, default.

b5-b4: INTR2 Source.

b5	b4	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port, default.
1	1	Secondary Serial Port.

b3-b2: INTR3 Source.

b3	b2	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port.
1	1	Parallel Port, default.

b1-b0: INTR4 Source.

b1	b0	
0	0	Disabled, tri-stated, default.
0	1	Disabled, tri-stated.
1	0	Secondary Serial Port.
1	1	Parallel Port.

Configuration Register #09H (R/W)

General Purpose Chip Select High Address decode.

b7-b0 = A9-A2 Address Decode.

Configuration Register #0AH (R/W)

General Purpose Chip Select Low Address decode, Masks, and Enable.

b7-b5: -GPCS Mask for address bit 3-1.
- 0 = No mask.
- 1 = Mask (not used in decoding).

b4: Reserved.

b3: -GPCS A1 address decode.

b2: -IDEENL Buffer Enable.
- 0 = Disabled, default. -IDEENL does not qualify DBDIR.
- 1 = Enabled, -IDEENL qualifies DBDIR.

b1: -GPCS Enable.
- 0 = Disabled, default. -GPCS is disabled (high).
- 1 = Enabled Chip Select.

b0: -GPCS Buffer Enable.
- 0 = Disabled, default. -GPCS does not qualify DBDIR.
- 1 = Enabled, -GPCS qualifies DBDIR.

Configuration Register #0BH (R/W)

Interrupt Polarity Select and Power Down.

b7: INTR4 Polarity Select.

b6: INTR3 Polarity Select.

b5: INTR2 Polarity Select.

b4: INTR1 Polarity Select.
- 0 = Active High, default.
- 1 = Active Low; tri-stated when inactive.

b3: Primary Serial Port Power Down.

b2: Secondary Serial Port Power Down.
- 0 = Normal mode, default.
- 1 = Power Down mode.
  - All outputs are tri-stated, all inputs are disabled.
  - Outputs: TxD, -RTS, -DTR are tri-stated.
  - Inputs: RxD, -CTS, -DSR, -DCD, -RI are disabled.

b1: Parallel Port Power Down.
- 0 = Normal mode, default.
- 1 = Power Down mode.
  - All outputs are tri-stated; all inputs are disabled.
  - Outputs: PD0-7, -STROBE, -SLCTIN, -INIT, -AUTOFD tri-stated.
  - Inputs: -ACK, BUSY, PE, SLCT, -ERROR are disabled.

b0: -GPCS/-OUT1 Output Select.
0 = -GPCS, default.
1 = -OUT1 of Modem Control Reg. of the Primary Serial Port.

Configuration Register #0CH (R/W)

b7: IDE Enable.
0 = IDE Disabled, default.
-HDCS, -IDEENL, -IDEENH are always disabled/high.
1 = IDE Enabled.
-HDCS, -IDEENL are enabled, and will be active when the correct addresses are selected; -IDEENH depends on the XT/AT mode bit and the -IOCS16 input.

b6: IDE AT/XT Select.
0 = IDE AT interface, default.
8/16 bit programmed I/O transfers. -IDEENL is active during I/O 3F6H, 3F7H, 1F0H-1F7H. -IDEENH is active when -IOCS16 is active and I/O address range 1F0H-1F7H. -HDCS is active during programmed I/O 1F0H-1F7H.
1 = IDE XT interface.
8 bit DMA and programmed I/O transfers. -IDEENL is active during programmed I/O 320H-323H or DMA (-HDACK is active). -HDCS is active only during programmed I/O 320H-323H.

b5: -FDCS Enable.
0 = -FDCS Disabled, default.
1 = -FDCS Enabled. -FDCS is active for I/O address 3F0H-3F7H.

b4: -FDCS Buffer Enable.
0 = -FDCS Buffer Disabled, default.
1 = -FDCS Buffer Enabled, -FDCS qualifies DBDIR.

b3: -RTCCS Enable.
0 = -RTCCS Disabled, default.
1 = -RTCCS Enabled. -RTCCS is active for I/O addresses 70H and 71H.

b2: -RTCCS Buffer Enable.
0 = -RTCCS Buffer Disabled, default.
1 = -RTCCS Buffer Enabled, -RTCCS qualifies DBDIR.

b1,0: Reserved = 0.

Configuration Register #0EH (R/W)

b7: Reserved.

b6: Primary Serial Port Test Enable.
0 = Normal mode, Test Disabled, default.
1 = Test Enabled, TxD1 outputs the baud rate.

b5: Secondary Serial Port Test Enable.
0 = Normal mode, Test Disabled, default.
1 = Test Enabled, TxD2 outputs the baud rate..

b4-0: Reserved = 0.

Configuration Register #0FH (R)

Configuration Register #0FH is the Config. Reg. Index address divided by 4.

Configuration Register #0FH (W)

Writing any value to CR#0FH brings the 82C601 out of the configuration mode.

Configuration Register #03H, #07H, #0DH
Not Used.

Getting into and out of the configuration mode

Getting into the configuration mode requires the correct order of 5 consecutive values and addresses to be written into I/O addresses 2FAH and 3FAH, as shown below. Steps 4 and 5 determine the address for the Configuration Register Index and Data pair. The lower address is the CRI, the higher address is the CRD (CRD = CRI+1). The CRI, CRD pair should be selected carefully so that they do not interfere with any other addresses in the system. The CRI address can be calculated by multiplying the value written in step 4 by 4. The value written in step 5 is the one's complement of value written in step 4. In the example below, the CRI was chosen to be 390H which corresponds to a value of E4H to be written into step 4. This results to 1BH, one's complement of E4H, to be written to 2FAH in step 5.
To exit the configuration mode, just write any value into Configuration Register #0FH.

To get into configuration mode:

1) Write 55H to 2FAH.
2) Write AAH to 3FAH.
3) Write 36H to 3FAH.
4) Write E4H to 3FAH (see above paragraph).
5) Write 1BH to 2FAH (see above paragraph).

***** In configuration mode *****

To exit from configuration mode:

7) Write 0FH to CR#0FH.

Example:
In this example the CRI will be 390H, and CR#0H will be set to AEH

```
;step 1
        MOV     DX,2FAH         ; I/O address 2FAH
        MOV     AL,55H
        OUT     DX,AL           ; write 55H into 2FAH
;step 2
        MOV     AL,0AAH         ;
        MOV     BX,3FAH         ; I/O address 3FAH
        OUT     DX,AL           ; write AAH into 3FAH
;step 3
        MOV     AL,36H
        OUT     DX,AL           ; write 36H into 3FAH
;step 4
        MOV     AL,0E4H         ; 390H divided by 4 = E4H
        OUT     DX,AL           ; write E4H into 3FAH
```

```
;step 5
        MOV         AL,1BH              ; 1BH = 1's complement of E4H
        MOV         DX,2FAH
        OUT         DX,AL               ; write 1BH into 2FAH

;***** Now we are in the configuration mode *****

; Set Config. Reg. #0H to AEH
        MOV         DX,390H             ; set CRI to 390H
        MOV         AL,00H              ; CR#0H
        OUT         DX,AL               ; set configuration register 00H
        INC         DX                  ; Config. Data Reg. = 391H
        MOV         AL,0AEH             ; Valid Config, Osc ON when PWRGD, Enable all
        OUT         DX,AL               ; write value into CRD

; Exit from configuration mode
        DEC         DX                  ; CRI
        MOV         AL,0FH              ; CR#0FH
        OUT         DX,AL
        INC         DX                  ; CDR
        OUT         DX,AL               ; Exit from config. mode
```

Configuration Register Summary

	b7	b6	b5	b4	b3	b2	b1	b0	
CR#00	VC	SP OSC ENABLE		RSVD	PP	S1	S2	RSVD	R/W
CR#01	RE	PP	S1 CONFIG			S2 CONFIG			R/W
CR#02	RSVD=0	S1	R1	T1	MS	S2	R2	T2	R/W
CR#03	NOT USED								N/A
CR#04	PSA9	PSA8	PSA7	PSA6	PSA5	PSA4	PSA3	RSVD=0	R/W
CR#05	SSA9	SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	RSVD=0	R/W
CR#06	PPA9	PPA8	PPA7	PPA6	PPA5	PPA4	PPA3	PPA2	R/W
CR#07	NOT USED								N/A
CR#08	INTR1 SOURCE		INTR2 SOURCE		INTR3 SOURCE		INTR4 SOURCE		R/W
CR#09	GPA9	GPA8	GPA7	GPA6	GPA5	GPA4	GPA3	GPA2	R/W
CR#0A	MASK3	MASK2	MASK1	RSVD	GPA1	IDEBEN	GPEN	GPBEN	R/W
CR#0B	INT4PS	INT3PS	INT2PS	INT1PS	PSPD	SSPD	PPPD	G/OSEL	R/W
CR#0C	IDEEN	IDESEL	FDCSEN	FDCBEN	RTCSEN	RTCBEN	RSVD=0	RSVD=0	R/W
CR#0D	NOT USED								N/A
CR#0E	RSVD	S1TEST	S2TEST	RSVD=0	RSVD=0	RSVD=0	RSVD=0	RSVD=0	R/W
CR#0F	CONFIGURATION REGISTER INDEX								RO

Power Management

Power management functions are achieved using PWRGD pin and Configuration Register bits. PWRGD is an input to indicate to the 82C601 that the power supply is fully functional, thus the chip should be fully functional, i.e. all read/write commands are accepted. When PWRGD is inactive (low), the chip assumes that the power supply is not functional, the 82C601 isolates itself from the rest of the circuit; that is all inputs are disabled, all outputs are tri-stated, and all commands are ignored until PWRGD is restored to the active state.

Power Management Registers:

Config. Reg. #00H

b7: Valid Configuration bit.
- 0 = Invalid Configuration, default.
- 1 = Valid Configuration, Vcc is always present.

b6,b5: Serial Port Oscillator.
- 0 0 = Oscillator always ON, regardless of PWRGD, default.
- 0 1 = Oscillator is ON when PWRGD is high, otherwise it is OFF (tri-state).
- 1 0 = Oscillator is ON when PWRGD is high, otherwise it is OFF (tri-state).
  For laptop application, 01 or 10 should be used to reduce current draw.
- 1 1 = Oscillator is always OFF.

b4: Reserved.

b3: Parallel Port Enable.
- 0 = Parallel Port Disabled.
  When disabled, the parallel port appears disconnected from the host.
- 1 = Parallel Port Enabled, default.

b2: Primary UART Enable.

b1: Secondary UART Enable.
- 0 = UART Disabled.
  When disabled, the UART appears disconnected from the host.
- 1 = UART Enabled, default.

b0: Reserved.

Config. Reg. #0BH

b3: Primary Serial Port Power Down.

b2: Secondary Serial Port Power Down.
- 0 = Normal mode, default.
- 1 = Power Down mode.
  All outputs are tri-stated and all inputs are disabled, but all the UART registers are accessible. Reading read only registers produces undetermined data.
  Outputs: TxD, -RTS, -DTR, -OUT1 are tri-stated.
  Inputs: RxD, -CTS, -DSR, -DCD, -RI are disabled.

b1: Parallel Port Power Down.
- 0 = Normal mode, default.
- 1 = Power Down mode.
  All outputs are tri-stated and all inputs are disabled, but all registers are accessible. Read only registers produces undetermined data.
  Outputs: PD0-7, -STROBE, -SLCTIN, -INIT, -AUTOFD are tri-stated.
  Inputs: -ACK, BUSY, PE, SLCT, -ERROR are disabled.

SERIAL PORT CONTROLLER

The serial ports are fully compatible to the 16450 ACE registers. The programmable features allow data rates ranging from 50 baud to 115.2 Kbaud; 5 to 8 bit character size with 1, 1.5, 2 start or stop bits; even, odd, sticky or no parity; and prioritized interrupts. An Interrupt from each UART is enabled or disabled (tri-stated) using the OUT2 bit. If a "1" is written to OUT2, the UART interrupt is enabled. Writing "0" tri-states the interrupt.
There is a difference between the Primary Serial Port and the Secondary Serial Port. OUT1 of Primary Serial Port can be selected to become an output. -GPCS output can be configured to be either OUT1 of the Primary Serial Port or a General Purpose Chip Select depending upon CR#0BH<0>. If CR#0BH= 0, then it is -GPCS (default); otherwise if CR#0BH= 1, then it becomes the OUT1 pin of the Primary Serial Port.

MOTHER-BOARD mode:

The serial port base addresses are relocated by writing different values to Config. Reg. #04H and/or #05H. Interrupts for Primary Serial Port and Secondary Serial Port depend on the values written to the Interrupt Source Register (Config. Reg. #08H). In this mode the serial port base addresses (CR#04H, CR#05H) and interrupt sources (CR#08H) are programmable.

ADAPTER mode:

The base addresses are determined by PSP0-1, SSP0-1, and ASP0-1 input combinations. ASP0 and ASP1 are used only when Primary Serial Port/Secondary Serial Port are selected to be COM3/COM4 pairs; these pins determine the address pairs. SP1IRQ is the interrupt for the Primary Serial Port, SP2IRQ is for the Secondary Serial Port, and PPIRQ is for the parallel port. Any of these interrupts can be jumpered to the appropriate IRQ lines. Customarily, the Primary Serial Port is assigned as COM1: 3F8H-3FFH with SP1IRQ connected to IRQ4; and the Secondary Serial Port is assigned as COM2: 2F8H-2FFH, SP2IRQ is connected to IRQ3. SP1IRQ can be assigned to IRQ3, IRQ4, or IRQ5 pins; conversely SP2IRQ can be assigned to IRQ3, IRQ4, or IRQ7. But the Primary Serial Port interrupt **can not** be the same as the Secondary Serial Port designation, that is, interrupts cannot be shared in the ADAPTER mode.

PSP1	PSP0	Address	SSP1	SSP0	Address	ASP1	ASP0	COM3	COM4
0	0	3F8H	0	0	2F8H	0	0	338H	238H
0	1	2F8H	0	1	COM3 (*)	0	1	3E8H	2E8H
1	0	COM3 (*)	1	0	COM4 (*)	1	0	2E8H	2E0H
1	1	Disabled	1	1	Disabled	1	1	220H	228H

Note: (*) Addresses are determined by ASP1,ASP0 combination.

Serial Port Register Definition

00H-RO: **Receive Buffer (DREN=0)**
00H-WO: **Transmit Buffer (DREN=0)**

01H-R/W: **Interrupt Enable (DREN=0)**
- b7-4: Not Used = "0"
- b3: Modem Status Interrupt Enable
- b2: Line Status Interrupt Enable
- b1: Transmit Register Empty Interrupt Enable

b0: Received Data Interrupt Enable
0 = Interrupt Disabled, default
1 = Interrupt Enabled

00H-R/W: Divisor Low Byte (DREN=1)
01H-R/W: Divisor High Byte (DREN=1)

	1.8432 MHz Xtal			3.072 MHz Xtal		
Baud	Dec	Hex	% Err	Dec	Hex	% Err
300	384	0180	--	640	0280	--
1200	96	0060	--	160	00A0	--
2400	48	0030	--	80	0050	--
4800	24	0018	--	40	0028	--
9600	12	000C	--	20	0014	--
19.2K	6	0006	--	10	000A	--
38.4K	3	0003	--	5	0005	--
56K	2	0002	2.86	3	0003	14.3
115.2K	1	0001	--	2	0002	16.7
192K	--	--	--	1	0001	--

02H-RO: Interrupt Code Register

b7-3: Not Used = "0"

b2-1: Interrupt Code

b2-1	Priority	Type	Source	Reset
1 1	1st	Receive Status	Errors: Overrun Parity, Framing, Break	Read Line Status Reg.
1 0	2nd	Data Available	Rx Buffer Full	Read Rx Buffer
0 1	3rd	Tx Reg. Empty	Tx Reg. Empty	Read Int. Reg. or Write to Tx Reg.
0 0	4th	Modem Status	CTS, DSR, RI, DCD	Read Modem Status Reg.

b0: Interrupt Pending
0 = Interrupt Pending
1 = No Pending Interrupt, default

03H-R/W: Line Control Register

b7: Divisor Register Enable Bit
0 = Disable Divisor Register and Enable Rx/Tx Register, default
1 = Enable Divisor Register and Disable Rx/Tx Register

b6: Break Control Enable
0 = Disable Break Control, default
1 = Enable Break Control, TxD is forced to "0"

b5: Sticky Parity Enable
0 = Disable Sticky Parity, default
1 = Enable Sticky Parity

b4: Parity Select, this bit is meaningless unless parity is enabled (b3 = "1")
0 = Odd Parity, default
1 = Even Parity. Parity bit is "1" when there are even number of "1"s

b3: Parity Enable
0 = Disable Parity, parity bit is not generated nor checked
1 = Enable Parity Logic

b3	b4	b5	Description
0	x	x	No parity generated nor checked
1	0	0	Odd Parity
1	0	1	Parity bit is generated and checked as "1"
1	1	0	Even Parity
1	1	1	Parity bit is generated and checked as "0"

b2: Stop Bits
0 = One Stop Bit
1 = 1.5 Stop Bit if data length is 5 bits, 2 Stop Bits if data length is 6, 7 or 8 bits

b2	b1	b0	Stop Bits
0	x	x	1 Bit
1	0	0	1.5 Bits
1	0	1	2 Bits
1	1	x	2 Bits

b1-0: Data Length

b1	b0	Data Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

04H-R/W: Modem Control Register

b7-5: Not Used = "0"

b4: Internal Loopback
0 = Loopback Disabled
1 = Loopback Enabled
TxD is set to "1", and the following signals are looped back:
TxD to RxD, -RTS to -CTS, -DTR to -DSR, -OUT1 to -RI, -OUT2 to -DCD

b3: INTR 3-state control (-OUT2)
0 = 3 stated
1 = Enabled

b2: -OUT1 output, Primary Serial Port only and if CR#0BH<0> = "1"
0 = -OUT1 is "1"
1 = -OUT1 is "0"

b1: -RTS output
0 = -RTS is "1"
1 = -RTS is "0"

b0: -DTR output
0 = -DTR is "1"
1 = -DTR is "0"

05H-R/W: Line Status Register

b7: Not Used = "0"

b6: Transmit Registers Empty
0 = Either Tx Data Reg. or Tx Shift Reg. is not empty
1 = Both Tx Data Reg. and Tx Shift Reg. are empty

b5: Tx Data Register Empty
0 = Tx Data Reg. contains data
1 = Tx Data Reg. is empty and can be written

b4: Break Indication
0 = No Break Condition
1 = Break Detected
Successive "0"s longer than a full transmission received.

b3: Framing Error
0 = No Framing Error
1 = Framing Error
Invalid Stop bit received.

b2: Parity Error
0 = No Parity Error
1 = Parity Error
Received parity bit differs than calculated parity bit.

b1: Overrun Error
0 = No Overrun Error
1 = Overrun Error
Rx Buffer has not been read before the next character is received, thus overwriting the previous character.

b0: Data Available
0 = Data not Available
1 = Data Available
Rx Buffer contains received data.

06H-R/W: Modem Status Register

- b7: Complement of -DCD input
- b6: Complement of -RI input
- b5: Complement of -DSR input
- b4: Complement of -CTS input
- b3: Change in -DCD input since the last read command
- b2: -RI input changes from low to high
- b1: Change in -DSR input since the last read command
- b0: Change in -CTS input since the last read command

07H-R/W: Scratch Pad Register

Serial port Connector

The 82C601 receives and transmits TTL level signals. These signals should be buffered to achieve the desired interface. For example for RS232, 1488/1489 or 145406 type buffers can be used. The connector for the serial port is either a male 25 pin D-shell or a male 9 pin D-shell. Typically the signals are connected as shown below.

DB9	DB25	I/O	Name	DB9	DB25	I/O	Name
--	1	-	N/C	1	8	I	DCD
2	2	O	-TxD	--	9-19	-	N/C
3	3	I	-RxD	4	20	O	DTR
7	4	O	RTS	--	21	-	N/C
8	5	I	CTS	9	22	I	RI
6	6	I	DSR	--	23-25	-	N/C
5	7	-	Ground				

PARALLEL PORT CONTROLLER

The Parallel port is compatible to the IBM PC XT/AT Parallel Port, plus PS/2 like extended mode for bidirectional mode. When the parallel port is disabled, all outputs and register contents are preserved. Upon power up the control signals are inactive, the data register is cleared to 00H, and the status register reflects the status signals.

MOTHER-BOARD mode

In this mode, the Parallel Port can be disabled or powered down through the Configuration Register. In power down mode, all registers are accessible, but the input signals are disabled, and the output signals are tri-stated.

ADAPTER mode

In the ADAPTER mode, the parallel port is configured as **AT compatible printer** mode only. Programmability is not available in this mode; therefore the chip can not be reconfigured. The parallel port base address is determined through PP0 and PP1 select pins.

PP1	PP0	Base Address
0	0	3BCH (LPT1)
0	1	378H (LPT2)
1	0	278H (LPT3)
1	1	Disabled

Parallel Data Port: Base address (R/W)

b7-0: Parallel Port Data.

Parallel Status Port: Base + 01H (R)

b7: -BUSY indicates the status of -BUSY printer signal, inverted.
0 = Printer is busy and not ready to accept data.
1 = Ready to accept data.

b6: -ACK indicates the status of -ACK printer signal.
0 = Printer has received the data and is ready for the next one.
1 = Data has not been received.

b5: PE (Paper End), indicates that the printer is out of paper.
0 = Normal condition.
1 = Printer is out of paper.

b4: SLCT indicates the status of SLCT printer signal. When active, the printer is selected
0 = Printer not selected.
1 = Printer is selected

b3: -ERROR indication.
0 = Error has been detected by the printer.
1 = No error detected by the printer.

b2-0: Reserved = 0.

Parallel Control Port: Base +02H (R/W)

b7,6: Reserved.

b5: Parallel Control Direction, valid in extended mode only (CR#2<6> = 1).
In Printer mode, the direction is always out, regardless of the state of this bit.
0 = Output/Write.
1 = Input/Read.

b4: IRQEN, Interrupt Request Enable.
0 = IRQ disabled.
1 = IRQ enabled, generates interrupt when -ACK changes from active to inactive

b3: SLCTIN (pin 17, -SLCTIN), inverted output,
0 = Printer not selected.
1 = Printer selected.

b2: -INIT (pin 16, -INIT).
0 = Initializes the printer.
1 = Normal mode.

b1: AUTOFD (pin 14, -AUTOFD), inverted output.
0 = No autofeed.
1 = Generate line feed after the end of each line

b0: STROBE (pin 1, -STROBE), inverted output.
0 = No Strobe.
1 = Generate -STROBE signal.

Parallel Port Connector

The parallel port connector is a female 25 pin D-shell. The parallel port signals can be connected directy from the 82C601 to the connector. Typically the signals are assigned to the pins as shown below.

Pin	I/O	Name	Pin	I/O	Name
1	O	-STROBE	13	I	SLCT
2-9	I/O	PD0-PD7	14	O	-AUTOFD
10	I	-ACK	15	I	-ERROR
11	I	BUSY	16	O	-INIT
12	I	PE	17	O	-SLCTIN

INTEGRATED DRIVE ELECTRONICS INTERFACE

The IDE interface allows users to utilize hard disks with embedded controller (AT and XT interface). The 82C601 provides the control signals for the IDE interface and the IDE buffers, as shown below:

-IDEENL:	Low Byte Buffer Enable (AT and XT).
-IDEENH:	High Byte Buffer Enable (AT only).
-HDCS:	Primary Hard Disk Chip Select, decodes 1F0H-1F7H (AT) or 320H-323H (XT).
-FDCS:	Primary Floppy Disk Chip Select, I/O decode 3F0H-3F7H (AT and XT).
-IOCS16:	When active it indicates 16 bit I/O transfer (AT only).
IDED7:	D7 of the IDE interface should be connected to this pin (AT only).
-HDACK:	Hard Disk DMA Acknowledge (XT only).

-IDEENL becomes active when the 82C601 decodes addresses 1F0H-1F7H, 3F6H, and 3F7H in the AT mode, or 320H-323H and DMA transfers (-HDACK=0) in the XT mode. -IDEENH becomes active only when -IOCS16 is active and address range 1F0H-1F7H, and in AT mode (CR#0CH<6>=0). -IOCS16 is generated by the Hard Disk Controller when it requires a 16 bit transfer. IDED7 should be connected directy to data bit 7 of the IDE interface. The AT mode supports programmed I/O only (8 and 16 bit). XT mode supports only 8 bit DMA and 8 bit programmed I/O. Pin 66 is multiplexed, in the AT mode it is -IOCS16, in the XT mode it is -HDACK signal.

There are 2 modes of the IDE interface:

AT mode: 8/16 bit programmed I/O only (no DMA). AT mode decodes addresses 1F0H-1F7H, 3F6H and 3F7H. Normal transfer is 8 bit; 16 bit transfer is performed when -IOCS16 is active and on data register (1F0H). Both -IDEENL (low buffer enable) and -IDEENH (high buffer enable) are active during 16 bit transfer. -HDCS is active whenever the 82C601 decodes programmed I/O address 1F0H-1F7H. -IDEENL is active on all AT mode addresses. On the low byte buffer, only 7 bits (D0-D6) are connected to the data bus. Bit 7 is a special case; it is sourced from the 82C601. On the IDE interface , IDED7 is connected directly to the connector. D7 of the 82C601 provides data bit 7 to the host interface. Normally the 82C601 functions as buffer for D7. Except when reading 3F7H, D0-D7 of the 82C601are tri-stated, -IDEENL is enabled to transfer data bits 0-6 from the IDE to the host; D7 should be supplied by the Floppy Disk Interface.

XT mode: 8 bit programmed I/O or DMA (no 16 bit). Normally DMA transfer is done for the data register (320H) only. During a DMA cycle (indicated by active AEN and -HDACK) -IDEENL is active, allowing the data to flow through the low byte buffer. XT mode decodes I/O address range 320H-323H.

Digital Input Register Definition (3F7H, read only)

b7: -Diskette Change, Diskette interface status (FDC).
b6: -Write Gate (HDC).
b5: -Head Select 3/Reduced Write Current (HDC).
b4: -Head Select 2 (HDC).
b3: -Head Select 1 (HDC).
b2: -Head Select 0 (HDC).
b1: -Drive Select 1 (HDC).
b0: -Drive Select 0 (HDC).

Fixed Disk Register (3F6H, write only)

b7-4: Not Used.
b3: HD3EN.
b2: RESET.
0 = Normal operation, default.
1 = Generate reset to HDC.
b1: -IRQEN.
0 = Enabled interrupt.
1 = Disable interrupt, default.
b0: Reserved.

Game Port Interface (ADAPTER mode only)

-GAMEWR and -GAMERD decode I/O address 200H-207H qualified with -IOW and -IOR respectively. The game port decode is not included in PBDIR buffer control, thus it should be connected directly to the SD bus. Register definition:

bit #	Name	Description
7	BTN7	Fire button 4
6	BTN6	Fire button 3
5	BTN5	Fire button 2
4	BTN4	Fire button 1
3	POS3	Joystick 4 position
2	POS3	Joystick 3 position
1	POS3	Joystick 2 position
0	POS3	Joystick 1 position

ABSOLUTE MAXIMUM RATINGS:

Symbol	Min	Max	Unit
Supply Voltage (Vcc)	3.0	7.0	Volts
Supply Current (Icc)		tbd	mA
Input Voltage (Vi)	-0.5	5.5	Volts
Operating Temperature (Ta)	0	70	C
Storage Temperature (Tstg)	-40	125	C

DC CHARACTERISTICS:

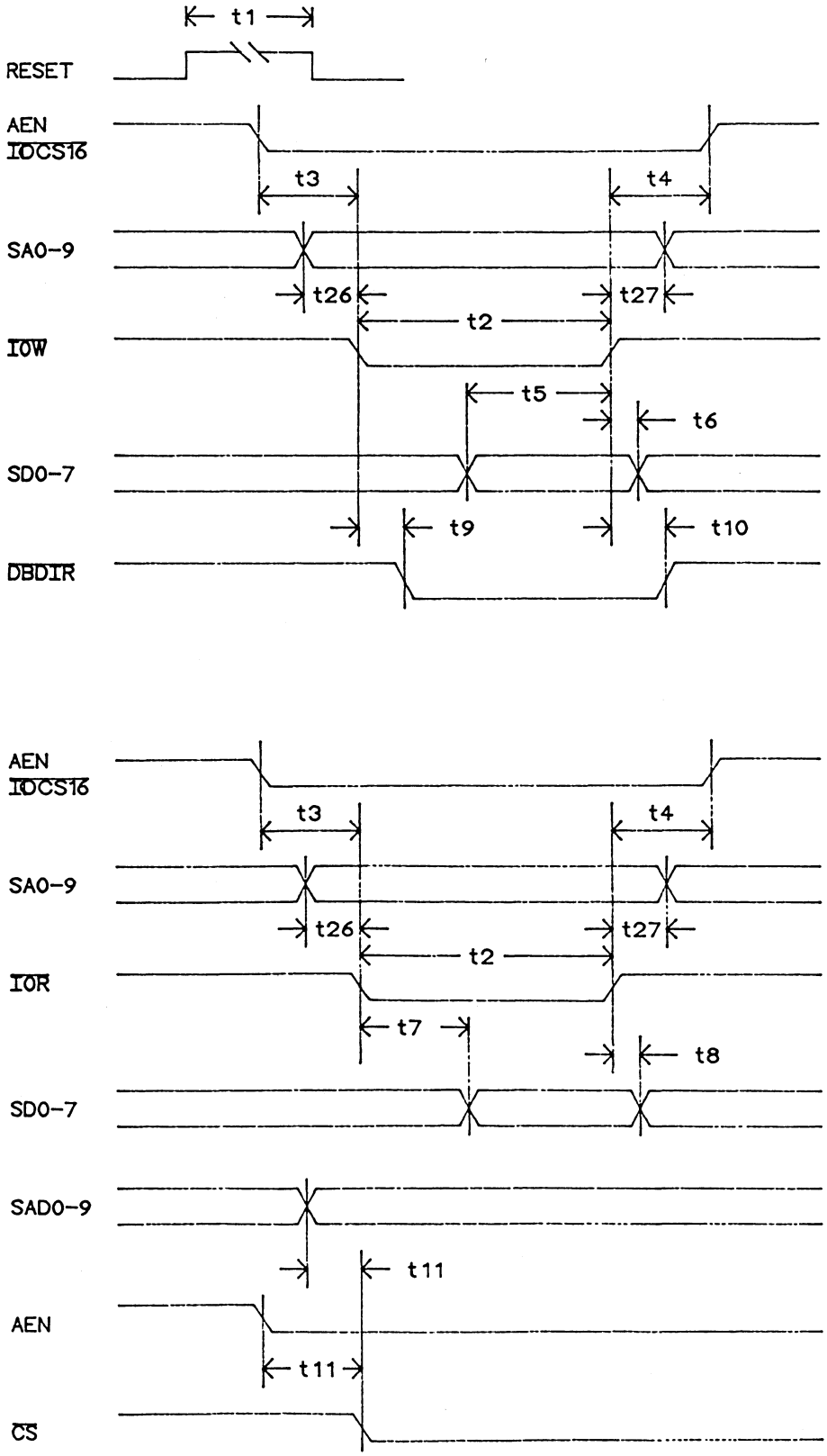
Type	Symbol	Min	Typ	Max	Unit	Test Condition
	Vcc	4.5	5.0	5.5	V	
OL	Iol	4.0			mA	Vol_max=0.4V
	Ioh	-1.0			mA	Voh_min=2.4V
O	Iol	8.0			mA	Vol_max=0.4V
	Ioh	-1.0			mA	Voh_min=2.4V
O1	Iol	16			mA	Vol_max=0.5V
	Ioh	-200			uA	Voh_min=2.4V
T,	Ioh	24			mA	Vol_max=0.5V
O2	Iol	-8			mA	Voh_min=2.4V
	Iil			-20	uA	Vcc_max, Vil=0.4V, all inputs
	Iih			20	uA	Vcc_max, Vih=2.7V, all inputs
	Vil			0.8	V	All inputs
	Vih	2.0			V	
	Vol			0.4	V	Iol_max, Vcc_min,Vil_max, Vih=2V
	Voh	2.4			V	Vcc_min, Ioh_max, Vil=0.5V, Vih=2V
	Istby			tbd	uA	Standby current without clocks, @ Vcc_min, PWRGD active

Note:
- OL = Low Output buffer
- O = Normal Output buffer
- T = Tristate High Output buffer
- O1 = High Output buffer
- O2 = High Output buffer
- I = TTL Input buffer
- IS = Schmitt Trigger Input buffer

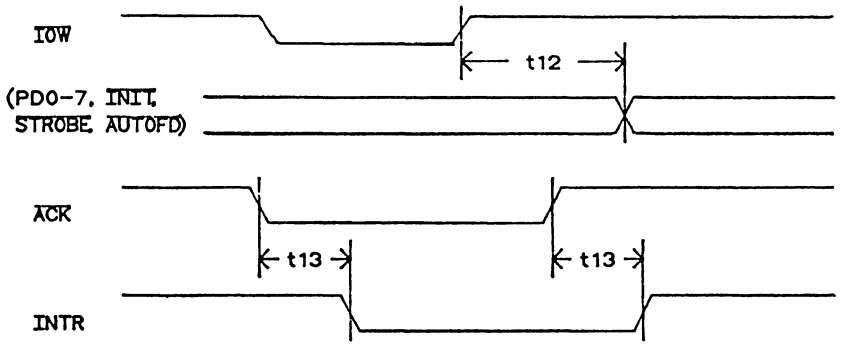
AC CHARACTERISTICS:

Sym	Description	min	max	unit	
Host Interface Timing					
t1	RESET width		1		us
t2	-IOR, -IOW width		150		ns
t3	AEN, -IOCS16 setup time to -IOR, -IOW		40		ns
t4	AEN, -IOCS16 hold time from -IOR, -IOW		10		ns
t26	SA setup time to -IOR, -IOW		40		ns
t27	SA hold time from -IOR, -IOW		10		ns
t5	SD setup time to -IOW		40		ns
t6	SD hold time from -IOR		10		ns
t7	SD delay from -IOR		60		ns
t8	SD hold time from -IOR		10	80	ns
t9	DBDIR active delay from -IOR, -IOW			40	ns
t10	DBDIR inactive delay from -IOR, -IOW			80	ns
t11	-CS delays from AEN, SA			40	ns
Parallel Port Timing					
t12	PD,-INIT,-STROBE,-AUTOFD,-SLCTIN delay from SD			100	ns
t13	INTR delay from ACK			60	ns
IDE Interface Timing					
t14	-IDEENL, -IDEENH delay from AEN, -IOCS16			40	ns
t15	-IDEENL, -IDEENH delay from SA			40	ns
t16	IDED7 to SD7 delay (read cycle)			60	ns
t17	SD7 to IDED7 delay (write cycle)			40	ns
DMA Interface Timing					
t18	-DACK setup time to -IOR, -IOW		40		ns
t19	-DACK hold time from -IOR, -IOW		40		ns
t20	-DACK to -IDEENL, -IDEENH delay			40	ns
t21	AEN, -IOCS16 to -IDEENL, -IDEENH delay			40	ns
Serial Port Timing					
t21	-IOW to -RTS, -DTR, -OUT1 delay			100	ns
t22	-IOW to INTR 3-state delay		10	100	ns
t23	INTR active delay from -CTS, -DSR, -DCD			100	ns
t24	INTR inactive delay from -IOR			100	ns
t25	INTR inactive delay from -IOW			100	ns

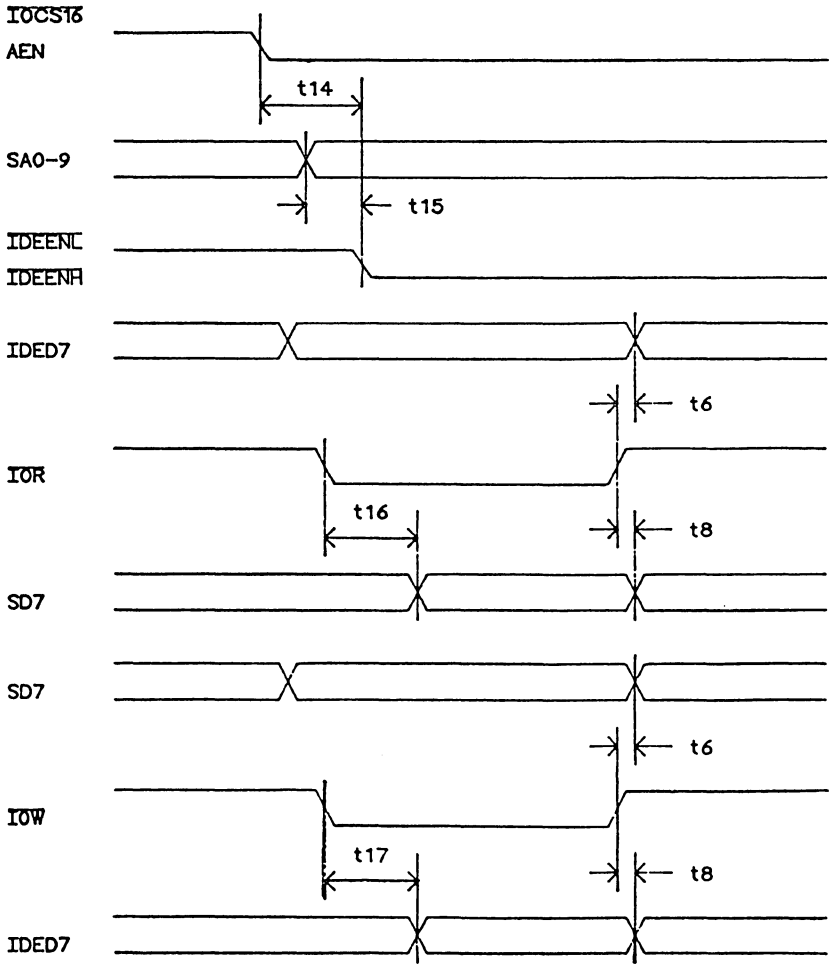
HOST INTERFACE TIMING



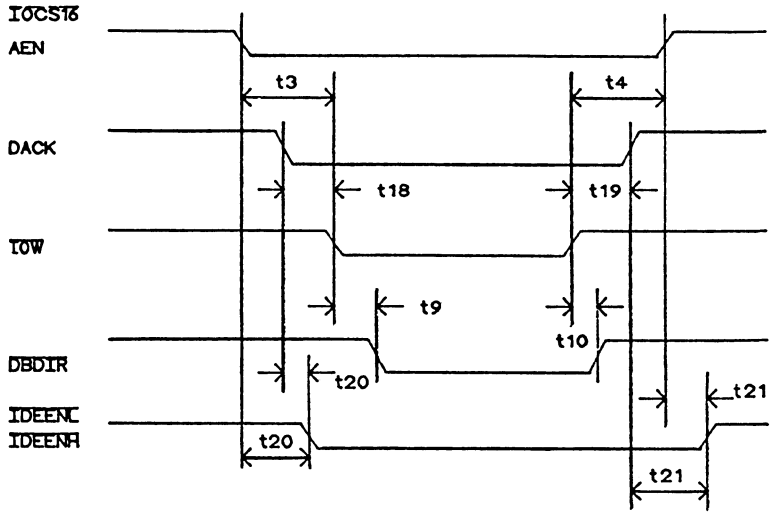
PARALLEL PORT TIMING



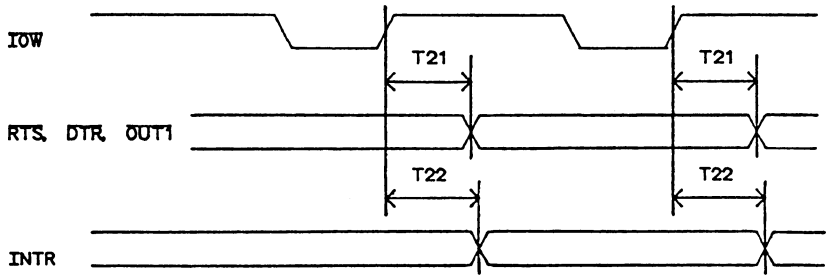
IDE INTERFACE TIMING

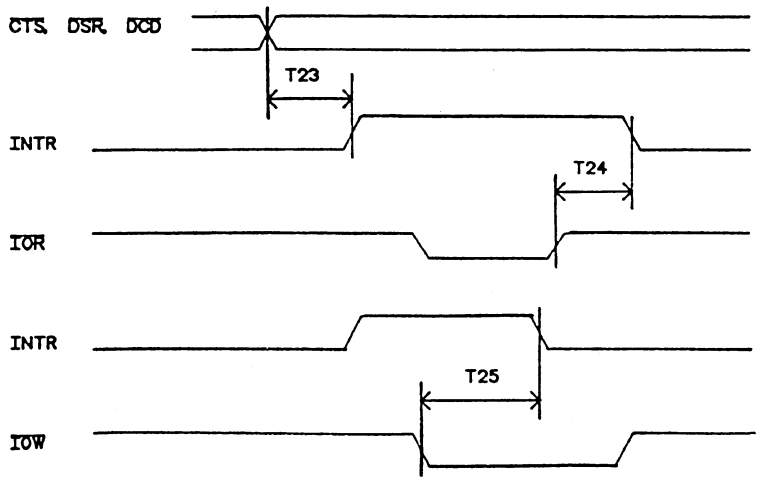


DMA TIMING



SERIAL PORT TIMING

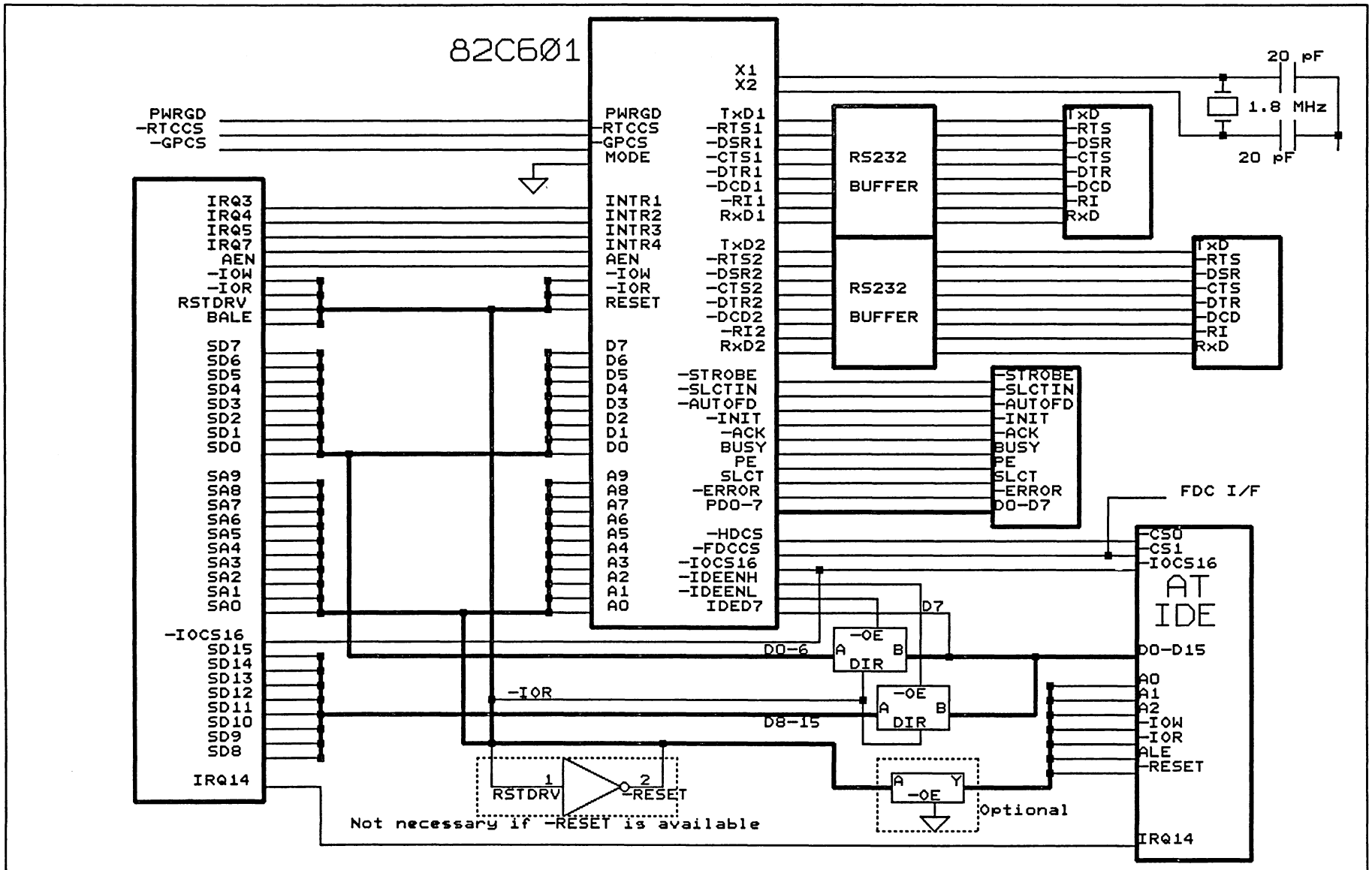




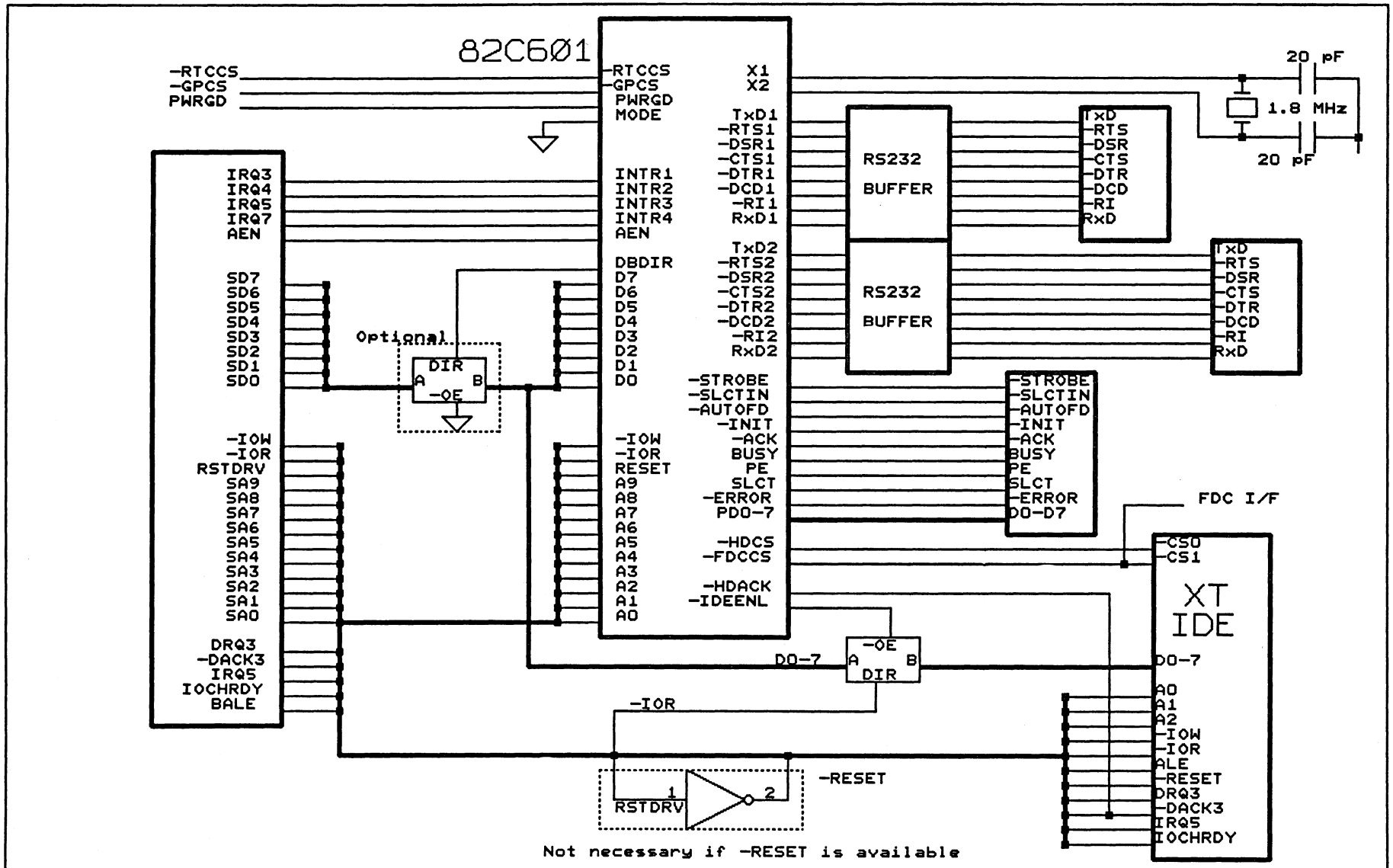
84 PLCC Pinout

1 - -RTCCS(PP1)
2 - Vcc
3 - -GPCS(PP0)
4 - IDED7(PSP1)
5 - -HDCS(PSP0)
6 - -IDEENH(-GAMEWR)
7 - -IDEENL(-GAMERD)
8 - -FDCS(ASP0)
9 - INTR4(ASP1)
10 - Vcc
11 - N/C
12 - Vss
13 - INTR3(PPIRQ)
14 - INTR2(SP1IRQ)
15 - INTR1(SP2IRQ)
16 - Vss
17 - DBDIR
18 - A0
19 - A1
20 - A2
21 - A3
22 - A4
23 - A5
24 - A6
25 - A7
26 - A8
27 - A9
28 - AEN
29 - -IOR
30 - -IOW
31 - RESET
32 - N/C
33 - D0
34 - D1
35 - D2
36 - D3
37 - Vss
38 - D4
39 - D5
40 - D6
41 - D7
42 - PD7
43 - PD6
44 - Vcc
45 - PD5
46 - PD4
47 - PD3
48 - PD2
59 - PD1
50 - PD0
51 - -STROBE
52 - -SLCTIN
53 - N/C
54 - -INIT
55 - -AUTOFD
56 - Vss
57 - -ACK
58 - BUSY
59 - PE
60 - SLCT
61 - -ERROR
62 - -CTS1
63 - -DSR1
64 - -DCD1
65 - -RI1
66 - RxD1
67 - -RTS1
68 - -DTR1
69 - TxD1
70 - -CTS2
71 - -DSR2
72 - -DCD2
73 - -RI2
74 - N/C
75 - RxD2
76 - -RTS2
77 - -DTR2
78 - TxD2
79 - PWRGD(SSP0)
80 - -IOCS16(SSP1)
81 - X1
82 - X2
83 - MODE
84 - Vss

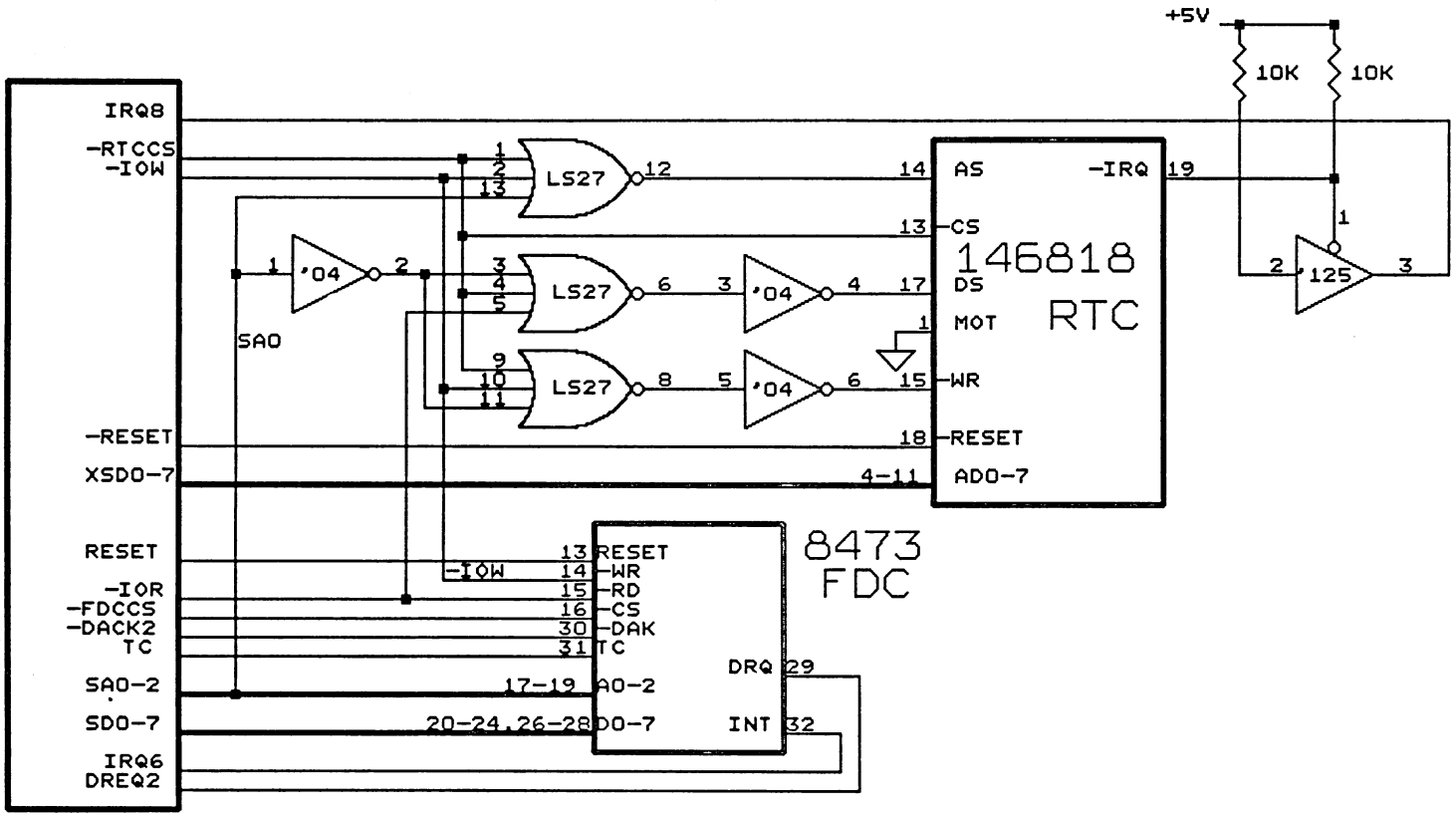
Index:



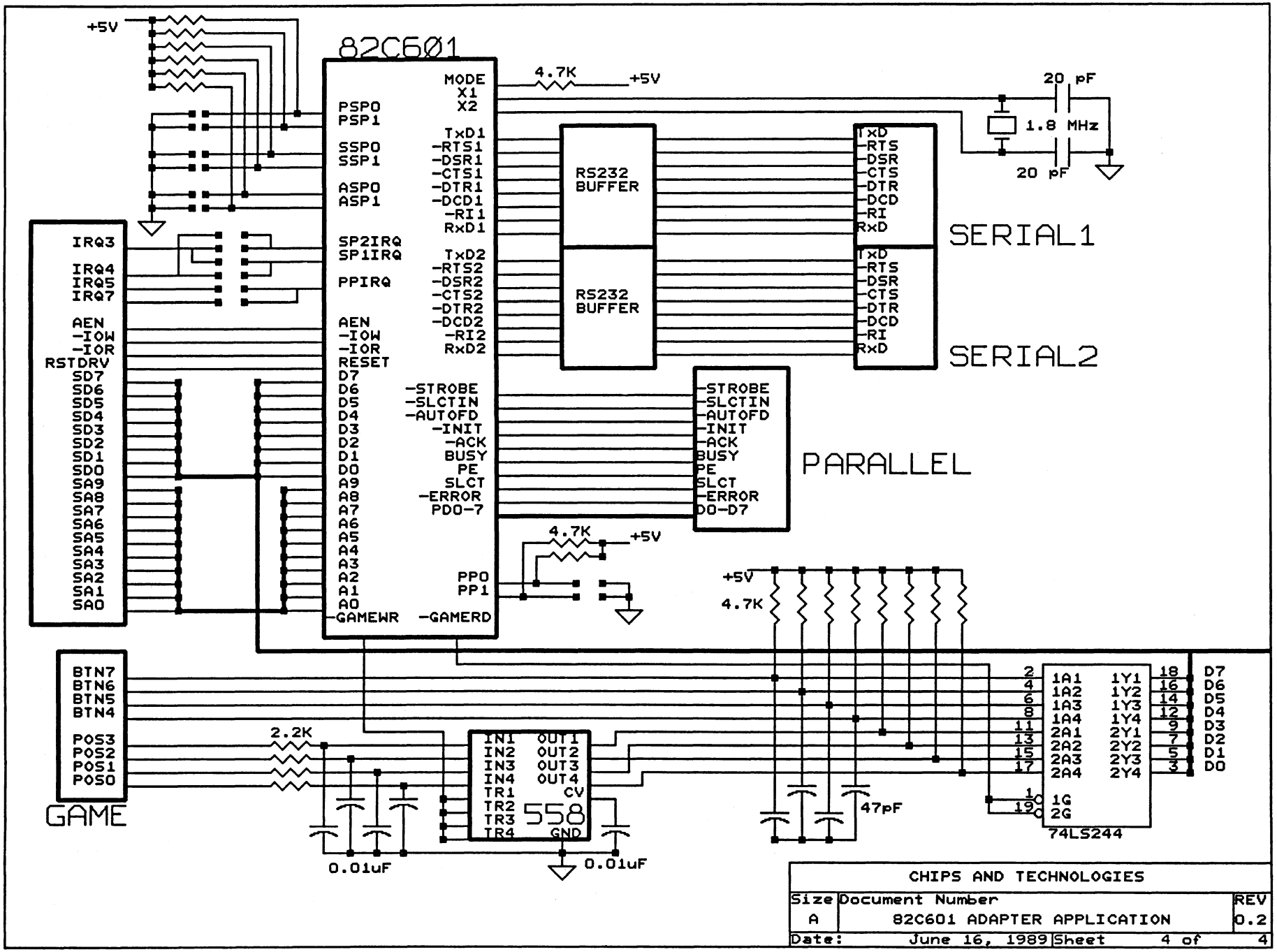
CHIPS AND TECHNOLOGIES		
Size	Document Number	REV
A	82C601 MOTHER BOARD APPLICATION	0.3
Date: June 16, 1989	Sheet 1 of	4



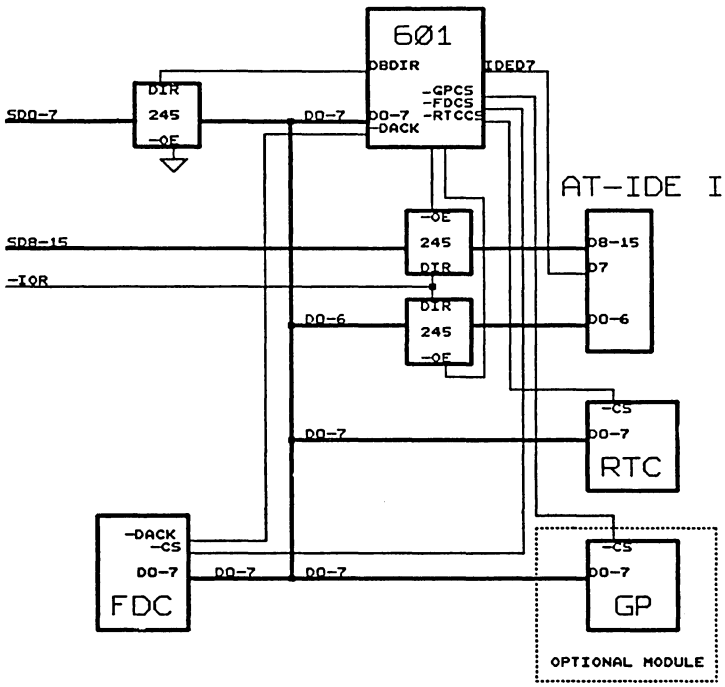
CHIPS AND TECHNOLOGIES		
Size	Document Number	REV
A	82C601 MOTHER BOARD W/ XT-IDE	0.3
Date: June 16, 1989	Sheet 2 of 4	



CHIPS AND TECHNOLOGIES		
Size: A	Document Number: 82C601 FDC & RTC INTERFACE	REV: 0.3
Date: June 16, 1989	Sheet 3 of 4	

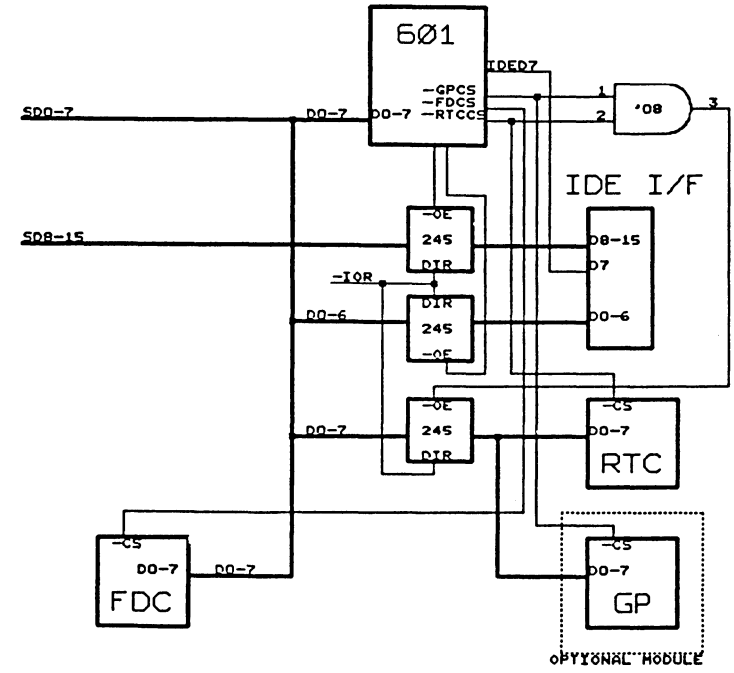


CHIPS AND TECHNOLOGIES		
Size: A	Document Number: 82C601 ADAPTER APPLICATION	REV: 0.2
Date: June 16, 1989	Sheet 4 of 4	



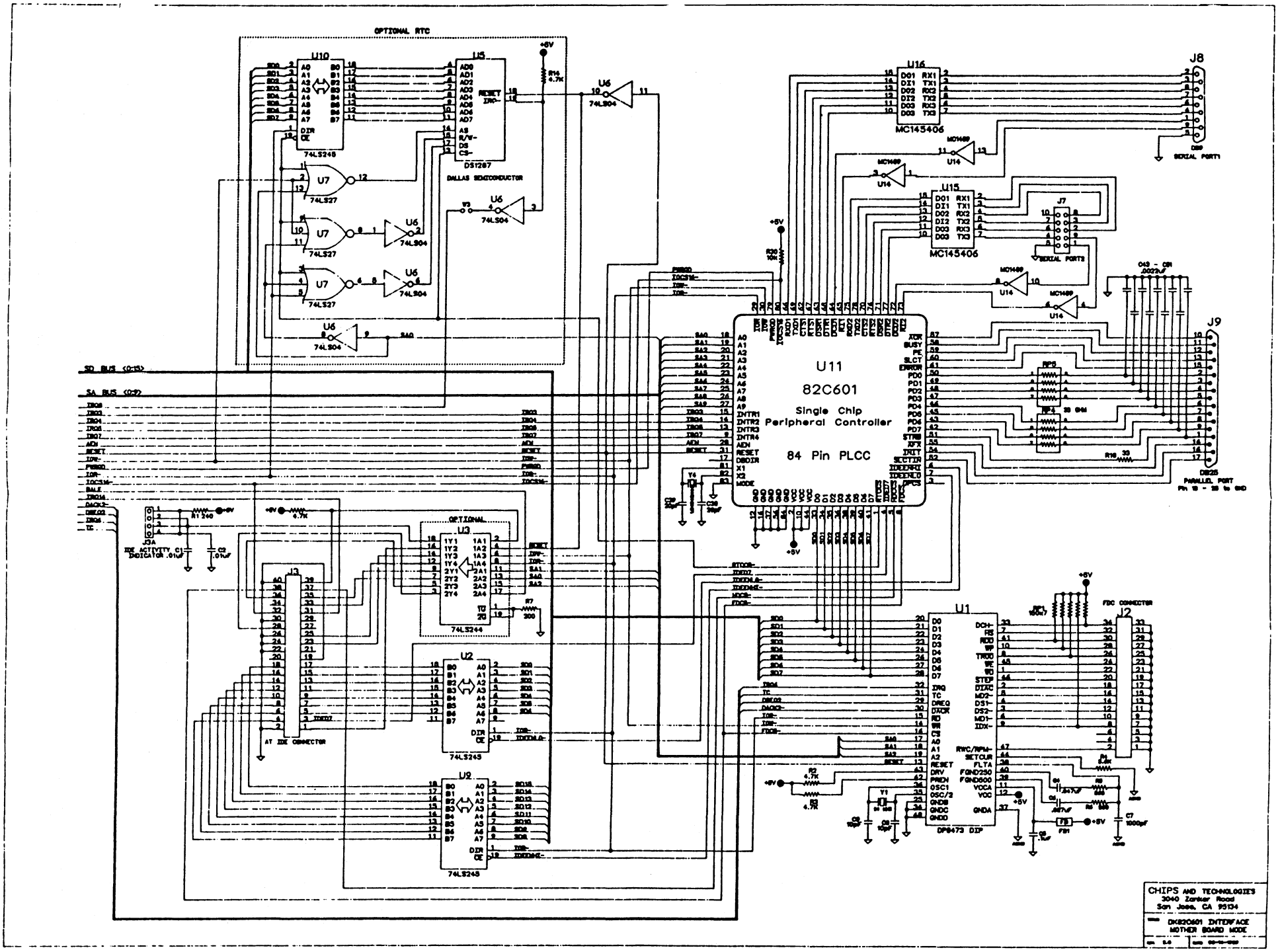
1 BUFFER: RTC+GP+IDE+FDC
FDC @ DMA

CHIPS AND TECHNOLOGIES		
Size A	Document Number ONE BUFFER	REV 0.1
Date: March 27, 1989	Sheet 1 of 5	



1 BUFFER: RTC+GP

CHIPS AND TECHNOLOGIES		
Size A	Document Number ONE BUFFER	REV 0.1
Date: March 27, 1989	Sheet 2 of 5	


OPTIONAL RTC
U11
82C601
Single Chip
Peripheral Controller
84 Pin PLCC
U1
DP8473 DIP
U2
74LS245
U3
74LS244
U5
DS1287
DALLAS SEMICONDUCTOR
U6
74LS04
U7
74LS27
U9
74LS245
U10
74LS245
U14
MC1489
U15
MC145406
U16
MC145406
J2
FDC CONNECTOR
J3A
IDE ACTIVITY CONNECTOR
J3
AT IDE CONNECTOR
J7
SERIAL PORT2
J8
DB9
SERIAL PORT1
J9
DB25
PARALLEL PORT
SD BUS (0:15)
SA BUS (0:9)
CHIPS AND TECHNOLOGIES
3040 Zanker Road
San Jose, CA 95134
DK82C601 INTERFACE
MOTHER BOARD MODE