Signetics

82S105 (PLS105)
Field-Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic

Product Specification

Military
Application Specific Products

DESCRIPTION

The 82S105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 16 external inputs, I_{0-15}, with six internal inputs, P_{0-5}, fed back from the State Register to form up to 48 transition terms (AND terms).

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

FEATURES

- Field-programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition Complement Array
- Positive edge-trigger clock
- Programmable asynchronous preset or Output Enable
- Power-on preset to all "1" of internal registers
- f_{MAX} = 10.5MHz
- 650mW power dissipation (typical)
- TTL compatible
- Single +5V supply
- 3-state outputs

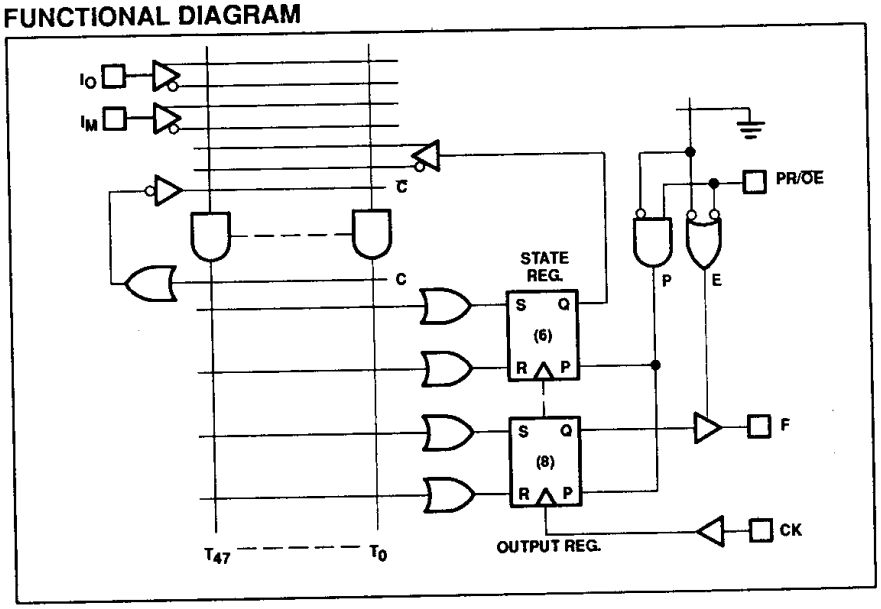
APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

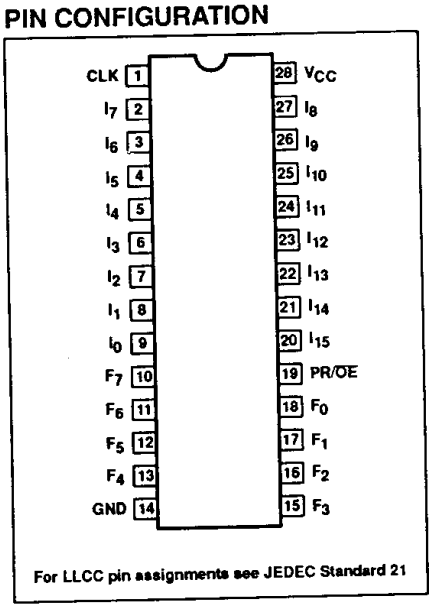
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP 600mil-wide	82S105/BXA
28-Pin CLCC	82S105/B3A
28-Pin Ceramic FlatPack	82S105/BYA

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



For LLCC pin assignments see JEDEC Standard 21

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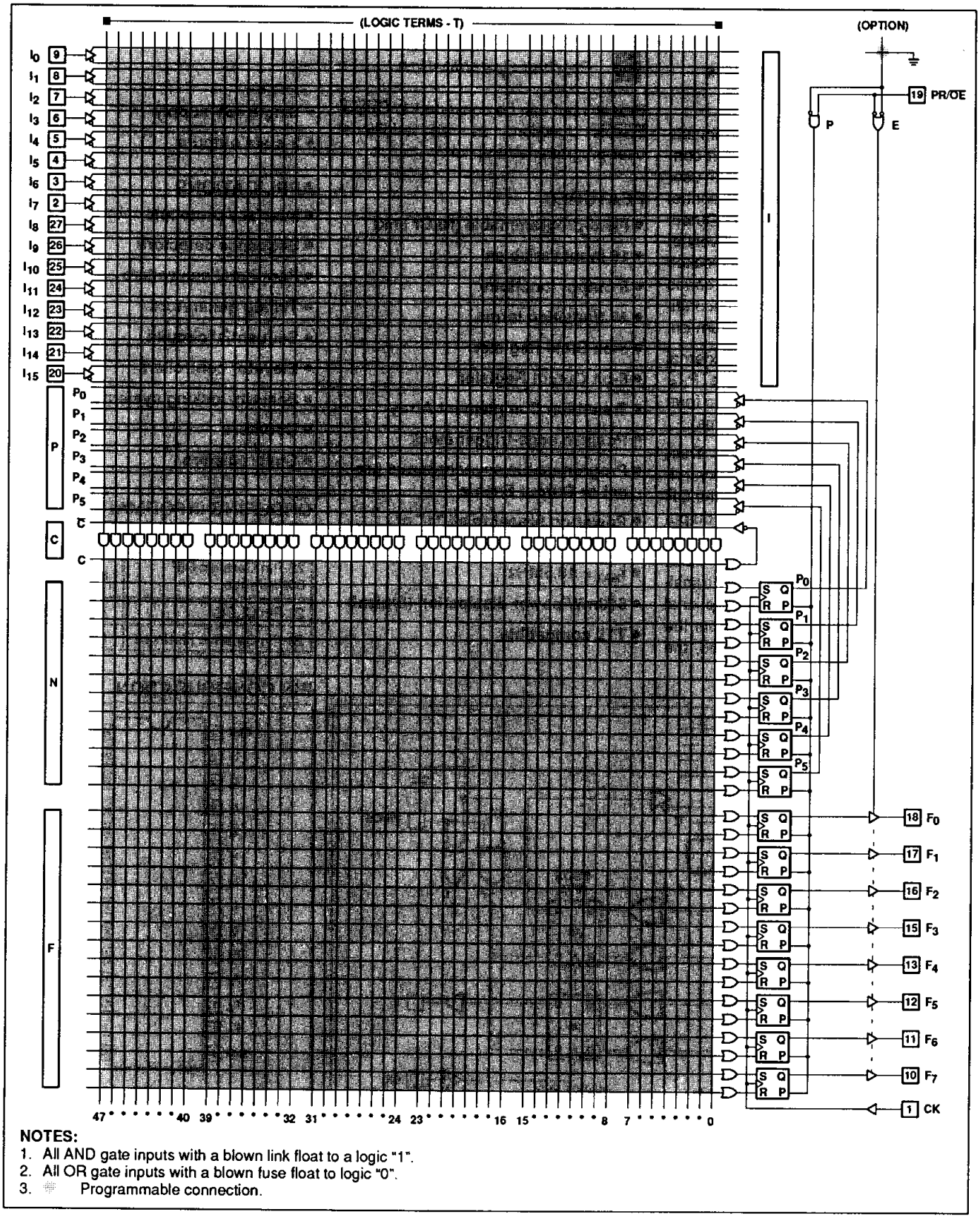
FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ✱ Programmable connection.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 - 8 20 - 27	I_{1-15}	**Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I_0	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-5} reflect the contents of State Register bits P_{0-5}. The contents of each Output Register remains unaltered.	Active-High/Low
10 - 13 15 - 18	F_{0-7}	**Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits Q_{0-7}, when enabled. When I_0 is held at +10V, $F_{0-5} = (P_{0-5})$, and $F_{6,7}$ = Logic "1".	Active-High
19	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F_{0-7} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers F_{0-7} from the Output Register.	Active-High (H) Active-Low (L)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_{IK}	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_A	Operating temperature range	-55	+125	°C
T_{STG}	Storage temperature range	-65	+150	°C

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DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
Input Voltage						
V_{IH}	High	V_{CC} = 5.5V	2			V
V_{IL}	Low	V_{CC} = 4.5V			0.8	V
V_{IK}	Clamp[4]	V_{CC} = Min, I_{IK} = -18mA		-0.8	-1.2	V
Output Voltage						
V_{OH}	High[5]	V_{CC} = 4.5V, I_{OH} = -2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.5	V
Input Current						
		V_{CC} = 5.5V				
I_{IH}	High	V_I = 5.5V		<1	50	µA
I_{IL}	Low	V_I = 0.45V		-10	-150	µA
I_{IL}	Low (CK input)	V_I = 0.45V		-50	-350	µA
Output Current						
		V_{CC} = 5.5V				
$I_{O(OFF)}$	Hi-Z state[7]	V_O = 5.5V		1	60	µA
		V_O = 0.45V		-1	-60	µA
I_{OS}	Short circuit[4,8]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = 5.5V		120	185	mA
Capacitance[7,10]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		8	13	pF
C_{OUT}	Output	V_O = 2.0V		10	15	pF

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AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[11]	LIMITS Max	UNIT
Pulse Width							
t_{CKH}	Clock[12] High	CK-	CK+	40	15		ns
t_{CKL}	Clock Low	CK+	CK-	40	15		ns
t_{CKP1}	Period (w/o C-array)	CK+	CK+	95	40		ns
t_{CKP2}	Period (w/C-array)[10]	CK+	CK+	135	60		ns
t_{PRH}	Preset pulse	PR+	PR-	40	15		ns
Setup Time							
t_{IS1}	Input	CK+	Input±	60			ns
t_{IS2}	Input (through Complement array)[13]	CK+	Input±	100			ns
t_{VS}	Power-on preset[13]	CK-	V_{CC}+	5	-10		ns
t_{PRS}	Preset[10]	CK-	PR-	5	-10		ns
Hold Time							
t_{IH}	Input[10]	Input±	CK+	10	-10		ns
Propagation Delay							
t_{CKO}	Clock	Output±	CK+		15	35	ns
t_{OE}	Output Enable[13]	Output-	OE-		20	40	ns
t_{OD}	Output Disable[13]	Output+	OE+		20	40	ns
t_{PR}	Preset	Output+	PR+		18	45	ns
t_{PPR}	Power-on preset[10]	Output+	V_{CC}+		0	20	ns
Frequency of Operation							
f_{MAX}	w/o C-array					10.5	MHz
f_{MAX}^C	w/C-array[10]					8.3	MHz

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{OE}$ and a logic High stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a Low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, the outputs open.
10. Guaranteed, but not tested.
11. All typical values are at V_{CC} = 5V, T_A = +25°C.
12. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 30ns.
13. Not testable on unprogrammed devices.

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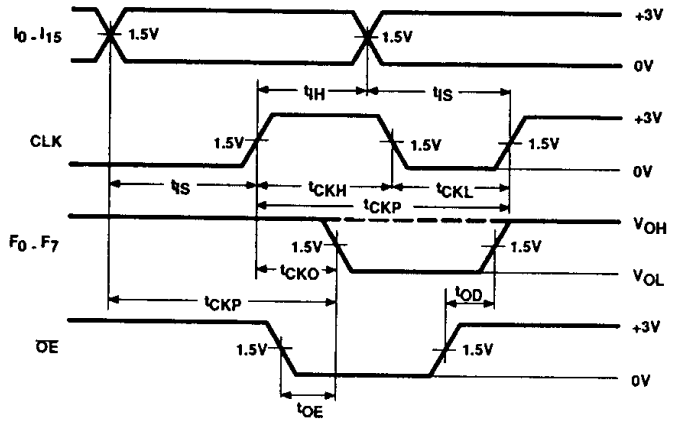
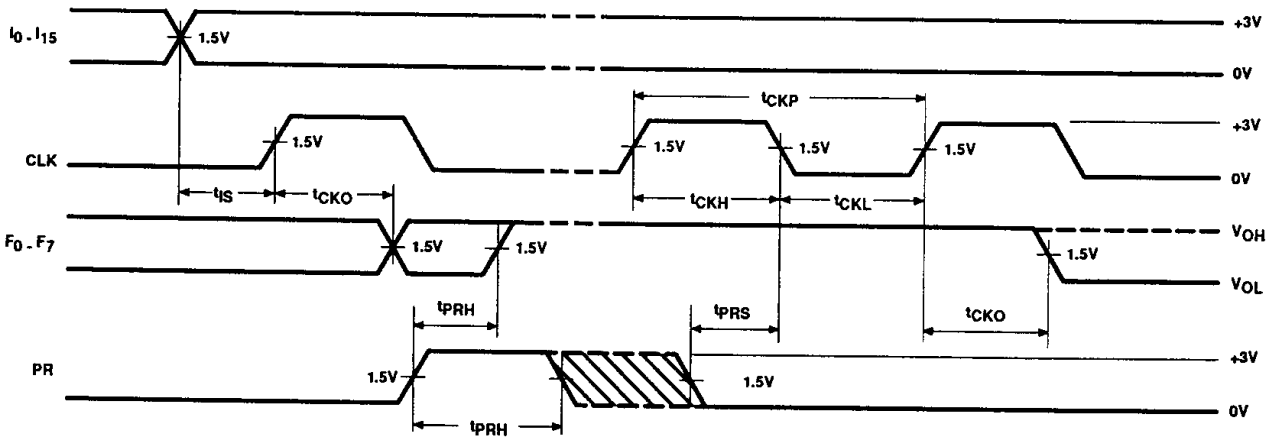
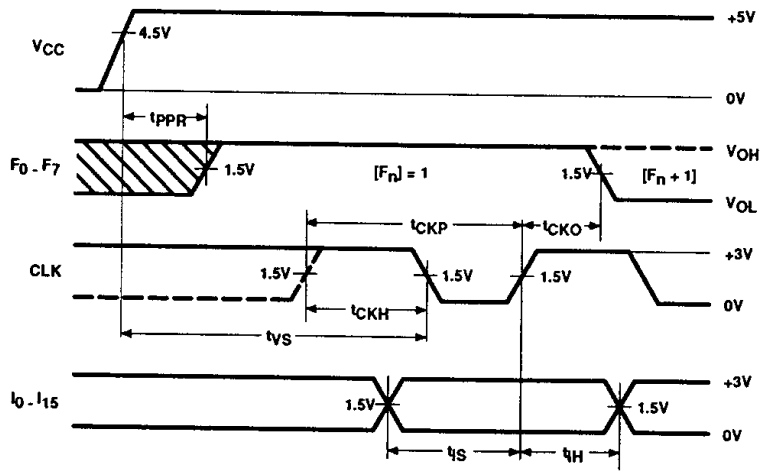
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



Power-On Preset

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TIMING DEFINITIONS

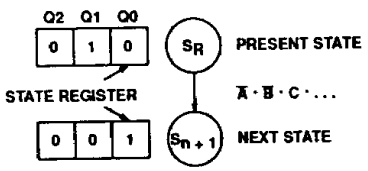
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Operating period — when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{CKP2}	Operating period — when using Complement Array.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).

SYMBOL	PARAMETER
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{CKO}	Delay between positive transition of Clock and when outputs become valid (with PR/$\overline{OE}$ Low).

SYMBOL	PARAMETER
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the Off-State.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

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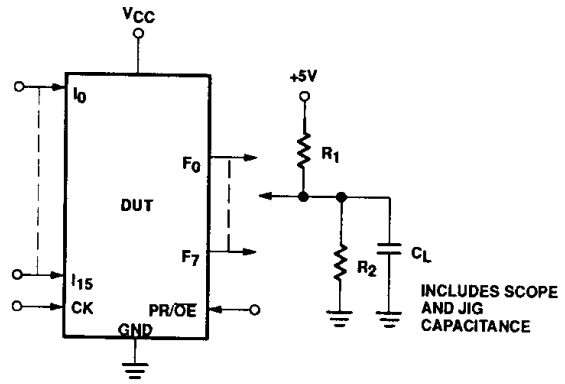
TRUTH TABLE

V_{CC}	OPTION							
	PR	$\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

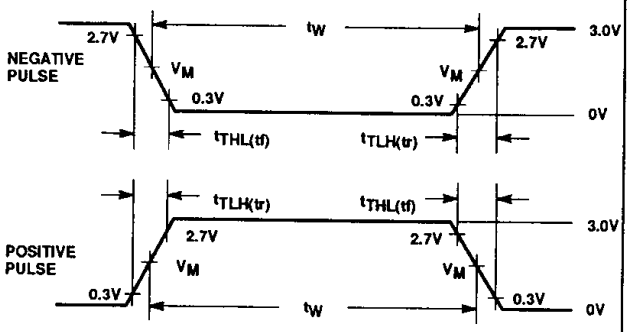
NOTES:
1. Positive Logic $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$; $T_n = C(I_0\, I_1\, I_2 \ldots)(P_0\, P_1 \ldots P_8)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

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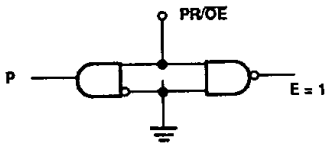
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

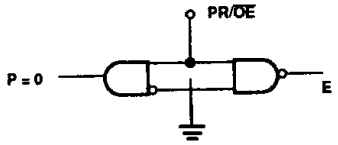
With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term T_n is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

PRESET/OE OPTION - (P/E)



OPTION	CODE
PRESET	H

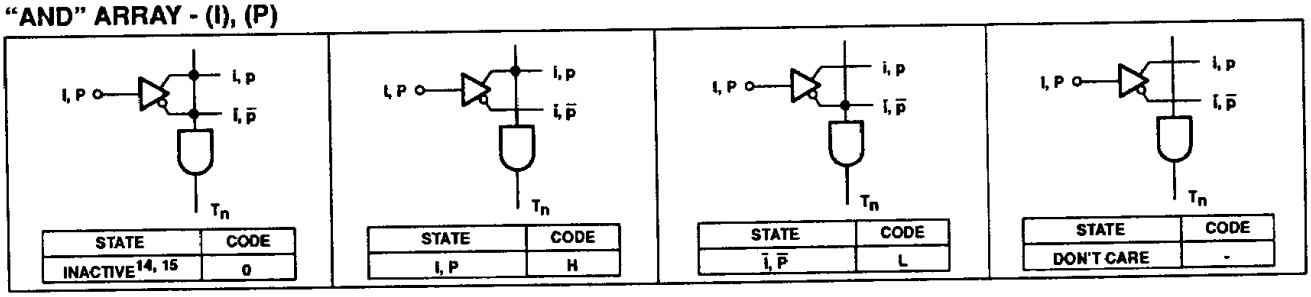


OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE 82S105:

The 82S105 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY - (I), (P)



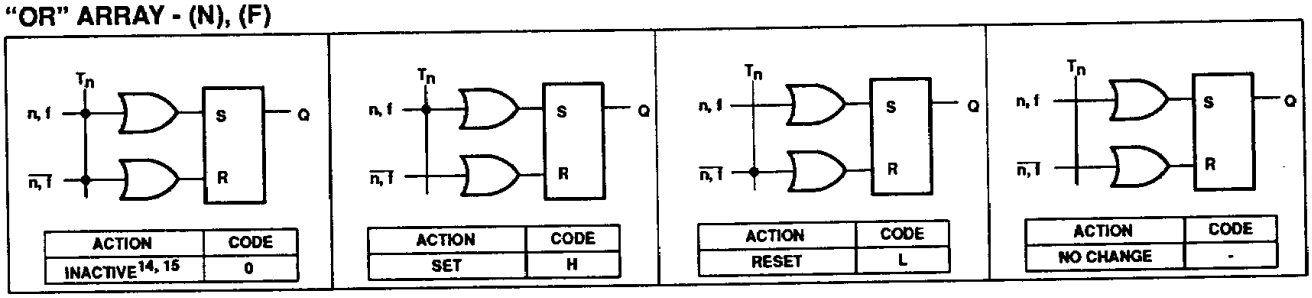
STATE	CODE
INACTIVE[14, 15]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{I}$, $\overline{P}$	L

STATE	CODE
DON'T CARE	-

"OR" ARRAY - (N), (F)



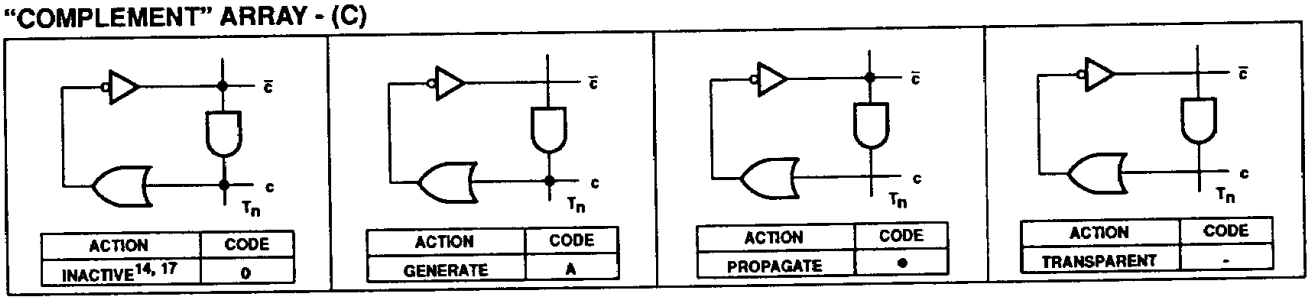
ACTION	CODE
INACTIVE[14, 15]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	-

"COMPLEMENT" ARRAY - (C)



ACTION	CODE
INACTIVE[14, 17]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	-

NOTES:

14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
15. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

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FPLS PROGRAM TABLE

CUSTOMER NAME _____
PURCHASE ORDER # _____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____
PROGRAM TABLE _____
REV _____
DATE _____

PROGRAM TABLE ENTRIES

AND

INACTIVE	0	C_n
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	—	

INACTIVE	0	I_m, P_s
I, P	H	
$\overline{I}$, $\overline{P}$	L	
DON'T CARE	—	

OR

INACTIVE	0	Ns, Fr
SET	H	
RESET	L	
NO CHANGE	—	

OPTION

PRESET	H	P/E
$\overline{OE}$	L	

TERM	C_n	AND: INPUT (I_m) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (P_s) 5 4 3 2 1 0	REMARKS	OPTION (P/E) OR: NEXT STATE (Ns) 5 4 3 2 1 0	OPTION (P/E) OR: OUTPUT (Fr) 7 6 5 4 3 2 1 0
0						
1						
2						
3						
4						
5						
6						
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42						
43						
44						
45						
46						
47						
PIN NO.		20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9				10 11 12 13 15 16 17 18
VARIABLE NAME						

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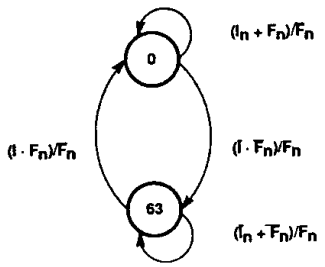
TEST ARRAY

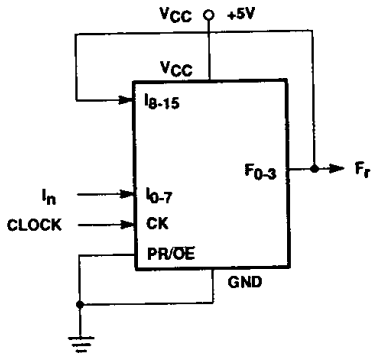
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-7} as shown in the test circuit timing diagram.



State Diagram



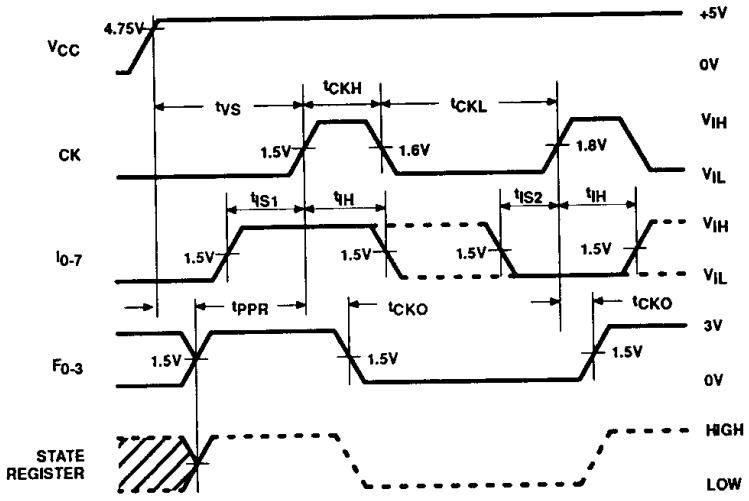
FPLS Under Test

TEST ARRAY PROGRAM

TERM	C	AND: INPUT (Im) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 5	4	3	2	1	0	OPTION (P/E) H; OR; NEXT STATE (Ns) 5	4	3	2	1	0	OUTPUT (Fr) 7	6	5	4	3	2	1	0
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	C	AND: INPUT (Im) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PRESENT STATE (Ps) 5	4	3	2	1	0	OPTION (P/E) H; OR; NEXT STATE (Ns) 5	4	3	2	1	0	OUTPUT (Fr) 7	6	5	4	3	2	1	0
48	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	•	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Test Array Deleted

Signetics Packaging Information

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Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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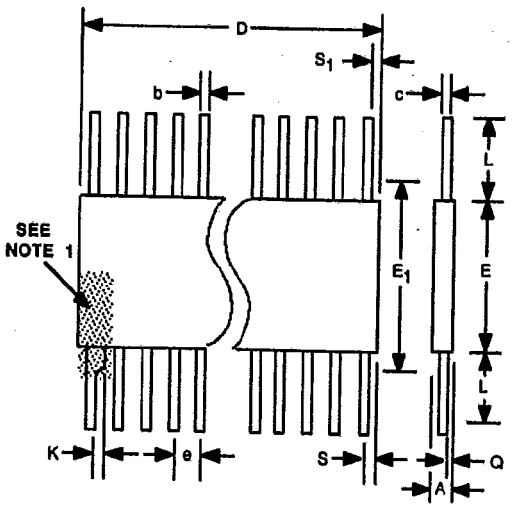
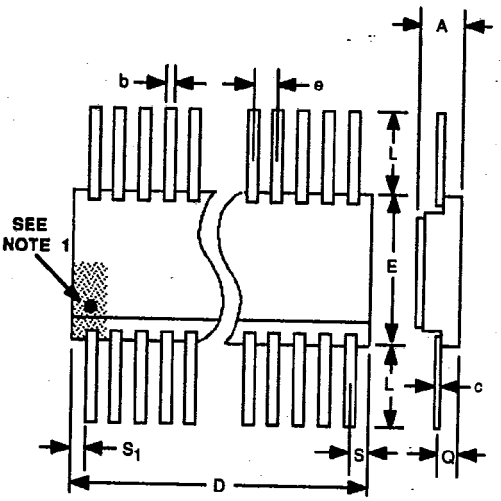
CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

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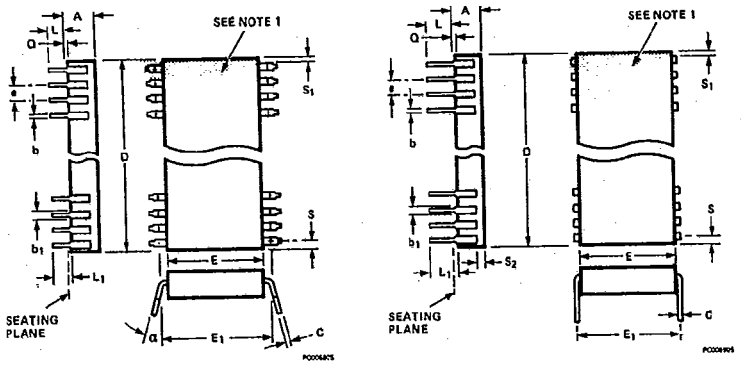
Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1

Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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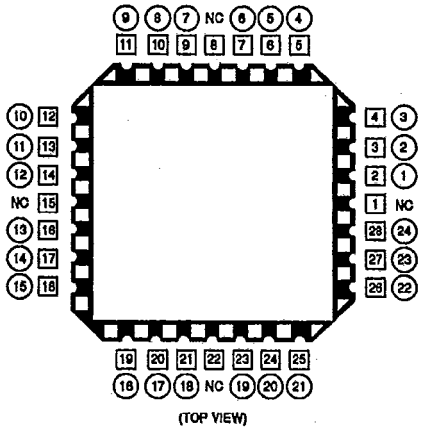
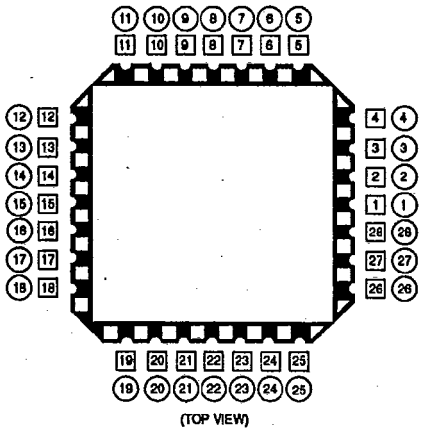
Packaging Information

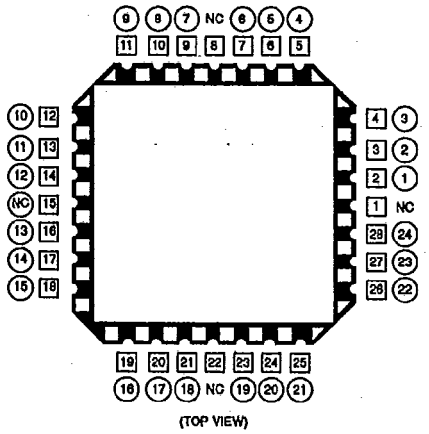
LEADLESS CHIP CARRIER (LLCC) PINOUTS



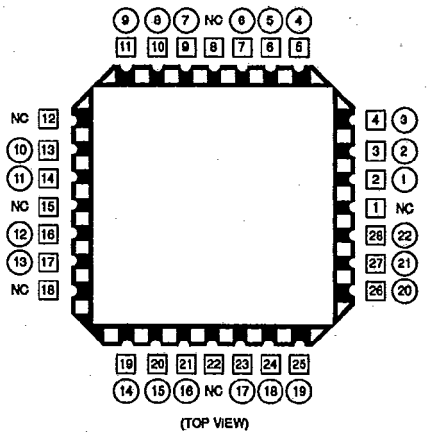
24–Lead Logic Pinout for 28 Terminal Chip Carrier



26–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect