

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S16 and 82S17 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to $25\mu\text{A}$ for a "1" level, and $-250\mu\text{A}$ (S82S16/17) or $-100\mu\text{A}$ (N82S16/17) for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S16 and 82S17 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to $+75^\circ\text{C}$) specify N82S16/17, B or F. For the military temperature range (-55°C to $+125^\circ\text{C}$) specify S82S16/17, F only.

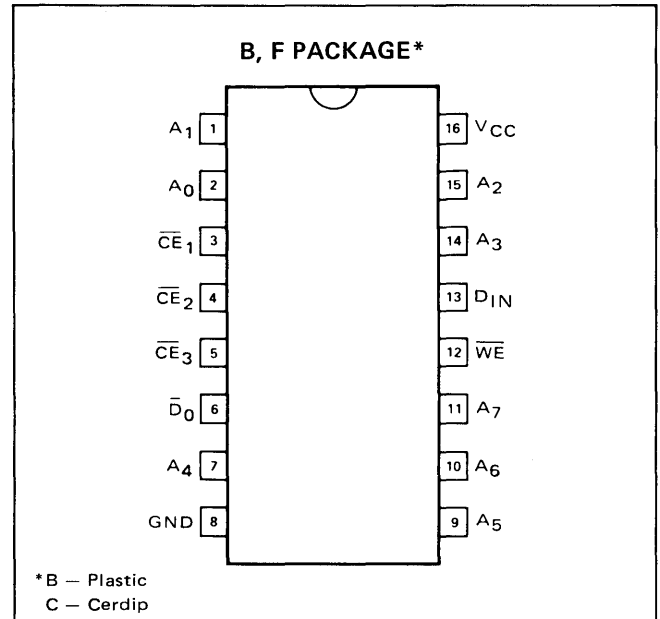
FEATURES

- ORGANIZATION – 256 X 1
- ADDRESS ACCESS TIME:
S82S16, S82S17 – 70ns, MAXIMUM
N82S16, N82S17 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
S82S16, S82S17 – 70ns, MAXIMUM
N82S16, N82S17 – 55ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT TYPICAL
- INPUT LOADING:
S82S16, S82S17 – ($-250\mu\text{A}$) MAXIMUM
N82S16, N82S17 – ($-100\mu\text{A}$) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- 16 PIN CERAMIC DIP
- OUTPUT OPTION:
TRI-STATE – 82S16
OPEN COLLECTOR – 82S17

APPLICATIONS

- BUFFER MEMORY
- WRITABLE CONTROL STORE
- MEMORY MAPPING
- PUSH DOWN STACK
- SCRATCH PAD

PIN CONFIGURATION



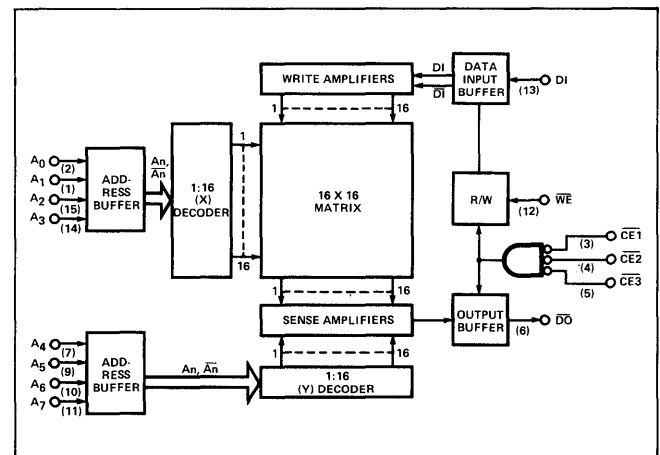
TRUTH TABLE

MODE	$\overline{\text{CE}}^*$	$\overline{\text{WE}}$	D_{IN}	$\overline{\text{D}}_{\text{OUT}}$	
				82S16	82S17
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

**"0" = All $\overline{\text{CE}}$ inputs low; "1" = one or more $\overline{\text{CE}}$ inputs high.

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power Supply Voltage	+7	Vdc
V _{IN} Input Voltage	+5.5	Vdc
V _{OUT} High Level Output Voltage (82S17)	+5.5	Vdc
V _O Off-State Output Voltage (82S16)	+5.5	Vdc
T _A Operating Temperature Range		
S82S16/17	-55° to +125°	°C
N82S16/17	0° to +75°	°C
T _{stg} Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS S82S16/17 -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
 N82S16/17 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	N82S16/17			S82S16/17			UNIT	NOTES
		MIN	TYP ²	MAX	MIN	TYP ²	MAX		
V _{IH} High-Level Input Voltage	V _{CC} = MAX	2.0			2.0			V	1
V _{IL} Low-Level Input Voltage	V _{CC} = MIN			0.85			0.8	V	
V _{IC} Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	V	1, 8
V _{OH} High-Level Output Voltage (82S16)	V _{CC} = MIN, I _{OH} = -3.2mA	2.6			2.4			V	1, 6
V _{OL} Low-Level Output Voltage	V _{CC} = MIN, I _{OL} = 16mA		0.35	0.45		0.35	0.5	V	1, 7
I _{OLK} Output Leakage Current (82S17)	V _{OUT} = 5.5V		1	40		1	40	μA	5
I _{O(OFF)} Hi-Z State Output Current (82S16)	V _{OUT} = 5.5V		1	40		1	50	μA	5
	V _{OUT} = 0.45V		-1	-40		-1	-50	μA	5
I _{IH} High-Level Input Current	V _{CC} = MAX, V _{IN} = 5.5V		1	25		1	25	μA	8
I _{IL} Low-Level Input Current	V _{CC} = MAX, V _{IN} = 0.45V		-10	-100		-10	-250	μA	8
I _{OS} Short-Circuit Output Current (82S16)	V _{CC} = MAX, V _O = 0V	-20		-70	-20		-70	mA	3
I _{CC} V _{CC} Supply Current (82S16/17)	V _{CC} = MAX		80	115		80	120	mA	4
	V _{CC} = MAX, T _A = +125°C						99	mA	4
C _{IN} Input Capacitance	V _{IN} = 2.0V	V _{CC} = 5.0V		5			5	pF	
C _{OUT} Output Capacitance	V _{OUT} = 2.0V			8			8		

NOTES:

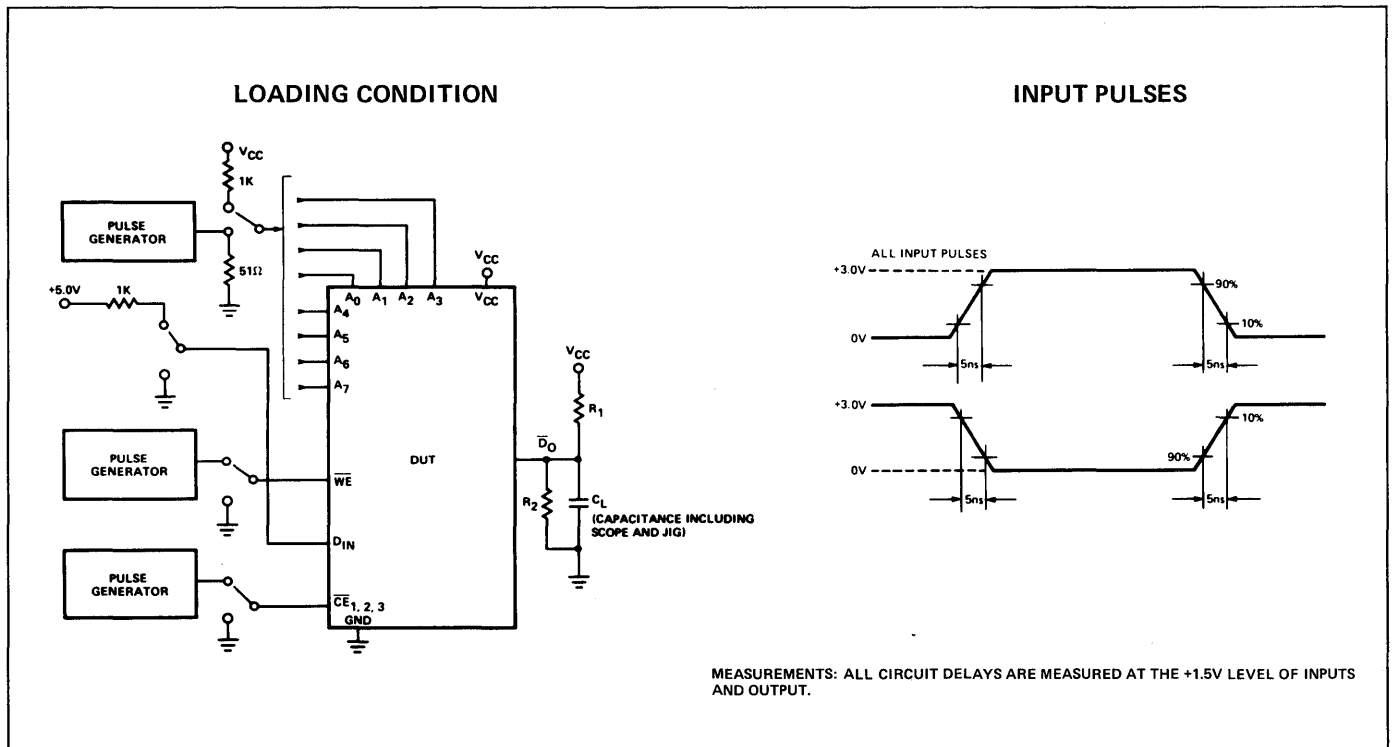
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to CE₁, CE₂ and CE₃.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS

S82S16/17 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 N82S16/17 $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS	S82S16/17			N82S16/17			UNIT
		MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	
Propagation Delay								
T _{AA}	Address Access Time		40	70		40	50	ns
T _{CE}	Chip Enable Access Time	R ₁ = 270Ω R ₂ = 600Ω C _L = 30pF	30	40		30	40	ns
T _{CD}	Chip Enable Output Disable Time		30	40		30	40	ns
T _{WD}	Write Enable to Output Valid Time		30	55		30	40	ns
Write Set-up Times								
T _{WSA}	Address to Write Enable	R ₁ = 270Ω R ₂ = 600Ω C _L = 30pF	20	5		20	5	ns
T _{WSD}	Data In to Write Enable		50	40		40	30	ns
T _{WSC}	$\overline{\text{CE}}$ to Write Enable		10	0		10	0	ns
Write Hold Times								
T _{WHA}	Address to Write Enable	R ₁ = 270Ω R ₂ = 600Ω C _L = 30pF	10	0		5	0	ns
T _{WHD}	Data In to Write Enable		10	0		5	0	ns
T _{WHC}	$\overline{\text{CE}}$ to Write Enable		10	0		5	0	ns
T _{WP}	Write Enable Pulse Width	Note 2	40	20		30	15	ns

AC TEST LOAD

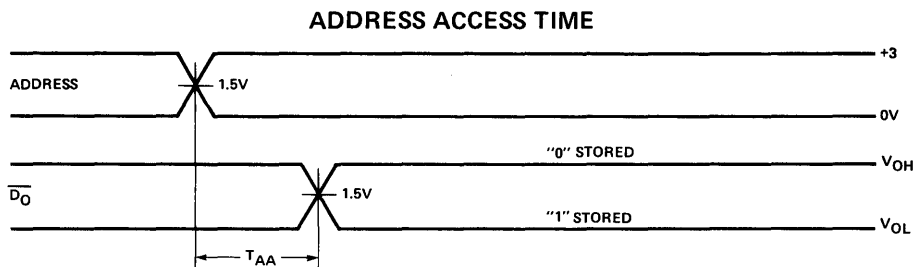


NOTES:

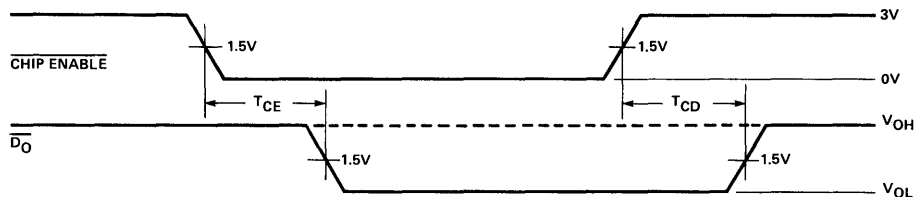
1. Typical values are at $V_{CC} = +5.0\text{V}$, and $T_A = +25^{\circ}\text{C}$.
2. Minimum required to guarantee a WRITE into the slowest bit.

SWITCHING PARAMETERS MEASUREMENT INFORMATION

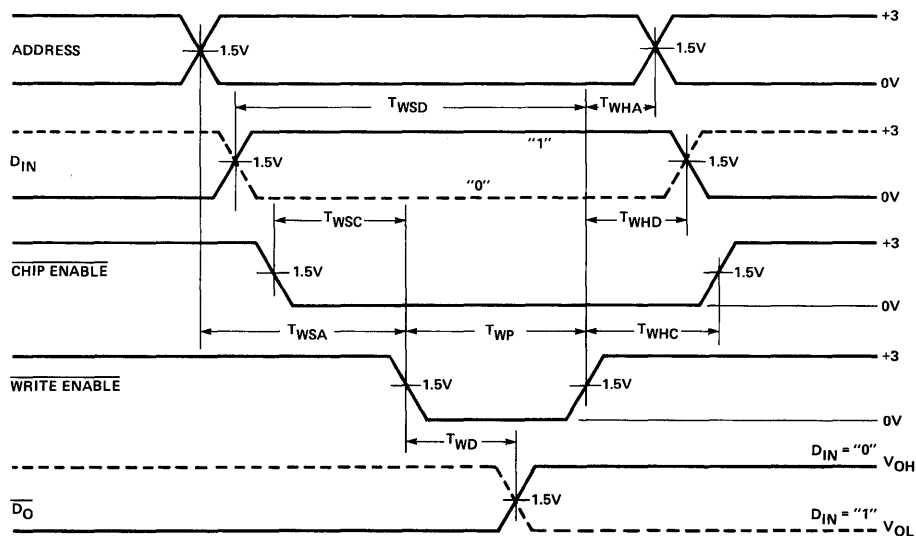
READ CYCLE



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T _{CE}	Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.	T _{WP}	Width of WRITE ENABLE pulse.
T _{CD}	Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.	T _{WSA}	Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
T _{AA}	Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.	T _{WSD}	Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
T _{WSC}	Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.	T _{WD}	Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.
T _{WHD}	Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.	T _{WHC}	Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
		T _{WHA}	Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.