DESCRIPTION

The 82S214 and 82S215 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers.

The 82S214 and 82S215 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizat ons. A D-type latch is used to enable the Tri-State output d ivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or high Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S214 and 82S215 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S214/215 I. For the military temperature range (−55°C to +125°C) specify S82S214/215 I.

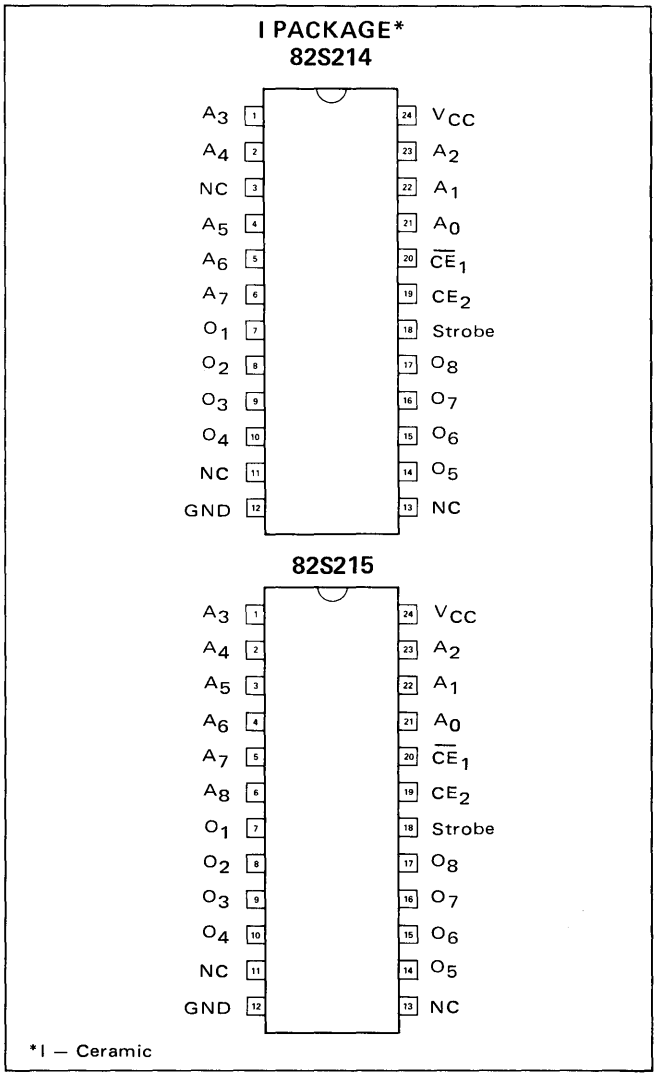
FEATURES

- ORGANIZATION:
  - 82S214 – 256 X 8
  - 82S215 – 512 X 8
- ADDRESS ACCESS TIME:
  - S82S214/215 – 90ns, MAXIMUM
  - N82S214/215 – 60ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING:
  - S82S214/215 – (−150μA) MAXIMUM
  - N82S214/215 – (−100μA) MAXIMUM
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- FULLY COMPATIBLE WITH 82S114 AND 82S115 SIGNETICS PROMS

APPLICATIONS

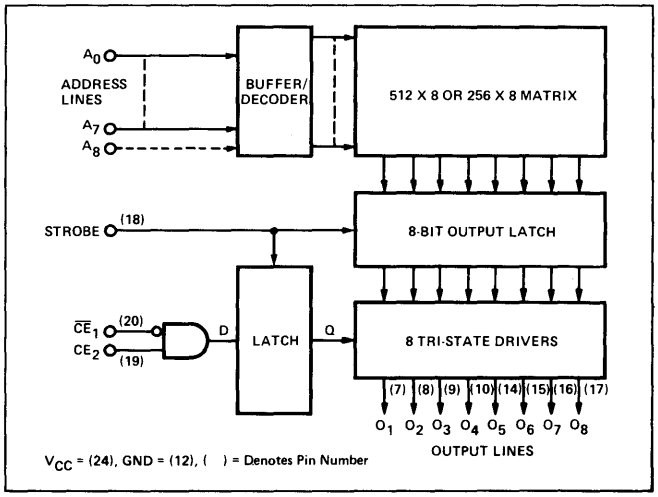
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S214/215)	0° to +75°	°C
	(S82S214/215)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS

N82S214/215 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
S82S214/215 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100			−150	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25			50	μA
V_{IL}	"0" Level Input Voltage				.85			.8	V
V_{IH}	"1" Level Input Voltage		2.0			2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6mA			0.5			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE}_1$ = "0", CE_2 = "1", I_{OUT} = −2mA, "1" STORED	2.7	3.3		2.4	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE}_1$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE}_1$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40			−100	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V $\overline{CE}_1$ = "1" or CE_2 = 0		8			8		pF
I_{CC}	V_{CC} Supply Current			130	175		130	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	−15		−85	mA

SWITCHING CHARACTERISTICS

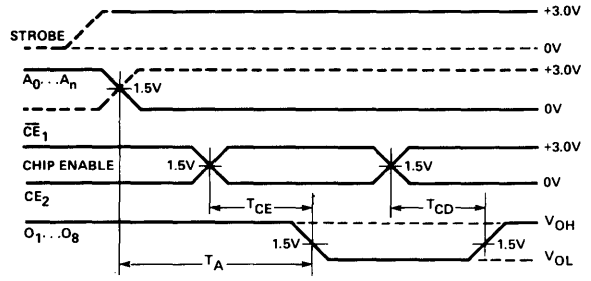
N82S214/215 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
S82S214/215 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60		35	90	ns
T_{CE}	Chip Enable Access Time	R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF (Note 4)		20	40		20	50	ns
T_{CD}	Chip Disable Time			20	40		20	50	ns
T_{ADH}	Address Hold Time		0	−10		5	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		10	0		ns
T_{SW}	Strobe Pulse Width	LATCHED READ ONLY	30	20		40	20		ns
T_{SL}	Strobe Latch Time	R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF (Note 5)	60	35		90	35		ns
T_{DL}	Strobe Delatch Time				30			35	ns
T_{CDS}	Chip Enable Set-up Time		40			50			ns

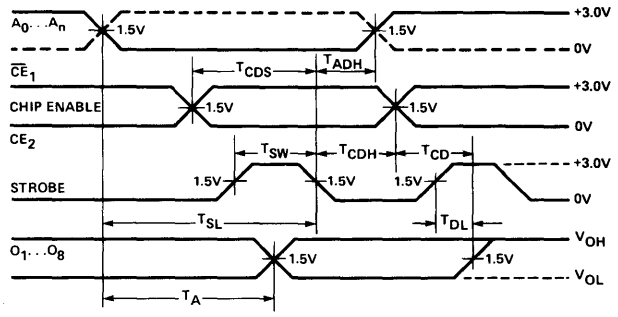
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner idential to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

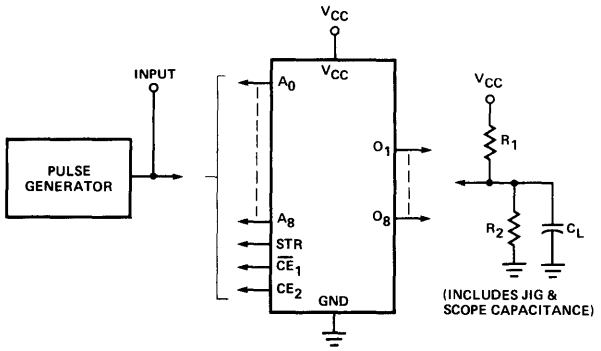
TRANSPARENT READ[5]
(Output Latches Not Used)



LATCHED READ[6]
(Output Latches Used)



AC TEST LOAD AND WAVEFORMS



INPUT PULSES