

DATA SHEET

80C562/83C562

Single-chip 8-bit microcontroller

Product specification

1992 Jan 08

IC20 Data Handbook

Single-chip 8-bit microcontroller

80C562/83C562

Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

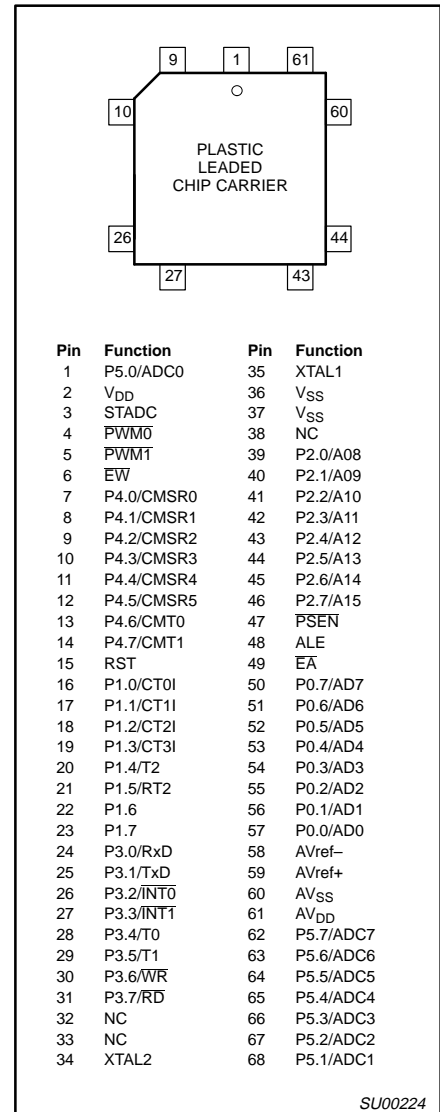
The 8XC562 contains a non-volatile 256×8 read-only program memory, a volatile 256×8 read/write data memory (83C562) (the 80C562 is ROMless), a volatile 256×8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in $1\mu\text{s}$ and 40% in $2\mu\text{s}$. Multiply and divide instructions require $4\mu\text{s}$.

FEATURES

- 80C51 instruction set
- $8\text{k} \times 8$ ROM expandable externally to 64k bytes
- 256×8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing eight synchronized, timed outputs
- An 8-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
 - 0 to $+70^\circ\text{C}$
 - -40 to $+85^\circ\text{C}$
 - -40 to $+125^\circ\text{C}$

PIN CONFIGURATION



Single-chip 8-bit microcontroller

80C562/83C562

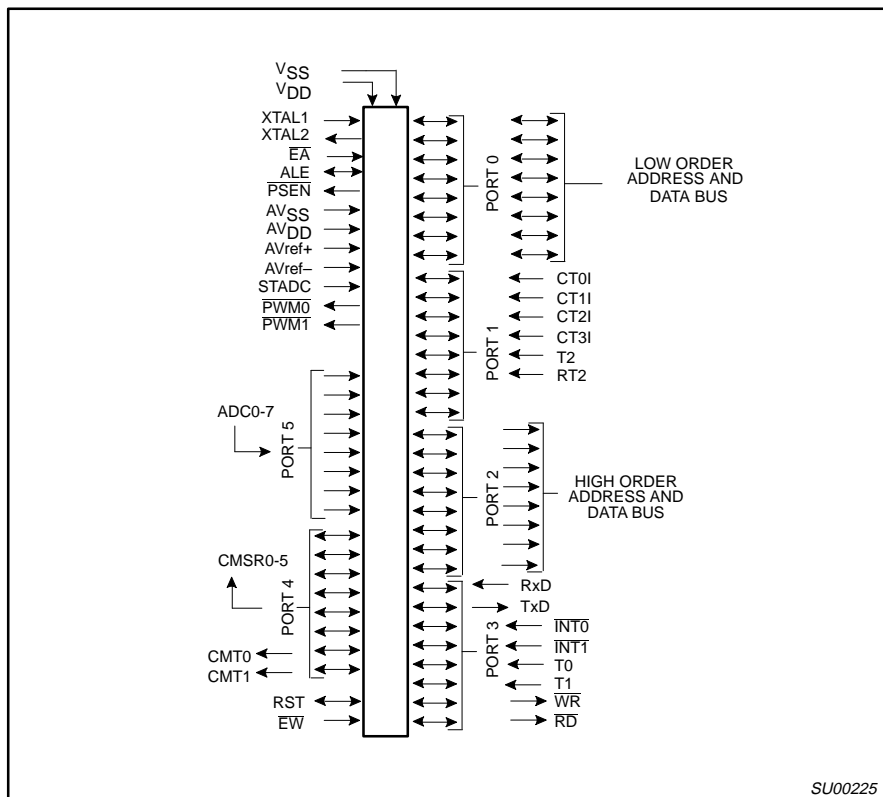
ORDERING INFORMATION

| PHILIPS PART ORDER NUMBER PART MARKING | | PHILIPS NORTH AMERICA PART ORDER NUMBER | | Drawing Number | EPROM | Drawing Number | TEMPERATURE RANGE °C AND PACKAGE | FREQ MHz |
|--|--------------------|---|--------------|----------------|---------------------------|----------------|--|----------|
| ROMless | ROM | ROMless | ROM | | | | | |
| PCB80C562-16WP | PCB83C562-16WP/xxx | S80C562-4A68 | S83C562-4A68 | SOT188 | S87C552-4A68 ² | SOT188-3 | 0 to +70, Plastic Leaded Chip Carrier | 16 |
| | | | | | S87C552-4K68 ² | 1473A | 0 to +70, Plastic Leaded Chip Carrier w/Window | 16 |
| PCF80C562-12WP | PCF83C562-12WP/xxx | S80C562-2A68 | S83C562-2A68 | SOT188 | S87C552-5A68 ² | SOT188-3 | -40 to +85, Plastic Leaded Chip Carrier | 12 |
| | | | | | S87C552-5K68 ² | 1473A | -40 to +85, Plastic Leaded Chip Carrier w/Window | 12 |
| PCA80C562-12WP | PCA83C562-12WP/xxx | S80C562-6A68 | S83C562-6A68 | SOT188 | | | -40 to +125, Plastic Leaded Chip Carrier | 12 |

NOTES:

- 80C562 and 83C562 frequency range is 1.2MHz–12MHz or 1.2MHz–16MHz.
- 87C552 frequency range is 3.5MHz–16MHz. For full specification, see the 87C552 data sheets.
- xxx denotes the ROM code number.

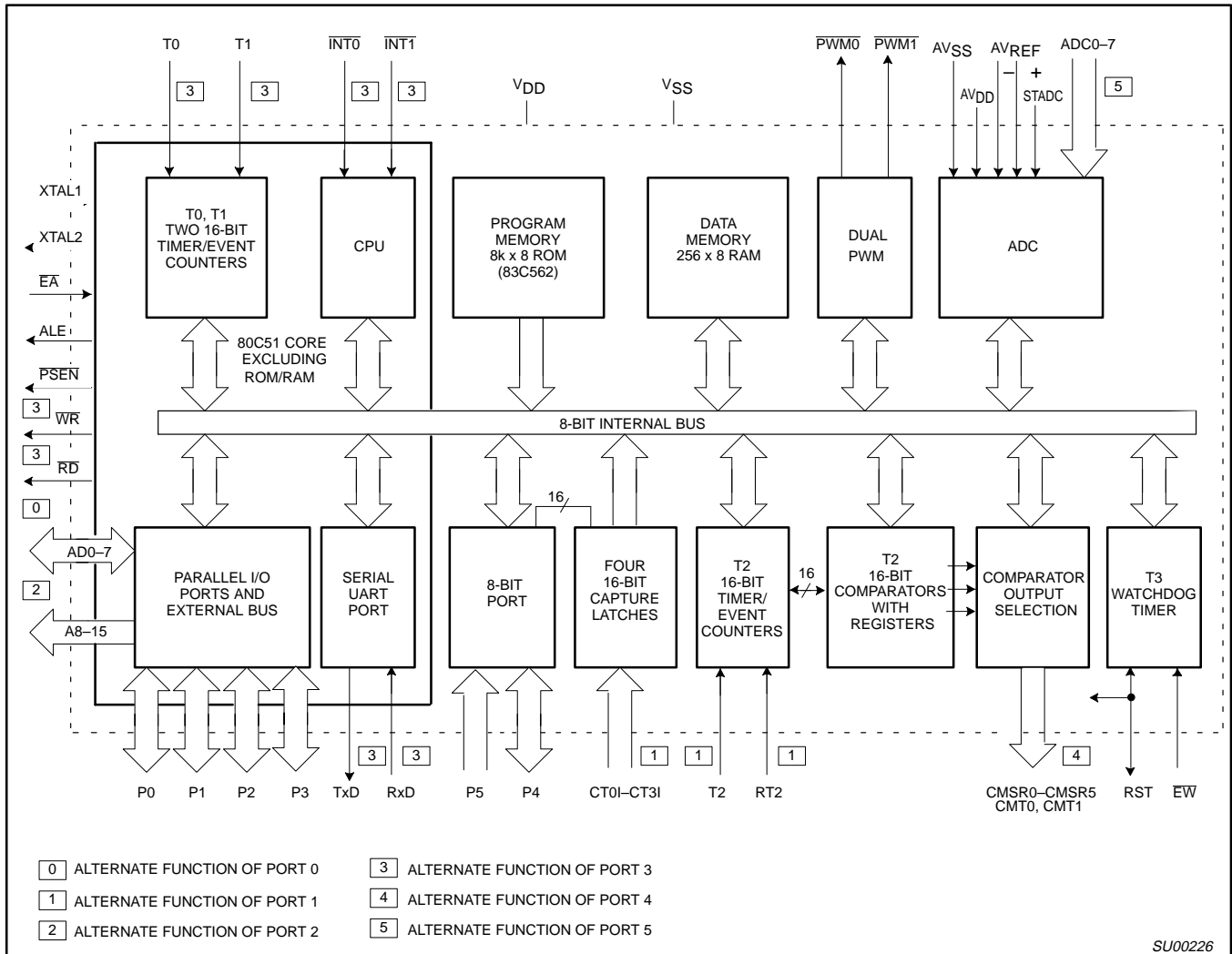
LOGIC SYMBOL



Single-chip 8-bit microcontroller

80C562/83C562

BLOCK DIAGRAM



SU00226

Single-chip 8-bit microcontroller

80C562/83C562

PIN DESCRIPTION

| MNEMONIC | PIN NO. | TYPE | NAME AND FUNCTION |
|--------------------|-------------|------|--|
| V _{DD} | 2 | I | Digital Power Supply: +5V power supply pin during normal operation, idle and power-down mode. |
| STADC | 3 | I | Start ADC Operation: Input starting analog to digital conversion (ADC operation can also be started by software). |
| PWM ₀ | 4 | O | Pulse Width Modulation: Output 0. |
| PWM ₁ | 5 | O | Pulse Width Modulation: Output 1. |
| EW | 6 | I | Enable Watchdog Timer: Enable for T3 watchdog timer and disable power-down mode. |
| P0.0–P0.7 | 57–50 | I/O | Port 0: Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. |
| P1.0–P1.7 | 16–23 | I/O | Port 1: 8-bit I/O port. Alternate functions include: (P1.0–P1.7): Quasi-bidirectional port pins. CT0I–CT3I (P1.0–P1.3): Capture timer input signals for timer T2. T2 (P1.4): T2 event input RT2 (P1.5): T2 timer reset signal. Rising edge triggered. |
| | 16–23 | I/O | |
| | 16–19 | I/O | |
| | 20 | I | |
| | 21 | I | |
| P2.0–P2.7 | 39–46 | I/O | Port 2: 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08–A15). |
| P3.0–P3.7 | 24–31 | I/O | Port 3: 8-bit quasi-bidirectional I/O port. Alternate functions include: RxD(P3.0): Serial input port. TxD (P3.1): Serial output port. INT0 (P3.2): External interrupt. INT1 (P3.3): External interrupt. T0 (P3.4): Timer 0 external input. T1 (P3.5): Timer 1 external input. WR (P3.6): External data memory write strobe. RD (P3.7): External data memory read strobe. |
| | 24 | | |
| | 25 | | |
| | 26 | | |
| | 27 | | |
| | 28 | | |
| | 29 | | |
| | 30 | | |
| | 31 | | |
| P4.0–P4.7 | 7–14 | I/O | Port 4: 8-bit quasi-bidirectional I/O port. Alternate functions include: CMSR0–CMSR5 (P4.0–P4.5): Timer T2 compare and set/reset outputs on a match with timer T2. CMT0, CMT1 (P4.6, P4.7): Timer T2 compare and toggle outputs on a match with timer T2. |
| | 7–12 | O | |
| | 13, 14 | O | |
| P5.0–P5.7 | 68–62, 1 | I | Port 5: 8-bit input port. ADC0–ADC7 (P5.0–P5.7): Alternate function: Eight input channels to ADC. |
| RST | 15 | I/O | Reset: Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows. |
| XTAL1 | 35 | I | Crystal Input 1: Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used. |
| XTAL2 | 34 | O | Crystal Input 2: Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used. |
| V _{SS} | 36, 37 | I | Digital ground. |
| PSEN | 47 | O | Program Store Enable: Active-low read strobe to external program memory. |
| ALE | 48 | O | Address Latch Enable: Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. |
| EA | 49 | I | External Access: When EA is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When EA is held at TTL low level, the CPU executes out of external program memory. EA is not allowed to float. |
| AV _{REF-} | 58 | I | Analog to Digital Conversion Reference Resistor: Low-end. |
| AV _{REF+} | 59 | I | Analog to Digital Conversion Reference Resistor: High-end. |
| AV _{SS} | 60 | I | Analog Ground |
| AV _{DD} | 61 | I | Analog Power Supply |

NOTE:

- To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} +0.5V or V_{SS} – 0.5V, respectively.

Single-chip 8-bit microcontroller

80C562/83C562

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To ensure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers

remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

| MODE | PROGRAM MEMORY | ALE | PSEN | PORT 0 | PORT 1 | PORT 2 | PORT 3 | PORT 4 | PWM0/PWM1 |
|------------|----------------|-----|------|--------|--------|---------|--------|--------|-----------|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data | Data | High |
| Idle | External | 1 | 1 | Float | Data | Address | Data | Data | High |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data | Data | High |
| Power-down | External | 0 | 0 | Float | Data | Data | Data | Data | High |

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

| PARAMETER | RATING | UNIT |
|--|--------------|------|
| Voltage on any other pin to V _{SS} | -0.5 to +6.5 | V |
| Input, output DC current on any single I/O pin | 5.0 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.0 | W |
| Storage temperature range | -65 to +150 | °C |

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Single-chip 8-bit microcontroller

80C562/83C562

DC ELECTRICAL CHARACTERISTICS $V_{SS}, AV_{SS} = 0V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|----------------|---|---|-----------------|-----------------|------------|
| | | | MIN | MAX | |
| V_{DD} | Supply voltage PCB8XC562 PCF8XC562 PCA8XC562 | | 4.0 | 6.0 | V |
| | | | 4.0 | 6.0 | V |
| | | | 4.5 | 5.5 | V |
| I_{DD} | Supply current operating: PCB8XC562 PCF8XC562 PCA8XC562 | See notes 1 and 2 $f_{OSC} = 16MHz$ $f_{OSC} = 12MHz$ $f_{OSC} = 12MHz$ | | 45 | mA |
| | | | | 34 | mA |
| | | | | 30 | mA |
| I_{ID} | Idle mode: PCB8XC562 PCF8XC562 PCA8XC562 | See notes 1 and 3 $f_{OSC} = 16MHz$ $f_{OSC} = 12MHz$ $f_{OSC} = 12MHz$ | | 10 | mA |
| | | | | 8 | mA |
| | | | | 7 | mA |
| I_{PD} | Power-down current: PCB8XC562 PCF8XC562 PCA8XC562 | See notes 1 and 4; $2V < V_{PD} < V_{DD} \text{ max}$ | | 50 | μA |
| | | | | 50 | μA |
| | | | | 100 | μA |
| Inputs | | | | | |
| V_{IL} | Input low voltage, except \overline{EA} | | -0.5 | $0.2V_{DD}-0.1$ | V |
| V_{IL1} | Input low voltage to \overline{EA} | | -0.5 | $0.2V_{DD}-0.3$ | V |
| V_{IH} | Input high voltage, except XTAL1, RST | | $0.2V_{DD}+0.9$ | $V_{DD}+0.5$ | V |
| V_{IH1} | Input high voltage, XTAL1, RST | | $0.7V_{DD}$ | $V_{DD}+0.5$ | V |
| I_{IL} | Logical 0 input current, ports 1, 2, 3, 4 | $V_{IN} = 0.45V$ | | -50 | μA |
| I_{TL} | Logical 1-to-0 transition current, ports 1, 2, 3, 4 | See note 5 | | -650 | μA |
| $\pm I_{IL1}$ | Input leakage current, port 0, \overline{EA} , STADC, EW | $0.45V < V_I < V_{DD}$ | | 10 | μA |
| Outputs | | | | | |
| V_{OL} | Output low voltage, ports 1, 2, 3, 4 | $I_{OL} = 1.6mA^6$ | | 0.45 | V |
| V_{OL1} | Output low voltage, port 0, ALE, \overline{PSEN} , $\overline{PWM0}$, $\overline{PWM1}$ | $I_{OL} = 3.2mA^6$ | | 0.45 | V |
| V_{OH} | Output high voltage, ports 1, 2, 3, 4 | $V_{DD} + 5V \pm 10\%$ $-I_{OH} = 60\mu A$ $-I_{OH} = 25\mu A$ $-I_{OH} = 10\mu A$ | 2.4 | | V |
| | | | $0.75V_{DD}$ | | V |
| | | | $0.9V_{DD}$ | | V |
| V_{OH1} | Output high voltage (port 0 in external bus mode, ALE, \overline{PSEN} , $\overline{PWM0}$, $\overline{PWM1}$) ⁷ | $V_{DD} + 5V \pm 10\%$ $-I_{OH} = 400\mu A$ $-I_{OH} = 150\mu A$ $-I_{OH} = 40\mu A$ | 2.4 | | V |
| | | | $0.75V_{DD}$ | | V |
| | | | $0.9V_{DD}$ | | V |
| V_{OH2} | Output high voltage (RST) | $-I_{OH} = 400\mu A$ $-I_{OH} = 120\mu A$ | 2.4 | | V |
| | | | $0.8V_{DD}$ | | V |
| R_{RST} | Internal reset pull-down resistor | | 50 | 150 | k Ω |
| C_{IO} | Pin capacitance | Test freq = 1MHz, $T_{amb} = 25^\circ C$ | | 10 | pF |

Single-chip 8-bit microcontroller

80C562/83C562

DC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|----------------------|--|--|-----------------------|-----------------------|----------------|
| | | | MIN | MAX | |
| Analog Inputs | | | | | |
| AV _{DD} | Analog supply voltage: PCB8XC562 PCF8XC562 PCA8XC562 | AV _{DD} = V _{DD} ±0.2V AV _{DD} = V _{DD} ±0.2V AV _{DD} = V _{DD} ±0.2V | 4.0 4.0 4.5 | 6.0 6.0 5.5 | V V V |
| AI _{DD} | Analog supply current: operating: | Port 5 = 0 to AV _{DD} | | 1.2 | mA |
| AI _{ID} | Idle mode: PCB8XC562 PCF8XC562 PCA8XC562 | | | 50 50 100 | μA μA μA |
| AI _{PD} | Power-down mode: PCB8XC562 PCF8XC562 PCA8XC562 | 2V < AV _{PD} < AV _{DD} max | | 50 50 100 | μA μA μA |
| AV _{IN} | Analog input voltage | | AV _{SS} -0.2 | AV _{DD} +0.2 | V |
| AV _{REF} | Reference voltage: AV _{REF-} AV _{REF+} | | AV _{SS} -0.2 | AV _{DD} +0.2 | V V |
| R _{REF} | Resistance between AV _{REF+} and AV _{REF-} | | 5 | 25 | kΩ |
| C _{IA} | Analog input capacitance | | | 15 | pF |
| t _{ADS} | Sampling time | | | 6t _{CY} | μs |
| t _{ADC} | Conversion time (including sampling time) | | | 24t _{CY} | μs |
| DL _e | Differential non-linearity ^{8, 9, 10} | | | ±1 | LSB |
| IL _e | Integral non-linearity ^{8, 11} | | | ±1 | LSB |
| OS _e | Offset error ^{8, 12} | | | ±1 | LSB |
| G _e | Gain error ^{8, 13} | | | 0.4 | % |
| M _{CTC} | Channel to channel matching | | | ±1 | LSB |
| C _t | Crosstalk between inputs of port 5 ¹⁴ | 0–100kHz | | -60 | dB |

NOTES:

- See Figures 8 through 12 for I_{DD} test conditions.
- The operating supply current is measured with all output pins disconnected; XTAL1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS} + 0.5V; V_{IH} = V_{DD} - 0.5V; XTAL2 not connected; EA = RST = Port 0 = EW = V_{DD}; STADC = V_{SS}.
- The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS} + 0.5V; V_{IH} = V_{DD} - 0.5V; XTAL2 not connected; Port 0 = EW = V_{DD}; EA = RST = STADC = V_{SS}.
- The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = EW = V_{DD}; EA = RST = STADC = XTAL1 = V_{SS}.
- Pins of ports 1, 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9V_{DD} specification when the address bits are stabilizing.
- Conditions: AV_{REF-} = 0V; AV_{DD} = 5.0V, AV_{REF+} = 5.12V. ADC is monotonic with no missing codes.
- The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. (See Figure 1.)
- The ADC is monotonic; there are no missing codes.
- The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
- The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
- The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
- This should be considered when both analog and digital signals are simultaneously input to port 5.

Single-chip 8-bit microcontroller

80C562/83C562

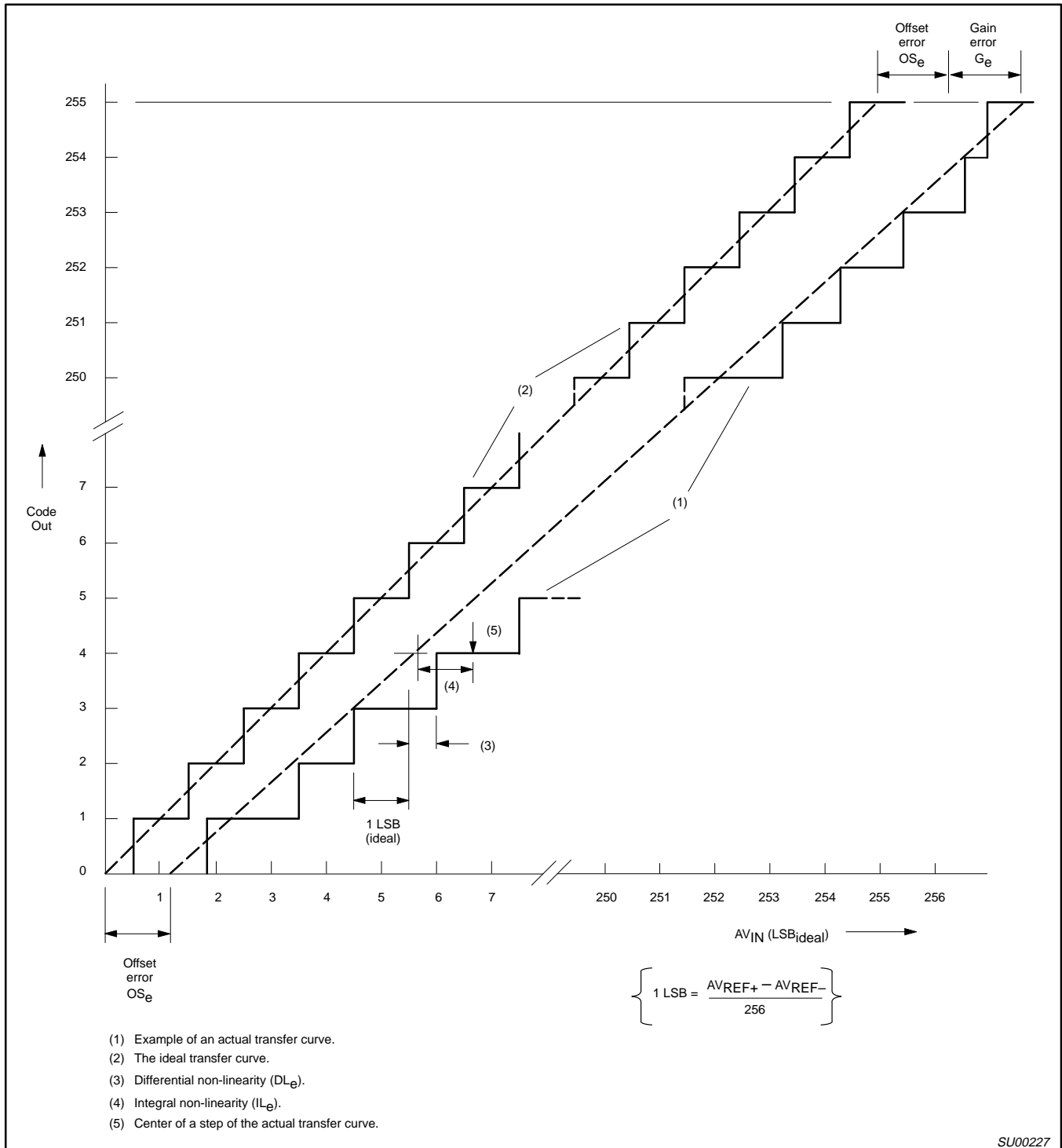


Figure 1. ADC Conversion Characteristic

Single-chip 8-bit microcontroller

80C562/83C562

AC ELECTRICAL CHARACTERISTICS^{1, 2}

| SYMBOL | FIGURE | PARAMETER | 12MHz CLOCK | | VARIABLE CLOCK | | UNIT |
|-----------------------|--------|---|-------------|-----|-----------------|-----------------|------|
| | | | MIN | MAX | MIN | MAX | |
| $1/t_{CLCL}$ | 2 | Oscillator frequency | | | 1.2 | 16 | MHz |
| t_{LHLL} | 2 | ALE pulse width | 127 | | $2t_{CLCL}-40$ | | ns |
| t_{AVLL} | 2 | Address valid to ALE low | 28 | | $t_{CLCL}-55$ | | ns |
| t_{LLAX} | 2 | Address hold after ALE low | 48 | | $t_{CLCL}-35$ | | ns |
| t_{LLIV} | 2 | ALE low to valid instruction in | | 234 | | $4t_{CLCL}-100$ | ns |
| t_{LLPL} | 2 | ALE low to \overline{PSEN} low | 43 | | $t_{CLCL}-40$ | | ns |
| t_{PLPH} | 2 | \overline{PSEN} pulse width | 205 | | $3t_{CLCL}-45$ | | ns |
| t_{PLIV} | 2 | \overline{PSEN} low to valid instruction in | | 145 | | $3t_{CLCL}-105$ | ns |
| t_{PXIX} | 2 | Input instruction hold after \overline{PSEN} | 0 | | 0 | | ns |
| t_{PXIZ} | 2 | Input instruction float after \overline{PSEN} | | 59 | | $t_{CLCL}-25$ | ns |
| t_{AVIV} | 2 | Address to valid instruction in | | 312 | | $5t_{CLCL}-105$ | ns |
| t_{PLAZ} | 2 | \overline{PSEN} low to address float | | 10 | | 10 | ns |
| Data Memory | | | | | | | |
| t_{AVLL} | 3, 4 | Address valid to ALE low | 43 | | $t_{CLCL}-35$ | | ns |
| t_{RLRH} | 3 | \overline{RD} pulse width | 400 | | $6t_{CLCL}-100$ | | ns |
| t_{WLWH} | 4 | \overline{WR} pulse width | 400 | | $6t_{CLCL}-100$ | | ns |
| t_{RLDV} | 3 | \overline{RD} low to valid data in | | 252 | | $5t_{CLCL}-165$ | ns |
| t_{RHDX} | 3 | Data hold after \overline{RD} | 0 | | 0 | | ns |
| t_{RHDZ} | 3 | Data float after \overline{RD} | | 97 | | $2t_{CLCL}-70$ | ns |
| t_{LLDV} | 3 | ALE low to valid data in | | 517 | | $8t_{CLCL}-150$ | ns |
| t_{AVDV} | 3 | Address to valid data in | | 585 | | $9t_{CLCL}-165$ | ns |
| t_{LLWL} | 3, 4 | ALE low to \overline{RD} or \overline{WR} low | 200 | 300 | $3t_{CLCL}-50$ | $3t_{CLCL}+50$ | ns |
| t_{AVWL} | 3, 4 | Address valid to \overline{WR} low or \overline{RD} low | 203 | | $4t_{CLCL}-130$ | | ns |
| t_{QVWX} | 4 | Data valid to \overline{WR} transition | 23 | | $t_{CLCL}-60$ | | ns |
| t_{DW} | 4 | Data before \overline{WR} | 433 | | $7t_{CLCL}-150$ | | ns |
| t_{WHQX} | 4 | Data hold after \overline{WR} | 33 | | $t_{CLCL}-50$ | | ns |
| t_{RLAZ} | 3 | \overline{RD} low to address float | | 0 | | 0 | ns |
| t_{WHLH} | 3, 4 | \overline{RD} or \overline{WR} high to ALE high | 43 | 123 | $t_{CLCL}-40$ | $t_{CLCL}+40$ | ns |
| External Clock | | | | | | | |
| t_{CHCX} | 5 | High time ³ | 20 | | 20 | | ns |
| t_{CLCX} | 5 | Low time ³ | 20 | | 20 | | ns |
| t_{CLCH} | 5 | Rise time ³ | | 20 | | 20 | ns |
| t_{CHCL} | 5 | Fall time ³ | | 20 | | 20 | ns |

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and \overline{PSEN} = 100pF, load capacitance for all other outputs = 80pF.
- These values are characterized but not 100% production tested.

Single-chip 8-bit microcontroller

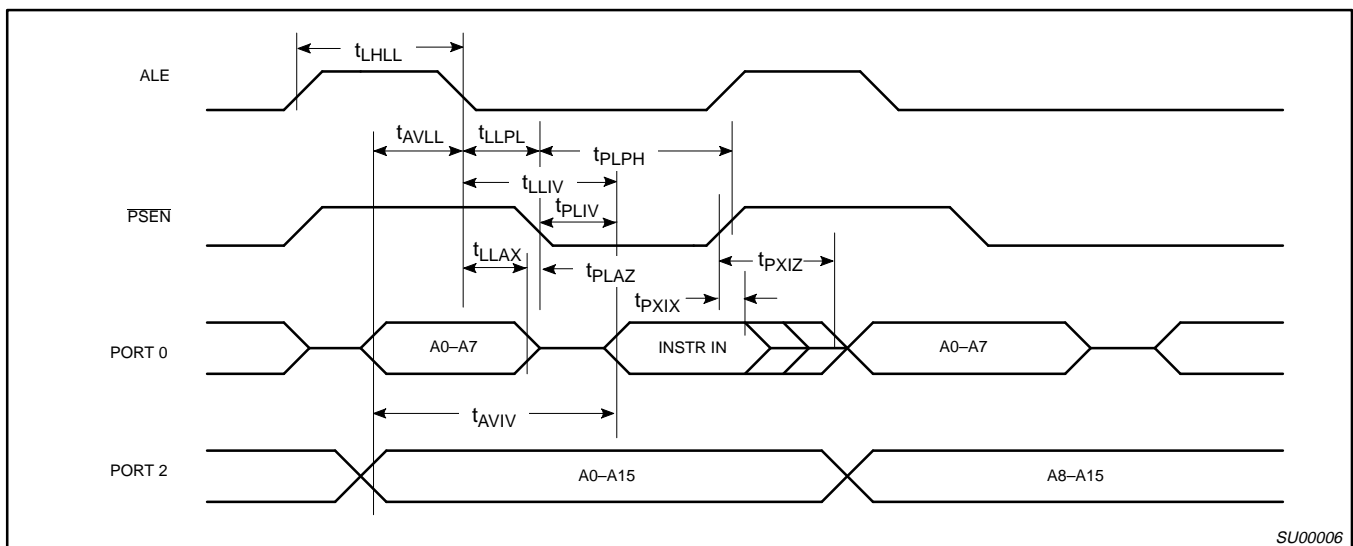
80C562/83C562

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:
 A – Address
 C – Clock
 D – Input data
 H – Logic level high
 I – Instruction (program memory contents)
 L – Logic level low, or ALE
 P – $\overline{\text{PSEN}}$

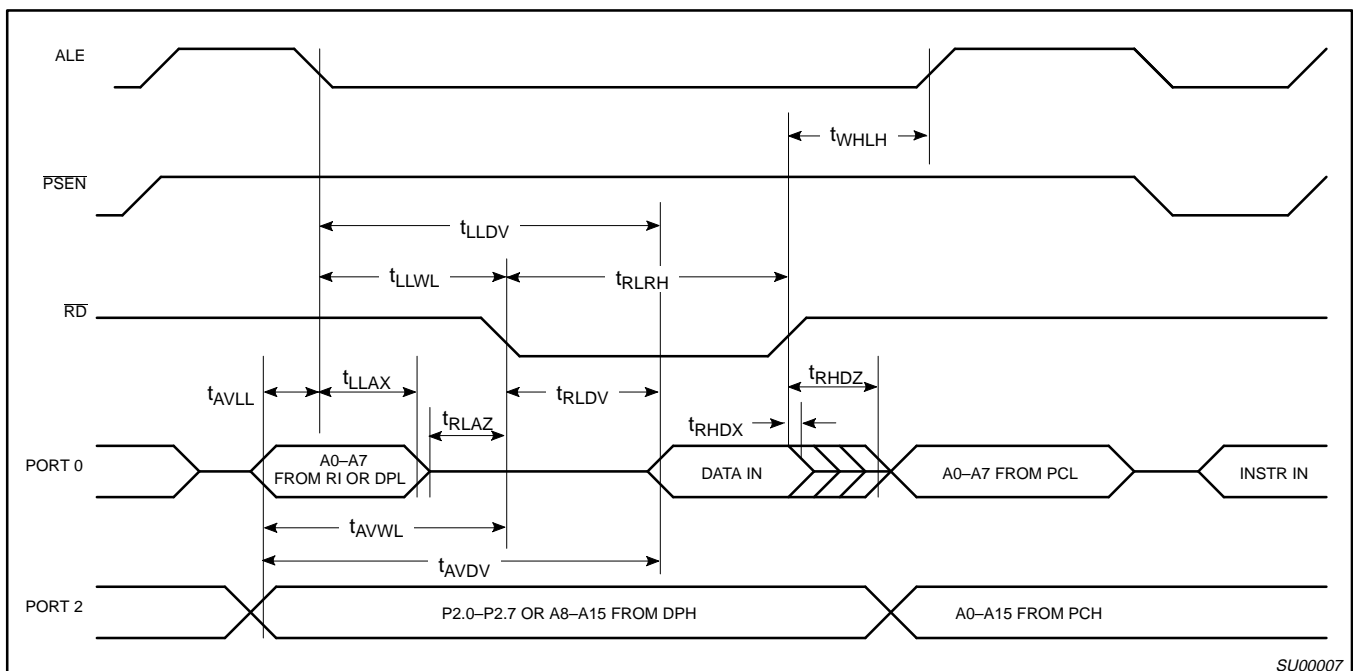
Q – Output data
 R – $\overline{\text{RD}}$ signal
 t – Time
 V – Valid
 W – $\overline{\text{WR}}$ signal
 X – No longer a valid logic level
 Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.



SU00006

Figure 2. External Program Memory Read Cycle



SU00007

Figure 3. External Data Memory Read Cycle

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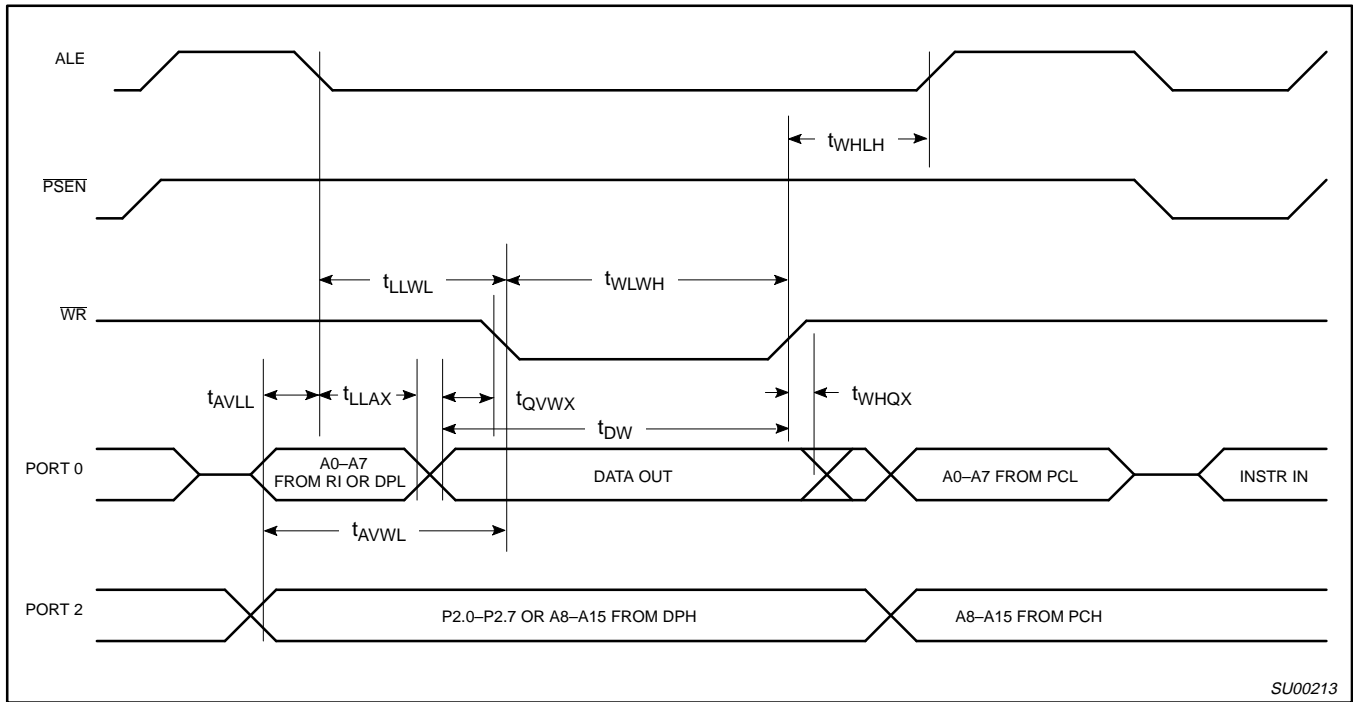


Figure 4. External Data Memory Write Cycle

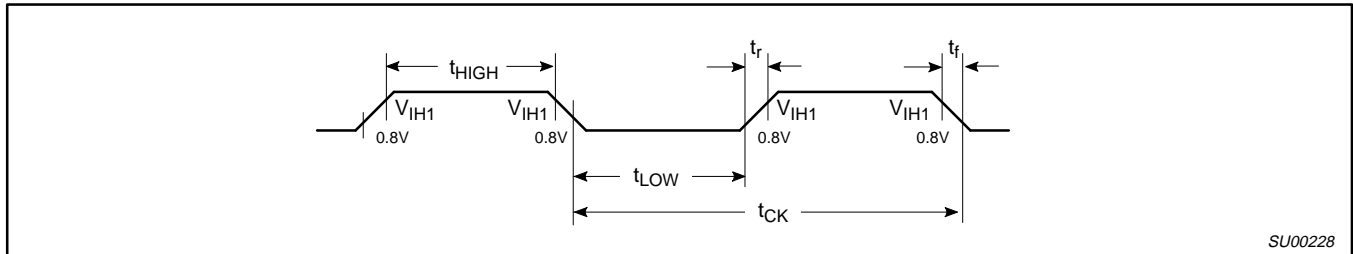


Figure 5. External Clock Drive XTAL1

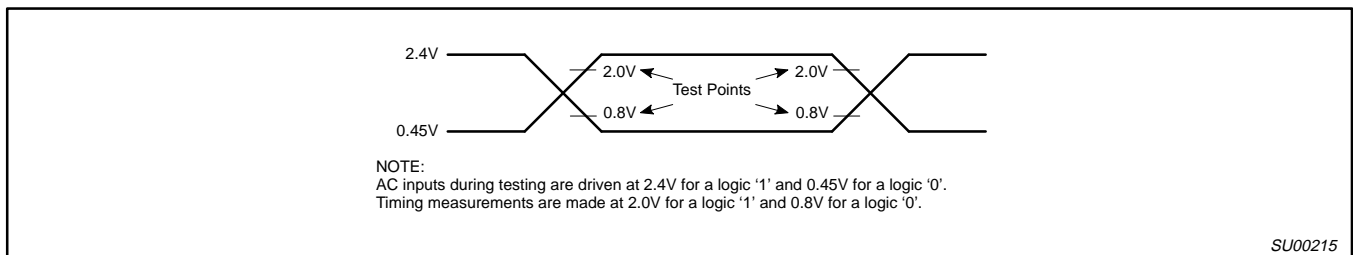


Figure 6. AC Testing Input/Output

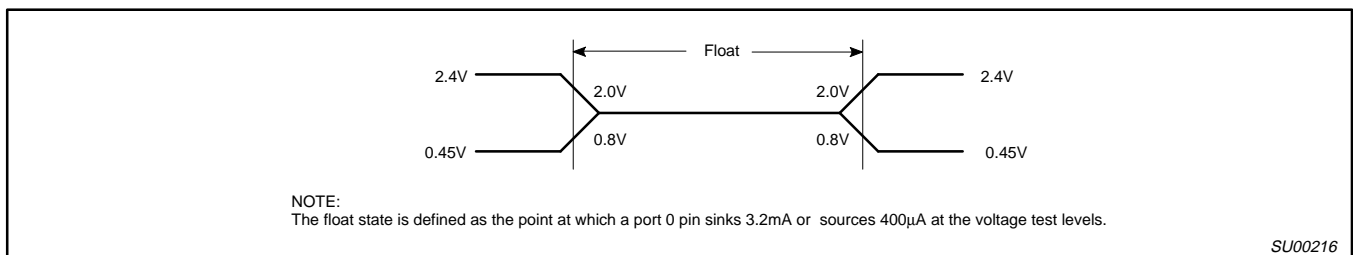


Figure 7. AC Testing Input, Float Waveform

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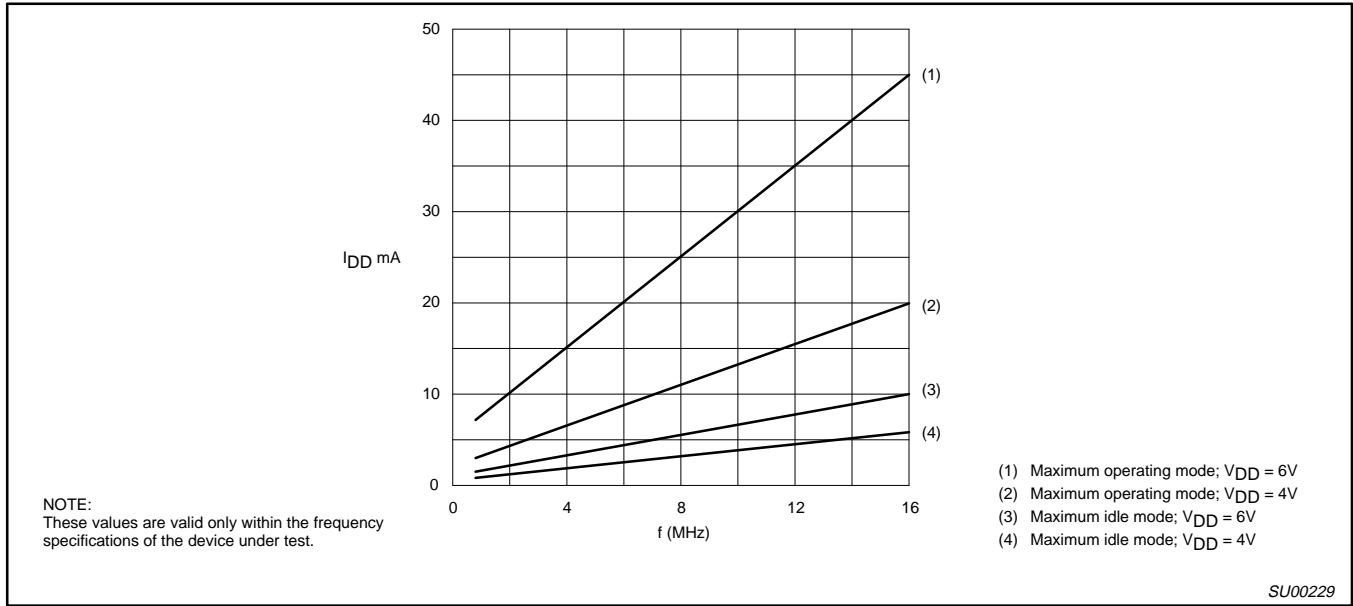


Figure 8. Supply Current (I_{DD}) as a Function of Frequency at XTAL1 (f_{osc})

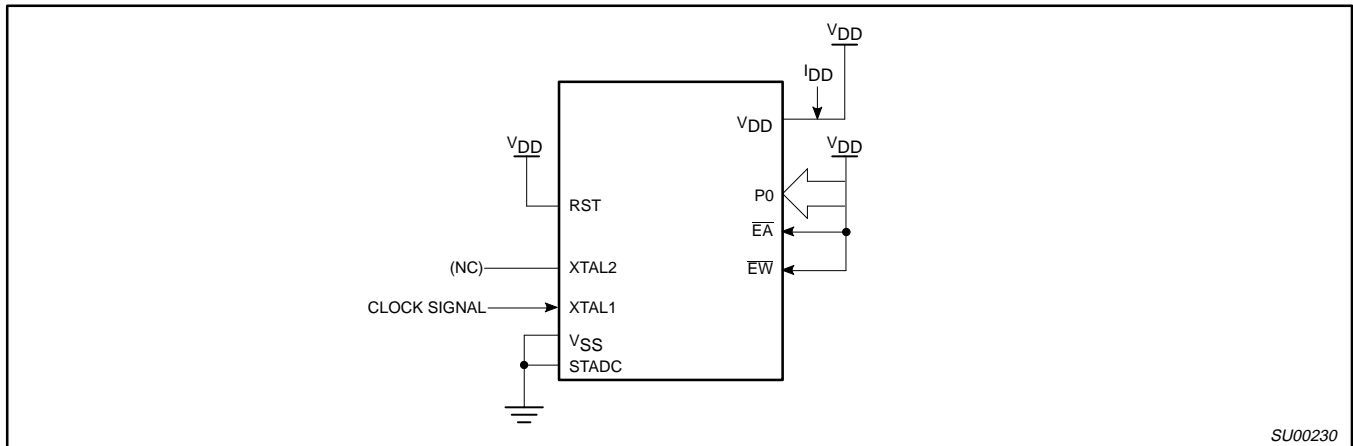


Figure 9. I_{DD} Test Condition, Active Mode
All other pins are disconnected

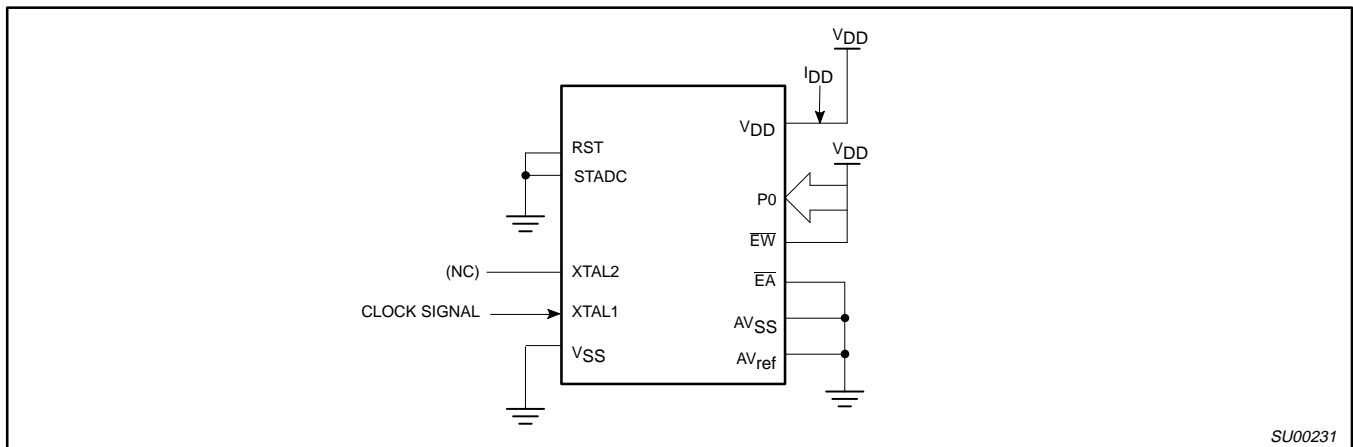
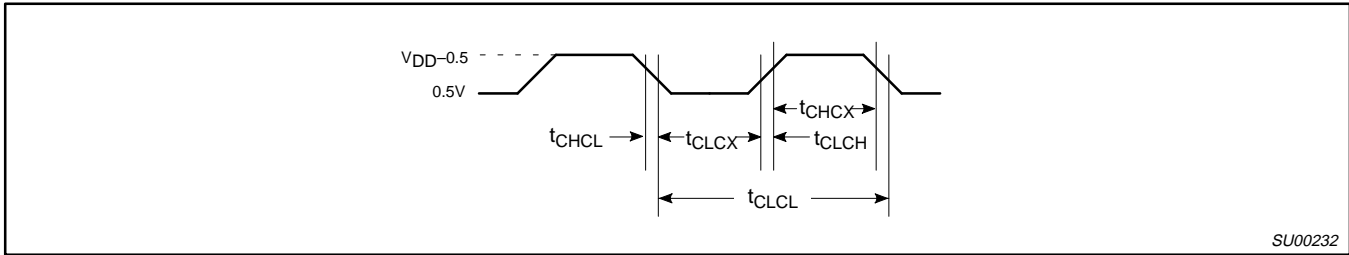


Figure 10. I_{DD} Test Condition, Idle Mode
All other pins are disconnected

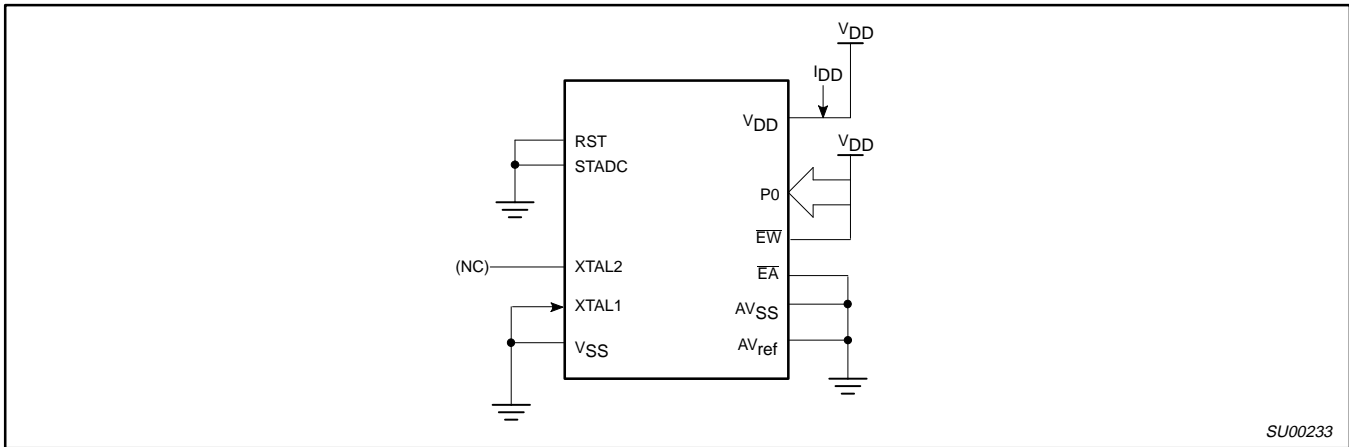
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SU00232

Figure 11. Clock Signal Waveform for I_{DD} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 10\text{ns}$



SU00233

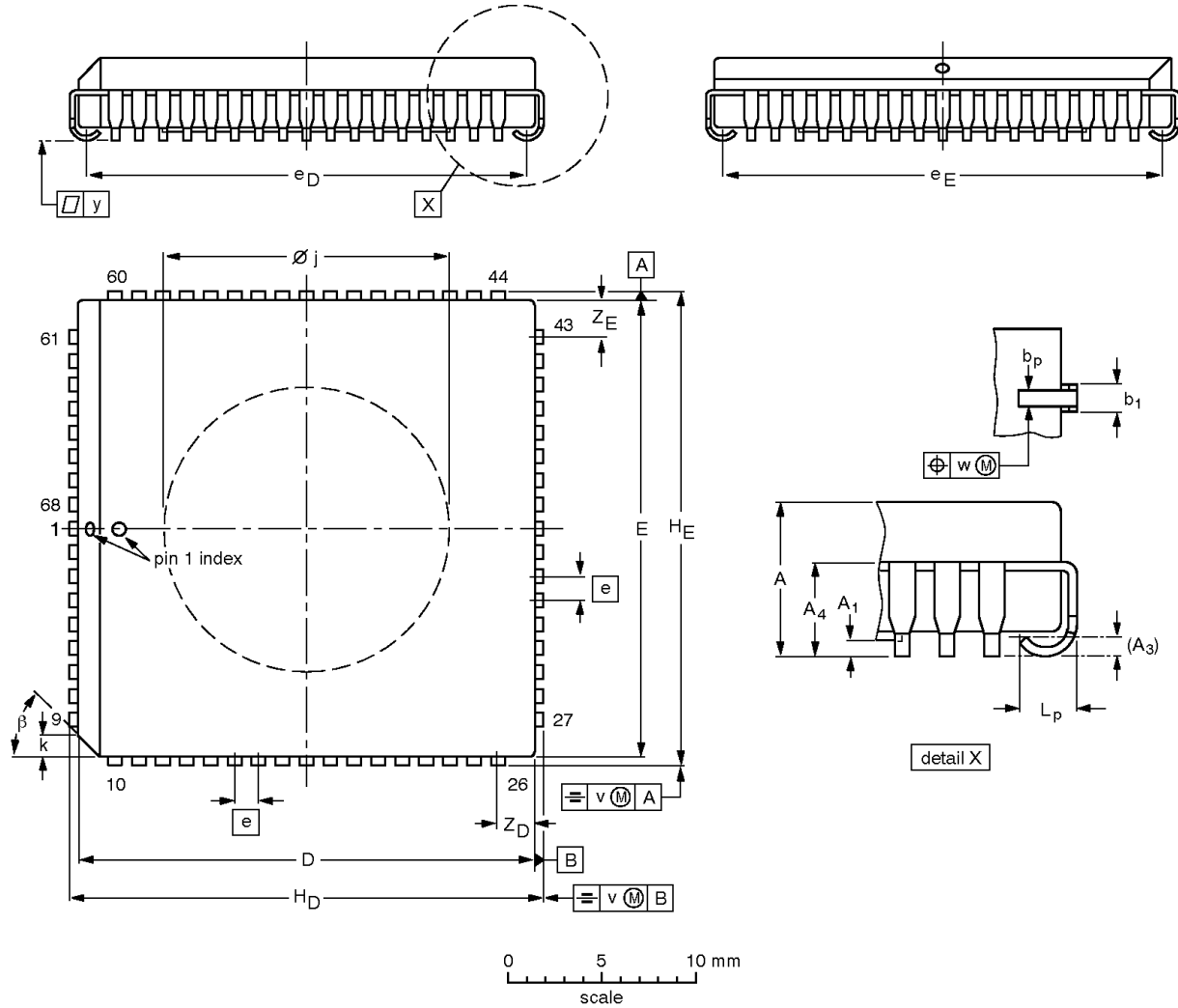
Figure 12. I_{DD} Test Condition, Power Down Mode
 All other pins are disconnected. $V_{DD} = 2\text{V to } 5.5\text{V}$

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PLCC68: plastic leaded chip carrier; 68 leads; pedestal

SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A | A ₁ min. | A ₃ | A ₄ max. | b _p | b ₁ | D ⁽¹⁾ | E ⁽¹⁾ | e | e _D | e _E | H _D | H _E | k | \varnothing_j | L _p | v | w | y | Z _D ⁽¹⁾ max. | Z _E ⁽¹⁾ max. | β |
|--------|----------------|------------------------|----------------|------------------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|----------------|-----------------|----------------|-------|-------|-------|---------------------------------------|---------------------------------------|---------|
| mm | 4.57 4.19 | 0.13 | 0.25 | 3.05 | 0.53 0.33 | 0.81 0.66 | 24.33 24.13 | 24.33 24.13 | 1.27 | 23.62 22.61 | 23.62 22.61 | 25.27 25.02 | 25.27 25.02 | 1.22 1.07 | 15.34 15.19 | 1.44 1.02 | 0.18 | 0.18 | 0.10 | 2.06 | 2.06 | 45° |
| inches | 0.180 0.165 | 0.005 | 0.01 | 0.12 | 0.021 0.013 | 0.032 0.026 | 0.958 0.950 | 0.958 0.950 | 0.05 | 0.930 0.890 | 0.930 0.890 | 0.995 0.985 | 0.995 0.985 | 0.048 0.042 | 0.604 0.598 | 0.057 0.040 | 0.007 | 0.007 | 0.004 | 0.081 | 0.081 | |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT188-3 | 112E10 | MO-047AE | | | | 92-11-17 95-02-25 |

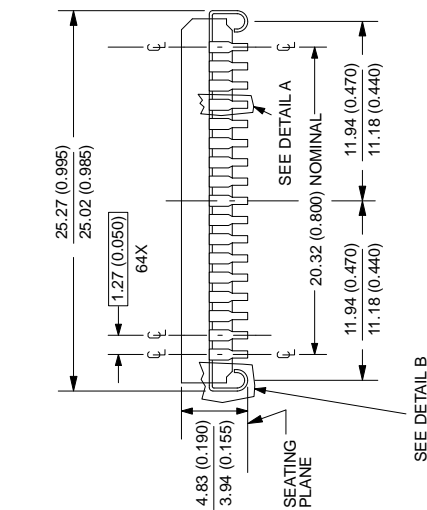
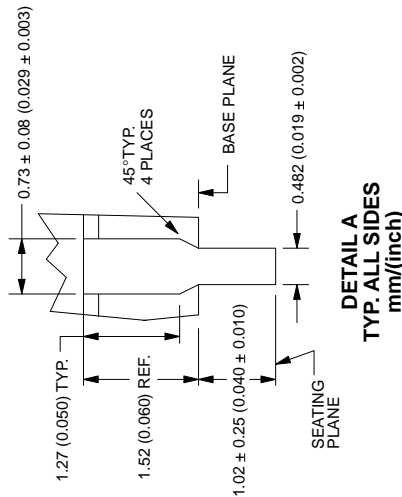
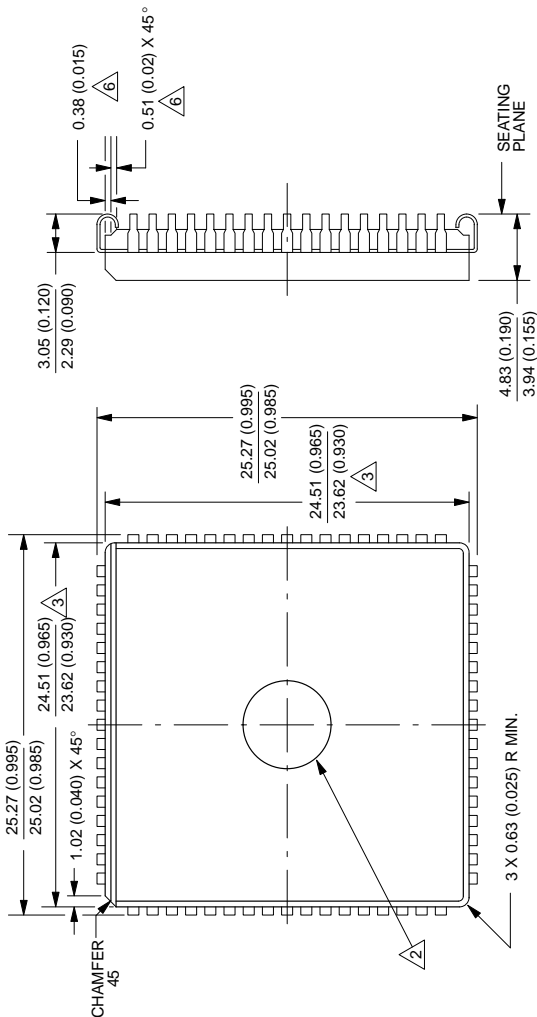
Single-chip 8-bit microcontroller

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1473A 68-PIN CERQUAD J-BEND (K) PACKAGE

NOTES:

1. All dimensions and tolerances to conform to ANSI Y14.5-1982.
2. UV window is optional.
3. Dimensions do not include glass protrusion. Glass protrusion to be 0.005 inches maximum on each side.
4. Controlling dimension millimeters.
5. All dimensions and tolerances include lead trim offset and lead plating finish.
6. Backside solder relief is optional and dimensions are for reference only.



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80C562/83C562

NOTES

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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