SMC

# Twisted-Pair Interface and Manchester Encoder/Decoder

- *83C694D*

Data sheet

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# 1.0 INTRODUCTION

## 1.1 DOCUMENT SCOPE

This document describes the function and operation of the 83C694D Twisted-Pair Interface and Manchester Encoder/Decoder. It includes a description of external logic necessary for the efficient use of this device and its proper role in the chip set which includes the 83C690 and 83B692 as shown in Figure 1-1. Figure 1-2 provides a functional block diagram of the 83C694D chip itself.

## 1.2 FEATURES

Features of the 83C694D include:

- Twisted-Pair interface solution for IEEE 802.3 10BaseT Standard
- Compatible with Ethernet II (10BASE5) and Cheapernet (10BASE2) IEEE 802.3 Standards
- Smart Squelch© digital noise filter at receive and collision inputs to reject noise and digital noise on twisted-pair receive inputs.
- Direct connection to the transceiver (AUI) cable
- 16V fault protection at the AUI transmitter interface
- 10 Mbps Manchester encoding/ decoding with receive clock recovery
- Low power, 1.25µ CMOS technology
- TTL/MOS-compatible controller interface
- Externally-selectable half- or full-step modes of operation at AUI TX± outputs
- Loopback capability for diagnostics
- Single station interface operation
- Link test generation and digital equalization for twisted-pair transmitter
- Automatic phase detection
- AUI/TP autoselect
- Built-in LED drivers for transmit, receive, link test and polarity status indicators

## 1.3 GENERAL DESCRIPTION

The 83C694D is used for applications where Twisted-Pair Interface (TPI) and/or Attachment Unit Interface (AUI) functions are required. Its two main functions are to:

1. Receive a digital data stream from a low-level input signal and
2. Convert a digital output data stream into an analog high-current signal for transmission across a network cable.

This means that the 83C694D serves as the logical link between a network cable on one end and a digital controller chip (such as the 83C690) on the other end.

To accomplish these two functions, the 83C694D consists of these components: Manchester encoder/decoder, balanced drivers and receivers, onboard crystal oscillator, signal translator, diagnostic circuit, and protocol timers and state machines.

The remainder of this data sheet contains the following information:

**Section 2** discusses the system architecture including an explanation of all chip circuits.

**Section 3** provides pin descriptions.

**Section 4** provides DC Operating Characteristics.

**Section 5** provides AC Operating Characteristics including Interface Timing diagrams.

**Section 6** provides the PLCC package diagram of this chip.

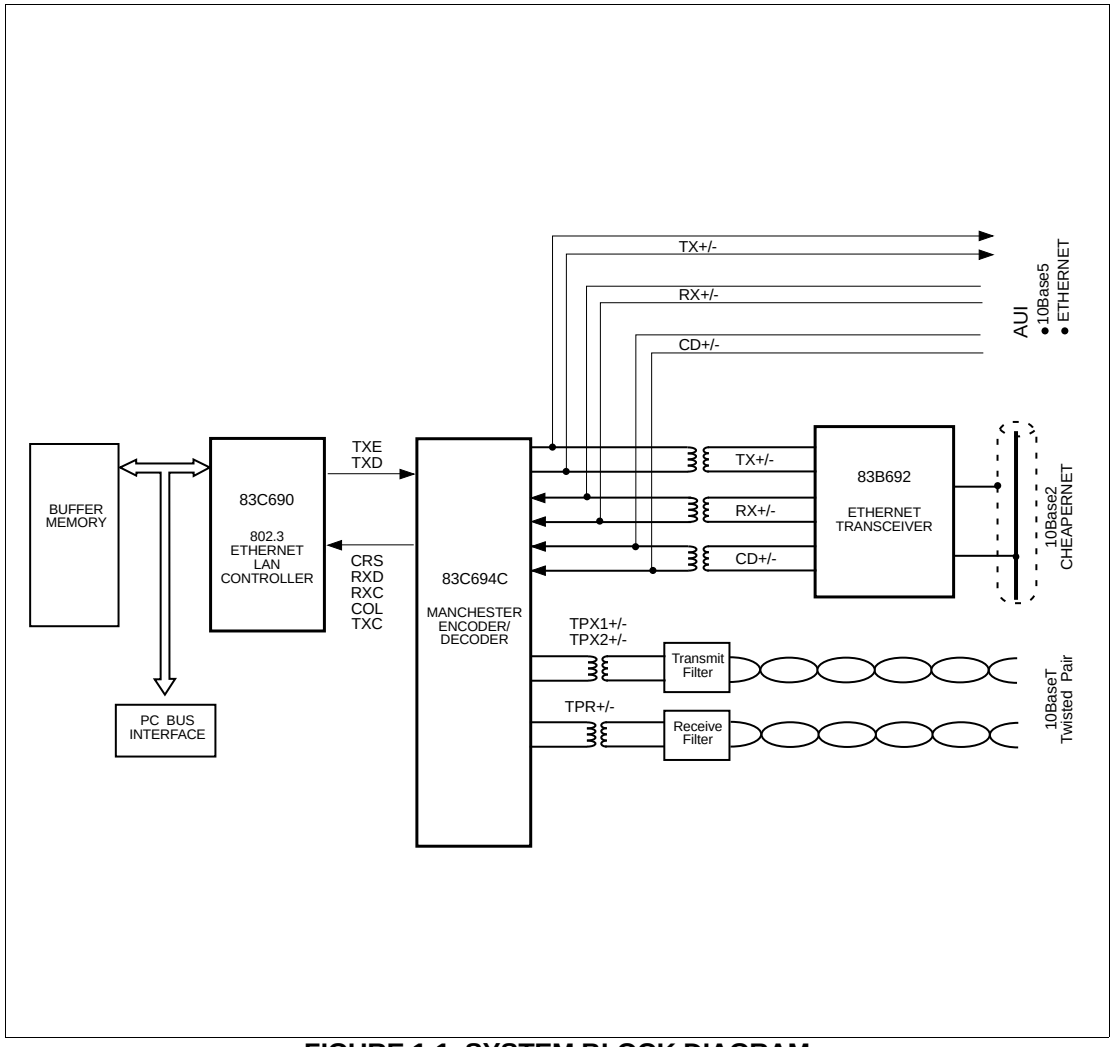



**FIGURE 1-1. SYSTEM BLOCK DIAGRAM**

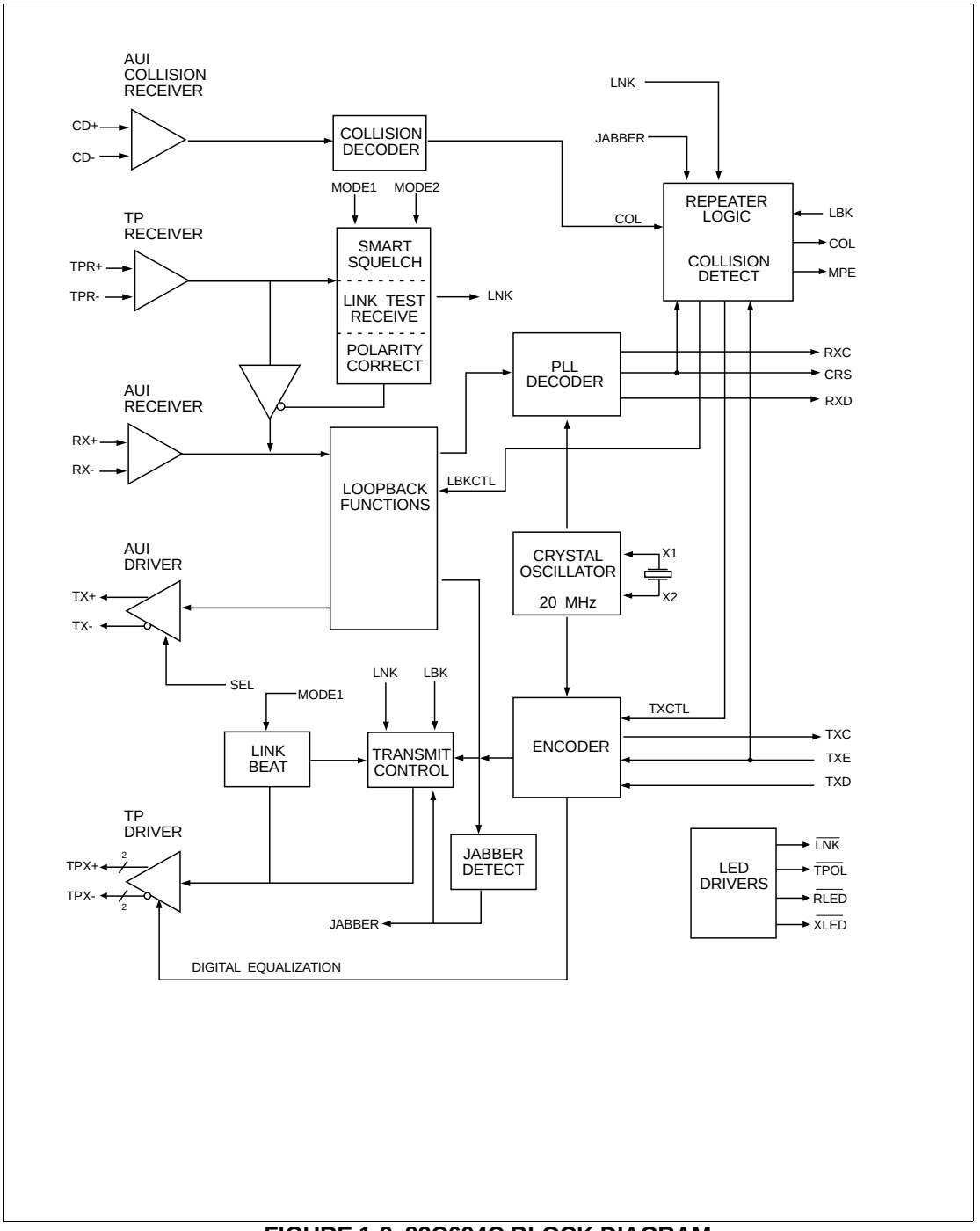



**FIGURE 1-2. 83C694C BLOCK DIAGRAM**

## 2.0 ARCHITECTURE

The 83C694D can be used as an AUI device or as a twisted-pair interface device.

When used in combination TPI/AUI applications, the 83C694D is part of a three-device set that implements the complete IEEE 802.3-compatible network node electronics (see Figure 1-1).

The 83C690 Ethernet LAN Controller (ELC) and the 83B692 Ethernet Transceiver (ET) comprise the other two devices in the set. The 83C690 provides media access protocol functions and performs buffer management tasks, while the 83B692 serves as a coaxial cable line driver/receiver and collision detector.

The 83C694D Twisted-Pair Interface provides the interface between the 83C690 ELC and the 83B692 ET. When transmitting, the device converts non-return-to-zero (NRZ) data from the controller into Manchester encoded data, then sends this data to the transceiver.

When receiving, the device reverses the process using an analog phase-locked loop that decodes 10 Mbit/sec signals with up to ±20 nsec of jitter.

When the 83C694D is used as a twisted-pair (TP) interface, its on-chip transmitter and receiver (separate from the AUI inputs and outputs) connect to the network through a transformer and filter. In this application, the 83C694D is used with the 83C690 providing controller and protocol functions, and the 83B692 is not used.

The 83C694D Twisted-Pair Interface is comprised of these functional blocks:

- Oscillator
- Manchester Encoder and Differential Driver
- Manchester Decoder
- Collision Translator
- Loopback Capabilities
- TP Differential Driver
- TP Differential Receiver
- Link Test Function
- AUI / TP Autoselect
- Jabber & SQE Test Functions
- Status Indications

The rest of this section describes each of these circuits in more detail, including suggestions, where appropriate, for designing external circuits consistent with the 802.3 standard.

### 2.1 OSCILLATOR

Control is provided either by a 20 MHz, parallel resonant crystal connected between X1 and X2, or by an external clock connected at X1. The oscillator's 20 MHz output is divided in half to generate the 10 MHz transmit clock for the Ethernet LAN controller and to provide the internal clock signals for the encoding and decoding circuits.

Figure 2-1 provides a diagram of this connection.

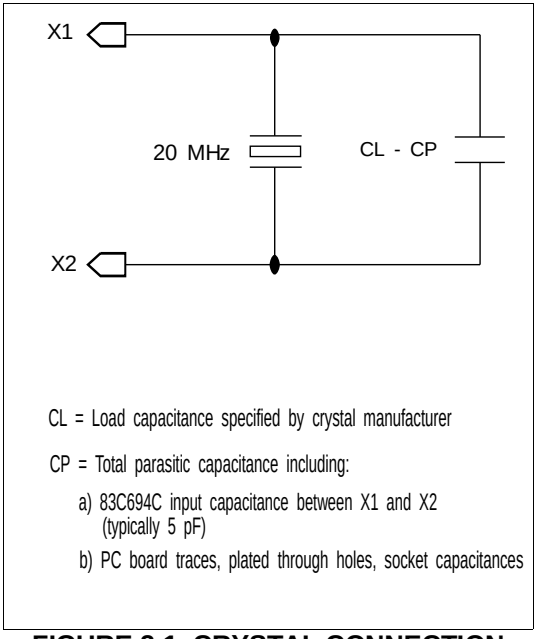



**FIGURE 2-1. CRYSTAL CONNECTION DIAGRAM**

## 2.2 MANCHESTER ENCODER/ DIFFERENTIAL DRIVER

Data encoding and transmission begins when the transmit enable input (TXE) goes high and continues as long as the TXE remains high. It is essential that the transmit enable and transmit data inputs meet the setup and hold time requirements for the rising edge of the transmit clock.

Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is one, or at the boundary of the bit cell if the last bit is zero.

The AUI differential line driver, which has the ability to drive up to 50 meters of twisted-pair AUI/Ethernet transceiver cable, provides the emitter-coupled logic (ECL) level signals.

With the SEL input, select one of two modes, full-step or half-step. When SEL is low, TX+ is positive in relation to TX- in the idle state. When SEL is high, TX+ and TX- are equal in the idle state. Figures 5-1 through 5-3 illustrate AUI transmit timing. An external interface circuit utilizing these signals might resemble Figure 2-2. In such a configuration, the transmit interface circuit could utilize an isolation transformer leading to the 83B692 which would then drive the coax signal to the network. Another option would use the AUI connector which would go to external equipment.

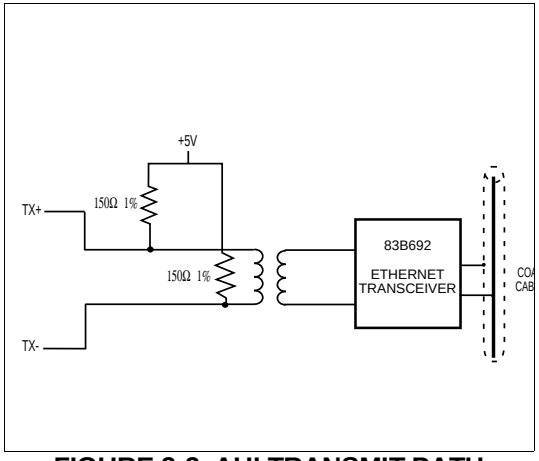



**FIGURE 2-2. AUI TRANSMIT PATH**

## 2.3 MANCHESTER DECODER

Decoding is accomplished by a differential input receiver circuit and an analog phase-locked loop that separates the Manchester-encoded data stream into clock signals and NRZ data.

To prevent noise at the AUI RX+ or RX- input from falsely triggering the decoder, a squelch circuit rejects signals with pulse widths less than 20 nsec (negative going), or with levels less than -175 mV. When the input exceeds the squelch limits, the analog phase-locked loop locks onto the incoming signal and the 83C694D decodes a data frame. The carrier sense (CRS) is activated, and the receive data (RXD) and receive clock (RXC) become available within five bit times. At the end of a frame, when the normal mid-bit transition on the differential input ceases, carrier sense is de-activated. The receive clock remains active for an additional five bit times. Figures 5-4 through 5-6 illustrate the receive timing. An external interface circuit for RX+ and RX- might be designed like Figure 2-3.

To avoid signal corruption caused by excessive voltage fluctuation on the power supply, it is desirable to externally implement a voltage regulation system consisting of a 5.1-volt zener diode. Typically, as shown in Figure 2-4, the diode's cathode is connected to pin 20, pin 23, the VCC side of the OSR resistor, the VCC side of the BSR resistor, and a 510Ω ¼-Watt resistor which goes from the zener's cathode to the 12-volt power supply.

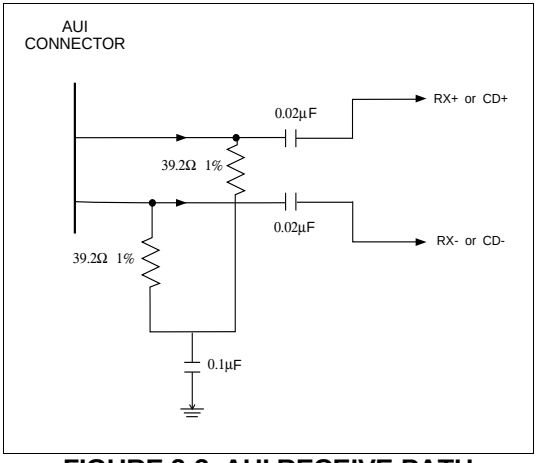



**FIGURE 2-3. AUI RECEIVE PATH**

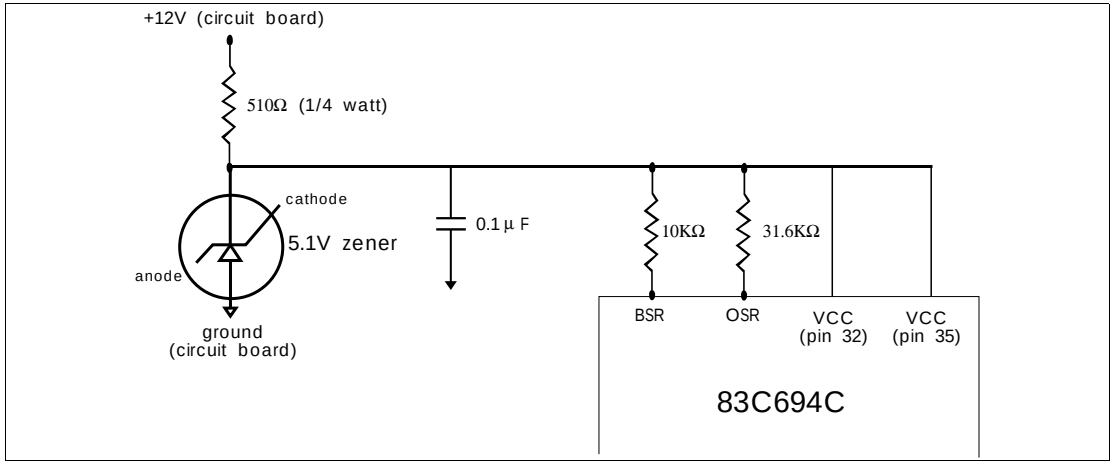



**FIGURE 2-4. ZENER DIODE VOLTAGE REGULATION FOR 12 VOLTS**

It is also helpful to place a decoupling capacitor between the diode's cathode and ground as shown in Figure 2-4.

## 2.4 COLLISION TRANSLATOR

When the 83C694D is used as an AUI device, a separate Ethernet transceiver detects collisions on the coaxial cable and generates a 10 MHz signal, which is monitored by the 83C694D through the collision detect pins. The presence of the signal activates the collision detect (CD) pin connected to the 83C690 causing the controller to stop transmitting. The collision detect output is deactivated within 160 nsec. after the absence of the 10 MHz signal. Figure 5-7 illustrates the collision timing. An external interface circuit for CD+ and CD- is designed exactly like an external interface for RX+ and RX-. See Figure 2-3.

## 2.5 TP DIFFERENTIAL DRIVER

The TP driver can transmit through up to 100m of unshielded twisted-pair (UTP) cable. The driver includes a circuit for transmit equalization, which attenuates low frequency components of the transmit waveform. This reduces the zero crossing jitter of the received signal and avoids the use of a receive equalizer.

There are two pulse widths transmitted: 50 nsec and 100 nsec. When a pulse width of 100 nsec is sent, both drivers (TPX1+ and TPX2+) turn on and drive a high level. This provides a greater amplitude at the start of the pulse; however, halfway through the pulse TPX2 turns off, thereby reducing the amplitude after 50 ns. A narrow pulse is transmitted at the same amplitude as the first half of the wide pulses. The resistor ratio is calculated to produce the best signal wave shape at the receiving end assuming a UTP cable length of 100 meters.

Figure 2-6 shows the basic twisted-pair transmit path along with its timing and one possible external transmit interface design. Typical values for resistance on TPX2 pins are 261Ω, while TPX1 pins use 65Ω. The 2.4KΩ parallel resistor is used to match the output resistance of the transmitter to the twisted-pair cable.

At the receive end of the cable, a 100Ω termination resistor is commonly used. To verify the operation of the circuit, measure the TPX signals differentially.

In designing the external circuits to connect the 83C694D transmit outputs to the cable, use a transmit filter followed by an isolation transformer and, in the most practical applications, a common mode choke for FCC compliance. The common mode choke may not always be needed in every application; however, the isolation transformer is always needed and the transmit filter is strongly recommended; without it, high frequency radiation may exceed FCC limits.

## 2.6 TP DIFFERENTIAL RECEIVER

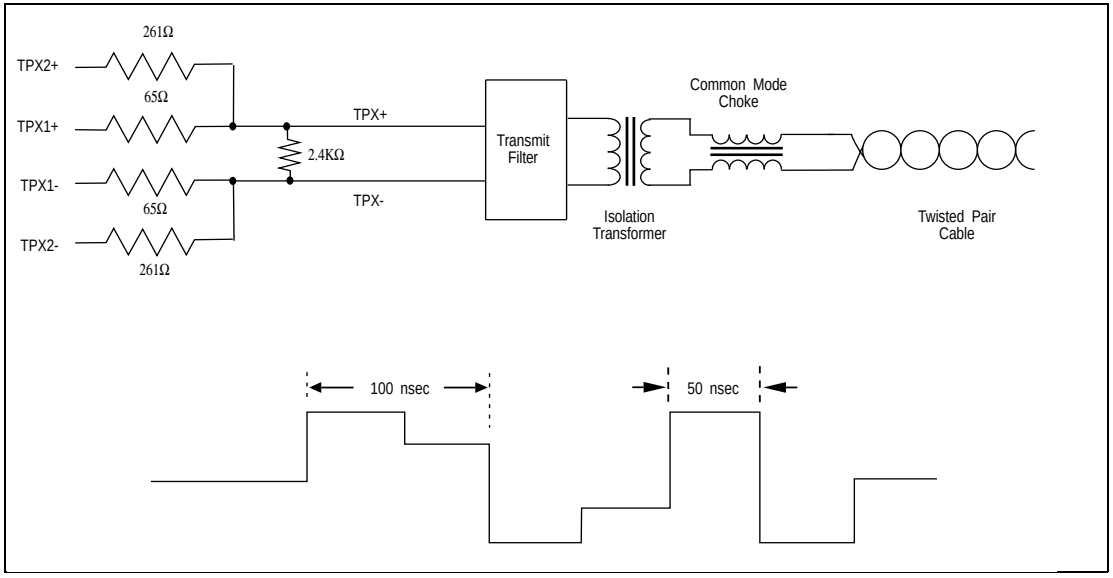



**FIGURE 2-6. TWISTED-PAIR TRANSMIT PATH AND TIMING**

The signal received from the unshielded cable can be noisy, so minimum voltage and timing limits must be met before the receiver logic is enabled. A "smart squelch"© digital noise filter is used in addition to the analog squelch circuit in the receiver. The smart squelch circuit provides extra protection against false collisions and false link connections.

If the input polarity is reversed, it will be automatically detected and corrected. When this happens, the $\overline{\text{TPOL}}$ output pin will go high to signal the controller or to turn off the polarity indicator LED.

The phase-locked loop and Manchester decoder are the same circuits used by the AUI receiver.

An external interface circuit for TPR+ and TPR- might be designed like Figure 2-5.

## 2.7 LOOPBACK FUNCTION

When the loopback input goes high it causes the 83C694D to send serial data from the transmit data input through the encoder, and back through the phase-locked loop and decoder to the receive data output. The transmit driver is in the idle state during loopback mode and the receiver circuitry and collision detection are disabled. Loopback can be enabled during either AUI or TP (10BaseT) operation. Transmit data is always looped back during TP operation, simulating the physical broadcast characteristic of 802.3 coaxial cable networks.

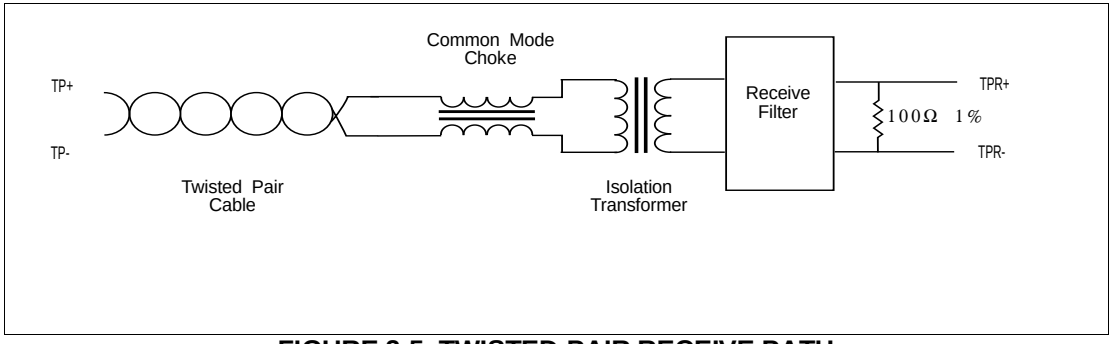



**FIGURE 2-5. TWISTED-PAIR RECEIVE PATH**

The 83C694D supports the IEEE 802.3 loopback design (section 14.2.1.3) which provides for continuous loopback from transmit to receive in normal operation. This means that transmitted data is always looped back during TP operation, simulating the physical broadcast characteristics of 802.3 coaxial cable networks.

### 2.8 LINK TEST FUNCTION

Each TP driver transmits a short positive pulse periodically when it is not sending data as shown in Figure 5-4. These pulses are received at the other end of the TP cable, signalling that the link is operating correctly. The time between link test pulses is compared to the expected range at the receiver, to avoid false detection of noise pulses as link test pulses.

If the link test fails (no pulses or data received in a fixed time period), then the LNK pin is set high and data transmit and receive on the TP interface is disabled.

### 2.9 AUI/TP AUTOSELECT

The 83C694D can automatically select which media to transmit and receive on, based on the link test state. If the link test fails, the AUI transmitter and receiver are enabled while the TP transmitter, receiver, and loopback are disabled. If link test passes, the AUI operation is disabled and TP operation is re-enabled. The only exception to this is when MODE1 is set low and TP operation is enabled continuously.

### 2.10 JABBER AND SQE TEST FUNCTIONS

If TXE is high for greater than 46 ms, the TP transmitter will be disabled and COL will go active high. If TXE then goes low for more than 368 ms, the TP transmitter will be re-enabled and COL will go low.

In TP operation, a short pulse will be output on COL after each packet is transmitted. This is required as a test of the TP transmit/receive path, and is called SQE Test or CD Heartbeat.

### 2.11 STATUS INDICATIONS

To assist in installation and management of the network, indicator LEDs can be driven by four outputs from the 83C694D. These show the result of Link Test, polarity check, and transmit or receive activity.

An LED test feature is built into the 83C694D. All LEDs turn on for 2/3 second after a reset to the device.

### 2.12 TEST MODE

Three test modes can be selected when the SEL pin is set to intermediate voltages. These modes and their corresponding voltages are:

- Internal counter speedup (1.75 V)
- RXC and RXD enable (2.5 V)
- Output tristate (3.5 V)

Internal counter speedup is used for fast board-level testing of timed functions such as LED power-up blink and link test pulse period.

RXC and RXD enable is used to test internal VCO functions without using a full data packet receive.

Output tristate is used during board-level testing to enable short/open testing. It is also used to test other devices resident on the board. This function does not tristate transmit (pins 22-27) or X2 outputs.

## 3.0 PIN DESCRIPTION

Figure 3-1 illustrates the signal names and pin locations on the 44-pin PLCC 83C694D package. Table 3-1 lists the signal names and descriptions for the 83C694D.

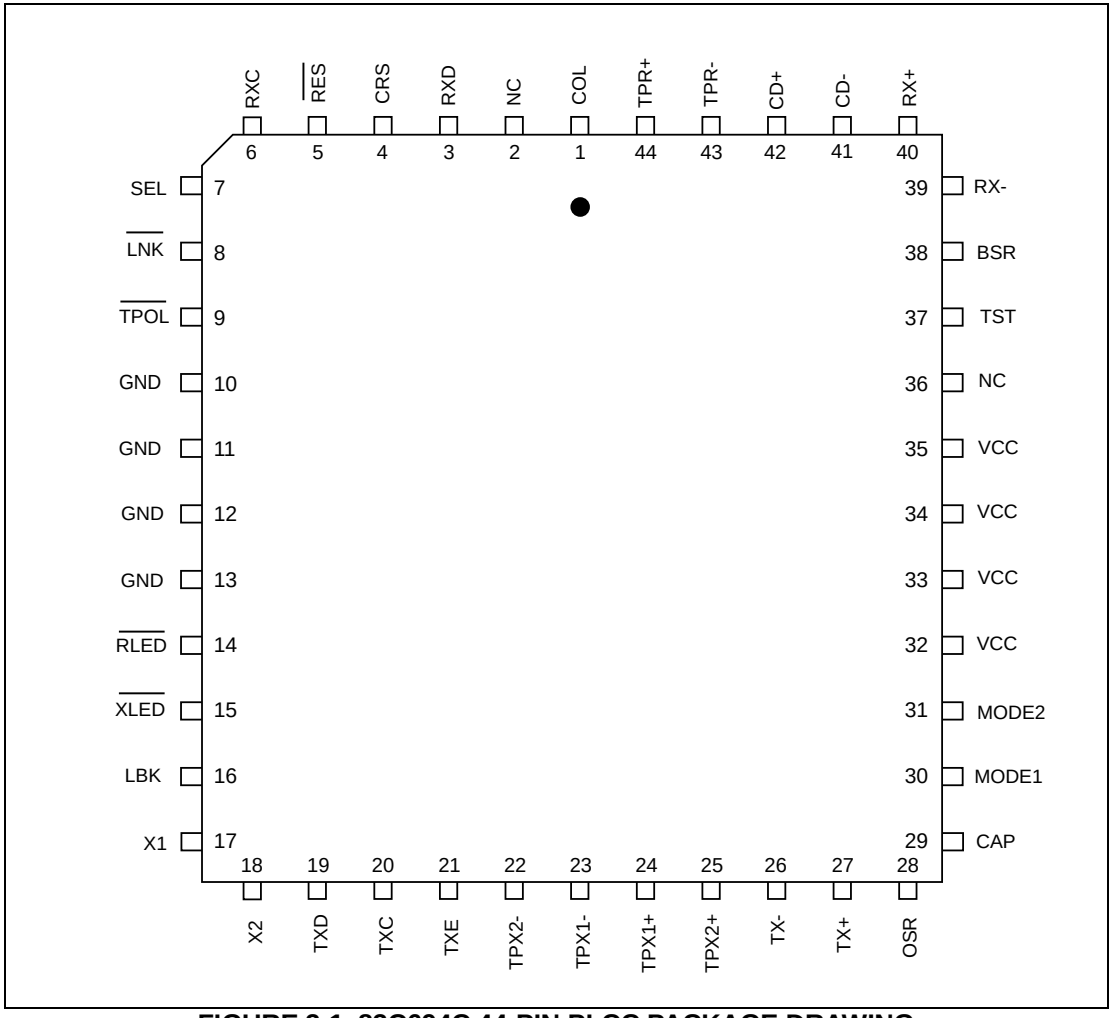



**FIGURE 3-1. 83C694C 44-PIN PLCC PACKAGE DRAWING**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 1 | COL | Collision Detect | O | A 10 MHz (+25%,-15%) signal at the CD inputs (DTE mode) produces a logic high at the COL output. When no signal is present at the CD inputs, the COL output goes low. In 10BaseT operation, the COL output goes high when TPR+ and TPR- are active while a packet is being transmitted on TPX+/TPX-.<br><br>COL also goes high during SQE test or jabber condition. |
| 2 | NC | No Connect | I | Do not connect any circuitry to this pin. |
| 3 | RXD | Receive Data | O | This is the NRZ data output from the on-chip decoder and phase-locked loop. This signal should be sampled by the controller at the rising edge of receive clock. A high level is binary "one", a low level is binary "zero". |
| 4 | CRS | Carrier Sense | O | CRS (DTE mode) goes high when valid data is present at the RX+/RX- inputs or TPR+/TPR- inputs. It goes low after the last bit is received at the inputs. |
| 5 | $\overline{\text{RES}}$ | Reset/Synch | I | When $\overline{\text{RES}}$ is low, all internal nodes are set to a known state except for internal clock distribution. This improves testing procedures. Normal operation is enabled on the rising edge of $\overline{\text{RES}}$ and while $\overline{\text{RES}}$ is high. The $\overline{\text{RES}}$ pin includes an internal pull up resistor, so it may be left open if unused. |
| 6 | RXC | Receive Clock | O | When the phase-locked loop acquires a valid receive signal, a 10MHz clock signal (recovered from receive data) is output on RXC. RXC is low during idle (5 bit times after receive activity stops). |
| 7 | SEL | Mode Select | I | When SEL is high, TX+ and TX- outputs are at the same voltage in idle state, providing a "zero" differential. When SEL is low, TX+ is positive with respect to TX- in idle state. Also, three test modes may be selected by setting the SEL pin to voltages between low and high levels. Refer to section 2.13 for more on test modes. |

**TABLE 3-1. PIN DESCRIPTION**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 8 | $\overline{\text{LNK}}$ | TwPr Link Status | O | If valid data or Link Test pulses are received on TPR+/TPR-, $\overline{\text{LNK}}$ is low (link status OK). When no data or Link Test pulses are received, $\overline{\text{LNK}}$ is high. The $\overline{\text{LNK}}$ pin can sink 10mA to drive an external LED. |
| 9 | $\overline{\text{TPOL}}$ | TwPr Link Polarity | O | $\overline{\text{TPOL}}$ is low when positive polarity Link Test pulses or data packets are received on TPR+/TPR- (normal operation). $\overline{\text{TPOL}}$ is high when negative polarity Link Test pulses or data packets are received (link wiring polarity reversed). When $\overline{\text{TPOL}}$ is low, it can sink 10mA to drive an external LED. |
| 10 – 13 | GND | Negative Supply | | Pin 10 provides negative supply for analog circuits. Pin 11 provides negative supply for digital circuits. Pin 12 provides negative supply for digital/pad circuits. Pin 13 provides negative supply for VCO circuits. |
| 14 | $\overline{\text{RLED}}$ | Receive LED Driver | O | When active low, $\overline{\text{RLED}}$ sinks 10 mA to drive an external LED. If no data is received, $\overline{\text{RLED}}$ is high. If data is received, $\overline{\text{RLED}}$ will go low for approximately 50ms longer than the received packet length.<br><br>All LED current is controlled internally and requires no external resistors between the chip and an external LED.<br><br>The external LED must be connected from +5V to the device pin. If LEDs are not used, then the four pins can be used as logic outputs. |
| 15 | $\overline{\text{XLED}}$ | Transmit LED Driver | O | When active low, $\overline{\text{XLED}}$ sinks 10mA to drive an external LED. When there is no transmission (TXE inactive), $\overline{\text{XLED}}$ is high. When data is transmitted, $\overline{\text{XLED}}$ goes active low for approximately 50ms longer than the transmitted packet length. $\overline{\text{XLED}}$ does not go active low for Link Test pulses. |

**TABLE 3-1. PIN DESCRIPTION cont.**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 16 | LBK | Loopback | I | A high level enables loopback of TXD to RXD/RXC. A low level enables normal transmit/receive operation. The LBK pin includes an internal pull-down resistor, so it may be left open if unused. |
| 17 | X1 | Crystal/Ext. Input | I | X1 is driven by an external clock frequency source or is connected to one terminal of the 20MHz crystal.<br><br>The IEEE 802.3 standard requires 0.01% absolute accuracy on the transmitted signal frequency. Stray capacitance can shift the crystal's frequency out of range, causing it to exceed the 0.01% tolerance. To remedy this, extra load capacitance may be added.<br><br>To determine the amount of capacitance to add, measure the board capacitance and the capacitance between the X1 and X2 pins. Then add these values together, and subtract them from the crystal's required load capacitance. (Refer to Figure 2-1.) |
| 18 | X2 | Crystal Feedback | O | This output is connected to the other terminal of the 20MHz crystal. If X1 is driven with an external source, X2 must be left open. |
| 19 | TXD | Transmit Data | I | TXD is sampled on the rising edge of TXC when TXE is high. The NRZ data input here is encoded and transmitted on TX+/TX- or TPX+/TPX- as a differential signal. |
| 20 | TXC | Transmit Clock | O | This is a 10MHz clock signal derived from the internal 20MHz oscillator. It is enabled except when RES is low and MPE is high. |
| 21 | TXE | Transmit Enable | I | TXE enables encoding and transmission of the data input via TXD. It is sampled on the rising edge of TXC. |
| 22 | TPX2- | TwPr Transmit | O | TPX2- is used for 10BaseT only. It is the low current negative output pin. See TPX1+ for details. |
| 23 | TPX1- | TwPr Transmit | O | TPX1- is used for 10BaseT only. It is the high current negative output pin. See TPX1+ for details. |

**TABLE 3-1. PIN DESCRIPTION cont.**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 24 | TPX1+ | TwPr Transmit | O | In 10BaseT operation, data input via TXD is encoded and then transmitted on TPX pins. When transmit and receive are idle, Link Test pulses are periodically transmitted via TPX.<br><br>The TPX pins are connected to the twisted-pair medium via a transformer and filter, and use 5 external resistors for waveshaping as shown in Figure 2-6. TPX1+ is the high current positive output pin. |
| 25 | TPX2+ | TwPr Transmit | O | TPX2+ is used for 10BaseT only. It is the low current positive output pin. See TPX1+ for details. |
| 26<br>27 | TX-<br>TX+ | AUI Transmit | O | In AUI mode, TX+ and TX- transmit Manchester encoded data differentially to an external transceiver. Each output requires an external pull-up resistor of 150Ω 1% to +5V as shown in Figure 2-2. |
| 28 | OSR | VCO Bias Resistor | I | A resistor from OSR to +5V biases the internal VCO current. Nominal value is 31.6 KΩ 1%. |
| 29 | CAP | PLL Filter Cap | I | A capacitor (nominal value .02 μF) from CAP to ground is used as part of the filter for the internal phase-locked loop. |
| 30 | MODE1 | Mode Select 1 | I | With MODE1 low, TP mode is always selected. No Link Test pulses are transmitted or required on RX+/-. When MODE1 is high, AUI mode is selected at power on. When MODE1 is connected to RES, 10BaseT mode is selected at power on. After power on, if MODE1 is not low, 10BaseT mode is automatically selected if LNK goes low (otherwise AUI mode is selected). The MODE1 pin includes an internal pull-up resistor, so it can be left open if not used. |
| 31 | MODE2 | Mode Select 2 | I | When MODE2 is low, automatic link polarity correction is disabled (TP mode only). Auto-polarity correction is enabled when MODE2 is high. The MODE2 pin includes an internal pull up resistor, so it may be left open if not used. |

**TABLE 3-1. PIN DESCRIPTION cont.**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 32, 33, 34, 35 | VCC | Positive Supply | | Pin 32 is positive supply to the VCO. Pin 33 is positive supply for digital and transmit circuits. Pin 34 is positive supply for digital circuits. Pin 35 is positive supply for receive circuits. |
| 36 | NC | Not Connected | | Do not connect to this pin. |
| 37 | TST | Test Input | I | This pin must be tied low. |
| 38 | BSR | Bias Resistor | I | A resistor from BSR to VCC sets the internal bias levels. Nominal value is 10KΩ 1% resistor connected externally to +5V. If BSR is tied low, a low power mode is enabled and transmit/receive is disabled. |
| 39<br>40 | RX-<br>RX+ | AUI Receive | I | In AUI mode, the Manchester encoded data from an external transceiver is received on RX+/RX-. After timing recovery and decoding, it is output to the controller on RXD. With the standard 78Ω transceiver AUI cable, the differential input must be externally terminated. This requirement can be satisfied by connecting two 39.2Ω 1% resistors in series with an optional 0.1 μF common mode bypass capacitor as shown in Figure 2-3. Matched capacitors can also be added to protect the inputs from external faults. |
| 41<br>42 | CD-<br>CD+ | AUI Collision | I | In AUI mode, a 10 MHz collision presence signal from an external transceiver is received on CD+/CD-. The COL pin is then output high. The collision differential inputs, CD+ and CD-, must be terminated in the same manner as the receive inputs, RX+ and RX-. See Figure 2-3 for information on this design. |

**TABLE 3-1. PIN DESCRIPTION cont.**

| PIN NUMBER | MNEMONIC | SIGNAL NAME | I/O | DESCRIPTION |
|---|---|---|---|---|
| 43<br>44 | TPR-<br>TPR+ | Twisted-Pair Receive | I | In 10BaseT mode, Manchester encoded data is received via TPR+/TPR-. After timing recovery and decoding it is output to the controller on RXD. TPR+/TPR- are connected to the twisted-pair medium through a transformer and filter.<br><br>A 100Ω termination resistor is generally used before the circuit connects to the receive signal lines, TPR+ and TPR- inputs. See Figure 2-5 for information on this design.<br><br>The 83C694D automatically corrects for a misconnection of the + and - interface allowing operation without having to correct the wiring. |

**TABLE 3-1. PIN DESCRIPTION cont.**

# 4.0 DC ELECTRICAL SPECIFICATIONS

## 4.1 ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Vcc). . . . . 6V

TTL Input Voltage . . . . . 0 – 5.5V

Differential Input Voltage . . . . . -0.5 – 5.5V

Differential Output Voltage . . . . . 0 – 16V

Differential Output Current . . . . . -40 mA

Storage Temperature . . . . . -65°C (-85°F) to 150° (302°F)

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operation should be limited to conditions specified under DC Operating Characteristics.

## 4.2 RECOMMENDED OPERATING CONDITIONS

Supply Voltage (Vcc). . . . . 5V ±5%

Ambient Temperature . . . . . 0°C (32°F) to 70°C (158°F)

## 4.3 DC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F)

Vcc = +5V ±5%

**NOTE**

All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Vih | Input High Voltage (TTL and X1)[1] | 2.0 | – | V | – |
| | Input High Voltage (SEL) | 4.5 | – | V | – |
| Vil | Input Low Voltage (TTL, X1, SEL) | – | 0.8 | V | – |
| Iih | Input High Current (TTL, X1, SEL) | – | 50 | µA | Vin = Vcc |
| | Input High Current (RX± and CD± ) | – | 500 | µA | |
| Iil | Input Low Current (TTL, X1 and SEL) | – | -50 | µA | Vin = 0.5V |
| | Input Low Current (RX± and CD± ) | – | -500 | µA | |
| Vcl | Input Clamp Voltage (TTL) | – | -1.2 | V | Iin = -12mA |
| Voh | Output High Voltage (RXD, RXC, CRS, TXC, COL, X2 and LEDs)[2] | 3.5 | – | V | Ioh = -100µA |

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Vol | Output Low Voltage (RXD, RXC, CRS, TXC, COL) | – | 0.5 | V | Iol = 8mA |
| | Output Low Voltage (X2) | – | 0.7 | V | |
| | Output Low Voltage (LEDs) | – | 0.5 | V | Iol = 2 mA |
| Iol | Output Low Current (LEDs) | 10 | 25 | mA | 2V ≤ Vol ≤ 4V |
| Ios | Output Short Circuit Current (RXD, RXC, CRS, TXC, COL) | -40 | -200 | mA | – |
| Vod | Differential Output Voltage (TX±) | ±500 | ±1200 | mV | 78Ω termination and 150Ω from each output to Vcc |
| Vob | Differential Output Voltage Imbalance (TX±) | – | ±40 | mV | 78Ω termination and 150Ω from each output to Vcc |
| Voh | Output High Voltage (TPX1±) | Vcc - 0.6 | – | V | Ioh = -30mA |
| | Output High Voltage (TPX2±) | Vcc - 0.75 | – | V | Ioh = -14 mA |
| Vol | Output Low Voltage (TPX1±) | – | 0.6 | V | Ioh = 30 mA |
| | Output Low Voltage (TPX2±) | | 0.75 | V | Ioh = 14 mA |
| Vds | Differential Squelch Threshold (RX±, CD±) | -175 | -300 | mV | – |
| | Differential Squelch Threshold (TPR±) | 300 | 500 | mV peak | – |
| Vcm | Differential Input Common Mode Voltage (RX±, CD±) | 0 | 5.25 | V | – |
| Icc | Power Supply Current | – | 100 | mA | loopback active at 10 Mbit/sec |

**TABLE 4-1. DC OPERATING CHARACTERISTICS**

[1] TTL inputs are TXE, TXD, LBK, MODE1, MODE2, and $\overline{\text{RES}}$.

[2] LED drivers are $\overline{\text{RLED}}$, $\overline{\text{XLED}}$, $\overline{\text{LNK}}$, and $\overline{\text{TPOL}}$.

## 5.0 AC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F)
Vcc = 5V ± 5%

**NOTE**
All typical values are given for Vcc = 5V and Ta = 25°C (77°F).

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| | *Oscillator Specification* | | | | |
| $t_{XTH}$ | X1 rising edge to Transmit Clock High | 8 | – | 25 | nsec |
| $t_{XTL}$ | X1 rising edge to Transmit Clock Low | 8 | – | 25 | nsec |
| | *Transmit Specification* | | | | |
| $t_{TCD}$ | Transmit Clock Duty Cycle at 50% (10 MHz) | 42 | 50 | 58 | % |
| $t_{TCR}$ | Transmit Clock Rise Time (20 to 80%) | – | – | 8 | nsec |
| $t_{TCF}$ | Transmit Clock Fall Time (20 to 80%) | – | – | 8 | nsec |
| $t_{TDS}$ | Transmit Data Setup Time to Transmit Clock Rising Edge | 20 | – | – | nsec |
| $t_{TDH}$ | Transmit Data Hold Time from Transmit Clock Rising Edge | 0 | – | – | nsec |
| $t_{TES}$ | Transmit Enable Setup Time to Transmit Clock Rising Edge | 20 | – | – | nsec |
| $t_{TEH}$ | Transmit Enable Hold Time from Transmit Clock Rising Edge | 0 | – | – | nsec |
| $t_{TOD}$ | Transmit Output Delay from Transmit Clock Rising Edge | – | – | 60 | nsec |
| $t_{TOR}$ | Transmit Output Rise Time (20% to 80%) (TX±) | – | – | 8 | nsec |
| | Transmit Output Rise Time (TPX±) | – | 4.5 | – | nsec |
| $t_{TOF}$ | Transmit Output Fall Time (80% to 20%) (TX±) | – | – | 8 | nsec |
| | Transmit Output Fall Time (TPX±) | – | 4.5 | – | nsec |
| $t_{TOJ}$ | Transmit Output Jitter (TX±) | – | ±0.25 | – | nsec |
| $t_{TOH}$ | Transmit Output High before Idle in Half Step Mode | 200 | – | – | nsec |
| $t_{TOI}$ | Transmit Output Idle Time in Half Step Mode | – | – | 350 | nsec |
| $t_{LTPW}$ | Link Test Pulse Width | | 100 | | nsec |
| | *Receive Specification* | | | | |
| $t_{RCD}$ | Receive Clock Duty Cycle at 50% (10 MHz) | 40 | 50 | 60 | % |
| $t_{RCR}$ | Receive Clock Rise Time (20% to 80%) | – | – | 8 | nsec |
| $t_{RCF}$ | Receive Clock Fall Time (20% to 80%) | – | – | 8 | nsec |
| $t_{RDR}$ | Receive Data Rise Time (20% to 80%) | – | – | 8 | nsec |
| $t_{RDF}$ | Receive Data Fall Time (80% to 20%) | – | – | 8 | nsec |
| $t_{RDS}$ | Receive Data Stable from Receive Clock Rising Edge | ±40 | – | – | nsec |
| $t_{CSON}$ | Carrier Sense Turn on Delay (AUI) | – | – | 60 | nsec |
| | Carrier Sense Turn on Delay (TP) | – | – | 300 | nsec |
| $t_{CSOFF}$ | Carrier Sense Turn off Delay (AUI) | – | – | 160 | nsec |
| | Carrier Sense Turn off Delay (TP) | – | – | 160 | nsec |

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{DAT}$ | Decoder Acquisition Time (AUI) | – | – | 700 | nsec |
| | Decoder Acquisition Time (TP) | – | – | 950 | nsec |
| $t_{DREJ}$ | Differential Inputs Rejection Pulse Width (AUI) | 8 | 25 | 35 | nsec |
| | Differential Inputs Rejection Pulse Width (TP) | 8 | 20 | 30 | nsec |
| $t_{RD}$ | Receive Throughput Delay | – | – | 200 | nsec |
| *Collision Specification* | | | | | |
| $t_{COLON}$ | Collision Turn On Delay (AUI) | – | – | 60 | nsec |
| | Collision Turn On Delay (TP) | – | – | 900 | nsec |
| $t_{COLOFF}$ | Collision Turn Off Delay (AUI) | 100 | – | 160 | nsec |
| | Collision Turn Off Delay (TP) | – | – | 160 | nsec |
| $t_{SQEON}$ | SQE Test Start Delay (TP) | 0.6 | 1.0 | 1.6 | usec |
| $t_{SQED}$ | SQE Test Duration (TP) | 0.5 | 1.0 | 1.5 | usec |
| *Loopback Specification* | | | | | |
| $t_{LBS}$ | Loopback Setup Time | 35 | – | – | nsec |
| $t_{LBH}$ | Loopback Hold Time | 350 | – | – | nsec |
| *10BaseT Protocol Timers* | | | | | |
| | Link Test Transmit Period | 9.8 | – | 11.5 | msec |
| | Link Loss / Link Test Max. | 78 | – | 92 | msec |
| | Link Test Min. | 4.9 | – | 5.8 | msec |
| | Jabber On (transmit inhibit) | 39 | – | 46 | msec |
| | Jabber Off (transmit re–enable) | 314 | – | 368 | msec |

**TABLE 5-1. AC OPERATING CHARACTERISTICS**

### 5.1 TIMING DIAGRAMS

Figures 5–1 through 5–9 illustrate all timings. Table 5–2 lists all timing diagrams.

| Figure Number | Title |
|---|---|
| 5–1 | Transmit Timing – Start of Transmission |
| 5–2 | Transmit Timing – End of Transmission (last bit = 0) |
| 5–3 | Transmit Timing – End of Transmission (last bit = 1) |
| 5–4 | Transmit Timing – Link Test Pulse |
| 5–5 | Receive Timing – Start of Packet |
| 5–6 | Receive Timing – End of Packet (last bit = 0) |
| 5–7 | Receive Timing – End of Packet (last bit = 1) |
| 5–8 | Collision Timing (AUI) |
| 5–9 | Collision Timing (TP) |
| 5–10 | SQE Test Timing |
| 5–11 | Loopback Timing |
| 5–12 | Test Loads |

**TABLE 5–2. 83C694D TIMING DIAGRAMS**

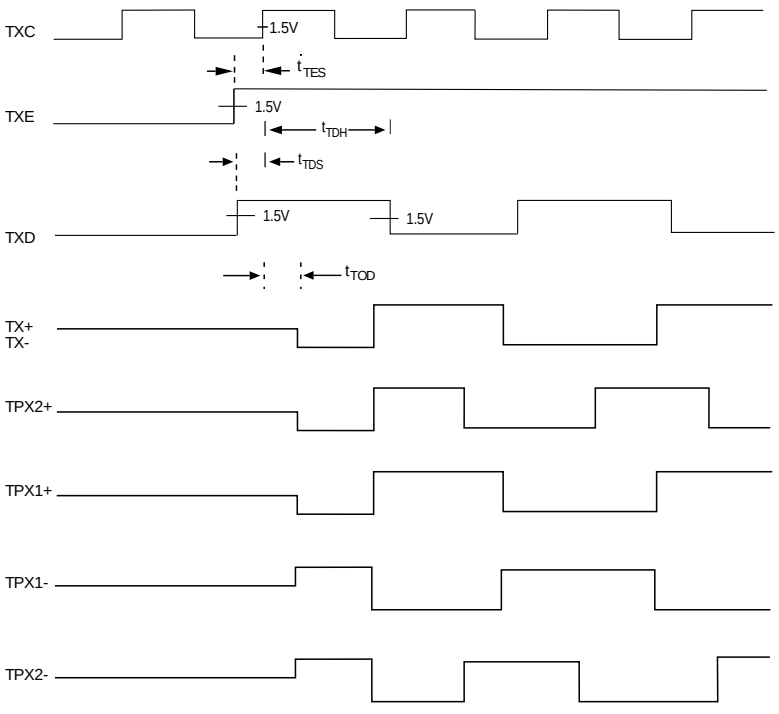



**FIGURE 5-1. TX TIMING - START OF TRANSMISSION**

**FIGURE 5-2. TX TIMING - END OF TRANSMISSION (LAST BIT=0)**

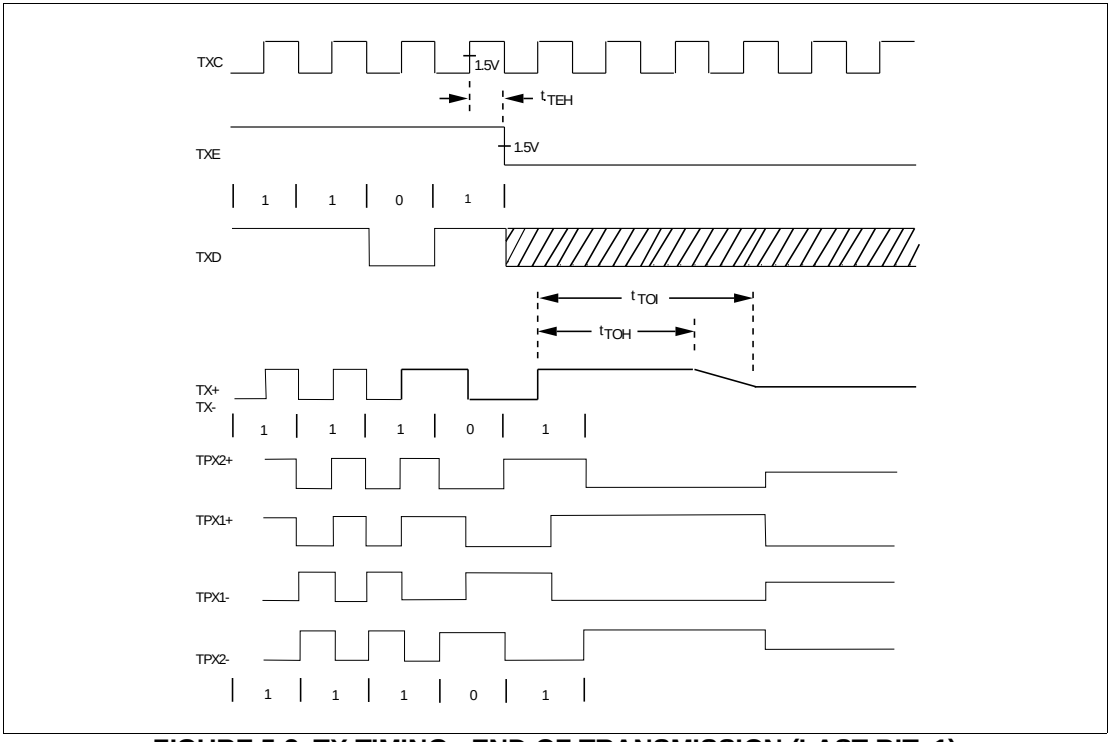



**FIGURE 5-3. TX TIMING - END OF TRANSMISSION (LAST BIT=1)**

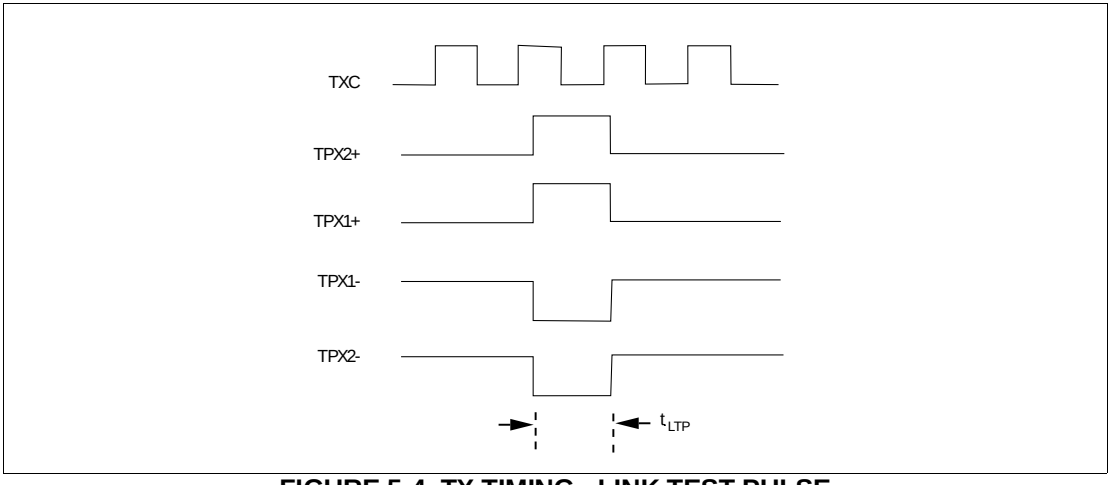



**FIGURE 5-4. TX TIMING - LINK TEST PULSE**

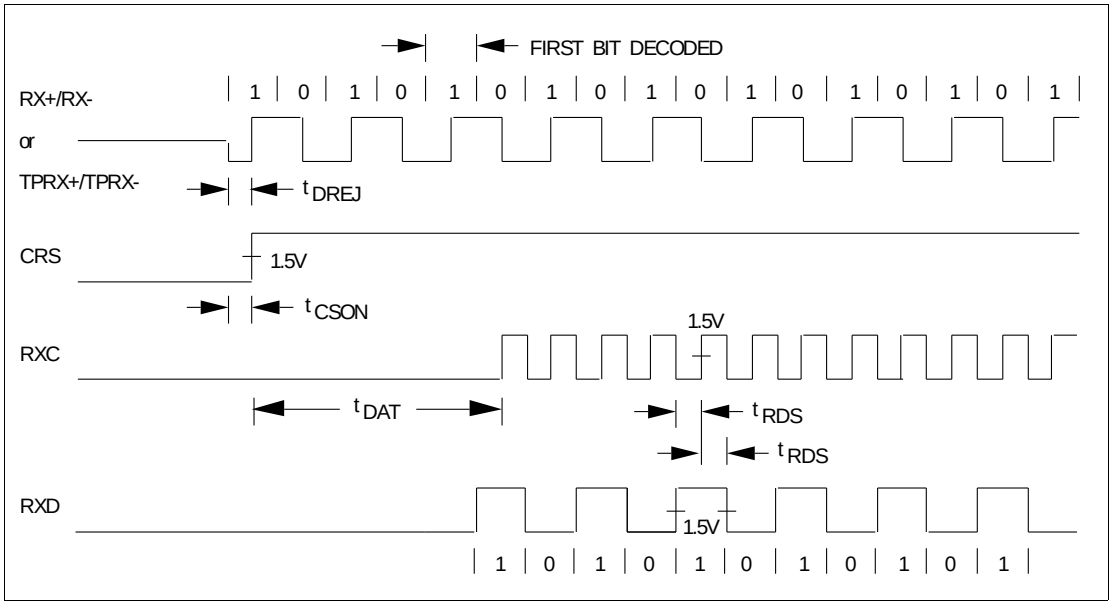



**FIGURE 5-5. RECEIVE TIMING - START OF PACKET**

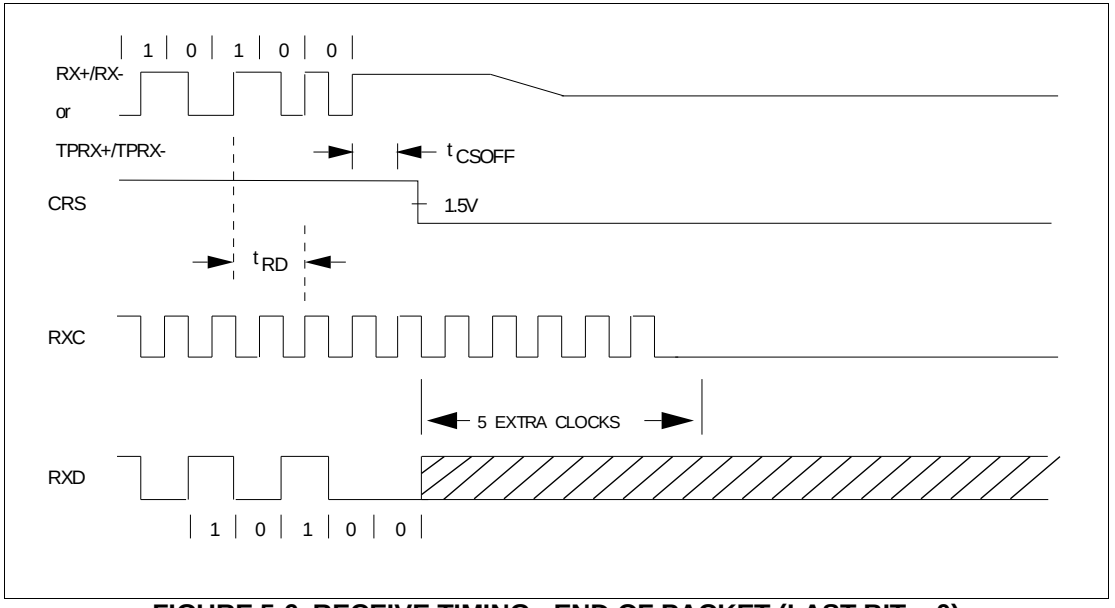



**FIGURE 5-6. RECEIVE TIMING - END OF PACKET (LAST BIT = 0)**

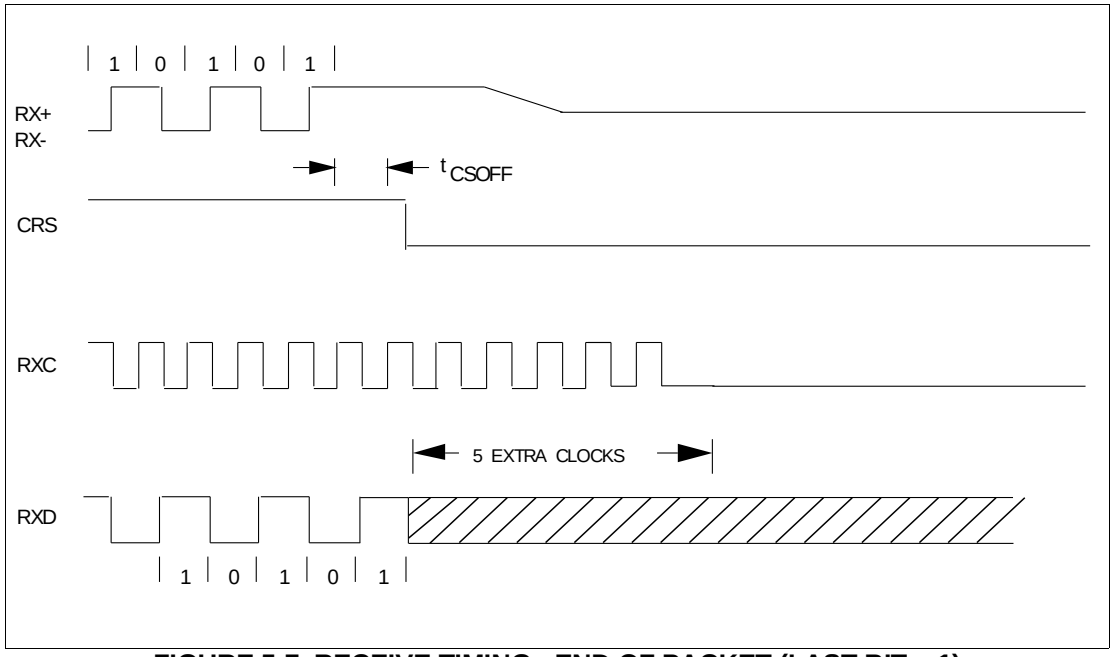



**FIGURE 5-7. RECEIVE TIMING - END OF PACKET (LAST BIT = 1)**

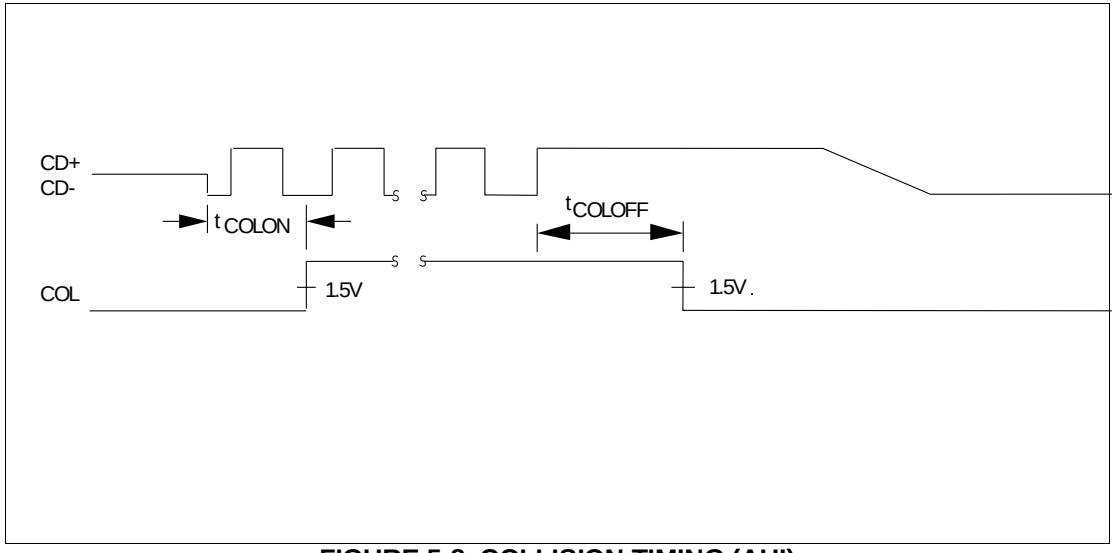



**FIGURE 5-8. COLLISION TIMING (AUI)**

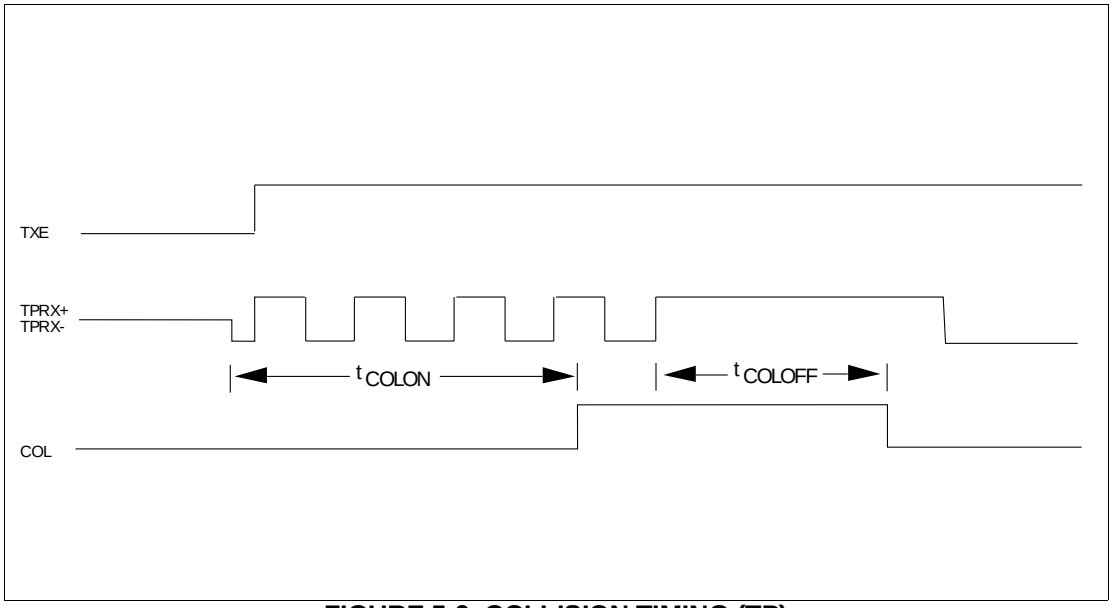



**FIGURE 5-9. COLLISION TIMING (TP)**

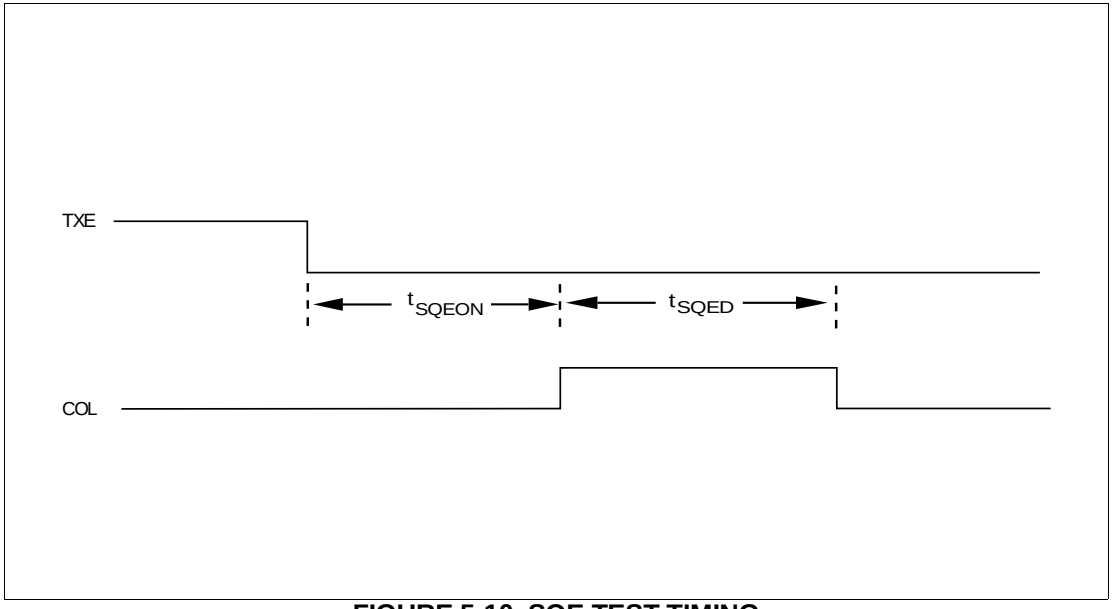



**FIGURE 5-10. SQE TEST TIMING**

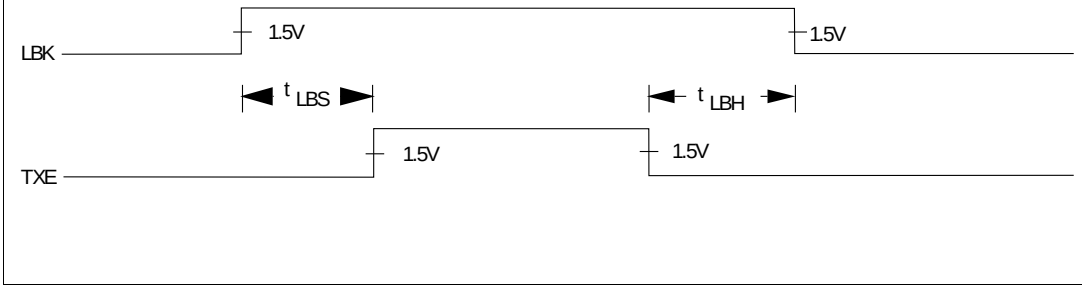
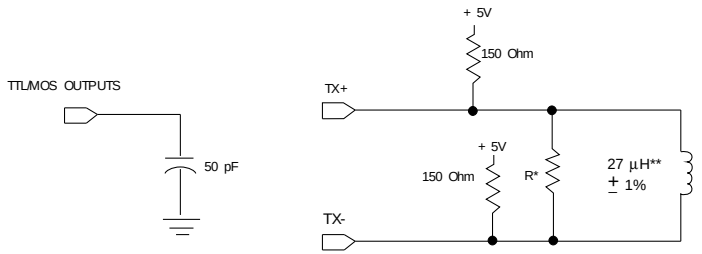



**FIGURE 5-11. LOOPBACK TIMING**




* R = 73 Ohm ± 1% and
R = 83 Ohm ± 1%

** 27 µH ± 1% inductor is used for test purposes. 100 µH tranformers (Valor LT 1101, or Pulse Engineering 64103) are recommended for application use.

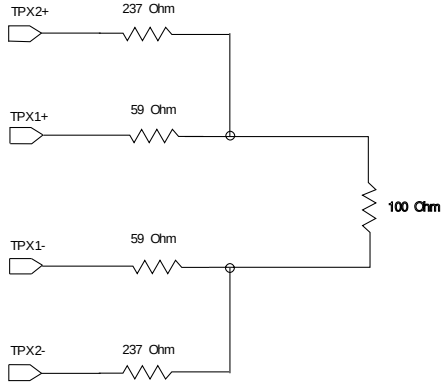



**FIGURE 5-12. TEST LOADS**

## 6.0 PACKAGE DESCRIPTION

Figure 6-1 illustrates the 44-pin PLCC package for the 83C694D. Refer to Table 6-1 for the dimensions given in this figure.

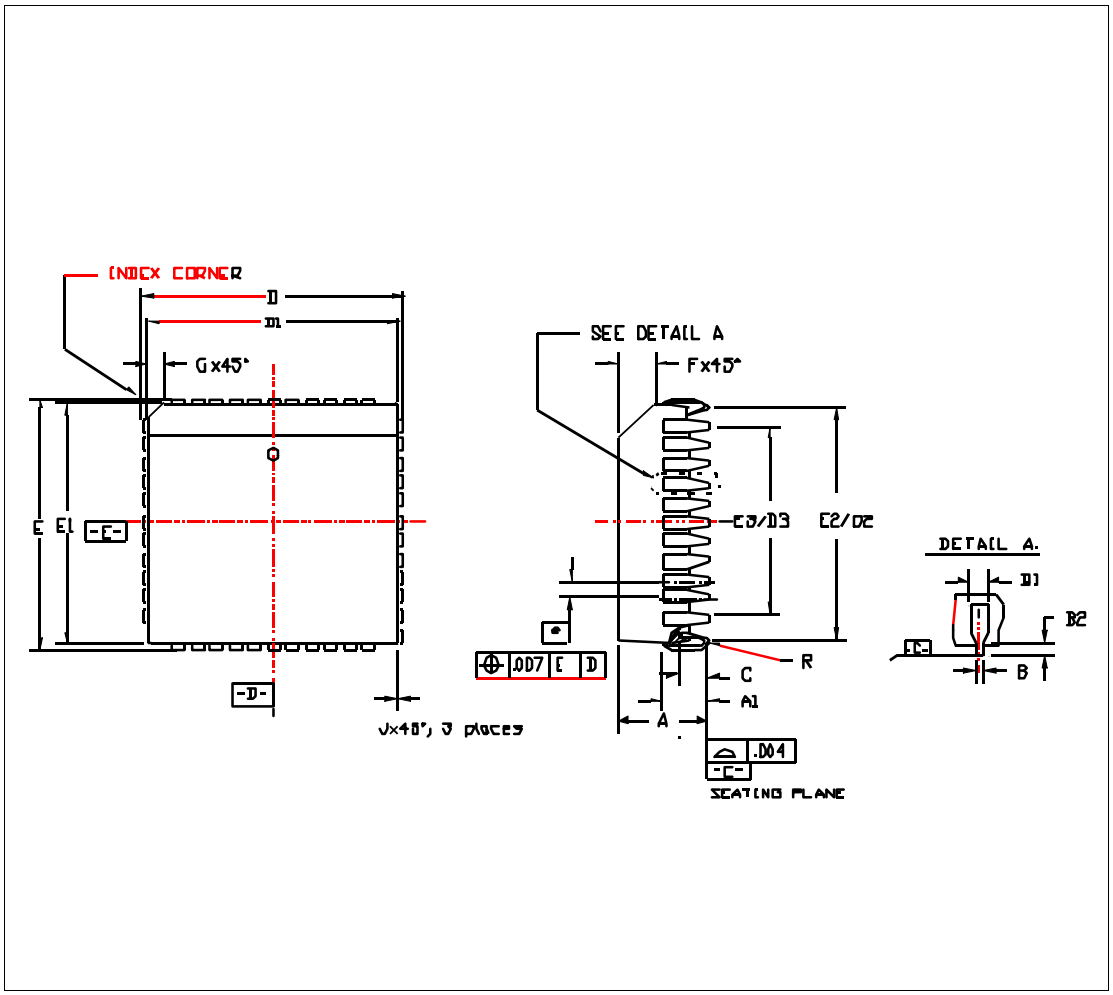



**FIGURE 6-1. 44-PIN PLCC PACKAGE DIAGRAM**

Table 6-1 provides acceptable ranges for the codes shown in Figure 6-1. All dimensions are in inches.

| Code | Dimension Ranges |
|---|---|
| A | .160 – .188 |
| A1 | .090 – .120 |
| B | .013 – .021 |
| B1 | .026 – .032. |
| B2 | .025 min |
| C | .020 – .045 |
| D/E | .685 – .695 |
| D1/E1 | .650 – .656 |
| D2/E2 | .600 – .630 |
| D3/E3 | .500 REF |
| e | .050 BSC |
| F | .042 – .060 |
| G | .042 – .048 |
| J | .000 – .028 |
| R | .025 – .045 |

**TABLE 6-1. PLCC PACKAGE DIMENSIONS**

Notes:

1. Coplanarity is .004" maximum
2. Tolerance on the position of the leads is .007"maximum
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is .010"

# Index