FemtoClocks™ Crystal-to-LVCMOS/ LVTTL Frequency Synthesizer

840002I

DATASHEET

General Description

The 840002I is a 2 output LVCMOS/LVTTL Synthesizer optimized to generate Fibre Channel reference clock frequencies. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL1:0): 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, and 53.125MHz. The 840002I uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 840002I is packaged in a 16-pin TSSOP package.

Features

- Two LVCMOS outputs @ 3.3V, 17Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS single-ended input
- Output frequency range: 46.66MHz - 233.33MHz
- VCO range: 560MHz - 700MHz
- Supports the following output frequencies: 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz and 53.125MHz
- RMS phase jitter @ 212.5MHz (637KHz - 10MHz): 0.83ps (typical)

  Typical phase noise at 212.5MHz:

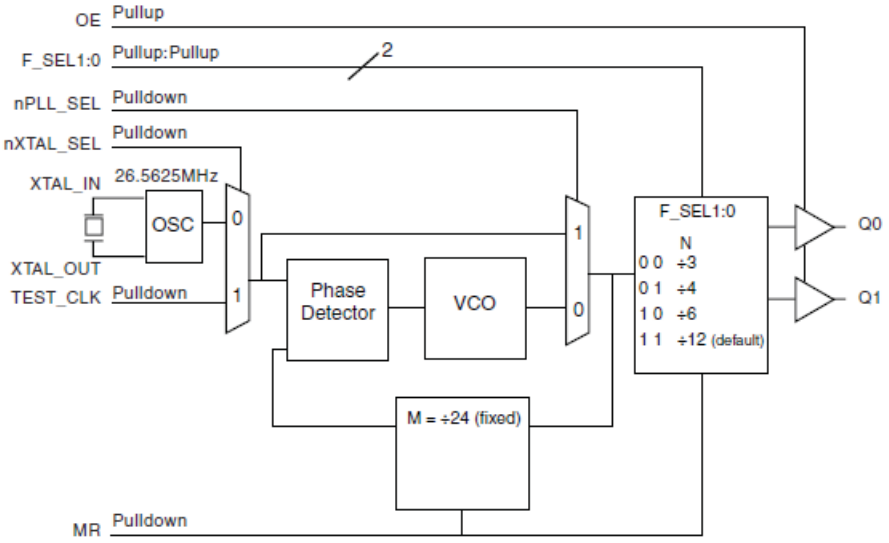
Offset	Noise Power
100Hz	-91.3 dBc/Hz
1KHz	-114.3 dBc/Hz
10KHz	-120.7 dBc/Hz
100KHz	-120.2 dBc/Hz

- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-Free package RoHS compliant

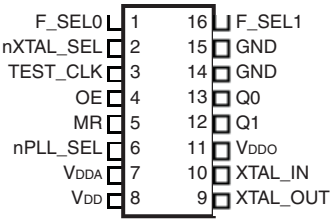
Frequency Select Function Table

Input Frequency (MHz)	Inputs					Output Frequency (MHz)
	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Ratio Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25

Block Diagram



Pin Assignment



840002I

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 16	F_SEL0, F_ SEL1	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels.
2	nXTAL_SEL	Input	Pulldown	Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
3	TEST_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL clock input.
4	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing active outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/n output divider. LVCMOS/LVTTL interface levels.
7	V_{DDA}	Power		Analog supply pin.
8	V_{DD}	Power		Core supply pin.
9, 10	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
11	V_{DDO}	Power		Output supply pin.
12, 13	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
14, 15	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance			8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	3.3V±5%	14	17	21	Ω
		2.5V±5%	16	21	25	Ω

Table 3. Frequency Select Function Table

Input Frequency (MHz)	Inputs					Output Frequency (MHz)
	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ or $2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, OR $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465V$	-0.3		0.8	V
			$V_{DD} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			5	µA
		F_SEL0:1, nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			150	µA
I_{IL}	Input Low Current	OE	$V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$	-150			µA
		F_SEL0:1, nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V±5\%$	2.6			V
			$V_{DDO} = 2.5V±5\%$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V$ or $2.5V±5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	F_SEL[1:0] = 00	186.67		226.67	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.67	MHz
tsk(o)	Output Skew; NOTE 1, 3				12	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz @ Integration Range: 637KHz - 10MHz		0.83		ps
		159.375MHz @ Integration Range: 637KHz - 10MHz		0.62		ps
		156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.59		ps
		106.25MHz @ Integration Range: 637KHz - 10MHz		0.80		ps
		53.125MHz @ Integration Range: 637KHz - 10MHz		0.68		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] 00	46		54	%
		F_SEL[1:0] = 00	42		58	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	F_SEL[1:0] = 00	186.67		226.67	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.67	MHz
tsk(o)	Output Skew; NOTE 1, 3				12	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz @ Integration Range: 637KHz - 10MHz		0.73		ps
		159.375MHz @ Integration Range: 637KHz - 10MHz		0.62		ps
		156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.56		ps
		106.25MHz @ Integration Range: 637KHz - 10MHz		0.76		ps
		53.125MHz @ Integration Range: 637KHz - 10MHz		0.72		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] 00	46		54	%
		F_SEL[1:0] = 00	42		58	%

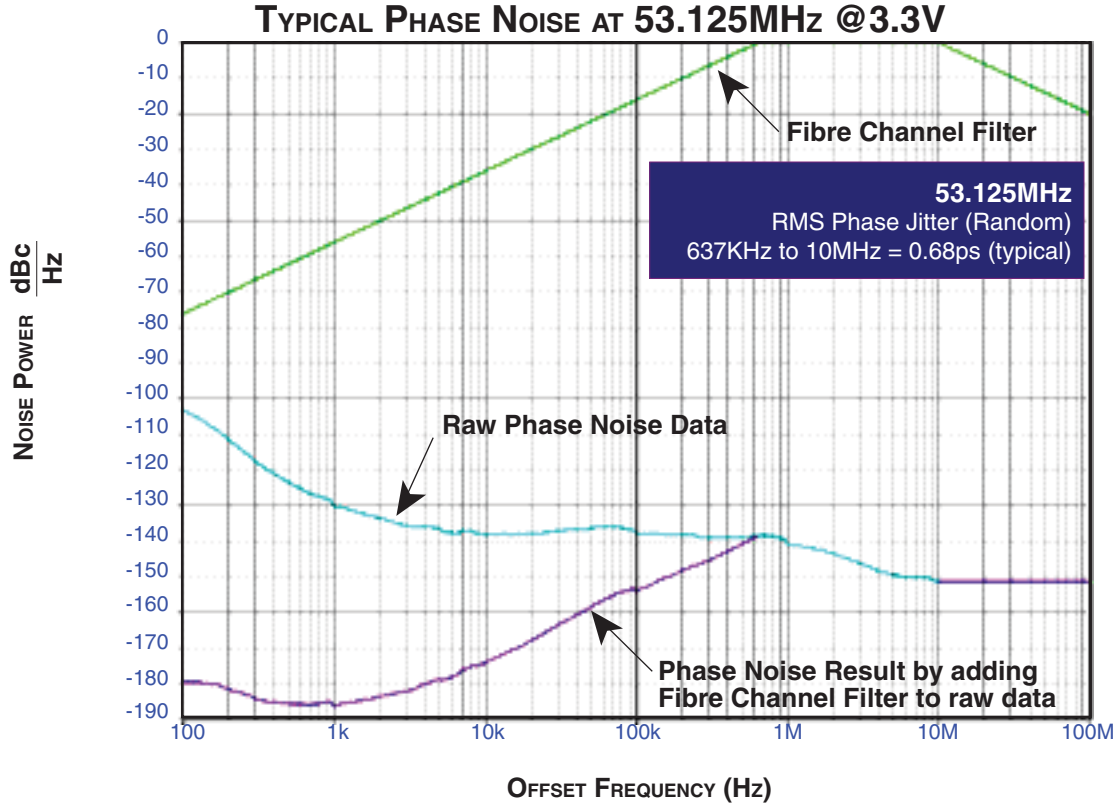
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

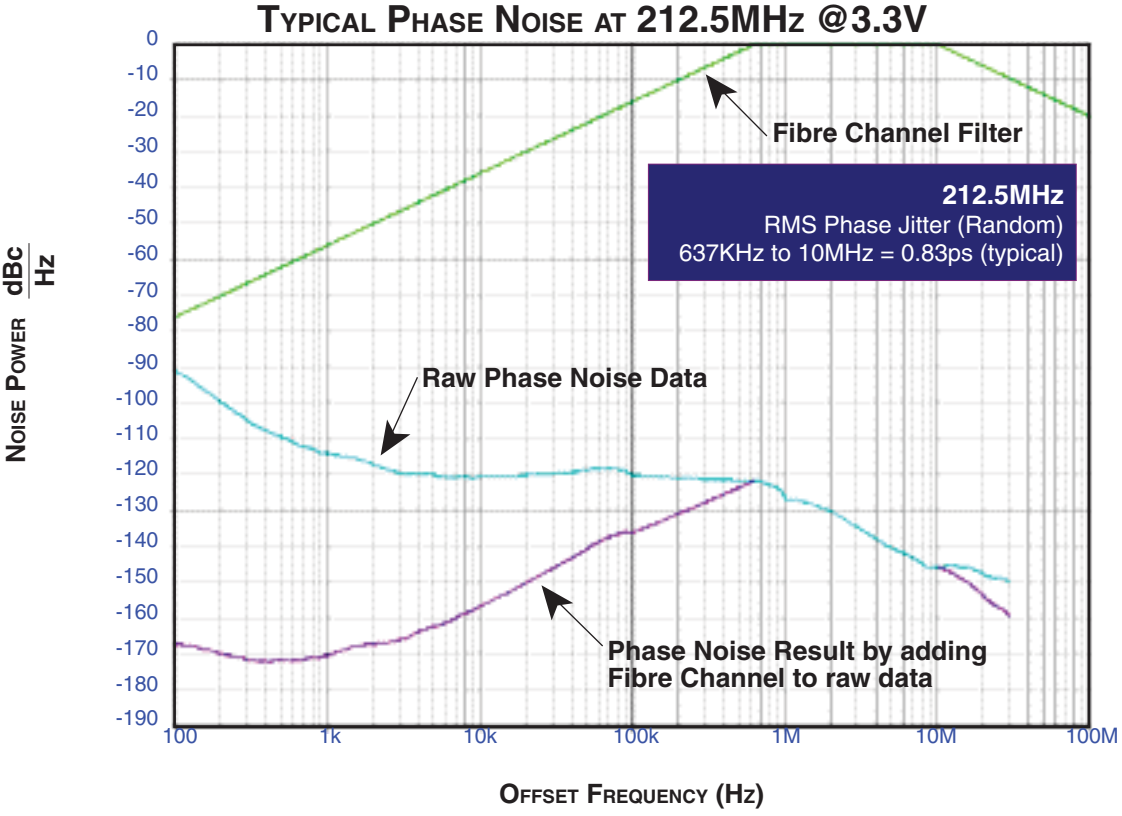
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	F_SEL[1:0] = 00	186.67		226.67	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.67	MHz
tsk(o)	Output Skew; NOTE 1, 3				12	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz @ Integration Range: 637KHz - 10MHz		0.78		ps
		159.375MHz @ Integration Range: 637KHz - 10MHz		0.67		ps
		156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.69		ps
		106.25MHz @ Integration Range: 637KHz - 10MHz		0.82		ps
		53.125MHz @ Integration Range: 637KHz - 10MHz		0.75		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL[1:0] ¹ 00	46		54	%
		F_SEL[1:0] = 00	42		58	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

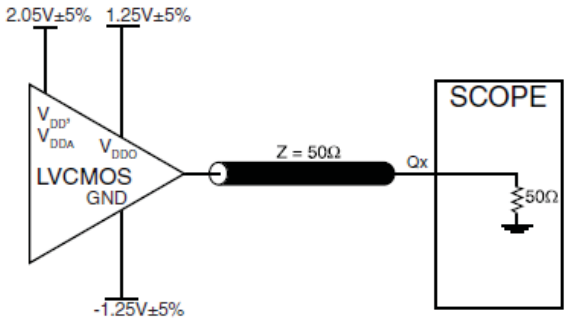
Typical Phase Noise at 53.125MHz @3.3V



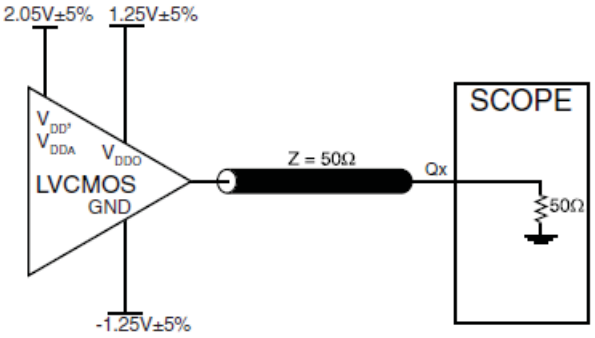
Typical Phase Noise at 212.5MHz @3.3V



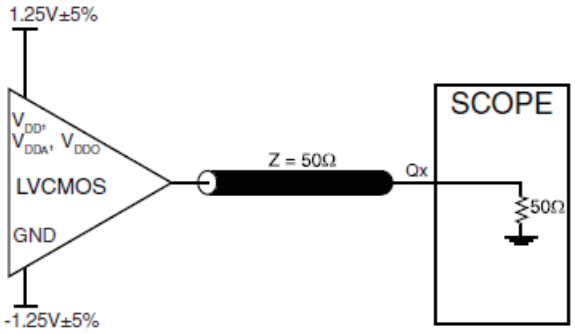
PARAMETER MEASUREMENT INFORMATION



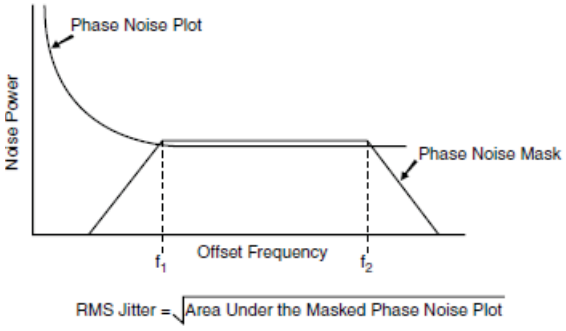
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



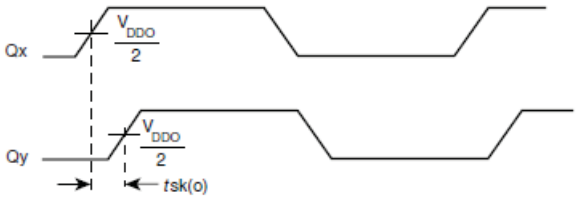
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



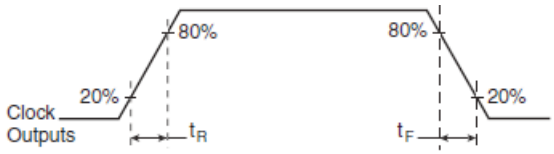
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



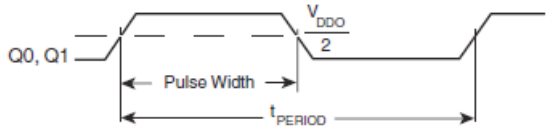
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 840002I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

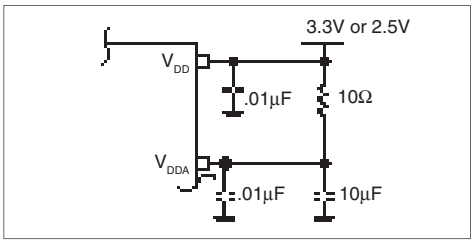


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 840002I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

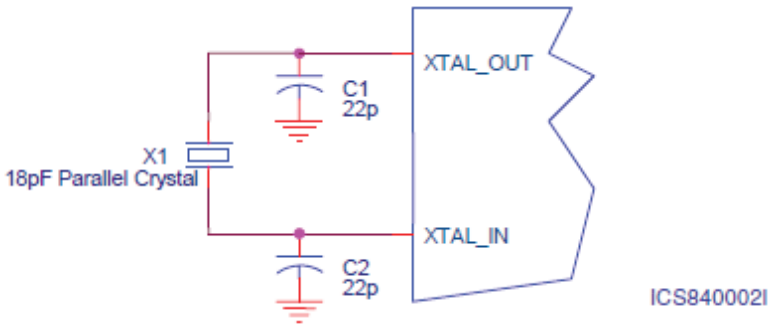


Figure 2. CRYSTAL INPUT INTERFACE

Layout Guideline

Figure 3 shows a schematic example of the 840002I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used. The C1=22pF and C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. 1KΩ pullup or pulldown resistors can be used for the logic control input pins.

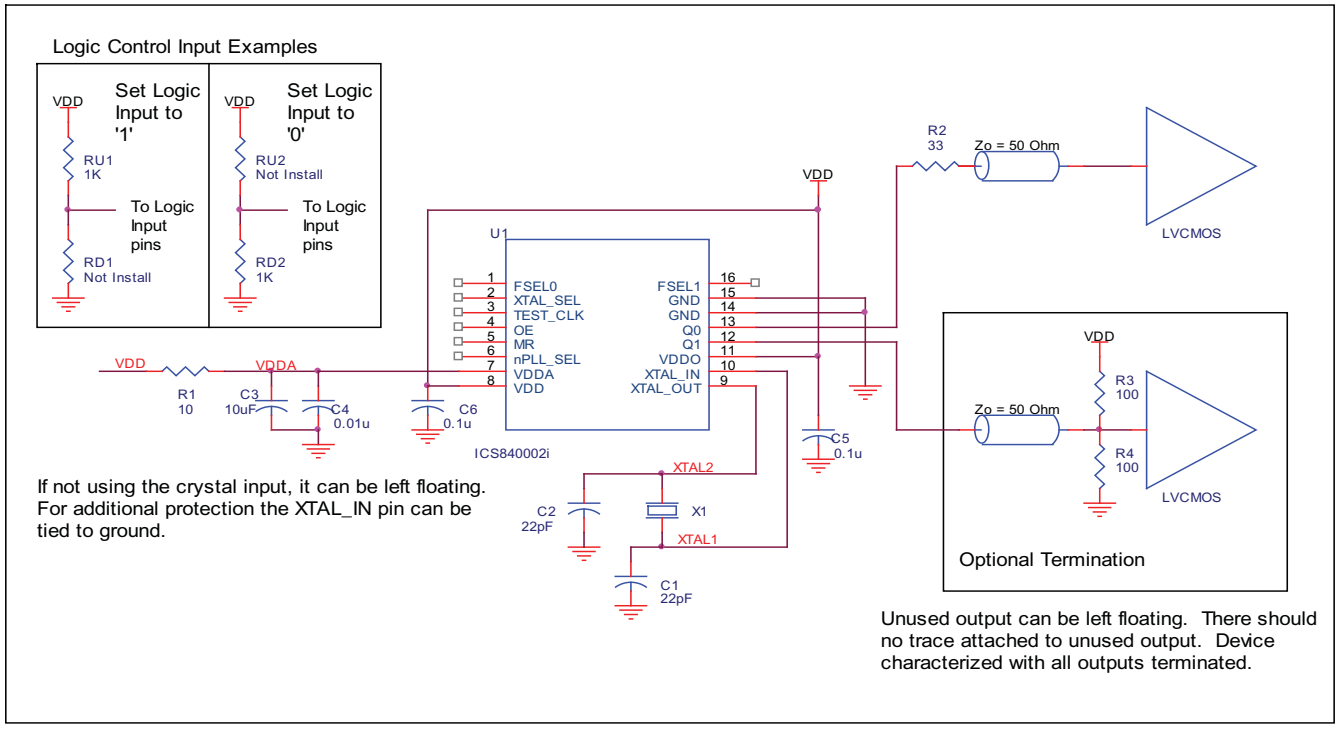


Figure 3. 840002I Schematic Example

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 840002I is: 3085

Package Outline - G Suffix for 16 Lead TSSOP

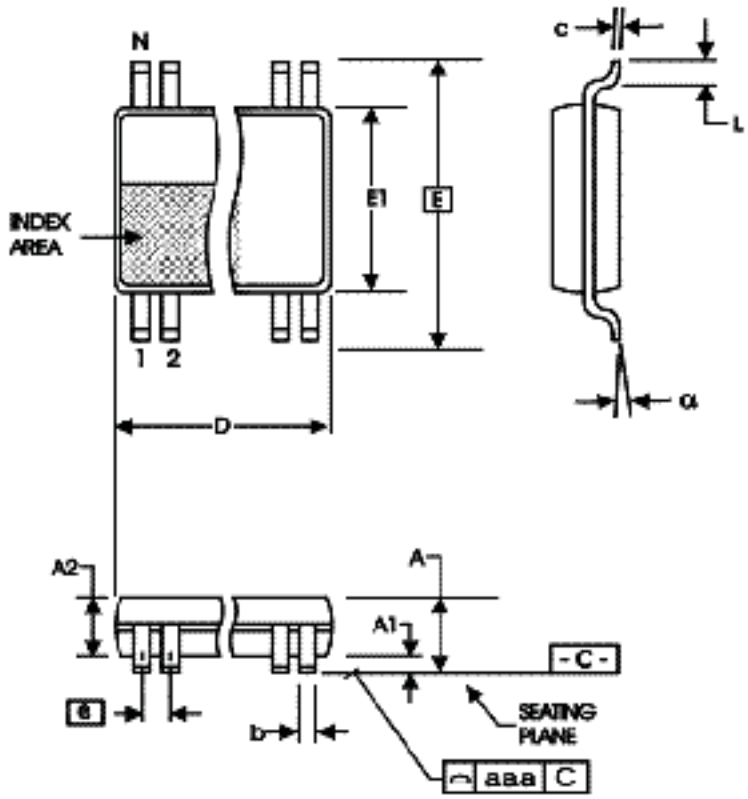


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840002AGILF	40002AIL	16 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
840002AGILFT	40002AIL	16 Lead “Lead-Free” TSSOP	2500 tape & reel	-40°C to 85°C

Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	13	Ordering Information Table - deleted quantity from tube count. Added *tape & reel* to count.	1/22/07
A	T9	13 15	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Deleted "ICS" from non-lead marking. Added Lead-free marking. Added Contact Page.	11/10/10
A	T9	13	Ordering Information - removed leaded devices. Updated data sheet format.	3/30/15

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