8450

Data Sheet

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List of Abbreviations and Acronyms

Term	Definition
3DES	Triple Data Encryption Standard
AES-128	128-bit Key Advanced Encryption Standard, FIPS 197
API	Application Programming Interface
ARC4	Alleged RC4
BITW	Bump-In-The-Wire
CBC	Cipher Block Chaining
CCM	Combined Counter Mode
CPU	Central Processing Unit
CSMA/CD	Carrier Sense-Multiple Access / Collision Detect
CTR	Counter Mode
DES	Data Encryption Standard
DH	Diffie-Hellman
DMA	Direct Memory Access
DPU	Data Protocol Unit
DSA	Digital Signature Algorithm
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
eSC	embedded Session Controller
ESP	Encapsulating Security Payload
FIFO	First-In First-Out
GbE	Gigabit Ethernet
GCM	Galois Counter Mode
GMAC	Gigabit Media Access Controller
GMII	Gigabit Media Independent Interface
HMAC	Hash Message Authentication Code
IKE	Internet Key Exchange
I^2C	Inter-Integrated Circuit Bus
IP	Internet Protocol
IPcomp	Internet Protocol Compression

Term	Definition
IPsec	Internet Protocol Security
JTAG	Joint Test Action Group
LZS	Limpel-Ziv Stac
MAC	Media Access Controller
MTU	Minimum Transmission Unit
NIC	Network Interface Card
PCI	Peripheral Component Interconnect
PCP	Post Crypto Processor
PK	Public Key
PL3	POS-PHY Level 3
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPCI	Packet Processing Command Interface
PRNG	Pseudo-Random Number Generator
RAM	Random Access Memory
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RNG	Random Number Generator
RoHS	Reduction of Hazardous Substances
ROM	Read-Only Memory
RSA	Rivest, Shamir, & Adleman
RTBI	Reduced Ten-Bit Interface
SA	Security Association
SAD, SADB	Security Association Database
SERDES	Serializer/Deserializer
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial GMII
SHA	Secure Hash Algorithm
SPD	Security Policy Database
SRAM	Synchronous Random Access Memory
SSL	Secure Sockets Layer

Term	Definition
TBI	Ten Bit Interface
TCAM	Ternary Content Addressable Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TLS	Transport Layer Security
TOE	TCP Offload Engine
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
VLAN	Virtual Local Area Network
VPN	Virtual Private Network
WAN	Wide Area Network

Preface

This document provides a description of the hardware and functional features contained in the 8450 FlowThrough™ security processor.

Please refer to the latest Product Release Notes for the tested and released product features, as well as the known hardware and software errata.

About This Document

This document assumes you are already familiar with the device technology and terminology.

This document is intended for integrators and application developers responsible for and familiar with software and hardware architecture of a target system. The datasheet is primarily used by the hardware design team. Software and applications developers will use other documents such as the User Manuals and Programming Guides.

Prerequisite

Before proceeding you should generally understand:

- Software and hardware of the target system
- General networking concepts
- General IPsec security concepts

Document Organization

This document is organized as follows:

Chapter 1, "8450 Product Description" provides an introduction/overview of the 8450 Security Processor.

Chapter 2, "Features" provides a generalized summary of the key features and functionality of the 8450.

Chapter 3, "Performance Summary" defines the 8450 supported performance parameters.

Chapter 4, "8450 Operation" presents a detailed description of the 8450 internal features and data flow through the device.

Chapter 5, "Host Messaging and System Configuration" provides an overview of the following: 8450 Messaging, Packet Fragmentation/Reassembly, Security Policy/SADB Management, Exception handling and System Boot.

Chapter 6, "Signal Description" details the various interface signals and functionality or each pin/signal of the 8450.

Chapter 7, "DC Specifications" shows absolute maximum ratings, thermal specifications, operating conditions, DC characteristics and power seqencing.

Chapter 8, "Timing Specifications" includes timing information for the DDR, GMAC, RMII and miscellaneous interfaces of the 8450.

Chapter 9, "Pinout and Mechanical Description" provides a pinout summary and mechanical packaging details for the 8450.

Related Documents

- *4450/8450 Product Release 2.1 Notes*, RN-0118
- *4450/8450 Performance Application Note*, AN-0168
- *4450/8450 Hardware Design Application Note*, AN-0145
- *4450/8450 Development Card User Guide*, UG-0157
- *4450/8450 User Guide*, UG-0150
- *4450/8450 SDK 2.1 Getting Started and Porting Guide*, UG-0145
- *FlowThrough Application Programming Interface Programmer's Guide*, UG-0147
- *Security Management Application Programming Interface Programmer's Guide*, UG-0148
- *Log Application Programming Interface Programmer's Guide*, UG-0149
- *Station Management User Guide*, UG-0146

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1 8450 Product Description

The 8450 is the 2nd generation security processor in the FlowThrough™ family. The 8450 security processor combines high performance throughput in a FlowThrough™ architecture, supporting Internet Protocol Security (IPsec) and Internet Protocol Compression (IPcomp) processing. A single packet can be processed through multiple of the above protocols in a pipelined manner, if required. Secure Real-Time Protocol (SRTP) and IPsec are supported as a prototype implementation in a single firmware build.

High Performance VPN: The Hifn 8450 FlowThrough Security processor supports complete IPsec, IPcomp protocol processing on a single chip. Optimized for dual gigabit in-line applications, the 8450 Security Processor achieves up to 4Gbps (2 Gbps full-duplex) sustained performance with simultaneous encryption/compression and authentication. At small packet sizes, the 8450 without IKE or SDRAM can process up to 900,000 IPsec packets per second.

Protocol Support: The 8450 FlowThrough Security Processor performs Ethernet link processing, security policy enforcement, Security Association (SA) look-up, and IPsec, IPcomp packet processing. The 8450 offers complete support for both IPv4 and IPv6 protocols and supports Jumbo (9022 byte) Ethernet frames. The host configures the security policy database (SPD), and the 8450 stores the security association database (SAD) context data for each security association in its on-chip memory or in off-chip DDR2 SDRAM.

The 8450 Security Processor is the ideal bump-in-the-wire (BITW) FlowThrough security solution for routers, remote access concentrators, VPN gateways, firewalls, WAN switches, Integrated Access Devices, VoIP and secure server NIC card applications. The 8450 also supports RFC3948 NAT traversal using ESP over UDP.

Simple System Interfacing: The 8450 is designed to easily and seamlessly interface with Gigabit MACs and PHYs, including all leading Network Processors, Communications Processors, and Gigabit Ethernet Switch and MAC devices, providing a turnkey security/ compression solution with minimal development effort. It provides two independent pairs of gigabit Ethernet interfaces, that gluelessly connect to standard RGMII/RTBI/SGMII or SERDES Interfaces on both the Host and Network ports. GMII/TBI are also available on the Host-side interfaces. The network-side and host-side interfaces may be configured differently, allowing the 8450 to provide interface conversion. The 8450 GMII (Host Only), and RGMII/SGMII (Host/Network) Interfaces can also be run in 10/100 speeds for Fast Ethernet applications. Both the Host-side and Network-side interfaces are independently configurable as either PHY or MAC personality.

On-Chip RAM: Integrated on-chip RAM is used for SPD, SAD, packet processing, Public Key processing, and RNG Processing. On-chip packet buffering enables optimal processing performance with minimal processing latency. The 8450 can store up to 200 SAs in on-chip memory for low tunnel-count systems. Note: The number of SA's supported on-chip may vary depending on the software release and the supported features. Please refer to the *Product Release Notes*, RN-0118, for additional information.

Integrated Public-Key Processing: The 8450 contains an integrated public-key accelerator subsystem. This unit speeds the computation of the large-vector math required for public-key operations such as Diffie-Hellman, RSA and DSA. The 8450 includes native support for public key modulus sizes up to 4096 bits.

AES Support: The advanced encryption standard, AES, is fully supported. The 8450 supports AES key lengths of 128 and 256-bits, in CBC, CTR, CCM and GCM modes.

Compatibility: The 8450 FlowThrough Security Processor is compliant with IETF standards for IPsec, IPcomp. Optional on-chip Internet Key Exchange (IKE) firmware assures interoperability.

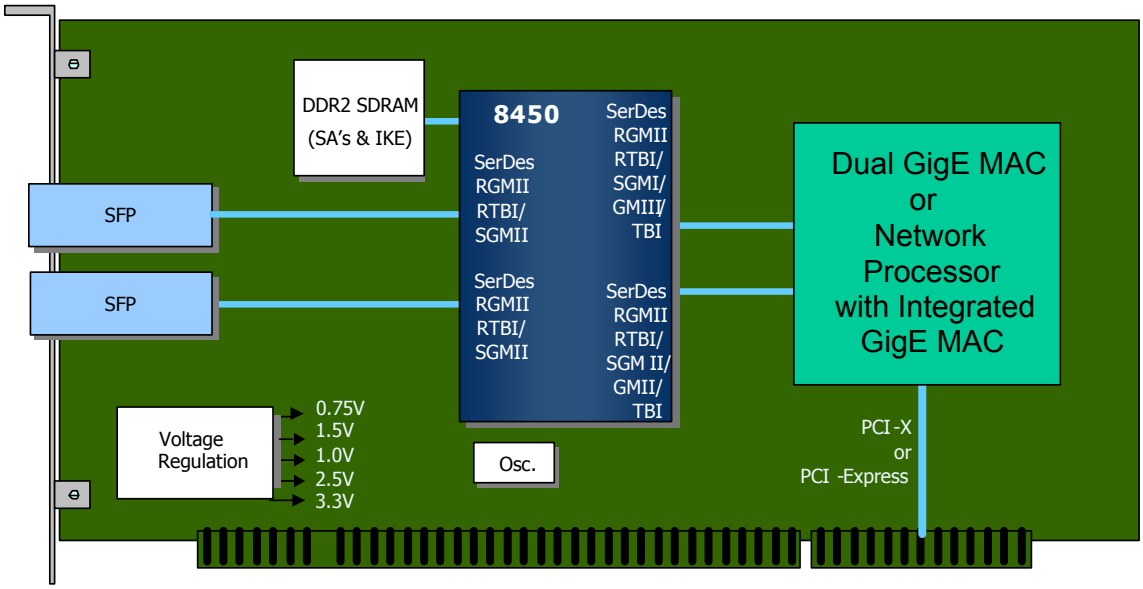


Figure 1-1. 8450 System Concept

The 8450 is typically interfaced between the Gigabit port on a GbE MAC, Network Processor, or Switch and the Gigabit Ethernet PHY. The 8450 supports two independent full-duplex gigabit Ethernet channels through four configurable GbE ports. The Host and Network GMII (Host Only), RGMII or SGMII interfaces can be configured to run at 10/100 speeds for applications only requiring 10/100 FE Compatibility. The control interface to the 8450 can be achieved using in-band Ethernet frames. An additional 100Mbps Ethernet RMII port allows an optional out-of-band control port. The 8450 also includes a single DDR2 SDRAM interface. The external memory can be used for storage of local SA records and/or for program and data storage for the on-board embedded Session Control (eSC) processor.

2 Features

2.1 All VPN Processing On-chip

- All IPsec and IPcomp processing occurs on chip; Host CPU not affected by VPN security
- Supports up to 256 on-chip policy entries (typically 128 per direction)
- Unlimited policy support via host-provided policy headers (EPP option)
- Up to 1,000,000 SA support via off-chip DDR2 SDRAM
- Optional IKE firmware available for execution in the on-chip eSC processor

2.2 High Performance

- Supports full duplex IPsec and IPcomp processing up to 4 Gbps data rates (2 Gbps full-duplex)
- Policy look-up, SA look-up, and secure packet processing at up to 700K packets per second (SDRAM enabled firmware)
- Performs all security processing through a single transit between host and network ports
- Integrated, enhanced public-key processor

For complete details about performance differences between algorithms and modes on the 8450 with the latest SDK firmware, please see *4450/8450 Performance Application Note,* AN-0168. The *4450/8450 Product Release Note,* RN-0118, for the SDK may also provide additional performance information.

2.3 Supports All Standard IPsec and IPcomp Modes & Algorithms

- IPsec in transport and tunnel modes: ESP with or without authentication enabled
- Full support for IPv4 and IPv6, including IPv4-in-IPv6 and IPv6-in-IPv4
- 128/256-bit AES (Advanced Encryption Standard) in CBC, CTR, GCM modes, DES/ 3DES in CBC mode
- SHA-1, SHA-256, MD5, (with HMAC) and AES-XCBC-MAC for authentication
- IP payload Compression (IPcomp) with LZS support
- Public-key support includes RSA, DSA, and Diffie-Hellmann
- Supports up to 8,192-bit modular arithmetic and exponentiation for public key operations (Note that the 4450/8450 Software Development Kit only supports 4,096-bit)

- True Hardware Random Number Generator

2.4 Supports Multiple Host Interfaces

- Four standard RGMII/RTBI/SGMII/SERDES interfaces (The Host-side interface can also support GMII/TBI. The four GMAC interfaces can optionally be configured for MII mode in 10/100 applications)
- Optional Out-of-Band Control interface via RMII interface for expandability, control, and configuration
- Compliant with IEEE 802.3 & IEEE 802.3z specifications
- Supports auto-negotiated 10/100/1000 Mbps data rates for GMII, RGMII and SGMII Interfaces. (TBI, RTBI and SERDES interfaces only support 1Gbps)
- Supports CSMA/CD (half-duplex) and IEEE 802.3x (full-duplex) flow control
- Supports 802.3Q VLAN tag detection for received frames
- Supports 802.3 jumbo frames (9022 bytes)
- Supports 802.3z bursting (half-duplex only)

2.5 On-chip Memory

- On-chip memory used for local SPD, SAD storage and packet buffering
- Reduces cost and board space when a limited number of secure tunnels is required

2.6 Software Support

- Software Development Kit (SDK)
- IPsec and IPcomp fast-path embedded firmware provided by Hifn and bootloaded into chip at power-up
- Optional IKE software fully integrated on chip
- Fragment reassembly (exception handling) may be performed on-chip in the eSC or off-chip in the host CPU, or Network Processor

2.7 Other Features

- Supports low-cost implementations with 324-pin HSBGA package
- On-chip PLL enables flexible low-cost external clock input
- IEEE 1149.1 JTAG support
- 1.0V core power with flexible I/O voltages.
- Typical power dissipation ~2.5W
- 0.13µ process

- RoHS Compliant Package
- Reference hardware design available

2.8 Ordering Information

Table 2-1. Ordering Information

Part Number	Speed	Package	Description
8450HA/3	200 MHz	324-ball HSBGA	8450 FlowThrough Security Processor
8450HA/3-K	200 MHz	324-ball HSBGA	8450 FlowThrough Security Processor with IKE option
8450HG/3	200 MHz	324-ball HSBGA RoHS Compliant	8450 FlowThrough Security Processor
8450HG/3-K	200 MHz	324-ball HSBGA RoHS Compliant	8450 FlowThrough Security Processor with IKE option

3 Performance Summary

This section summarizes the performance of the 8450 Security Processor functional units. For complete details about performance differences between algorithms and modes on the 8450 with the latest SDK firmware, please see *4450/8450 Performance Application Note,* AN-0168. The *4450/8450 Product Release Note,* RN-0118, for the SDK may also provide additional performance information.

The performance data reflects the following conditions:

- 200 MHz operating frequency
- Packets across single or multiple security associations
- Encoded text throughput

3.1 IPsec Protocol Performance

Table 3-1. Protocol Processing Performance

Protocol	Small-Packet Performance @ 200 MHz (Packets Per Second)	Large-Packet Performance @ 200 MHz (Gbps)
IPsec Tunnel Mode (AES-128 with SHA-1)	700 Kpps SDRAM firmware 900 Kpps NoSDRAM firmware	4.0 Gbps, 96% of line rate cleartext input
IPsec Transport Mode (AES-128 with SHA-1)	700 Kpps SDRAM firmware 900 Kpps NoSDRAM firmware	4.0 Gbps

Note

Performance numbers above represent an aggregate across both ports in full-duplex mode. Additional testing may cause the performance values in this table to be modified.

3.2 Public Key Performance

Table 3-2. Public Key Performance (200 MHz Operation)

8450 Operation at 200 MHz	Operations/second vs. Key Length (bits)			
	2048	1024	768	512
RSA private key	50	375	825	2,300
RSA public key (3-bit exponent)	1,175	2,000	6,800	12,400
Diffie-Hellman (180-bit exponent)	75	300	500	1,100
Diffie-Hellman (exponent = key size)	TBD	TBD	TBD	TBD
DSA sign	175	675	N/A	N/A
DSA verify	75	275	N/A	N/A

Note

1. Performance numbers assume a uniform distribution of ones and zeros in the exponent. Actual performance varies with the Hamming weight of the exponent.
2. Performance numbers assume that the public key module has unrestricted access to memory. Actual performance varies with the memory usage of other system components.
3. DSA sign/verify is normally only defined for a 1024-bit modulus.

4 8450 Operation

4.1 8450 Chip Architecture

The 8450 FlowThrough Security Processor contains several processing units comprising two major subsystems.

The "control path" subsystem contains the embedded Session Controller (eSC), Random Number Generator (RNG), the Public Key processor and an RMII interface for an out-of-band host control port or inter-chip communications in multi-chip applications. The eSC subsystem hosts the IKE protocol & exception handling and provides public key and RNG services.

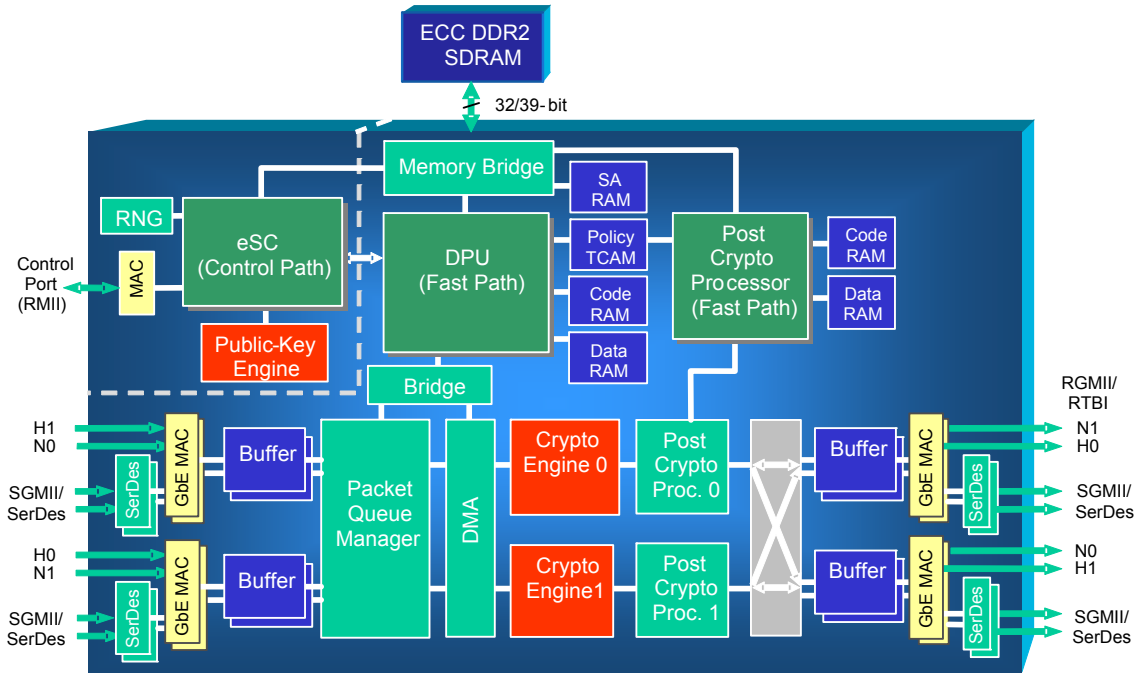


Figure 4-1. 8450 Block Diagram

The "fast data path" packet handling subsystem consists of all the blocks necessary for packet parsing and classification as well as the blocks to perform IPsec and IPcomp processing. Four full-duplex GbE MAC (Media Access Controller) cores provide the primary packet I/O. The packets are automatically moved through the crypto-processing pipeline via the Packet Queue Manager and DMA engines. The programmable DPU and PCP processors perform hardware-assisted packet policy look-up, SA look-up, and packet header and trailer processing.

4.2 8450 Packet Processing Operation

Inbound packets arrive over the network-side GMAC interface typically connected to the PHY device. The packet's payload is buffered and the DPU classifies the header as being IPsec and/or IPcomp and uses the SPI, protocol, destination address, ethernet interface, and VLAN ID to look-up the SA. Upon successful look-up, the DPU forwards the SA information along with the packet to the crypto algorithm processors. The DPU then performs the anti-replay check, and a post-crypto inbound policy check. The DPU then updates the SA with adjusted sequence numbers and packet/byte counters. The decoded packet is then egressed out the host GMAC port typically connected to the host subsystem.

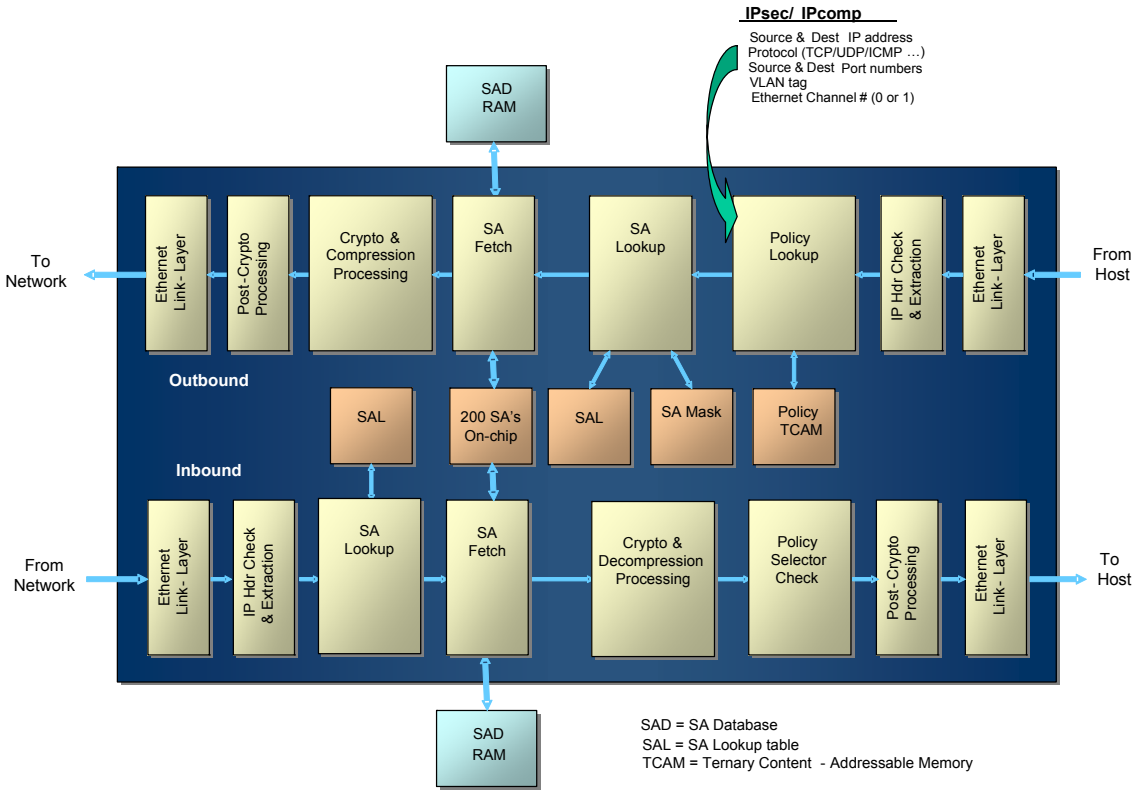


Figure 4-2. 8450 Processing Steps

Any errors in this process are captured to the eSC processor (or optionally the host) for statistics logging. Non-IPsec packets are checked against the SPD policy database and either discarded or forwarded to the host MAC port, depending on policy. IPsec packet fragments are forwarded to the host side MAC port for off-chip reassembly. The reassembled packets are then returned via the outbound MAC port with appropriate messaging, and re-inserted for inbound IPsec processing. Optionally, packet reassembly may occur on-chip in the eSC processor.

Outbound packets arrive over the Ethernet GMAC interface connected to the host-side media access (MAC) port. The packet's payload is buffered and the DPU performs a SPD policy look-up (based on the selectors defined for the security protocol), and then a SA look-up (based on the selectors defined for the security protocol), and checks the SA lifetime counters. The DPU also checks for exceptions and fragmentation. Upon successful

look-up, the DPU forwards the SA information along with the packet to the crypto algorithm processors. The DPU then updates the SA sequence number and counters. The encoded packet is then egressed out the Ethernet GMAC interface connected to the network-side physical device (PHY) port. Any errors in this process are captured to the eSC processor for statistics logging. Non-IPsec packets are checked against the SPD policy database and either discarded or forwarded to the network PHY port, depending on policy.

As noted above, reassembled packets received on the outbound host interface are processed as inbound and returned to the host-side interface.

Table 4-1. Description of the Primary Functional Units

Block	Description
eSC (embedded Session Controller)	The eSC controller performs the "control path" functions including IKE, SPD configuration, random number generation, optional packet reassembly handling, and exception handling.
DPU	The DPU performs "fast data path" functions including packet policy look-up, SAD look-up, IPsec header processing, and SA maintenance.
Crypto Processors	The crypto algorithm processors consist of a pipelined encryption, padding, and authentication engines, along with hardware for computing packet checksums. The crypto algorithm processors are configured by the DPU prior to the start of each packet or task.
Post Crypto Processor (PCP)	The Post-Crypto Processor handles packet header/trailer formatting and other "fast-path" functions after the packet has run through the Crypto Processor cores.
Public-Key Processor	The public-key processor provides hardware acceleration of public-key arithmetic computations. It supports modulus sizes of up to 8,192 bits.
Random Number Generator (RNG)	The 8450 contains a hardware true-random number generator. It is internally used to generate IKE keys.
Embedded SA Memory	The on-chip memory is used for the storage of up to 200 security associations. Note: The number of SA's supported on-chip may vary depending on the software release and the supported features. Please refer to Product Release Notes for additional information.
Embedded TCAM Memory	This on-chip Content Addressable Memory (CAM) is used for implementing efficient security policy and security association look-ups. Up to 256 policy entries are supported (generally 128 in each direction).
GMAC Cores	The 8450 supports four independent 1Gbps full-duplex Ethernet ports, two on the "network" side and two on the "host" side. The physical interfaces can either be RGMII/RTBI/SGMII/SERDES. The host side interfaces also optionally support GMII or TBI. Each GMAC port is internally connected to an inbound/outbound buffer. On the host side commands and unprocessed outbound packets are transferred from the host to the 8450, and inbound processed packets are transmitted to the host. On the network side outbound processed packets are transferred to the PHY device, and inbound unprocessed packets are received from the PHY device.
DDR2 SDRAM	The DDR2 SDRAM is required to store eSC program code/Data when running IKE on-chip or if it is necessary to support more than 200 SAs in a configuration.

4.3 Public Key Processing

The 8450 Public Key processing includes the eSC embedded processor and efficient Public Key acceleration hardware. To optimize the public key acceleration, the Public Key processor is equipped with dedicated OpCode-based exponentiation hardware. The Public Key processor operates on a batch of modular arithmetic instructions. Since each modular arithmetic instruction (nano instruction) execution is eSC independent, the eSC is only required to setup the Public Key engine with operands, issue instructions, and retrieve the result upon completion of Public Key processing.

4.4 Clock Domains

The 8450 has separate clock domains for the GMAC interfaces, the internal packet processing units, and the external SDRAM interfaces. The GMII/MII interfaces run at 125/25/2.5 MHz (corresponding to 1G, 100M or 10M interface speeds), the packet processing units run at 200MHz, and the SDRAM interfaces run at 200MHz.

The clock domains are controlled by a clock generation PLL, whose reference clock input is either single-ended (prefclk) or differential (srefclk_p, srefclk_n). When in Serdes or SGMII mode, the reference clock for the clock generation PLL must be the differential clock input driven at a frequency of 125MHz. When the Serdes/SGMII interface is not being used, the reference clock for the clock generation PLL is the single-ended clock input. The single-ended PLL reference input can be either 25MHz or 125MHz, selected by the **pll_mode**[1] select pin. With either input frequency, the appropriate clocks will be generated to support 10/100/1000 speeds assuming Serdes/SGMII mode is not selected. If Serdes (and/or TBI/RTBI) mode is selected for a given interface, operation is limited to 1G speed only for that interface.

5 Host Messaging and System Configuration

The 8450 supports in-band and out-of-band host messaging for the purpose of system boot and initialization, SPD & SAD management and exception handling, as well as IP packet fragment reassembly.

5.1 Gigabit Ethernet & RMII Host Interfaces

The two Host side Gigabit Ethernet Interfaces (host 0 and host 1) can be configured for either GMII/RGMII/SGMII/TBI/RTBI/SerDes signalling to accommodate data communications between the host based MAC and the 8450. The interface signally options for both host 0 and host 1 are configured to the same signalling option (i.e., GMII, RGMII, etc.) for each host port. The Gigabit Ethernet Interfaces may also be used for in-band 8450 to host communications. The 8450 supports an additional RMII interface that can be used for out-of-band host communications, messaging and management of the 8450. Figure 5-1 shows an example of the 8450 system connections.

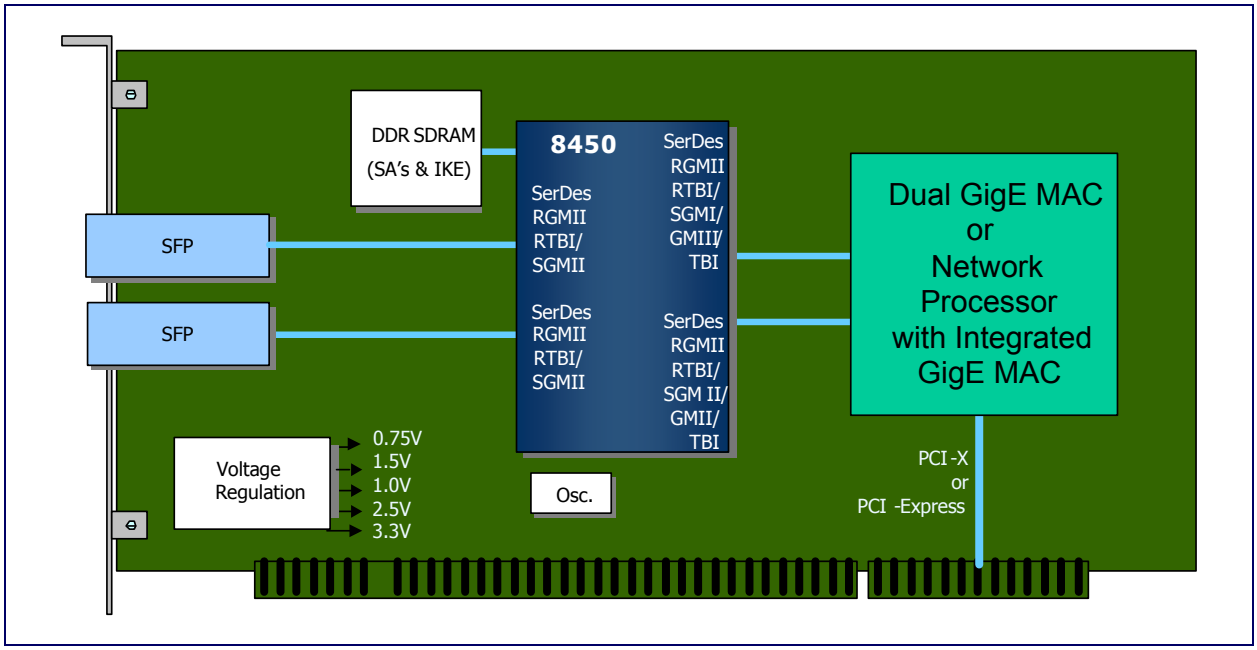


Figure 5-1. Example 8450 System Connection

5.2 8450 Host Messaging

The 8450 to host communications may be accomplished using in-band Ethernet frames. Command and status messages are encapsulated in a standard Ethernet frame using a unique Ethertype identifier (0x814F). Both the 8450 and host discriminate messages from data by using this special Ethertype identifier. The messages within the Ethernet frames are a Hifn-proprietary protocol designated PPCI (Packet Processing Command Interface).

As an alternative to in-band messaging, the host may also use the out-of-band RMII port for configuration and control. In this case, it is expected that the RMII port connects directly to a control processor, or through an Ethernet switch chip if multiple devices are being managed.

Note

The RMII port is not intended to be used across a network connection. It is to be used as a local management interface port only, similar to I^2C or PCI.

In either hardware connection, 8450-to-host communications are supported with a software hook placed in the low-level host 8450 device driver. Refer to the *44x0/84x0 User's Manual* for additional information.

5.3 Packet Fragmentation & Reassembly

Outbound IP packet fragmentation is handled inside the 8450. During outbound processing, the 8450 checks a per-flow MTU size and determines if IP fragmentation is required after crypto processing has completed. If required, the 8450 forms the IP headers for the fragmented IPsec packet, and forwards the IP fragments to the network port.

Inbound reassembly of fragmented packets (a.k.a. packet de-fragmentation) may be handled either by the eSC or in combination of 8450 and host-based software. If the implementation utilizes Hifn's optional IKE software package, then fragment reassembly can occur in the eSC. Otherwise, when the 8450 detects an inbound IP packet fragment, it will be encapsulated in a 8450-to-Host message Ethernet frame, and forwarded to the host. When the host determines that all fragments have been received and reassembled, the entire reassembled packet will be encapsulated and returned to the 8450 in an Ethernet message frame for inbound packet processing.

Packet fragmentation and reassembly are expensive operations on the 8450, as on most systems, and reliance on this functionality should be keep to a minimum through proper configuration of MTU sizes and Path MTU discovery (PMTU) where possible.

5.4 Security Policy and SA Database Management

The 8450 has internal facilities to support up to 256 security policies. These are created and managed via an API that communicates with the host-based user interface or to the optional embedded IKE implementation. The 8450 allows two security policy databases: one for inbound and one for outbound. The databases are an ordered list, and the actual policy lookup hardware resource is shared for inbound and outbound. It is the responsibility of the policy configuration software to allocate the entries so that the combined number does not exceed 256 entries.

The security association database (SAD) is initialized on power up, and typically maintained by the optional on-chip IKE firmware. For applications using host-based IKE, the host may directly inspect and modify both inbound and outbound SAD entries via the Hifn FlowThrough API. Refer to Hifn's *FlowThrough Application Programming Interface Programmer's Guide*, UG-0147, for more information on APIs.

5.5 Exception Handling

In the 8450, exceptions fall into three categories:

1. Packet Exceptions in the PPCI protocol (i.e. bad IP header, no SA for inbound packet, authentication failure)

2. Management Communications Exceptions in the PPCI protocol (i.e. No ACK received, out-of-sequence packet)

3. Chip Operation Exceptions (i.e. RAM parity error, bad Flash image, bad RNG etc.)

Generally, the Packet Exceptions are captured and processed by the IKE software. If IKE is running on-chip, then these exceptions are internally routed to the eSC processor and dealt with there. If IKE is running on the host system, then Packet Exceptions are encapsulated in a special Ethernet frame and forwarded to the host.

Management communications between the host system and the 8450 are carried over a proprietary protocol called PPCI (Packet Processing Command Interface). This protocol uses Ethernet frames with a Hifn Ethertype of 0x814F. Any exceptions that occur within this protocol are handled within the Hifn API code and PPCI handler through re-sends or higher-level software interaction.

Chip Operation Exceptions may be fatal (such as a memory parity error) where the chip is reset, or they may be recoverable with software intervention (such as a bad Flash image). Additional information on exception handling and the PPCI protocol is available in the *44x0/ 84x0 User's Manual.*

5.6 System Boot

The 8450's internal processors use a small pre-boot ROM image that is resident on the chip. These primitive instructions put the system into a state that searches for a boot source (either a local flash device or host interface) based on two configuration input pins. If no external flash is found, then the 8450 boot firmware enters a listening state, waiting for the boot message protocol over the host-side Gigabit Ethernet port 0 or the RMII port. The boot message protocol facilitates the rest of the boot code image downloading.

The boot code image can be located on the host, in an external Flash device, or on another 8450 device. Note that even if the device is configured to boot from Flash, a mechanism is still provided to boot from the host in order to allow initial Flash programming or to recover from a corrupted Flash. After the full image is downloaded, a complete system initialization is performed and the 8450 is ready to process data.

There are two pins that are sampled coming out of Reset and control the boot process, **dpu_gpio**[1]/***boot_config_1*** and **dpu_gpio**[0]/***boot_config_0***. These two pins are further defined in Section 6.7. Table 5-1 summarizes how these two pins are used to control the boot process.

If the ***boot_config_1*** pin is tied high it indicates that the 8450 has a Flash device connected. In order to boot from a Flash device, a minimal amount of SDRAM must be connected to the 8450. If ***boot_config_1*** is tied low it indicates that there is no Flash device connected to 8450, and the pre-boot code attempts to download boot code from one of the host Ethernet ports.

The ***boot_config_0*** pin indicates if downloading boot code from one of the host GMAC ports is permitted. This can be useful for FIPS 140-2 subsystem certification. If the ***boot_config_1*** pin is pulled low, then booting from one of the host GMAC ports is allowed. If ***boot_config_0*** pin is pulled high, then booting from the host 0 or host 1 GMAC port is not allowed.

The eSC processor first looks at the ***boot_config_1*** pin to see if a Flash is present. Then the DPU will look at ***boot_config_0*** to see if listening to the host GMAC ports is allowed. If there is no flash device (***boot_config_1*** = 0) or the flash boot fails, and listening to the host port times out (eSC listening to RMII port and DPU listening to host ports), then the eSC and DPU will each listen to each other for booting across the inter-connect bus used for inter-processor communication.

Table 5-1. Boot Process Summary

dpu_gpio[1]/ *boot_config_1*	dpu_gpio[0] / *boot_config_0*	DPU Boots from:	eSC Boots from:	Comments
0	0	Host 0/1 GMAC or eSC inter-connect bus	RMII port or DPU inter-connect bus	Normal system No flash
0	1	eSC inter-connect bus only (No GMAC)	RMII port.	FIPS-140 secure system boot[1] No flash
1	0	Flash Fail to Host GMAC or eSC	Flash. Fail to DPU or RMII	Normal system With flash[2]
1	1	Flash Fail to eSC Only (No Host GMAC boot)	Flash Fail to DPU or RMII	FIPS-140 secure system boot[1] With flash[2]

Note

1. A secure system boot is referring to a design where it is required to carefully control where the bootload software image comes from (such as in a FIPS-140 design). In such a system, a design may utilize a secure control processor attached to the RMII port for bootload and device management. These boot pin settings will not allow a boot image to be delivered over the GMAC host (or network) ports. Contact Hifn for availability of software support for this feature.

2. The SDRAM must be populated.

For full details on the software boot load process, refer to the *44x0/84x0 User's Manual*.

6 Signal Description

6.1 Signal Overview

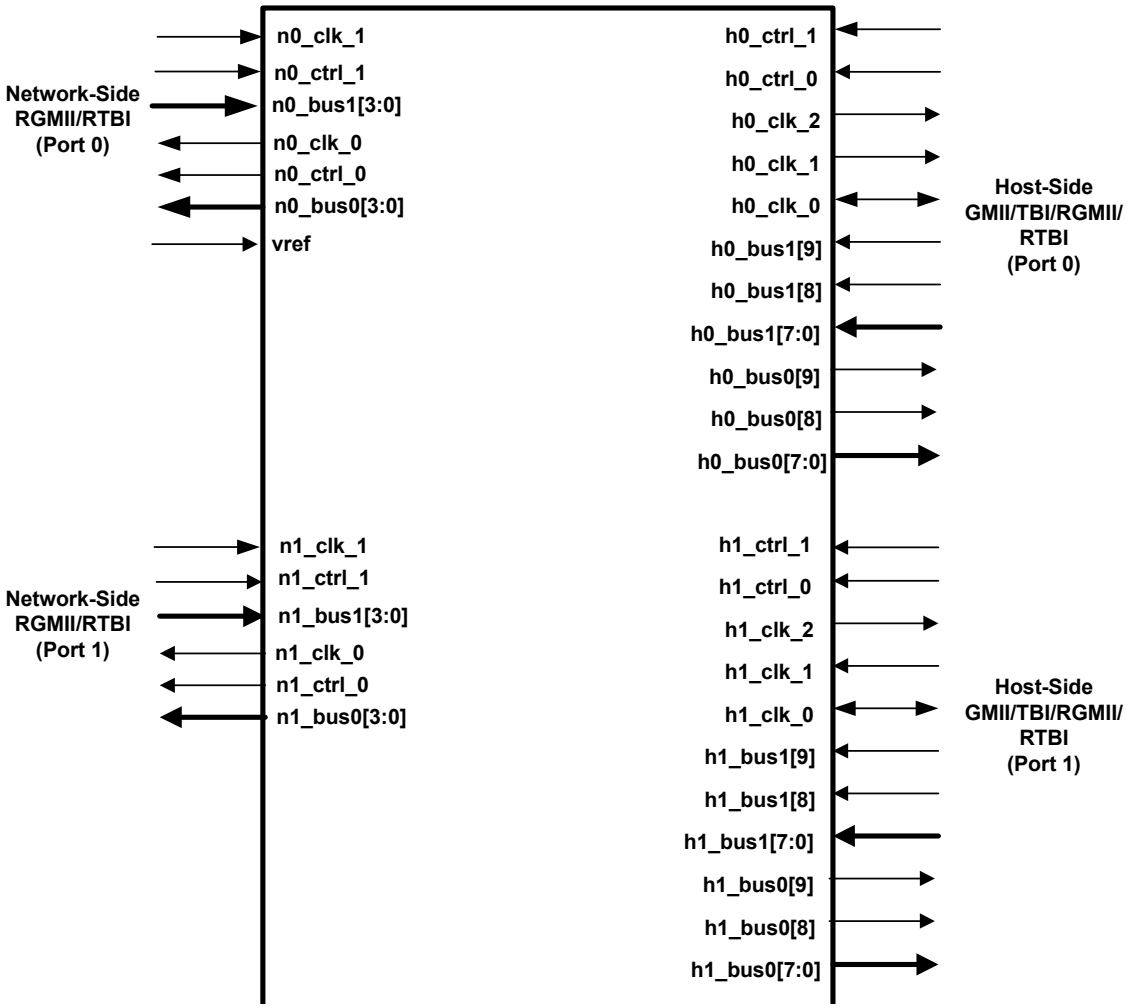


Figure 6-1. 8450 I/O Signals (First half of drawing)

Note

Depending on Ethernet interface configuration mode selected (Section 6.2), not all of the interface pins may be used. Refer to the specific diagrams in the appropriate sections below (Section 6.2.1 - 6.2.3).

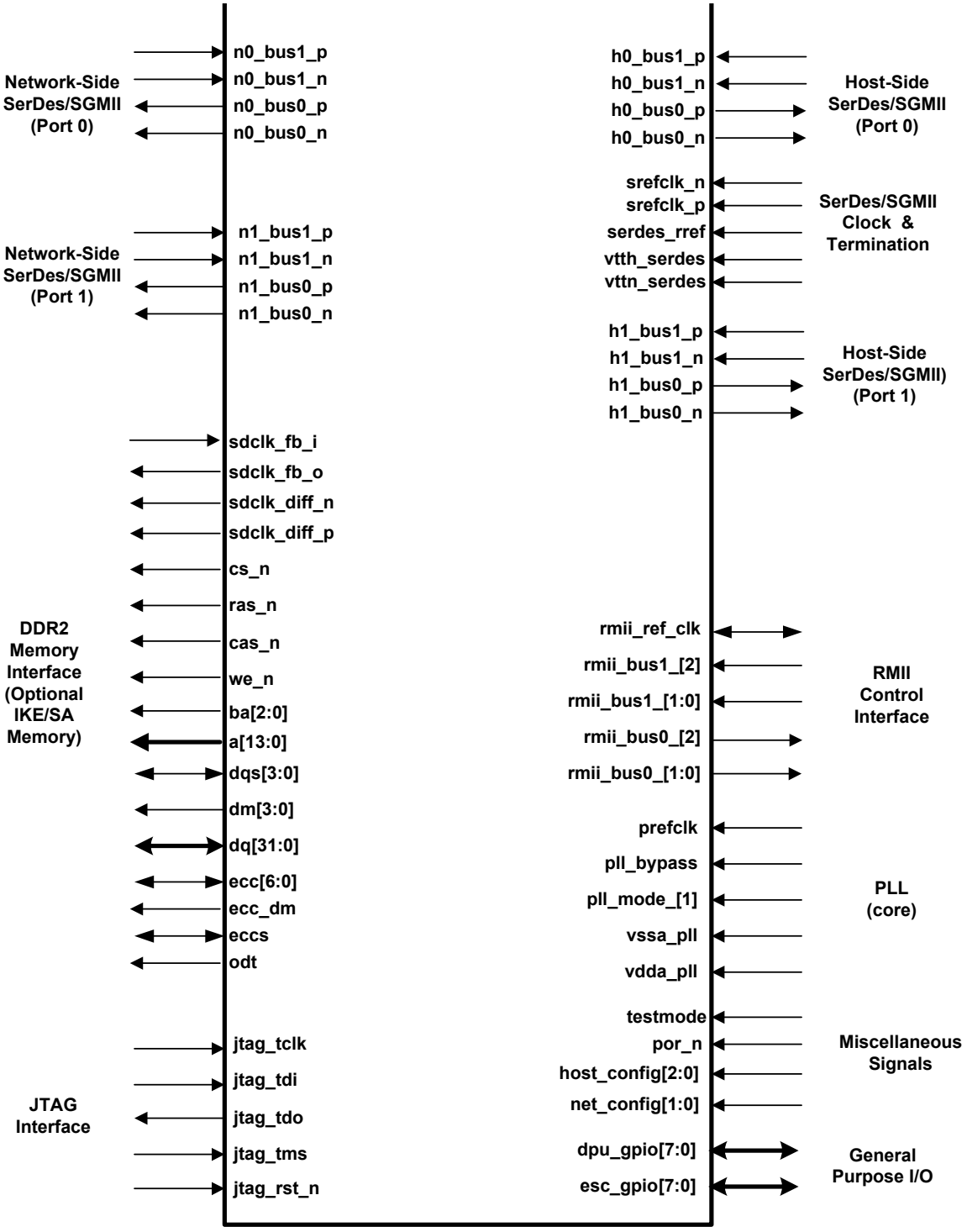


Figure 6-2. 8450 I/O Signals (Second half of drawing)

6.2 Ethernet Interfaces Signal Description

The 8450 is normally located in a system between a copper or fiber PHY and a Host's GMAC. The network side of the 8450 functions like a MAC device and the host side functions like a PHY. The host side interface provides six separate electrical signalling options which include: GMII/TBI, RGMII/RTBI, SGMII, and SERDES. For the network side interfaces, only RGMII/RTBI, SGMII and SERDES signalling options are available. GMII/TBI signalling is not supported on the network side. The GMAC interfaces are capable of running at 10/100/1000 speeds in either the GMII, RGMII or SGMII modes. The TBI, RTBI and SERDES interfaces only support 1 Gbps speeds and will not run at 10/100 speeds. Note that the 8450 is not designed to operate in asymmetric rate scenarios where for example the host side is running at 1 Gbps and the network side at 10 Mbps.

Three configuration pins, **host_config[2:0]** are provided to select one of eight operating configurations for the Host GMAC interfaces. The **net_config[1:0]** pins select one of four operating configurations for the Network GMAC Interfaces. See Table 6-1 and Table 6-2 for details on the GMAC Interface configurations.

Table 6-1. HOST Interface Modes

host_config[2:0]	Host Interfaces	MAC/PHY
000	RGMII	MAC or PHY
001	RTBI	MAC or PHY
010	SGMII	MAC or PHY
011	SerDes	MAC or PHY
100	GMII	MAC
101	GMII	PHY
110	TBI	MAC
111	TBI	PHY

Table 6-2. Network Interface Modes

net_config[1:0]	Network Interfaces	MAC/PHY
00	RGMII	MAC or PHY
01	RTBI	MAC or PHY
10	SGMII	MAC or PHY
11	SerDes	MAC or PHY

6.2.1 GMAC GMII/TBI Interface Usage (Host-side Only)

This section discusses the use of the Host Side GMAC interfaces h0 and h1 when configured to support operation in GMII or TBI modes.

6.2.1.1 GMAC GMII/TBI Pin Mappings (Host-side Only)

Table 6-3 contains five columns for the signal names and mapping for GMII and TBI mode. The leftmost column contains the 8450 pin name, and the next four columns contain the functional signal name, based on whether the port is defined as GMII or TBI, and whether the port functions as a MAC or a PHY device. For each port, Table 6-3 maps the 8450 pin names to the signal functions depending on the settings of the **host_config[2:0]** pins illustrated in Table 6-1.

Please note in Table 6-3 that the directions of the data and control signals associated with the terms "receive" and "transmit" depend on whether the port is a MAC or a PHY. For example, "receive" relates to data and control signals that are outputs on the PHY and inputs on the MAC. And "transmit" relates to data and control signals that are inputs on the PHY and outputs on the MAC. For the clocks, in MII mode both receive and transmit clocks are PHY driven. In GMII mode, the receive and transmit clocks are source driven. In TBI mode, the two receive clocks are shared with the MII receive and transmit clocks, which are both PHY driven; and the TBI transmit clock is shared with the GMII transmit clock.

In addition to the four GMII/TBI operating modes for each host port, there are two ports indicated by "hx_" in Table 6-3, host-side port 0 ("hx" = "h0"), and host-side port 1 ("hx" = "h1").

Table 6-3. 8450 GMII/TBI MAC/PHY modes pin mappings (Host Side Only)

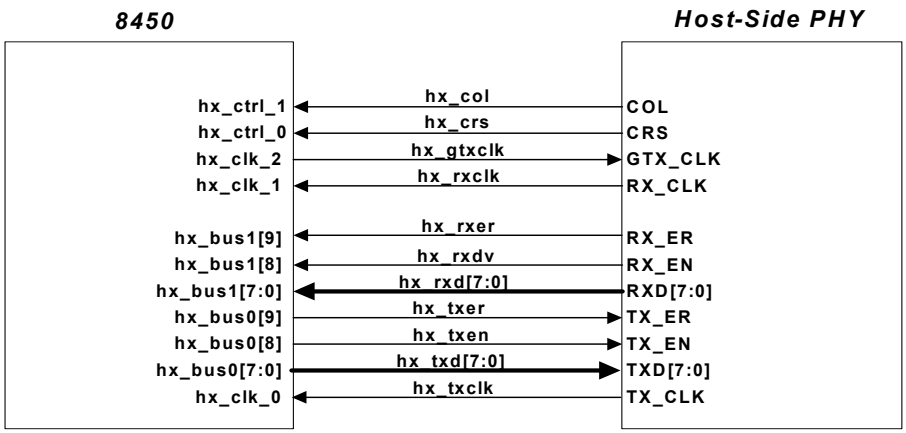
Pin Name	MAC-GMII		MAC-TBI		PHY-GMII		PHY-TBI	
	GMII Signal	I/O	TBI Signal	I/O	GMII Signal	I/O	TBI Signal	I/O
hx_ctrl_1	hx_col	in	n/a	in	hx_col	NC	n/a	NC
hx_ctrl_0	hx_crs	in	hx_sigdet	in	hx_crs	NC	hx_sigdet	NC
hx_clk_2	hx_gtxclk	out	hx_txpmaclk	out	hx_rxclk	out	hx_rxpmaclk	out
hx_clk_1	hx_rxclk	in	hx_rxpmaclk1	in	hx_gtxclk	in	hx_txpmaclk	in
hx_clk_0	hx_txclk	in	hx_rxpmaclk0	in	hx_txclk	out	hx_rxpmaclk0	out
hx_bus1[9}	hx_rxer	in	hx_rxd9	in	hx_txer	in	hx_txd9	in
hx_bus1[8}	hx_rxdv	in	hx_rxd8	in	hx_txen	in	hx_txd8	in
hx_bus1_[7:0]	hx_rxd[7:0]	in	hx_rxd[7:0]	in	hx_txd[7:0]	in	hx_txd[7:0]	in
hx_bus0[9}	hx_txer	out	hx_txd9	out	hx_rxer	out	hx_rxd9	out
hx_bus0[8]	hx_txen	out	hx_txd8	out	hx_rxdv	out	hx_rxd8	out
hx_bus0[7:0]	hx_txd[7:0]	out	hx_txd[7:0]	out	hx_rxd[7:0]	out	hx_rxd[7:0]	out

Note

hx = h0 or h1

Table 6-6 provides the functional signal names and mapping for the Network and Host ports if it is desired to run in RGMII/RTBI mode.

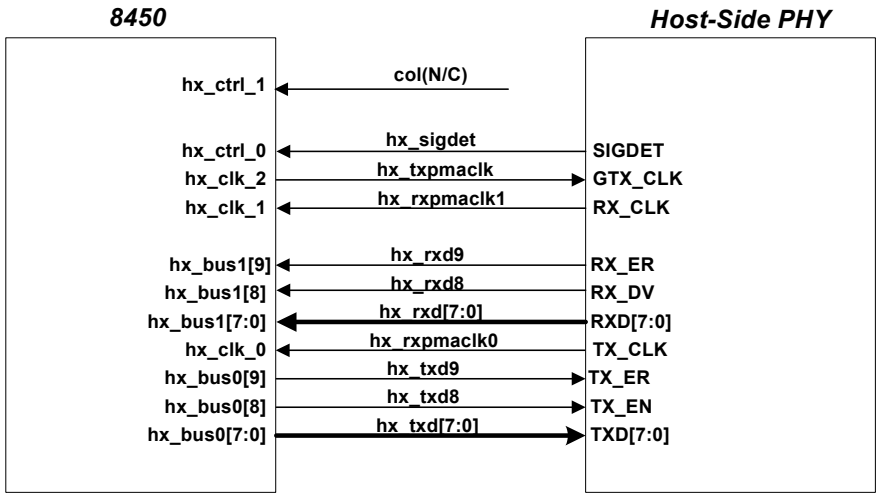
6.2.1.2 GMAC GMII/TBI Connection Diagrams (Host-side only)



Note

1. hx = h0 or h1.

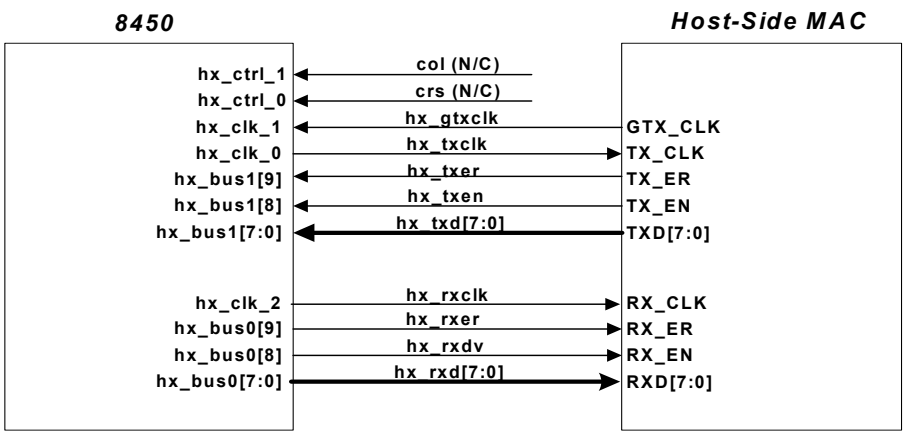
Figure 6-3. GMII MAC-Mode



Note

1. hx = h0 or h1.
2. col is internally terminated with a pulldown resistor.

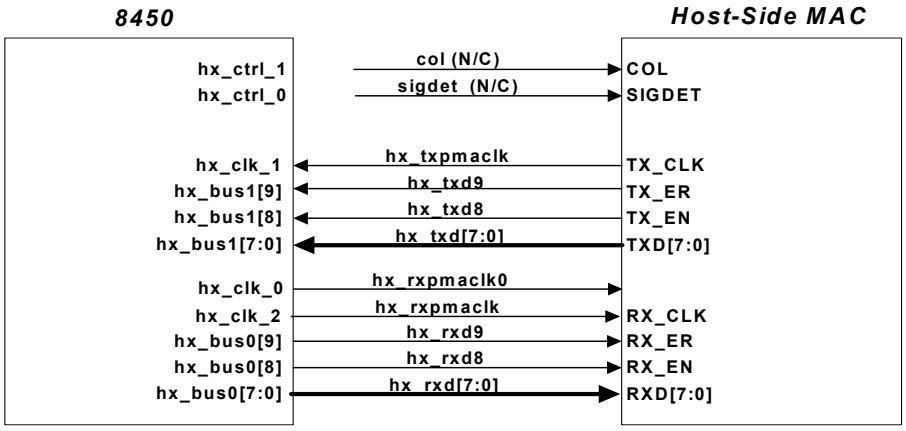
Figure 6-4. TBI MAC-Mode



Note

1. hx = h0 or h1.
2. col and crs are internally terminated with a pulldown resistor.

Figure 6-5. GMII PHY-Mode



Note

1. hx = h0 or h1.
2. col and sigdet are internally terminated by the 8450 and NOT DRIVEN by the 8450. col and sigdet may need termination on the MAC side.

Figure 6-6. TBI PHY-Mode

6.2.1.3 GMAC GMII/TBI Pin Descriptions (Host-side Only)

Table 6-4 contains the pin descriptions for either the host ports when configured in MAC mode.

Table 6-4. 8450 GMII/TBI pin descriptions - MAC mode (Host Only)

Pin Name	GMII/TBI Signal	I/O	Description
hx_ctrl_1	col	in	Collision Detect: asserted high asynchronously by PHY upon detection of a collision on the medium. Remains asserted as long as the collision condition persists. Only used with half-duplex connections. This signal must either be connected to the PHY or tied high.
hx_ctrl_0	GMII: crs; TBI: sigdet	in	Carrier Sense: asserted high asynchronously by the external PHY upon detection of a non-idle medium. In TBI mode, this signals PHY signal detection This signal must be asserted high for normal operation, and must either be connected to the PHY or tied high.
hx_clk_2	GMII: gtx_clk TBI: txpma_clk	out	In GMII mode, transmit data clock: sourced by the 8450 as a reference clock for transmitted data. Clock is 125MHz for GbE. In TBI mode, 125MHz reference for TX_DAT bus data.
hx_clk_1	GMII: rx_clk TBI: rx_pma_clk_1	in	In GMII mode, receive data clock: sourced by the PHY from recovered clock from incoming data. Clock is 125MHz for GbE, 25MHz for 100FE, 2.5MHz for 10Mb Ethernet. In TBI mode, receive PMA clock 1, 62.5MHz, clocking odd bytes from TBI interface on the rising edge of clock.
hx_clk_0	GMII: tx_clk TBI: rx_pma_clk_0	in	In GMII mode, transmit data clock: sourced by the PHY as a reference clock for transmitted data. Clock is 25MHz for 100FE, 2.5MHz for 10Mb Ethernet. In TBI mode, receive PMA clock 0, 62.5MHz, clocking even bytes from TBI interface on the rising edge of clock.
hx_bus1[9]	GMII: rx_er TBI: rx_dat[9]	in	In GMII mode, asserted high by the PHY if a media error is detected.In TBI mode, additional receive input. Used with other RX_DAT inputs to form ten bit bus RX_DAT[9:0].
hx_bus1[8]	GMII: rx_dv TBI: rx_dat[8]	in	In GMII mode, receive data valid: driven high by PHY to indicate valid recovered data on RX_DAT bus. In TBI mode, additional receive input. Used with other RX_DAT inputs to form ten bit bus RX_DAT[9:0].
hx_bus1[7:0]	rx_dat[7:0]	in	Receive data for GbE. Only RX_DAT[3:0] used for 10/100FE(MII mode.

Table 6-4. 8450 GMII/TBI pin descriptions - MAC mode (Host Only)

Pin Name	GMII/TBI Signal	I/O	Description
hx_bus0[9]	GMII: tx_er TBI: tx_dat[9]	out	In GMII mode, asserted high by the 8450 if a transmit error is detected. In TBI mode, additional transmit output. Used with other TX_DAT outputs to form ten bit bus TX_DAT[9:0].
hx_bus0[8]	GMII: tx_en TBI: tx_dat[8]	out	In GMII mode, valid transmit data driven high by 8450 on TX_DAT bus. In TBI mode, additional transmit output. Used with other TX_DAT outputs to form ten bit bus TX_DAT[9:0].
hx_bus0[7:0]	tx_dat[7:0]	out	Transmit data for GbE: Only TX_DAT[3:0] used for 10/100FE (MII mode.
Note hx = h0 or h1			

Table 6-5 contains the pin descriptions for either the host ports when configured in PHY mode.

Table 6-5. 8450 GMII/TBI pin descriptions - PHY mode (Host Only)

Pin Name	GMII/TBI Signal	I/O	Description
hx_ctrl_1	col	N/C	This input should not be connected in this (PHY) mode.
hx_ctrl_0	GMII: crs TBI: sigdet	N/C	This input should not be connected in this (PHY) mode.
hx_clk_2	GMII: rx_clk TBI: rx_pma_clk_1	out	In GMII mode, receive data clock: sourced by the PHY from recovered clock from incoming data. Clock is 125MHz for GbE, 25MHz for 100FE, 2.5MHz for 10Mb Ethernet. In TBI mode, receive PMA clock 1, 62.5MHz, clocking odd bytes from TBI interface on the rising edge of clock.
hx_clk_1	GMII: gtx_clk TBI: txpma_clk	in	In GMII mode, transmit data clock: sourced by the remove device as a reference clock for transmitted data. Clock is 125MHz for GbE. In TBI mode, 125MHz reference for TX_DAT bus data.
hx_clk_0	GMII: tx_clk TBI: rx_pma_clk_0	in	In GMII mode, transmit data clock: sourced by the PHY as a reference clock for transmitted data. Clock is 25MHz for 100FE, 2.5MHz for 10Mb Ethernet. In TBI mode, receive PMA clock 0, 62.5MHz, clocking even bytes from TBI interface on the rising edge of clock.
hx_bus1[9]	GMII: tx_er TBI: tx_dat[9]	in	In GMII mode, asserted high by the remove device if a transmit error is detected. In TBI mode, additional transmit output. Used with other TX_DAT outputs to form ten bit bus TX_DAT[9:0].

Table 6-5. 8450 GMII/TBI pin descriptions - PHY mode (Host Only)

Pin Name	GMII/TBI Signal	I/O	Description
hx_bus1[8]	GMII: tx_dv TBI: tx_dat[8]	in	In GMII mode, valid transmit data driven high by remote device on TX_DAT bus. In TBI mode, additional transmit output. Used with other TX_DAT outputs to form ten bit bus TX_DAT[9:0].
hx_bus1[7:0]	tx_dat[7:0]	in	Transmit data for GbE. Only TX_DAT[3:0] used for 10/100FE(MII mode.
hx_bus0[9]	GMII: tx_er TBI: tx_dat[9]	out	In GMII mode, asserted high by the PHY if a media error is detected. In TBI mode, additional receive input. Used with other RX_DAT inputs to form ten bit bus RX_DAT[9:0].
xhx_bus0[8]	GMII: rx_dv TBI: rx_dat[8]	out	In GMII mode, receive data valid: driven high by PHY to indicate valid recovered data on RX_DAT bus. In TBI mode, additional receive input. Used with other RX_DAT inputs to form ten bit bus RX_DAT[9:0].
hx_bus0[7:0]	rx_dat[7:0]	out	Receive data for GbE. Only RX_DAT[3:0] used for 10/100FE(MII mode.

Note

hx = h0 or h1

6.2.2 Host GMAC RGMII/RTBI Interface Usage

This section discusses the use of GMAC interfaces for the host side interfaces h0 or h1 when configured to support operation in RGMII or RTBI modes.

6.2.2.1 Host GMAC RGMII/RTBI Pin Mappings

Table 6-6. 8450 RGMII/RTBI MAC/PHY modes Host pin mappings

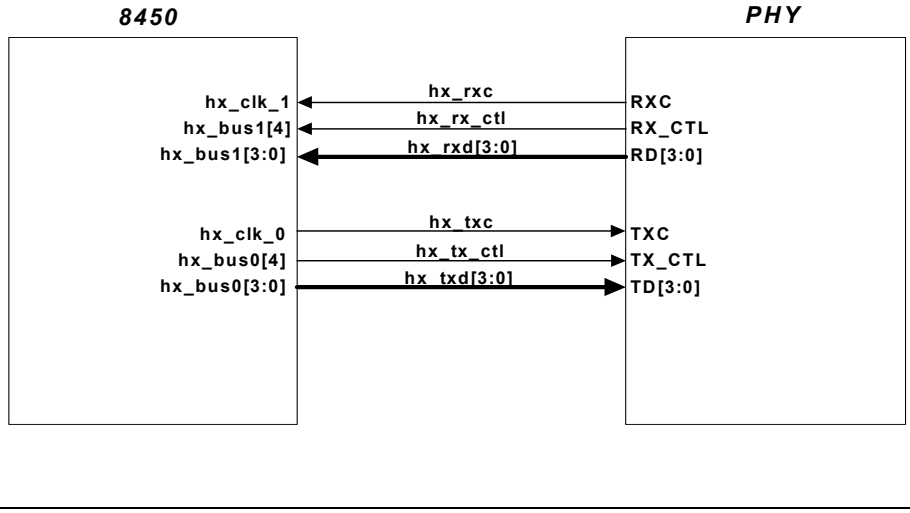
Pin Name	MAC-RGMII		MAC-RTBI		PHY-RGMII		PHY-RTBI	
	RGMII Signal	I/O	RTBI Signal	I/O	RGMII Signal	I/O	RTBI Signal	I/O
hx_clk_1	hx_rxc	in	hx_rxc	in	hx_txc	in	hx_txc	in
hx_bus1[4]	hx_rx_ctl	in	hx_rxd[4]	in	hx_tx_ctl	in	hx_txd[4]	in
hx_bus1[3:0]	hx_rxd[3:0]	in	hx_rxd[3:0]	in	hx_txd[3:0]	in	hx_txd[3:0]	in
hx_clk_0	hx_txc	out	hx_txc	out	hx_rxc	out	hx_rxc	out
hx_bus0[4]	hx_tx_ctl	out	hx_txd[4]	out	hx_rx_ctl	out	hx_rxd[4]	out
hx_bus0[3:0]	hx_txd[3:0]	out	hx_txd[3:0]	out	hx_rxd[3:0]	out	hx_rxd[3:0]	out

Note

hx = h0 or h1

Table 6-12 provides the functional signal names and mapping for the Host ports if it is desired to run in SERDES mode.

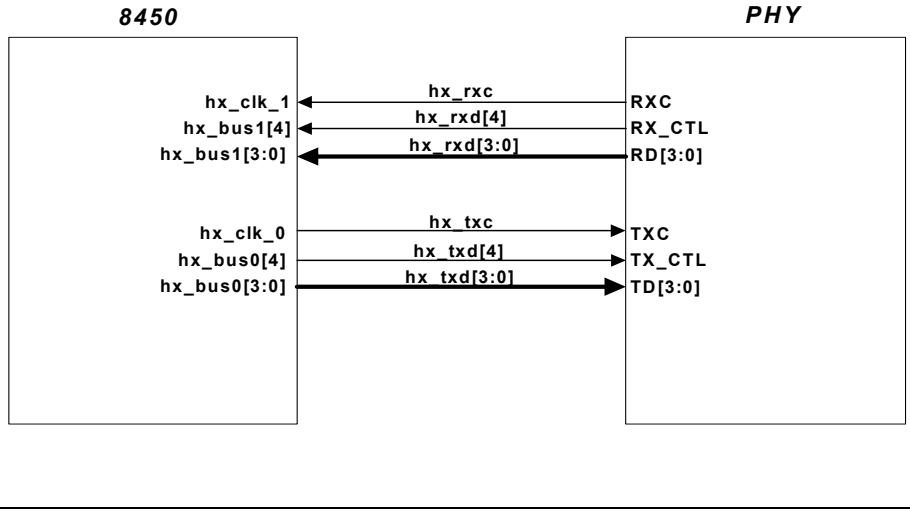
6.2.2.2 Host GMAC RGMII/RTBI Connection Diagrams



Note

1. hx = h0 or h1.

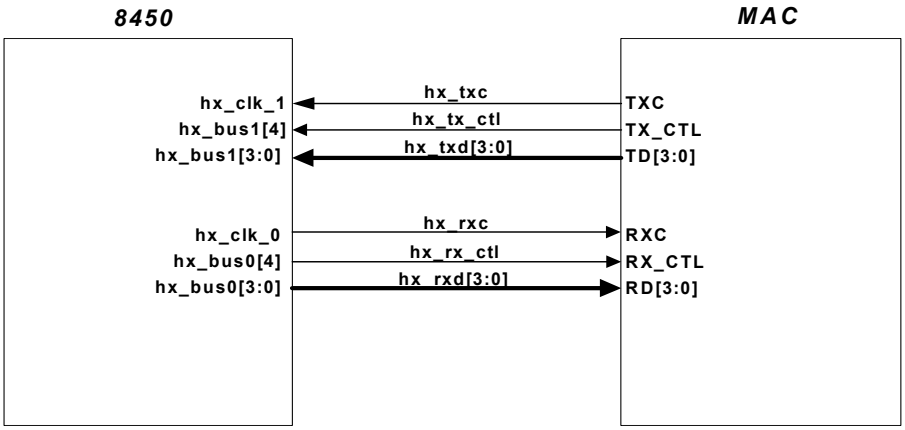
Figure 6-7. Host RGMII MAC-Mode



Note

1. hx = h0 or h1.

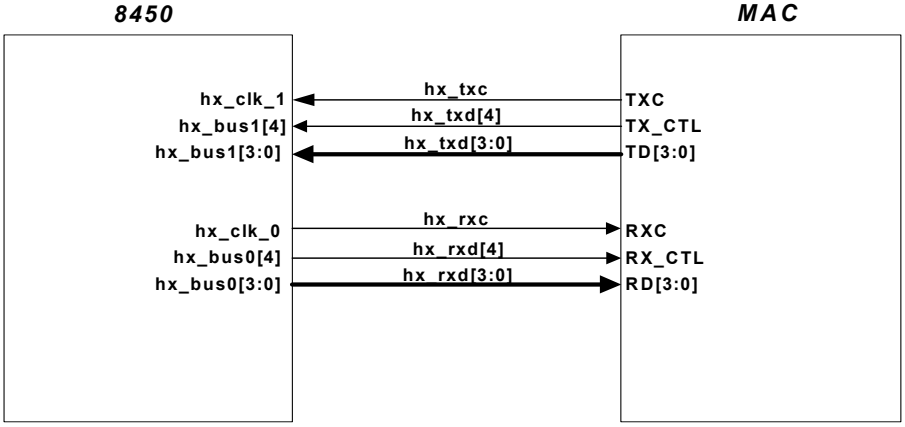
Figure 6-8. Host RTBI MAC-Mode



Note

1. hx = h0 or h1.

Figure 6-9. Host RGMII PHY-Mode



Note

1. hx = h0 or h1.

Figure 6-10. Host RTBI PHY-Mode

6.2.2.3 Host GMAC RGMII/RTBI Pin Descriptions

Table 6-7 contains the pin descriptions for the RGMII/RTBI host interface ports when configured in MAC mode.

Table 6-7. 8450 RGMII/RTBI Host pin descriptions - MAC mode

Pin Name	RGMII/RTBI Signal	I/O	Description
hx_clk_1	hx_rxc	in	The receive reference clock will be 125MHz, 25MHz or 2.5MHz.
hx_bus1[4]	RGMII: hx_rx_ctl RTBI: hx_rxd[4]	in	In RTBI mode, contains the fifth bit on the rising edge of rxc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv (i.e. rxdv XOR rxerr) on the falling edge of rxc.
hx_bus1[3:0]	hx_rxd[3:0]	in	In RTBI mode, contains bits [3:0] on the rising edge of rxc and bits [8:5] on the falling edge of rxc. In RGMII mode, bit [3:0] on rising edge of rxc, bits [7:4] on the falling edge of rxc.
hx_clk_0	hx_txc	out	The transmit reference clock will be 125MHz, 25MHz or 2.5MHz.
hx_bus0[4]	RGMII: hx_tx_ctl RTBI: hx_txd[4]	out	In RTBI mode, contains the fifth bit on the rising edge of txc and the tenth bit on the falling edge of rxc. In RGMII mode, txdv on the rising edge of txc and a logical derivative of txdv (i.e., txdv XOR txerr) on the falling edge of txc.
hx_bus0[3:0]	hx_txd[3:0]	out	In RTBI mode, contains bits [3:0] on the rising edge of txc and bits [8:5] on the falling edge of txc. In RGMII mode, bit [3:0] on rising edge of txc, bits [7:4] on the falling edge of txc.
Note hx = h0 or h1			

Table 6-8 contains the pin descriptions for the RGMII/RTBI host interface port when configured in PHY mode.

Table 6-8. 8450 RGMII/RTBI Host pin descriptions - PHY mode

Pin Name	RGMII/RTBI Signal	I/O	Description
hx_clk_1	hx_txc	in	The receive reference clock will be 125MHz, 25MHz or 2.5MHz.
hx_bus1[4]	RGMII: hx_tx_ctl RTBI: hx_txd[4]	in	In RTBI mode, contains the fifth bit on the rising edge of rxc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv (i.e., rxdv XOR rxerr) on the falling edge of rxc.
hx_bus1[3:0]	hx_txd[3:0]	in	In RTBI mode, contains bits [3:0] on the rising edge of rxc and bits [8:5] on the falling edge of rxc. In RGMII mode, bit [3:0] on rising edge of rxc, bits [7:4] on the falling edge of rxc.
hx_clk_0	hx_rxc	out	The transmit reference clock will be 125MHz, 25MHz or 2.5MHz.
hx_bus0[4]	RGMII: hx_rx_ctl RTBI: hx_rxd[4]	out	In RTBI mode, contains the fifth bit on the rising edge of txc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv(rxdv XOR rxerr) on the falling edge of rxc.
hx_bus0[3:0]	hx_rxd[3:0]	out	In RTBI mode, contains bits [3:0] on the rising edge of txc and bits [8:5] on the falling edge of txc. In RGMII mode, bit [3:0] on rising edge of txc, bits [7:4] on the falling edge of txc.
Note hx = h0 or h1			

6.2.3 Network GMAC RGMII/RTBI Interface Usage

This section discusses the use of GMAC interfaces for the network side interfaces n0 or n1 when configured to support operation in RGMII or RTBI modes.

6.2.3.1 Network GMAC RGMII/RTBI Pin Mappings

Table 6-9. 8450 RGMII/RTBI MAC/PHY modes Network pin mappings

Pin Name	MAC-RGMII		MAC-RTBI		PHY-RGMII		PHY-RTBI	
	RGMII Signal	I/O	RTBI Signal	I/O	RGMII Signal	I/O	RTBI Signal	I/O
nx_clk_1	nx_rxc	in	nx_rxc	in	nx_txc	in	nx_txc	in
nx_ctrl_1	nx_rx_ctl	in	nx_rxd[4]	in	nx_tx_ctl	in	nx_txd[4]	in
nx_bus1[3:0]	nx_rxd[3:0]	in	nx_rxd[3:0]	in	nx_txd[3:0]	in	nx_txd[3:0]	in
nx_clk_0	nx_txc	out	nx_txc	out	nx_rxc	out	nx_rxc	out

Table 6-9. 8450 RGMII/RTBI MAC/PHY modes Network pin mappings

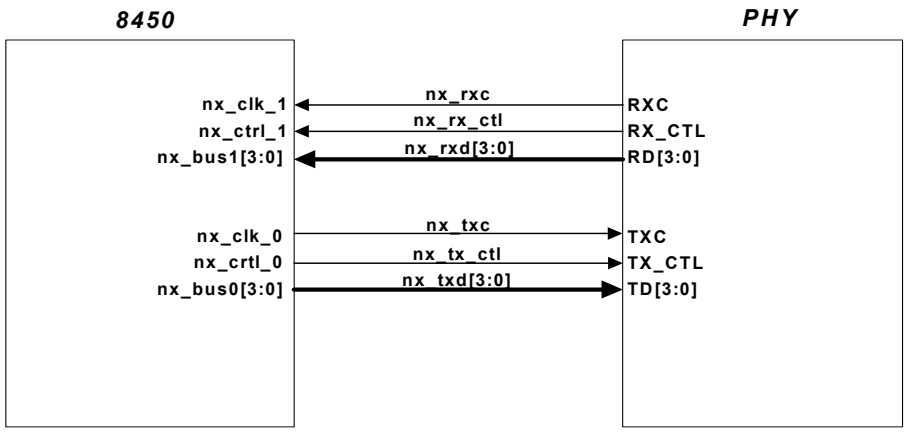
Pin Name	MAC-RGMII		MAC-RTBI		PHY-RGMII		PHY-RTBI	
	RGMII Signal	I/O	RTBI Signal	I/O	RGMII Signal	I/O	RTBI Signal	I/O
nx_ctrl_0	nx_tx_ctl	out	nx_txd[4]	out	nx_rx_ctl	out	nx_rxd[4]	out
nx_bus0[3:0]	nx_txd[3:0]	out	nx_txd[3:0]	out	nx_rxd[3:0]	out	nx_rxd[3:0]	out

Note

nx = n0 or n1

Table 6-12 provides the functional signal names and mapping for the Network ports if it is desired to run in SERDES mode.

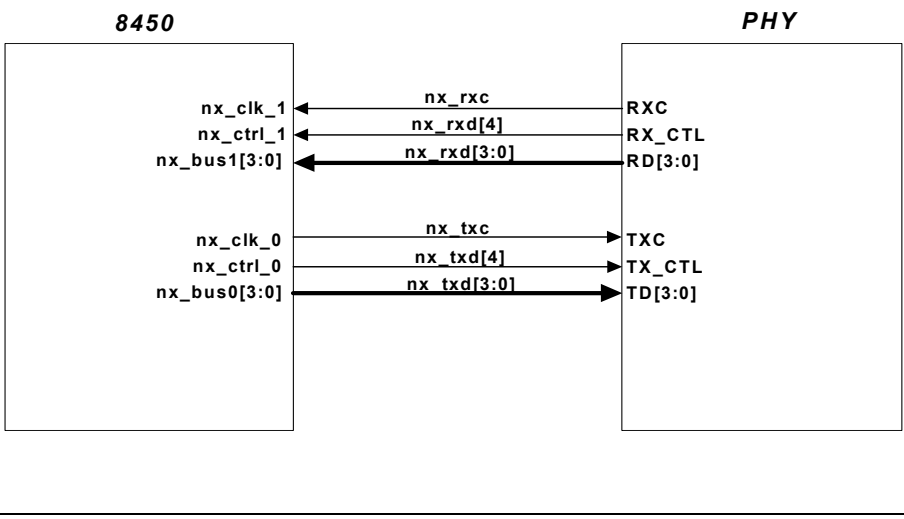
6.2.3.2 Network GMAC RGMII/RTBI Connection Diagrams



Note

1. nx = n0 or n1.

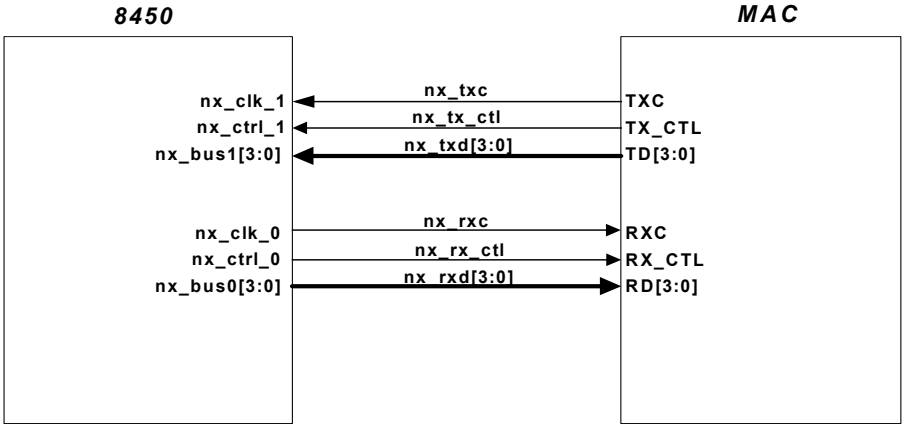
Figure 6-11. Network RGMII MAC-Mode



Note

1. nx = n0 or n1.

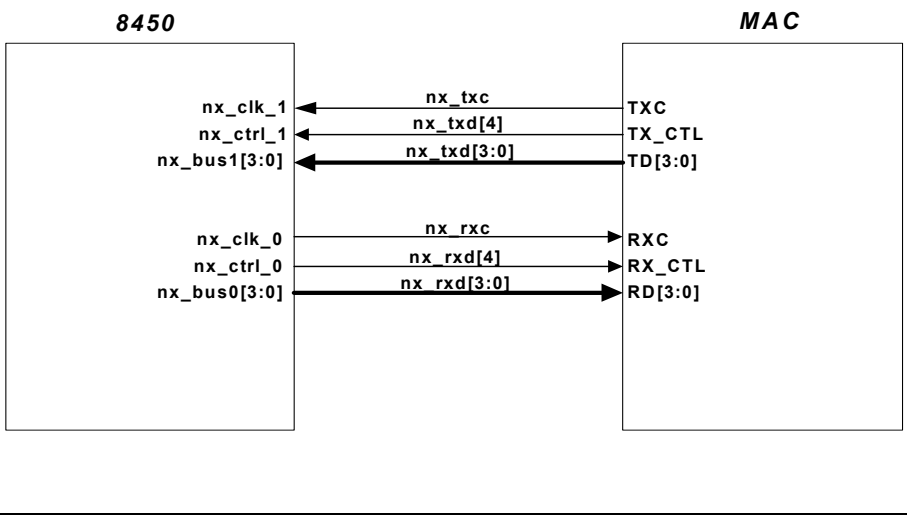
Figure 6-12. Network RTBI MAC-Mode



Note

1. nx = n0 or n1.

Figure 6-13. Network RGMII PHY-Mode



Note

1. nx = n0 or n1.

Figure 6-14. Network RTBI PHY-Mode

6.2.3.3 Network MAC RGMII/RTBI Pin Descriptions

Table 6-10 contains the pin descriptions for the RGMII/RTBI network interface ports when configured in MAC mode.

Table 6-10. 8450 RGMII/RTBI Network pin descriptions - MAC mode

Pin Name	RGMII/RTBI Signal	I/O	Description
nx_clk_1	nx_rxc	in	The receive reference clock will be 125MHz, 25MHz or 2.5MHz.
nx_ctrl_1	RGMII: nx_rx_ctl RTBI: nx_rxd[4]	in	In RTBI mode, contains the fifth bit on the rising edge of rxc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv (i.e. rxdv XOR rxerr) on the falling edge of rxc.
nx_bus1[3:0]	nx_rxd[3:0]	in	In RTBI mode, contains bits [3:0] on the rising edge of rxc and bits [8:5] on the falling edge of rxc. In RGMII mode, bit [3:0] on rising edge of rxc, bits [7:4] on the falling edge of rxc.
nx_clk_0	nx_txc	out	The transmit reference clock will be 125MHz, 25MHz or 2.5MHz.

Table 6-10. 8450 RGMII/RTBI Network pin descriptions - MAC mode

Pin Name	RGMII/RTBI Signal	I/O	Description
nx_ctrl_0	RGMII: nx_tx_ctl RTBI: nx_txd[4]	out	In RTBI mode, contains the fifth bit on the rising edge of txc and the tenth bit on the falling edge of rxc. In RGMII mode, txdv on the rising edge of txc and a logical derivative of txdv (i.e., txdv XOR txerr) on the falling edge of txc.
nx_bus0[3:0]	nx_txd[3:0]	out	In RTBI mode, contains bits [3:0] on the rising edge of txc and bits [8:5] on the falling edge of txc. In RGMII mode, bit [3:0] on rising edge of txc, bits [7:4] on the falling edge of txc.
Note nx = n0 or n1			

Table 6-11 contains the pin descriptions for the RGMII/RTBI network interface port when configured in PHY mode.

Table 6-11. 8450 RGMII/RTBI Network pin descriptions - PHY mode

Pin Name	RGMII/RTBI Signal	I/O	Description
nx_clk_1	nx_txc	in	The receive reference clock will be 125MHz, 25MHz or 2.5MHz.
nx_ctrl_1	RGMII: nx_tx_ctl RTBI: nx_txd[4]	in	In RTBI mode, contains the fifth bit on the rising edge of rxc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv (i.e., rxdv XOR rxerr) on the falling edge of rxc.
nx_bus1[3:0]	nx_txd[3:0]	in	In RTBI mode, contains bits [3:0] on the rising edge of rxc and bits [8:5] on the falling edge of rxc. In RGMII mode, bit [3:0] on rising edge of rxc, bits [7:4] on the falling edge of rxc.
nx_clk_0	nx_rxc	out	The transmit reference clock will be 125MHz, 25MHz or 2.5MHz.
nx_ctrl_0	RGMII: nx_rx_ctl RTBI: nx_rxd[4]	out	In RTBI mode, contains the fifth bit on the rising edge of txc and the tenth bit on the falling edge of rxc. In RGMII mode, rxdv on the rising edge of rxc and a logical derivative of rxdv(rxdv XOR rxerr) on the falling edge of rxc.
nx_bus0[3:0]	nx_rxd[3:0]	out	In RTBI mode, contains bits [3:0] on the rising edge of txc and bits [8:5] on the falling edge of txc. In RGMII mode, bit [3:0] on rising edge of txc, bits [7:4] on the falling edge of txc.
Note nx = n0 or n1			

6.2.4 GMAC SERDES & SGMII Interface Usage (Host/ Network)

This section discusses the use of GMAC interfaces for both the network and host side interfaces n0, n1, h0, h1 when configured to support operation in SERDES or SGMII modes.

The signal SERDES_RREF (ball number U10) is used to set the nominal drive current for the SERDES output. This signal should be connected through a 1K-1% ohm resistor to VDDS (1.0V).

For applications that use the SERDES/SGMII interface instead of the GMII/TBI interface, the control pins and clock pins for the unused interface may be connected through pull-down or pull-up resistors. Unused bus input pins may be terminated with pull-up or pull-down resistors. Unused bus output pins may be left unconnected.

6.2.4.1 GMAC SERDES & SGMII Pin Mappings (Host /Network)

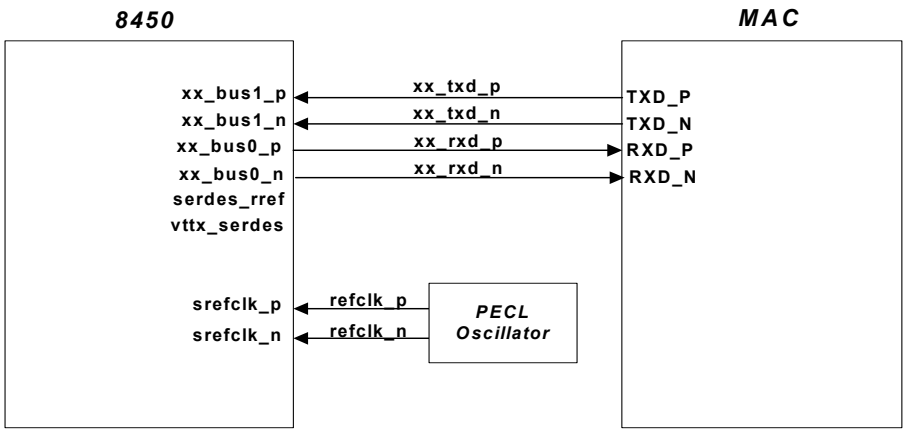
Table 6-12. 8450 SERDES and SGMII MAC/PHY modes pin mappings

Pin Name	MAC-SERDES		PHY-SERDES		MAC-SGMII		PHY-SGMII	
	SERDES Signal	I/O	SERDES Signal	I/O	SGMII Signal	I/O	SGMII Signal	I/O
srefclk_p	refclk_p	in	refclk_p	in	refclk_p	in	refclk_p	in
srefclk_n	refclk_n	in	refclk_n	in	refclk_n	in	refclk_n	in
xx_bus1_p	xx_rxd_p	in	xx_txd_p	in	xx_rxd_p	in	xx_txd_p	in
xx_bus1_n	xx_rxd_n	in	xx_txd_n	in	xx_rxd_n	in	xx_txd_n	in
xx_bus0_p	xx_txd_p	out	xx_rxd_p	out	xx_txd_p	out	xx_rxd_p	out
xx_bus0_n	xx_txd_n	out	xx_rxd_n	out	xx_txd_n	out	xx_rxd_n	out

Note

xx = n0, n1, h0 or h1

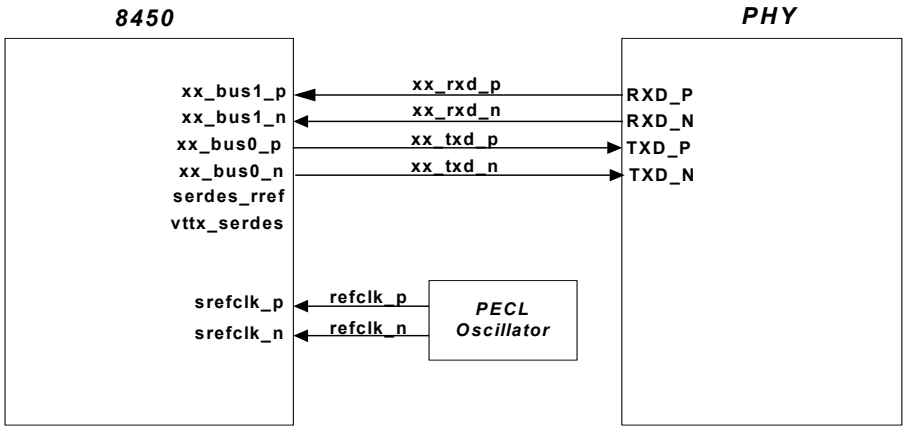
6.2.4.2 GMAC SERDES Connection Diagrams (Host/Network)



Note

1. xx = n0, n1, h0, or h1.
2. vttx_serdes = vtth_serdes or vttn_serdes.

Figure 6-15. SERDES PHY-Mode

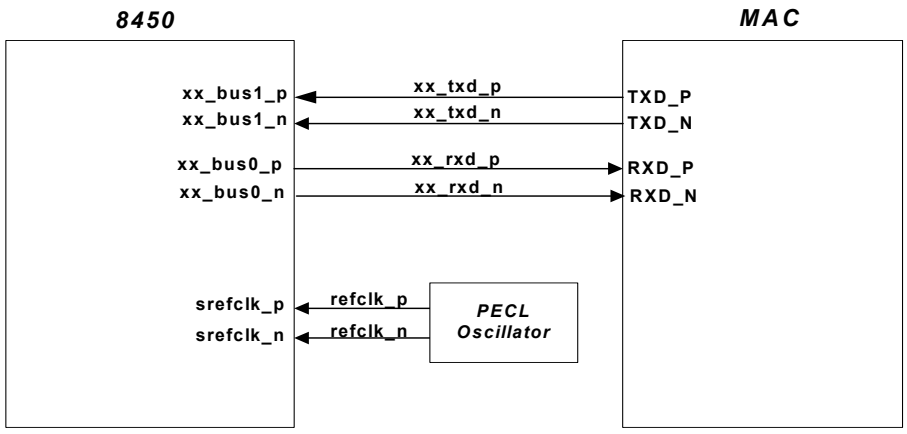


Note

1. xx = n0, n1, h0, or h1.
2. vttx_serdes = vtth_serdes or vttn_serdes.

Figure 6-16. SERDES MAC-Mode

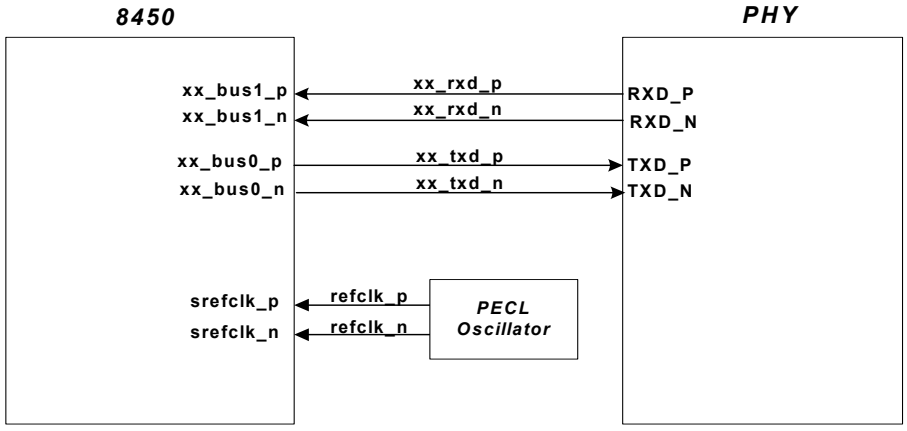
6.2.4.3 GMAC SGMII Connection Diagrams (Host/Network)



Note

1. xx = n0, n1, h0 or h1.

Figure 6-17. SGMII PHY-Mode



Note

1. xx = n0, n1, h0, or h1.

Figure 6-18. SGMII MAC-Mode

6.2.4.4 GMAC SERDES/SGMII Pin Descriptions (Host/Network)

Table 6-13 contains the pin descriptions for the SERDES and SGMII host and network interface ports when configured in PHY/MAC mode.

Table 6-13. 8450 SERDES/ SGMII pin descriptions - PHY/MAC mode

Pin Name	SERDES\SGMII (MAC) Signal	I/O	SERDES\SGMII (PHY) Signal	I/O	Description
refclk_p	refclk_p	in	refclk_p	in	reference clock input (positive), requires pull-down resistors if unused
refclk_n	refclk_n	in	refclk_n	in	reference clock input (negative), requires pull-down resistors if unused
xx_bus1_p	xx_rxd_p	in	xx_txd_p	in	data input (positive)
xx_bus1_n	xx_rxd_n	in	xx_txd_n	in	data input (negative)
xx_bus0_p	xx_txd_p	out	xx_rxd_p	out	data output (positive)
xx_bus0_n	xx_txd_n	out	xx_rxd_n	out	data output (negative)
Note xx = n0, n1, h0 or h1					

6.3 RMII Interface (Optional Control Interface)

Table 6-14 contains three columns for the signal name and pin mappings of the 100Mb RMII Ethernet port. The leftmost column contains the 8450 pin name, and the next two columns contain the functional signal name, based on whether the RMII port functions as a MAC or a PHY device. Table 6-14 maps the 8450 pin names to the signal functions depending on the settings of the RMII_PHY_MODE strap. There are two possibilities for the control port, as indicated in Table 6-6.

Please note in Table 6-14 that the directions of the data and control signals associated with the terms “receive” and “transmit” depend on whether the port is a MAC or a PHY. For example, “receive” relates to data and control signals that are outputs on the PHY and inputs on the MAC. And “transmit” relates to data and control signals that are inputs on the PHY and outputs on the MAC.

The supply signal RMII_VDD is assigned to ball number U13 as 3.3V Vdde.

Table 6-14. 8450 RMII modes pin mappings

Pin Name	MAC-MII		PHY-MII	
	RMII Signal	I/O	RMII Signal	I/O
rmii_ref_clk	rmii_ref_clk	out	rmii_ref_clk	in
rmii_bus1[2]	rmii_crs_rdv	in	rmii_txen	in
rmii_bus1[1:0]	rmii_rxd[1:0]	in	rmii_txd[1:0]	in

Table 6-14. 8450 RMII modes pin mappings

Pin Name	MAC-MII		PHY-MII	
	RMII Signal	I/O	RMII Signal	I/O
rmii_bus0[2]	mii_txen	out	rmii_crs_rdv	out
mii_bus0[1:0]	mii_txd[1:0]	out	rmii_rxd[1:0]	out

Note

The RMII Specification allows for rmii_ref_clk to be driven by an external source in any mode. The 8450 allows for either an input or output.

6.3.1 RMII Connection Diagrams

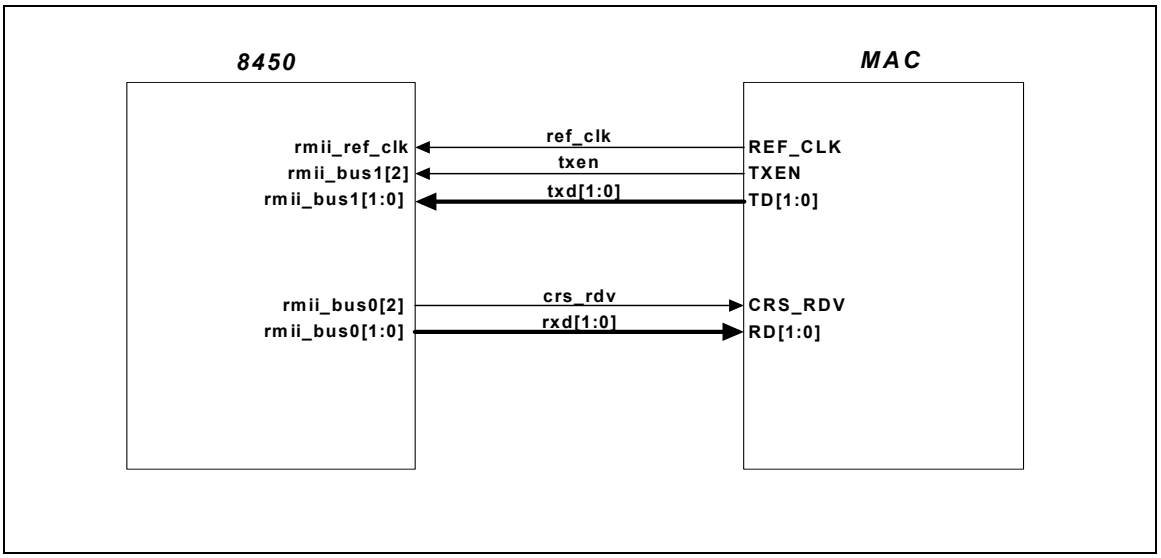


Figure 6-19. RMII PHY Mode

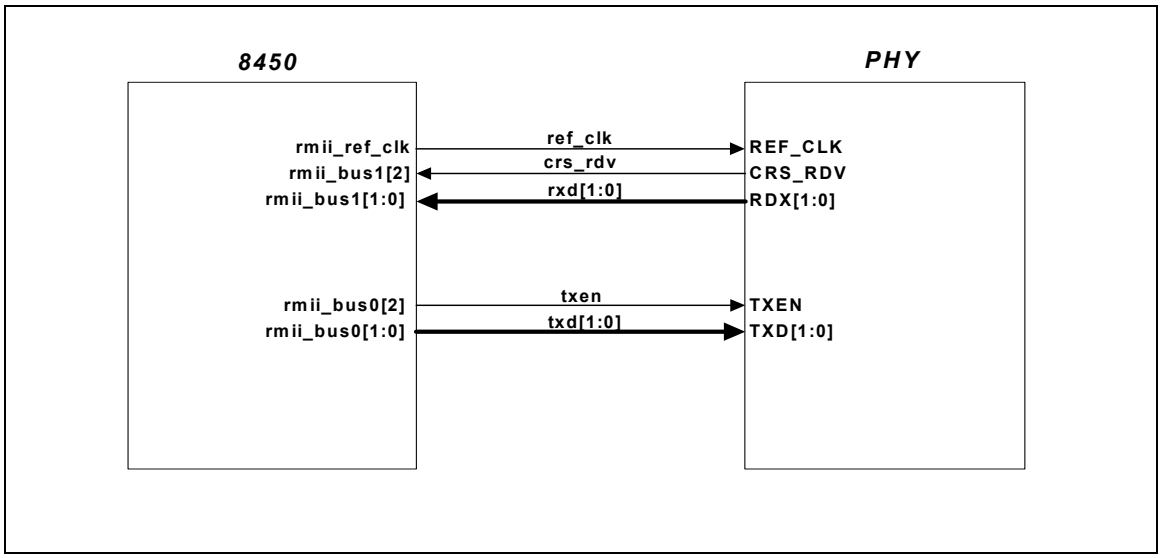


Figure 6-20. RMII MAC Mode

6.3.2 RMII Pin Descriptions (Optional Control Interface)

Table 6-15 contains the pin descriptions for the RMII control port when configured in MAC/PHY mode.

Table 6-15. 8450 RMII pin descriptions - MAC/PHY mode

Pin Name	RMII-MAC Signal	I/O	RMII-PHY Signal	I/O	Description
rmii_ref_clk	rmii_ref_clk	out	rmii_ref_clk	in	Reference Clock
rmii_bus1[2]	rmii_crs_rdv	in	rmii_txen	in	In MAC mode, Carrier Sense/Receive data Valid. In PHY mode, Transmit enable.
rmii_bus1[1:0]	rmii_rxd[1:0]	in	rmii_txd[1:0]	in	In MAC Mode, Receive Data. In PHY mode, Transmit Data
rmii_bus0[2]	rmii_txen	out	rmii_crs_rdv	out	In PHY mode, Carrier Sense/Receive data Valid. In MAC mode, Transmit enable
rmii_bus0[1:0]	rmii_txd[1:0]	out	rmii_rxd[1:0]	out	In MAC mode, Transmit Data. In PHY mode, Receive Data.

6.4 DDR2 SDRAM Interface

The 8450 DDR2 SDRAM interface is used for:

- External SA storage for the DPU (if additional SAs are required beyond the internal maximum value)
- eSC Code Storage and data memory (i.e., on-chip IKE)
- DPU/PCP Code Storage (Optional)

The 8450 provides a 32-bit DDR2 SDRAM interface that supports a single 200/400MHz SDRAM device and storage capacities from 2 MBytes up to 512 MBytes. A 7 bit ECC interface is optionally supported on the DDR2 SDRAM Interface.

Table 6-17 indicates the supported memory configurations for the DDR SDRAM.

Table 6-16. DDR2 Interface Signal Definition

Pin Name	SDRAM Signal	I/O	Description
sdclk_diff_n	CK	out	SDRAM Clock
sdclk_diff_p	CK_N	out	SDRAM Clock inverted
sdclk_fb_i	NA	in	DDR2 SDRAM De-skew PLL feedback clock input
sdclk_fb_o	NA	out	DDR2 SDRAM De-skew PLL feedback clock output
cs_n	CS_N	out	Chip Select (active low)
ras_n	RAS_N	out	Row address strobe (active low)
cas_n	CAS_N	out	Column address strobe (active low)
we_n	WE_N	out	Write Enable (active low)
ba[2]	BA[2]	out	Bank Address
ba[1:0]	BA[1:0]	out	Bank Address3
a[13]/cke	a[13]	out	Address 13/Clock Enable
a[12:0]	A[12:0]	out	Address
dm[3:0]	DM[3:0]	out	Data Mask
dqs[3:0]	DQS[3:0]	in/out	Data Strobe (one per byte)
dq[31:0]	DQ[31:0]	in/out	Data input/output
ecc[6:0]	ECC[6:0]	in/out	ECC data input/output
ecc_dm	ECC_DM	out	ECC data mask
eccs	ECCS	in/out	ECC strobe
odt	ODT	out	DDR2 on-die termination control

6.4.1 SDRAM Connection Diagrams

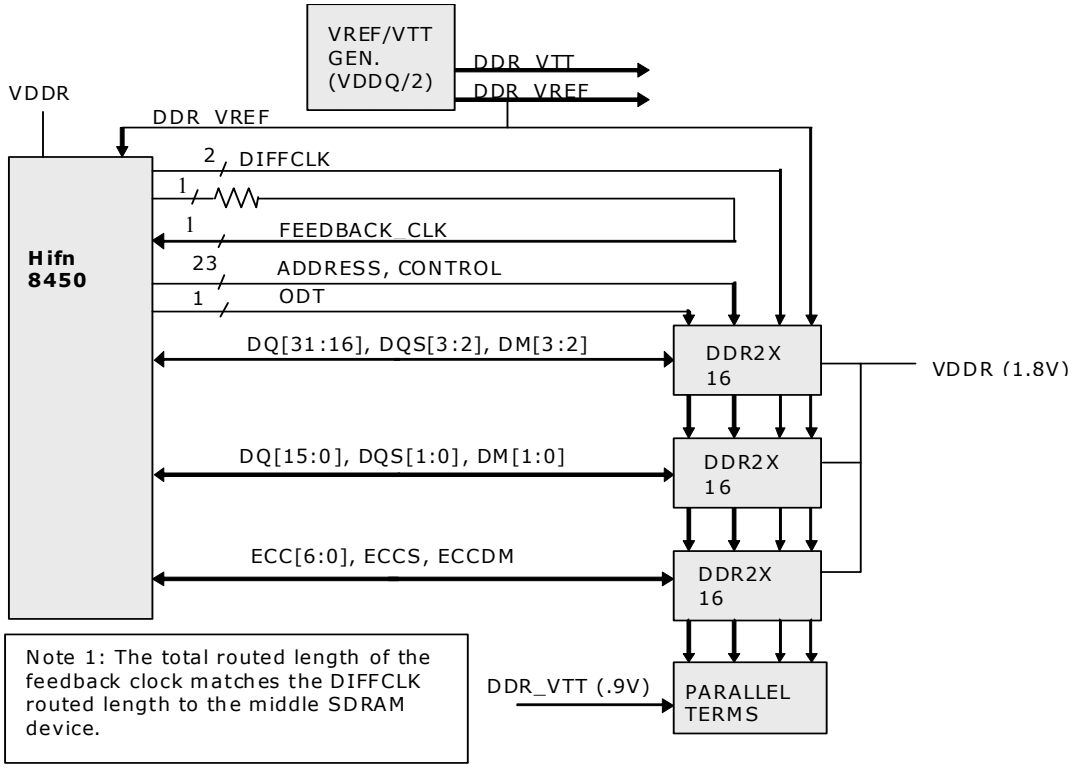


Figure 6-21. SDRAM Connection Diagram

6.4.2 DDR2 Memory Configurations

Table 6-17. DDR2 Memory Configuration

Device Configuration	Device Capacity	Number of Devices	Total Memory
16 Mbit x 16	256Mbits / 32MBytes	2	64 MBytes
32 Mbit x 16	512Mbits / 64MBytes	2	128 MBytes
64 Mbit x 16	1Gbits / 128MBytes	2	256 MBytes
128 Mbit x 16	2Gbits / 256MBytes	2	512 MBytes

The standard baseline memory configuration for the eSC running IKE is 64 Mbytes. However, if support for a large number of SAs is planned, then the larger memory configurations will be needed.

6.4.3 SDRAM Sizing

Sizing the required external SDRAM is dependent on the system application. The designer must consider whether,

- the Hifn IKE is going to run on the eSC (64 MBytes should be allowed for IKE.)
- a Non-IKE eSC image is needed (Generally, 32 MBytes of external SDRAM is an adequate allowance for a non-IKE image)
- more than the internal maximum number of SAs are required (An approximation of required memory for SA storage is 220 bytes per SA entry)

Additional details regarding memory sizing requirements will be detailed in the next revision of this data sheet.

6.4.4 No SDRAM Configuration

In the case where only the DPU firmware will be used and the on chip SA requirements are limited to the internal maximium number of SAs, the SDRAM can be eliminated from the design. This prevents the eSC from being used for any operations other than using the RMII port to communicate to the DPU.

Table 6-18 summarizes the DDR signals connections if the DDR interface is not used.

Table 6-18. No SDRAM Configuration

DDR Signal Name	Connection
DDR_CONFIG[2:0]	pull-down (0 ohms to 1 k-ohms)
VDDA_DDR_PLL	must be connected to 1.0V
VSSA_DDR_PLL	must be connected to ground
VREF_DDR_[2:0]	0.9V DDR2 Voltage Reference for SSTL bi-directional I/O
SDCLK_DIFF_P/N	open
SDCLK_FB_O	connect to SDCLK_FB_I through 50-ohm resistor
All control signals (includes ODT, CS_N, RAS_N, CAS_N, WE_N, BA[2:0], and A[13:0])	open
DQ[31:0], ECC[6:0]	open
DM[7:0], ECCDM	open
DQS[7:0], ECCS	pull-down (1 k-ohms)

6.5 PLL Interface

The 8450 provides an on-chip phase-locked loop (PLL) to generate clock signals for the entire chip. The GMII & MII interfaces will normally run from clocks supplied by the interface, however in certain loss-of-clock conditions they can be driven from internal clocks as well. The SERDES and SGMII interfaces also run from externally-supplied reference clocks. The PLL interface signals are all referenced to supply voltage VDDE.

Table 6-19. PLL Signal Interface

Signal Name	I/O Type	Description
prefclk	Input	System Reference Clock (25 or 125 MHz). Gigabit mode is supported with a either a 25MHz or 125MHz reference clock for GMII/TBI, RGMII/RTBI. If using SERDES/SGMII modes, the differential clock pair inputs (SREFCLK_P/N) are used for the reference clock. For these modes, the prefclk pin is unused and should be terminated to ground through a 10 k-ohm resistor.
pll_bypass	Input	PLL Bypass Mode. Must be tied low for normal operation. Tie high for Hifn test mode.
pll_mode[1]	Input	PLL Modes: Selects between 25MHz and 125MHz input reference clock. 0 = 125MHz input reference clock 1 = 25Mhz input reference clock

6.6 JTAG Interface

The 8450 provides an IEEE 1149.1 JTAG interface for boundary scan. This feature helps test the interface of the chip during manufacturing tests, and the connection to the customer board during diagnostic tests. The JTAG interface signals are all referenced to supply voltage VDDE.

Table 6-20. JTAG Signal Interface

Signal Name	I/O Type	Description
jtag_tck	Input	JTAG test clock
jtag_tdi	Input	JTAG test data input
jtag_tdo	Output	JTAG test data output
jtag_tms	Input	JTAG test mode select.
jtag_rst_n	Input	JTAG test reset This should not be tied to the system reset signal. It is normally tied low at all times except during JTAG testing.

Table 6-21 below lists the JTAG IDs for each revision of the chip.

Table 6-21. JTAG Chip and Revision IDs

Model	JTAG ID	Revision ID
8450	0x2CCB74AD	0x02
8450	0x3CCB74AD	0x03

6.7 General Purpose Pins

There are two banks of eight General Purpose I/O pins for both the eSC and DPU processors. All pins default to input following reset, therefore all GPIO pins must be terminated to a known state. Internal registers accessed by the eSC and DPU processors control the I/O direction of each pin. The GPIO pins may have pre-defined primary or secondary (Reset Capture) uses as described below and summarized in Table 6-22.

The Reset Capture functionality is defined immediately following the deassertion of the hardware or software reset. The GPIO pins are latched on the deassertion of reset and the subsequent latched state is used for the secondary (Reset Capture) functionality. The GPIO may then be claimed for a Primary Use function following reset. The GPIO interface signals are all referenced to supply voltage VDDE.

Table 6-22. General Purpose I/O Pins

Signal Name	I/O Type	Primary Use	Reset Capture	Reset Capture Function
dpu_gpio[7]	I/O	DPU Status	Not Available	Not Available
dpu_gpio[6]	I/O	MDIO/SDA	Not Available	Not Available
dpu_gpio[5]	I/O	MDC/SCL	ddr_config_2	1=enable ODT, 0=no ODT
dpu_gpio[4]	I/O	Net0 TX_DISABLE	ddr_config_1	ddr_config_1
dpu_gpio[3]	I/O	Net1 TX_DISABLE	ddr_config_0	ddr_config_0
dpu_gpio[2]	I/O	Net0 RX_LOSS	RGMII/RTBI Voltage Level	1=1.5V HSTL, 0=2.5V LVCMOS
dpu_gpio[1]	I/O	Net1 RX_LOSS	boot_config_1	1=Flash, 0=No Flash
dpu_gpio[0]	I/O	unassigned	boot_config_0	1= Secure Boot, 0=Normal Boot
esc_gpio[7]	I/O	eSC Status	Not Available	Not Available
esc_gpio[6]	I/O	PHY Interrupt	Device_ID[2]	Device_ID[2]
esc_gpio[5]	I/O	unassigned	Device_ID[1]	Device_ID[1]
esc_gpio[4]	I/O	eSC_Flash_CS1	Device_ID[0}	Device_ID[0}
esc_gpio[3]	I/O	eSC_Flash_SO	RMII MAC/PHY	1=PHY, 0=MAC
esc_gpio[2]	I/O	eSC_Flash_SI	100M/1G Boot	1= 100M boot, 0= 1G boot
esc_gpio[1]	I/O	eSC_Flash_CLK	unassigned	unassigned
esc_gpio[0]	I/O	eSC_Flash_CS0	Not Available	Not Available

Boot Configuration

During the boot process, the DPU reads the **dpu_gpio**[1]/***boot_config_1*** and **dpu_gpio**[0]/***boot_config_0*** pins to determine how the boot process will occur. A resistor should be used to pull the ***boot_config_0*** and ***boot_config_1*** pins high or low during the boot phase. Using a resistor rather than directly tying this pin allows allows **dpu_gpio**[1] and **dpu_gpio**[0] to be used as general purpose I/O for other user defined function during normal operation after the boot process completes.

boot_config_1 - Flash Indicator. If asserted high indicates the presence of a Flash device connected to **esc_gpio**[4:0].

boot_config_0 - Secure Boot Mode. If asserted low allows booting from a Flash, the Host 0 GMAC Interface, or the RMII Control Interface. If asserted high, the 8450 will boot from either a Flash or the RMII Control Interface.

Status Indicators (Optional)

Both the DPU and eSC provide status indications once code has been downloaded and self tests have been run to verify functionality of each on board processor. The **dpu_gpio**[7]***/ DPU Status*** and **esc_gpio**[7]***/eSC Status*** pins can be optionally used to provide an indication of the status for each processor. However, these status pins toggle regularly during normal operation. Both the **dpu_gpio**[7] and **esc_gpio**[7] pins are active high outputs when used to indicate status and can be connected to drive an LED as an indicator. If the eSC is not used for running on-chip IKE or other eSC-based code, then the eSC Status pin is not required.

Flash Interface (Optional)

The Serial Flash Interface via the Serial Peripheral Interface is supported on **esc_gpio**[4:0] as a primary function. The **esc_gpio**[4:0] pins are programmed to function as the flash device interface when the **boot_config_1** pin is asserted high and will become active when the chip is booting. They can be reclaimed later and used for "general purpose' pins in a system in a system that does not use Flash, however they will again revert to their Flash functionality when the chip re-boots after a hard reset or power cycle.

Note

Note that a Flash may be connected, but only used for Persistent Storage and not for bootload. In this case, the **boot_config_1** pin state need not be asserted high.

Hifn provides code to emulate the Serial Peripheral Interface (SPI) type serial flash device bus with capacities from 128KBytes to 32MBytes on the **esc_gpio**[4:0] pins.

MDIO Signaling (Optional)

The MDIO signalling for PHY management may optionally be supported on **dpu_gpio**[5] and **dpu_gpio**[6] to function as the MDC and MDIO respectively. Only the "initiator" side of the MDIO function is supported, therefore the 8450 expects to be initiating communications with PHY devices. This interface does NOT support receiving MDIO queries from another MDIO master (such as a MAC device). Hifn provides Station Management Software (STM) to support this function. Since the STM software runs on the eSC, the external SDRAM must be populated in order to use the MDIO signalling.

In addition, for SFP applications, I2C signalling may optionally be supported on **dpu_gpio**[5] and **dpu_gpio**[6] to function as the SCL and SDA respectively. The STM software running on the eSC processor can configure the SFP and query its internal EEPROM via this interface.

Device ID

In applications requiring multiple 8450s, **esc_gpio**[6:4] may be used to set a device ID. The **device_id**[2:0] pins (**esc_gpio**[6:4]) are sampled and latched at reset and can be reclaimed for alternate uses for user defined functionality in normal operation. The Device ID pins should be tied high or low through separate resistors to allow for reuse during normal operation.

RGMI/RTBI Voltage Select

RGMII/RTBI signaling on the 8450 supports either 1.5V HSTL or 2.5V LVCMOS for both the host and network interfaces. The **dpu_gpio**[2]***/RGMII/RTBI voltage Level*** can optionally be used to select between 1.5V HSTL or 2.5V LVCMOS if tied high or low respectively. The voltage selection applies to both host and network sides assuming they both use one of the RGMII/RTBI interface options.

Boot Rate Select

The Boot Rate Select function allows the user to boot the 8450 Host 0 interface in either 100Mbps or 1Gbps depending on the level of the **esc_gpio**[2]/***100M/1G Boot*** signal. If asserted high following reset, the Host 0 port will attempt to boot from the host at 100Mbps. If asserted low, the Host 0 GMAC will boot at 1Gbps.

RMII MAC/PHY Select

The **esc_gpio**[3]***/RMII MAC/PHY*** signal following reset is used to configure the RMII Optional Control interface to boot in either PHY or MAC mode if the signal is asserted high or low following reset.

PHY Interrupt (Optional)

The PHY Interrupt input may be used with Hifn's Station Management (STM) software to connect to PHY Interrupts notifying the STM software that an auto negotiation event has occurred in the PHY.

DDR2 Configuration

In applications using external DDR2 memory, three gpio pins are used for determining memory sizing and use of On Die Termination (ODT). The **dpu_gpio**[4:3] pins (***ddr_config_1*** and ***ddr_config_0***) are used to select the DDR2 Memory configurations per the table below. For memory configurations between 64M and 256M, the **a**[13]**cke** functions as cke (clock enable). For the 512M Byte configuration, the functionality of pin **a**[13]**cke** is address pin **a**[13].

Table 6-23. DDR2 Memory Configuration Sizing

Memory Size	ddr_config_1	ddr_config_0
64 M Bytes	0	0

Table 6-23. DDR2 Memory Configuration Sizing

Memory Size	ddr_config_1	ddr_config_0
128 M Bytes	0	1
256 M Bytes	1	0
512 M Bytes	1	1

Fiber PHY Control Signals (Optional)

When the network ports are connected to a fiber optic PHY or an SFP module, the Transmitter Enable (TX EN) and Signal Detect (SigDet) signals from the PHY may be connected to the 8450 so that the optional Station Management (STM) software can manage these signals. There are two GPIO's assigned to this function for Network port 0 and two more for Network port 1.

Note that within the 8450, these signals have no direct impact on the data flow through the device. The SigDet signal(s) are simply monitored by the STM server and the state reported to the host. The TX EN signal(s) are driven out to the PHY by the STM server under command of the host.

Other GPIO Functionality (Optional)

Some of the remaining GPIO pins may have other Primary or Secondary (Reset Capture) uses defined after reset. Additional information on alternate functionality of the GPIO pins will be provided on a subsequent release of the data sheet.

6.8 Miscellaneous Pins

Table 6-24. Test and mode signal pins

Signal Name	I/O Type	Description
por_n	Input	Power-on-reset, active low
host_config[2:0]	Input	Configures the operating modes of the two Host-side GMAC data interfaces, as follows: Host Side — MAC/PHY 000: RGMII — MAC or PHY 001: RTBI — MAC or PHY 010: SGMII — MAC or PHY 011: SerDes — MAC or PHY 100: GMII — MAC 101: GMII — PHY 110: TBI — MAC 111: TBI — PHY
net_config[1:0]	Input	Configures the operating modes of the two Network-side GMAC data interfaces, as follows: Network Side — MAC/PHY 00: RGMII — MAC or PHY 01: RTBI — MAC or PHY 10: SGMII — MAC or PHY 11: SerDes — MAC or PHY
testmode	Input	Hifn internal test input. Tie low for normal operation.

6.9 Power and Ground Pins

Table 6-25. Power and Ground pins (Sheet 1 of 2)

Signal Name	I/O Type	Description
vdde	Power	3.3V External I/O power (includes RMII VDD)
vddh	Power	I/O VDD for Host GMII (3.3V) or RGMII (1.5V or 2.5V) If both host and network ports are configured for SERDES/ SGMII, it is acceptable to connect vddn and vddh to 3.3V. This may save some PCB real estate and reduce the component cost/count because a dedicated 2.5V power supply not required.
vddi	Power	1.0V Internal Core Logic Power
vddn	Power	I/O VDD for Network RGMII (1.5V or 2.5V) Interface If both host and network ports are configured for SERDES/ SGMII, it is acceptable to connect vddn and vddh to 3.3V. This may save some PCB real estate and reduce the component cost/count because a dedicated 2.5V power supply not required.
vddr	Power	DDR I/O power 1.8V (DDR2)
vdds	Power	SERDES VDD 1.0V
vdd_reserved	Input	3.3V Reference Voltage for PLL. This is a test pin used during the manufacturing process.
vss	Ground	Ground for Core logic and I/O
vref[_ddr[2:0]	Input	DDR Voltage Reference for SSTL bi-directional I/O 0.9V for DDR2
vref_netw	Input	0.75V Network Side GMACs Reference Voltage Should be tied to Ground if the 1.5V RGMII interface option is NOT used.
vref_host	Input	0.75V Host Side GMACs Reference Voltage Should be tied to Ground if the 1.5V RGMII interface option is NOT used.
vttn_serdes	Input	SERDES Network driver termination voltage (A/B) Variable depending on the Application vttn_serdes (V) VSW (ac, mV) 1.0 250 1.2 350 1.5 500 1.8 750 Provides a method for varying the voltage swing on the Network side SERDES differential ouputs. 1V p-p differential signaling is common, vttn is normally tied to 1.5 V.

Table 6-25. Power and Ground pins (Sheet 2 of 2)

Signal Name	I/O Type	Description
vtth_serdes	Input	SERDES Host driver termination voltage (C/D Variable depending on the application) vtth_serdes (V) VSW (ac, mV) 1.0 250 1.2 350 1.5 500 1.8 750 Provides a method for varying the voltage swing on the Host side SERDES differential ouputs. 1V p-p differential signaling is common, vttn is normally tied to 1.5 V.
vdda_serdes	Power	1.0V SERDES Analog Power
vssa_ddr_pll	Ground	De-skew PLL Analog Ground Supply
vdda_ddr_pll	Power	De-skew PLL Analog Power Supply
vdda_pll	Power	1.0V PLL Analog Power supply
vssa_pll	Ground	PLL Analog ground

7 DC Specifications

Note

The DC information in this chapter is preliminary and subject to change.

7.1 Absolute Maximum Ratings

Table 7-1. Absolute Maximum Ratings

DC Supply I/O Voltage (vdde)	-0.5V to +3.6V
DC Supply I/O Voltage (vddh) **Note** If Configured for HSTL, applying voltages beyond the absolute maximum 1.65V may damage the device.	-0.5V to +3.6V (LVCMOS) -0.5V to +1.65V(HSTL)
DC Supply Core Voltage (vddi)	-0.5V to +1.1V
DC Supply I/O Voltage (vddn)	-0.5V to +2.75V
DC Supply I/O Voltage (vddr)	-0.5V to +2.75V
DC Supply I/O Voltage (vdds)	-0.5V to +1.1V
DC Supply Analog Voltage (vdda_ddr_pll, vdda_pll)	-0.5V to +1.1V
DC Supply SERDES Analog Voltage (vdda_serdes)	-0.5V to +1.1V
DC Input Voltage (vref_host, vref_netw)	-0.5V to 0.825V
DC Reference Voltage (vref[2:0]_ddr)	-0.5V to (vddr\2) +/- 1%
DC Input voltage (vttn_serdes, vtth_serdes)	-0.5V to +1.98V
Storage Temperature	-40°C to +125°C

Warning

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

7.2 Package Thermal Specification

Table 7-2 shows the thermal specifications for the 324 pin HSBGA package.

Table 7-2. Thermal Resistance

Symbol	Parameter	Max	Units
θjc	Thermal Resistance, Junction to Case (infinite heatsink on package top)	3.9	°C/W
Tjmax	Maximum Junction Temperature	125	°C
	For an 8 layer PC board		
θja	Thermal Resistance, Junction to Ambient in still air	13.0	°C/W
θja at 200LFM	Thermal Resistance, Junction to Ambient at 200LF/M (1m/s) airflow	11.1	°C/W
θja at 400LFM	Thermal Resistance, Junction to Ambient at 400LF/M (2m/s) airflow	10.4	°C/W
	For an 4 layer PC board		
θja	Thermal Resistance, Junction to Ambient in still air	17.0	°C/W

Note

1. Significant variations in the thermal performance of a package can be expected due to system variables, such as PWB construction, adjacent devices, or actual air flow across the package.
2. A single device is mounted in the center of the card. Air flow is across the top and bottom of the test card.
3. Junction Temperature, Tj = (Theta_Ja x Power) + Ambient Temperature.
4. Ambient temperature is assumed to be 70°C.

7.3 Recommended Operating Conditions

Table 7-3. Recommended Operating Conditions

DC Supply I/O Voltage (vdde) Nominal: 3.3V	+3.0V to +3.6V
DC Supply I/O Voltage (vddh) Nominal: 3.3V (If host is configured for GMII - LVCMOS 3.3V)	+3.0V to +3.6V
DC Supply I/O Voltage (vddh, vddn) Nominal: 1.5V (Can be configured for either HSTL - 1.5V or LVCMOS - 2.5V)	+1.35 to +2.75V
DC Supply I/O Voltage (vdds) Nominal: 1.0V	+0.97V to +1.03V
DC Supply Voltage, Core power (vddi, vdda_pll, vdda_serdes) Nominal: 1.0V	+0.97V to +1.03V
DC Supply I/O Voltage (vddr) Nominal: 1.8V (for DDR2)	+1.7V to +1.9V
Ambient Operating Temperature	0°C to +70°C

Note

1. DC Supply Voltage limits are as delivered at the pins (balls) of the device.
2. The DC information is preliminary and subject to change

7.4 DC Characteristics

Table 7-4. DC Electrical Characteristics (GMAC Interfaces) (Sheet 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL_hstl15}	Low level input threshold voltage (RGMII/RTBI) Single Ended Logic levels	V_{ddn} = V_{ddh} =1.5V	-0.30		V_{vref} -0.1	V
V_{IH_hstl15}	High level input threshold voltage (RGMII/RTBI) Single Ended Logic levels	V_{ddn} = V_{ddh} =1.5V	V_{vref} +0.1			V
$V_{IL\_lvcmos25}$	Low level input threshold voltage (RGMI/RTBII)	V_{ddn} = V_{ddh} =2.5V			V_{vref} -0.1	V
$V_{IH\_lvcmos25}$	High level input threshold voltage (RGMII/RTBI)	V_{ddn} = V_{ddh} =2.5V	V_{vref} +0.1			V
V_{IN_diff}	Low level input threshold voltage (SGMII/SerDes)	V_{ddn} = V_{ddh} =2.5V	170		2000	mV
V_{RCM_diff}	Receiver common-mode voltage (SGMII/SerDes)	V_{ddn} = V_{ddh} =2.5V		0.70		mV
$V_{ILT\_lvcmos33}$	Low level input threshold voltage (GMII host Only) Single Ended Logic levels	V_{ddh} = 3.3V			V_{vref} -0.1	V
$V_{IHT\_lvcmos33}$	High level input threshold voltage (GMII host Only) Single Ended Logic levels	V_{ddh} = 3.3V	V_{vref} +0.1			V
$V_{IL\_lvcmos33}$	Low level input voltage (GMII host Only) Single Ended Logic levels	V_{ddh} = 3.3V			0.8	V
$V_{IH\_lvcmos33}$	High level input voltage (GMII host Only) Single Ended Logic levels	V_{ddn} = 3.3V	1.71			V
$V_{OH\_lvcmos33}$	High level output voltage (GMII host Only)	V_{ddh} 3.6V I_{OH} = -4mA	2.4			V
$V_{OL\_lvcmos33}$	Low level output voltage (GMII host Only)	V_{ddh} = 3.6V I_{OL} = 4mA	V_{ddn}		0.4	V
$V_{OH\_lvcmos25}$	High level output voltage (RGMII/ RTBI)	V_{ddn}=V_{ddh}= 2.5V I_{OH} =-100uA I_{OH} = -1mA I_{OH} = -2mA	2.1 2 1.7			V
$V_{OL\_lvcmos25}$	Low level output voltage (RGMII/ RTBI)	V_{ddh} = 2.5V I_{OH} =100uA I_{OH} = 1mA I_{OH} = 2mA	V_{ddn}		0.2 0.4 0.7	V
V_{OH_hstl15}	High level output voltage (RGMII/ RTBI)	V_{ddn} =V_{ddh} 1.5V I_{OH} = -8mA	V_{ddn}-0.4			V

Table 7-4. DC Electrical Characteristics (GMAC Interfaces) (Sheet 2 of 2)

V_{OL_hstl15}	Low level output voltage (RGMII/ RTBI)	V_{ddh} = 1.5V I_{OL} = 8mA			0.4	V
V_{SW_diff}	Output Voltage (peak-to-peak, single ended) (SGMII/SerDes)		200	500	750	mV
$V_{DIFF-PP\_diff}$	Output Voltage (peak-to-peak, differential) (SGMII/SerDes)		400	1000	1500	mV
V_{OL_diff}	Low-level Output Voltage (SGMII/SerDes)			V_{TT}- 1.5* V_{SW}		V
V_{OH_diff}	High-level Output Voltage (SGMII/SerDes)			V_{TT}- 0.5* V_{SW}		V
V_{TCM_diff}	Transmit common-mode voltage (SGMII/SerDes)			V_{TT}- V_{SW}		
R_{dc1_hstl15}	Class I SSTL 1.5 Single-ended Driver Series Output Resistance (RGMII/RTBI)		11	23	41	Ω
I_{ivttl}	Driver Output Min Current LVTTL/ LVCMOS Mode		18			mA
$I_{leakage}$	Driver Pad leakage in High Impedance State				25	µA
I_{ponddq_u}	Receiver Current Draw (un-terminated)				2.5	mA
I_{ponddq_t}	Receiver Current Draw (terminated)				2.2	mA
$I_{ppdnddq}$	Receiver IDDQ PON				100	µA
$R_{drv\_33\_16}$	Driver Series Output Resistance (3.3V-16mA)		12		25	Ω

Note

The DC information is preliminary and subject to change.

Table 7-5. DC Electrical Characteristics (SDRAM Interfaces)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ILT_sstl18}	Low level input threshold voltage (DDR2 SDRAM Interface)	V_{ddr} = 1.8V			V_{vref_ddr}- 0.05	V
V_{IHT_sslt18}	High level input threshold voltage (DDR2 SDRAM Interface)	V_{ddr} = 1.8V	V_{vref_ddr}+ 0.05			V
V_{IL_sstl18}	Low level input voltage (DDR2 SDRAM Interface)	V_{ddr} = 1.8V	-0.3			V
V_{IH_sslt18}	High level input voltage (DDR2 SDRAM Interface)	V_{ddr} = 1.8V			V_{ddr} +0.3	V

$V_{OL\text{-}sstl18}$	Low level output voltage (DDR2 - SSTL_18 Driver)	$V_{ddr=}$ 1.9V I_{OL} = 4mA			0	V
V_{OH_sstl18}	High level output voltage (DDR2 - SSTL_18 Driver)	V_{ddr} =1.9V I_{OH} = -4mA	V_{ddr}			V
$R_{TT1(eff)}$	R_{TT1} Effective Impedance Value		60	75	90	Ω
$R_{TT2(eff)}$	R_{TT1} Effective Impedance Value		120	150	180	Ω
$R_{aserddrv\_18}$	SSTL_18 Address Driver Series Output Resistance		9	16	25	Ω
$R_{eserddrv\_18}$	SSTL_18 Clock Driver Series Output Resistance		9	16	25	Ω
$R_{dserddrv\_18}$	SSTL_18 Data Driver Series Output Resistance		9	16	25	Ω
$I_{leakage}$	Driver Pad leakage				100	nA
I_{ponddq_u}	Receiver Current Draw (un-terminated)				250	µA
I_{ponddq_t}	Receiver Current Draw (terminated)				850	µA
I_{pdnddq}	Receiver IDDQ PON				10	nA

Note

The DC information is preliminary and subject to change.

Table 7-6. DC Electrical Characteristics (GPIO Interfaces)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IL\_lvcmos/lvttl}$	Low level input voltage (GPIO)	V_{dde} = 3.6V			0.8	V
$V_{IH\_lvcmos/lvttl}$	High level input voltage (GPIO)	V_{dde} = 3.6V	2.0			V
$V_{OL\_lvcmos/lvttl}$	Low level output voltage (GPIO)	V_{dde} = 3.6V I_{OL} = 4mA	0		0.4	V
$V_{OH\_lvcmos/lvttl}$	High level output voltage (GPIO)	V_{dde} = 3.6V I_{OH} = -4mA	V_{dde}-0.4		V_{dde}	V
$I_{OL\_lvcmos/lvttl}$	Low level Output current (GPIO)	V_{IN} = V_{ss} V_{dde} = 3.6V	- 6			mA
$I_{OH\_lvcmos/lvttl}$	High level Output current (GPIO)	V_{IN} = V_{dde} V_{dde} = 3.6V			6	mA
$R_{drv\_33\_6}$	Driver Series Output Resistance (3.3V-6mA)		30		67	Ω
$I_{leakage}$	Driver Pad Leakage	V_{dde} = 3.6V Pad voltage driven to 3.6V through 0.010 ohm load.			100	nA

Note

The DC information is preliminary and subject to change.

Table 7-7. DC Electrical Characteristics (Power and Current)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
P_{TOTAL}	Total Power dissipation	V_{dde} = 3.6V, V_{ddi}= 1.1V T = 25°C		2.5	3.1	W
$P_{I/O}$	I/O Power dissipation	V_{dde} = 3.6V, V_{ddi} = 1.1V T = 25°C		0.5		W
P_{CORE}	Core Power dissipation	V_{ddi} = 1.1V T = 25°C		2		W
I_{ddi_core}	Active Supply Current (vddi) (Core, includes SERDES logic and I/O)	V_{ddi}=1.0V T = 70°C			2.5	A
I_{ddi_pll}	Active Supply Current (vddi - pll) (PLL)	V_{ddi}=1.0V T = 70°C			0.01	A
I_{dde_io}	Active Supply Current (vdde) (GPIO)	V_{ddi} = 3.6V T = 70°C			0.10	A
I_{ddh}	Active Supply Current (vddh) (host Interface)	V_{ddh}=1.1V T = 70°C			0.25	A
I_{ddn}	Active Supply Current (vddn) (network Interface)	V_{ddn}=1.0V T = 70°C			0.25	A
I_{ddr}	Active Supply Current (vddr) (DDR2) (Includes ODT termination surge current (5-6ma per data group signal))	V_{ddr} = 1.8V T = 70°C			1.1	A
Ivtt	Active Supply Current (vttn, vtth) (Termination) Per connection (2 connections per chip)	V_{ttn} =V_{ttn}= 1.5V T = 70°C			0.06	A

Note

1. The DC information is preliminary and subject to change.
2. The current consumption for core, PLL, and I/O subsections represent peak instantaneous current requirements and should be used for power planning. The sum of these current requirements will exceed the maximum power numbers (PIO and PCORE), which represent average worst-case thermal parameters.

7.5 Power Sequencing

In order to prevent latch-up, it is recommended that the 44x0/84x0 power supplies be brought up starting with the highest voltage first and ending with the lowest voltage. It is also permitted to bring up the supplies simultaneously, making sure that the lower-voltage supplies do not exceed the higher-voltage supplies during the ramp. The intent is to make sure that there are no reverse-bias conditions during the power-on process that could cause improper operation or possible damage to the 44x0/84x0 chip. A minimum delay of 1ms should be allowed between the bring-up of each supply. To minimize potential bus conflicts, a maximum delay of 500ms for the complete power-up sequence should be adhered to. Please refer to the *4450/8450 Hardware Design Application Note* (AN-0145) for more detailed information.

8 Timing Specifications

8.1 AC Operating Conditions

Table 8-1. AC Operating Conditions

Symbol	Parameter	Conditions*
vddi, vdda_pll	Supply voltage - Core	1.0V ± 3%
vdde	Supply voltage - I/O, RMII	3.3V ± 5%
vddh	Supply voltage - Host Side Interface	3.3V ± 5% GMII 1.5V ± 5% RGMII
vddn	Supply voltage - Network Side Interface	1.5V ± 5% RGMII
vdds	Supply voltage - SGMII/SerDes	1.0V ± 3%
vddr	Supply voltage - SDRAM	1.8V ± 5% DDR2
vss	Ground potential	0V
TA	Ambient operating temperature	0°C to +70°C
CL	Capacitive pin loading	1.1 pF (typ)

Note

See derating information below for other load conditions.

8.2 PLL Ref Interface Clock Timing

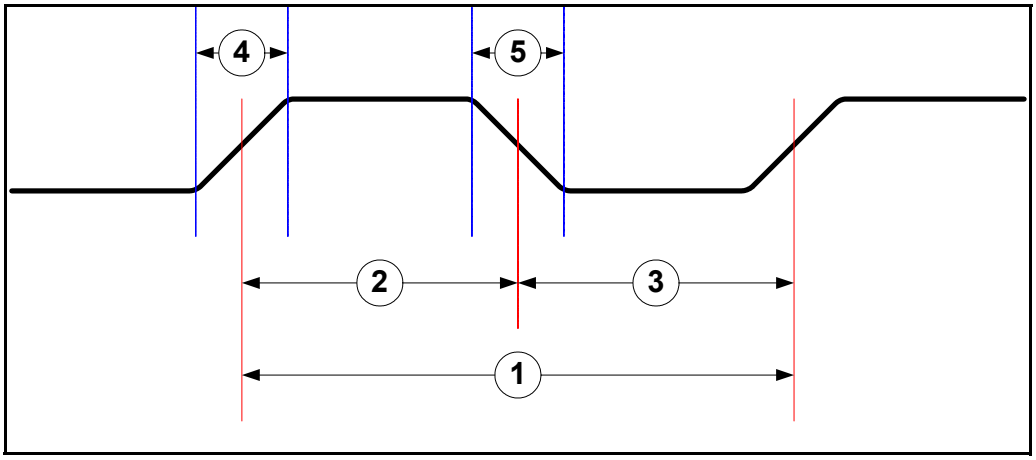


Figure 8-1. Input Bus Clock Timing

Table 8-2. 125 MHz PLL_REF Clock

Number	Description	Min	Nominal	Max	Units
1	Clock frequency		125		MHz
2	Clock width high	3.6			ns
3	Clock width low	3.6			ns
4	Clock rise time from V_{IL} to V_{IH}			2	ns
5	Clock fall time from V_{IH} to V_{IL}			2	ns
n/a	Duty cycle	45		55	%
n/a	Jitter (peak to peak)			200	ps
n/a	PLL lock time (500 reference clock cycles)			4	µsec

Table 8-3. 25 MHz PLL_REF Clock

Number	Description	Min	Nominal	Max	Units
1	Clock frequency		25		MHz
2	Clock width high	18			ns
3	Clock width low	18			ns
4	Clock rise time from V_{IL} to V_{IH}			4	ns
5	Clock fall time from V_{IH} to V_{IL}			4	ns
n/a	Duty cycle	45		55	%
n/a	Jitter (peak to peak)			200	ps
n/a	PLL lock time (500 reference clock cycles)			20	µsec

8.3 RMII Timing

The 8450 supports the 802.3-2002 standard specifications. With a PREFCLK input of 25MHz, this port supports 100 Mbps fast Ethernet RMII timing.

The only interface difference between RMII PHY and RMII MAC mode is the direction of the clock pin. In MAC mode, the clock is an output, and in PHY mode the clock is an input.

Table 8-4. RMII Timing

Mode	TXD		RXD	
	Setup	Hold	Setup	Hold
PHY	2.00 ns	2.00 ns	4.50 ns	2.50 ns
MAC	2.00 ns	2.00 ns	4.50 ns	2.50 ns

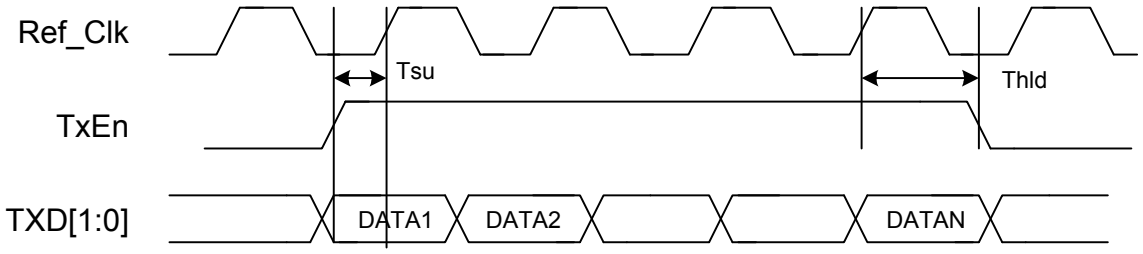


Figure 8-2. RMII Transmit Signal Timing

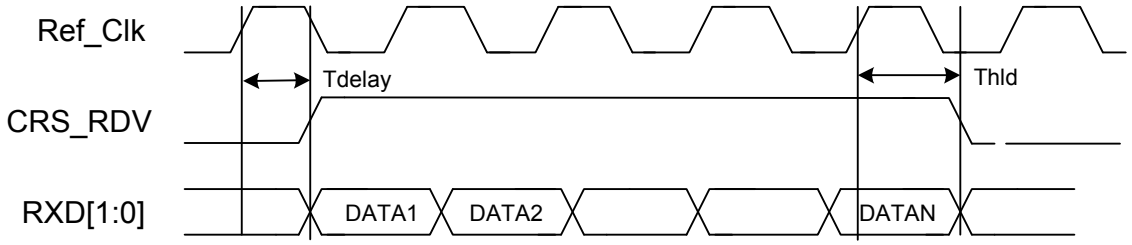


Figure 8-3. RMII Receive Signal Timing

8.4 GMII Timing (Host Interface)

The 8450 supports the 802.3-2002 standard specifications.

Table 8-5. GMII Mode I/O Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
MAC	1.00 ns	1.00 ns	2.00 ns	0.00 ns	2.50 ns	0.50 ns
PHY	1.00 ns	1.00 ns	2.00 ns	0.00 ns	2.50 ns	0.50 ns

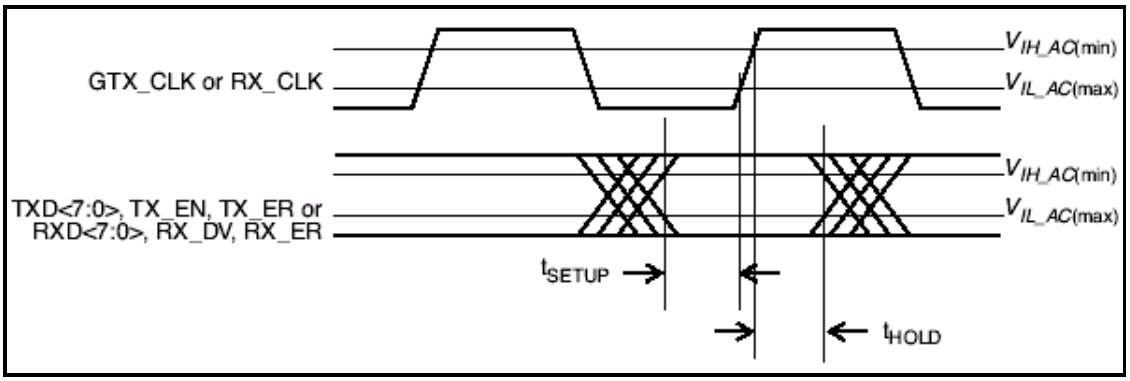


Figure 8-4. GMII Transmit & Receive Timing

8.5 TBI Timing (Host Interface)

The 8450 supports the 802.3-2002 standard specifications. For TBI MAC and PHY modes, the 8450 can operate with 0.05ns less than the IEEE 802.3 specification requirements. All other timing numbers match the 802.3 specification.

Table 8-6. TBI Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
MAC	1.00	1.00	2.45 ns	1.45 ns	2.00 ns	1.00 ns
PHY	1.00	1.00	1.95 ns	0.95 ns	2.50 ns	1.50 ns

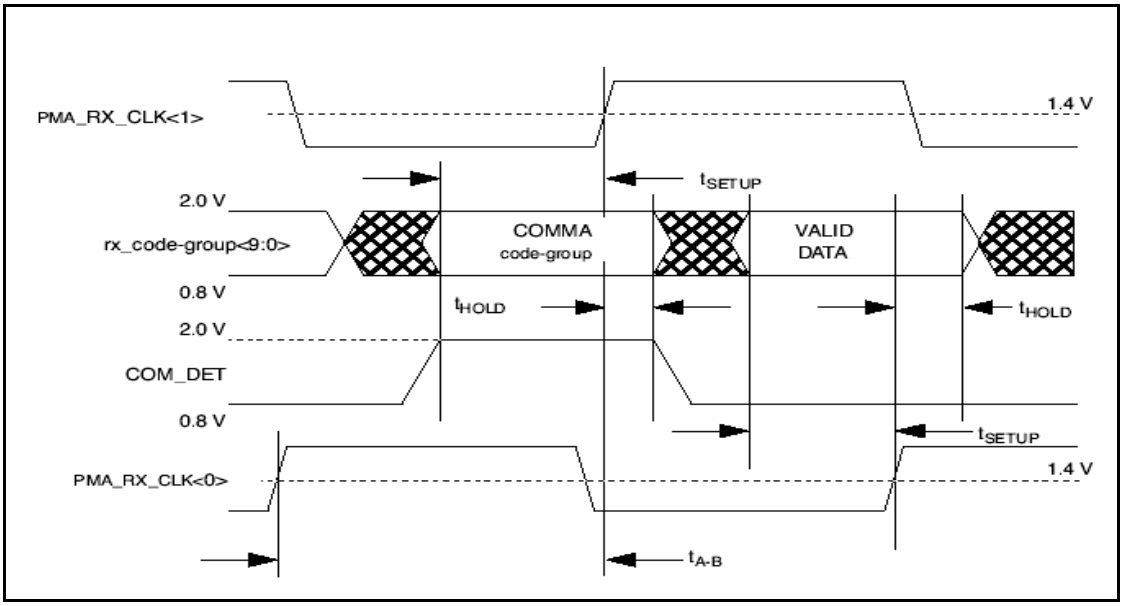


Figure 8-5. TBI Receive Timing

8.6 RTBI Timing

Table 8-7. RTBI Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
RTBI	0.75ns	0.75ns	1.00 ns	1.00 ns	1.20 ns	1.20 ns

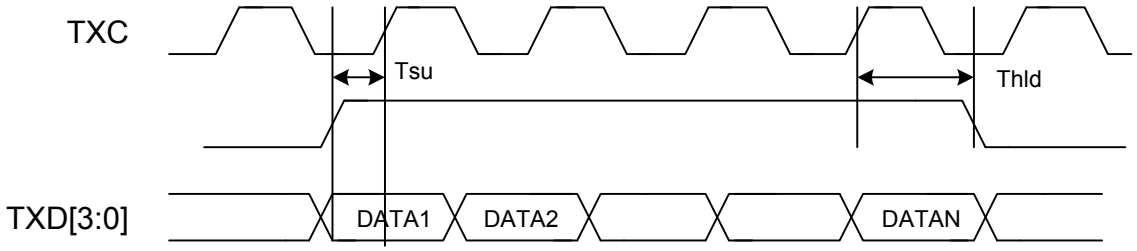


Figure 8-6. RTBI Transmit Signal Timing

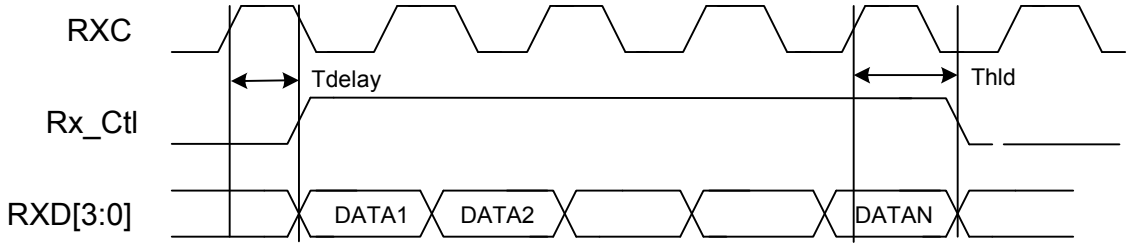


Figure 8-7. RTBI Receive Signal Timing

8.7 RGMII Timing

Note that not all PHYs meet these RGMII timing requirements. Careful attention should be given to the specific PHY specification and its possible board routing implications.

Table 8-8. RGMII Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
RGMII	0.75 ns	0.75 ns	1.00 ns	1.00 ns	1.20 ns	1.20 ns

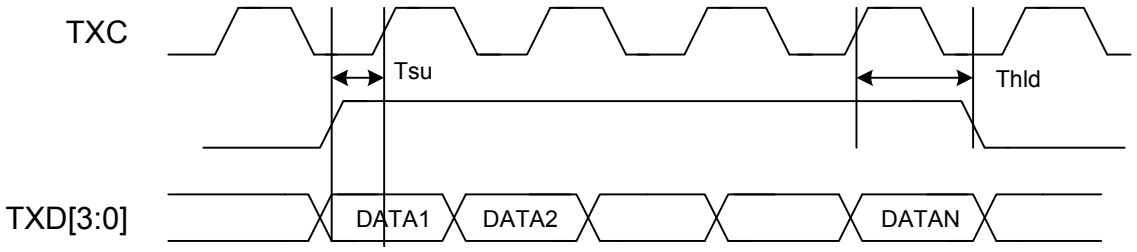


Figure 8-8. RGMII Transmit Signal Timing

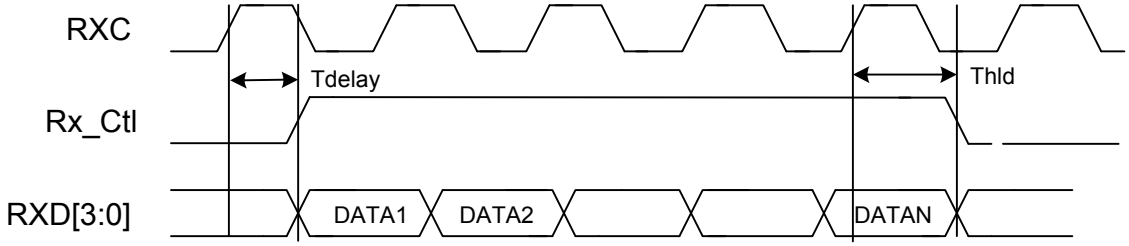


Figure 8-9. RGMII Receive Signal Timing

8.8 SGMII Timing

Table 8-9. SGMII Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
SGMII	0.75 ns	0.75 ns	1.00 ns	1.00 ns	1.20 ns	1.20 ns

8.9 SerDes Timing

Table 8-10. SerDes Timing

Mode	Rise Time	Fall Time	Input Signals		Output Signals	
	(max)	(max)	Setup	Hold	Setup	Hold
SerDes	0.75 ns	0.75 ns	1.00 ns	1.00 ns	1.20 ns	1.20 ns

8.10 SDRAM Timing

The 8450 only supports DDR2 SDRAM. The SDRAM interface signal timing is derived from the PLL Ref clock. The table below summarizes the timing parameters for the SDRAM Controller. All timing is relative to the external SDRAM Clock.

Please see the *4450/8450 Hardware Design Application Note* for more details on routing guidelines and general information about the DD2 interface. The timing numbers shown in Table 8-11 are only a subset of all the DDR2 timing requirements, but represent the most relevant.

Table 8-11. SDRAM Interface Timing

Symbol	Parameter	Min	Max	Units
Tck	Clock cycle time	5000	5000	ps
Tch	Clock high level width	2250	2250	ps
Tcl	Clock low level width	2250	2250	ps
Thp	Clock half period	2250		ps
Th	Address/Ctrl Hold	800		ps
Ts	Address/Ctrl setup	1000		ps
Tdh	DQ/DM hold	500		ps
Tds	DQ/DM setup	500		ps
Tdqss	Write to first DQS	WL -0.25	WL+ 0.25	Tck
Tdqsq	DQS-DQ skew		450	ps
Tqhs	DQ hold skew factor		550	ps
Tqh	DQ/DQS hold	1700		ps
Tac	DQ access time from CK	-700	700	ps
Tdqsck	DQS access time from CK	-600	600	ps

Note

WL is the write latency of the DDR2 DRAM (in clock cycles). The Tdqss parameter indicates that the edge of the DQS signal must be no more than +/- 0.25 of a clock period away from the appropriate clock edge.

8.11 Flash Device Timing

The 8450 supports both reading and writing of SPI type Flash devices, up to a tbd MHz clock rate. The Flash device interface signal timing is derived from an internal CPU toggling GPIO pins. Additional details regarding the SPI interface via the **esc_gpio**[4:0] pins is described in Section 6.7.

Table 8-12 and Figure 8-10 describe the read and write timing.

Table 8-12. Flash Device Read and Write Timing

Symbol	Parameter	Min	Max	Units
Twh	Clock high period	22		ns
Twl	Clock low period	22		ns
Tcs	CS high period	250		ns
Tcss	CS (setup) to Clock	250		ns
Tcsh	Clock to CS (hold)	250		ns
Tv	Read data valid		20	ns

Table 8-12. Flash Device Read and Write Timing

Tho	Read data hold	0		ns
Tdis	Read data hi-Z		20	ns
Tsu	Write data set up	5		ns
Th	Write data hold	10		ns

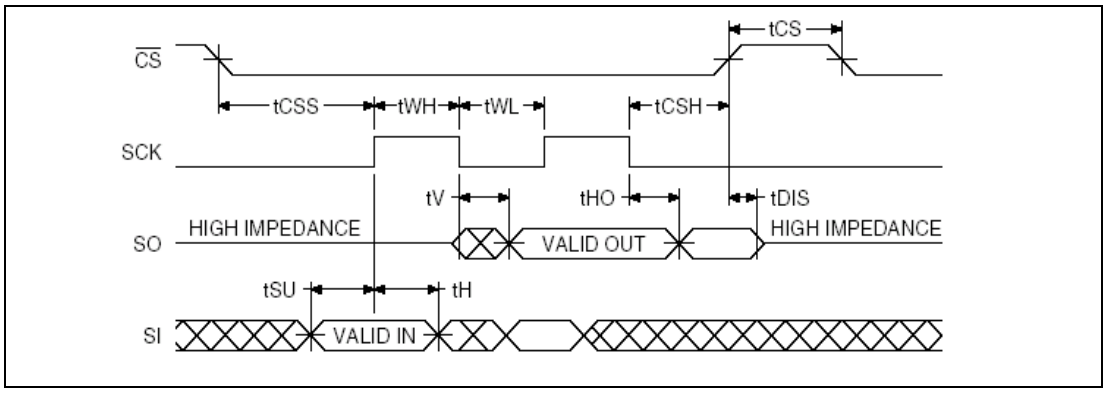


Figure 8-10. Flash device read and write timing (SPI mode 0)

8.12 MDIO Timing

This device supports a subset of the 802.3-2002 MDIO management interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows the 8450 to monitor and control the PHY device(s) that are connected to the network side ports. If the host system GMAC will control the system PHY device with its own MDIO connection, then the 8450 pins are unused. When the 8450 acts as the sole system GMAC these pins are used as defined in the 802.3 MDIO specification and referenced in Section 6.7. Hifn includes Station Management (STM) Software as a part of it's SDK.

The 8450 supports the low speed MDIO operating mode, and this is illustrated in Figure 8-11. In this mode, the MDC clock signal operates at a frequency of 2.5 MHz.

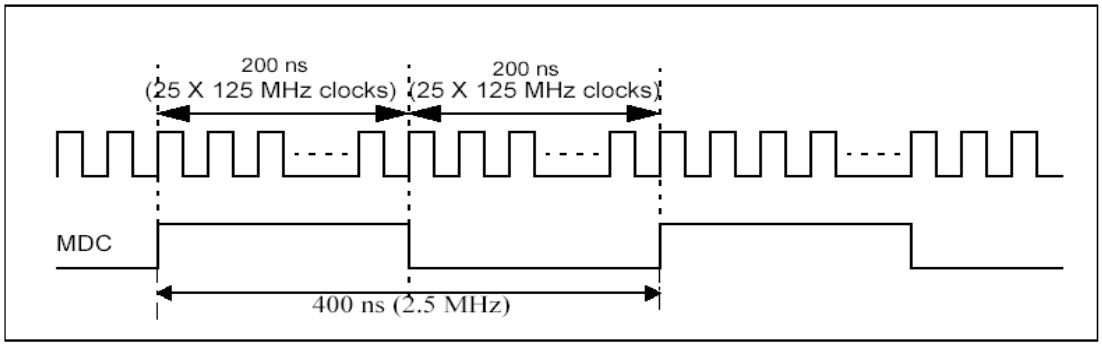


Figure 8-11. Low-speed MDIO Operation

Table 8-13. MDIO Timing

Symbol	Parameter	Min	Max	Units
Tsu	MDIO Setup prior to MDC High	10		ns
Thold	MDIO Hold after MDC High	10		ns
Tprop	MDC to MDIO Output Delay	0	20	ns

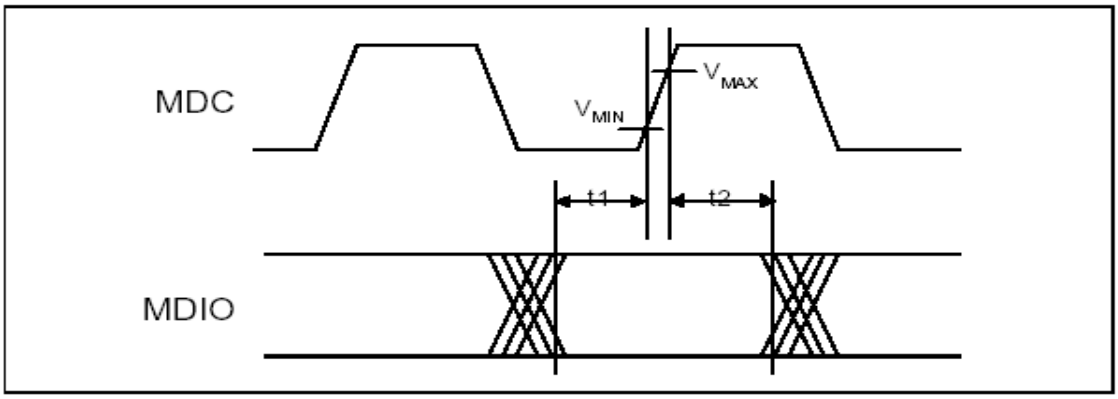


Figure 8-12. MDIO Write Timing

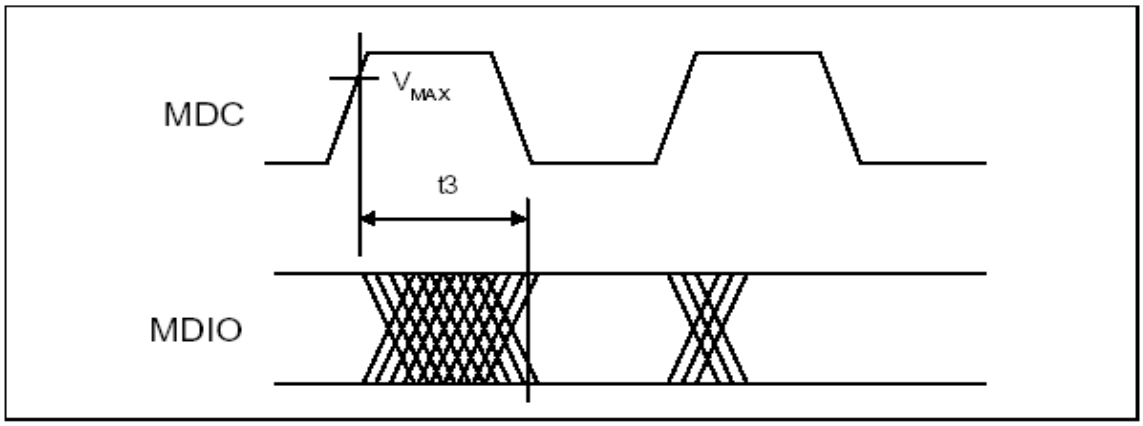


Figure 8-13. MDIO Read Timing

8.13 IEEE 1149.1 (JTAG) Timing

The JTAG interface signal timing is derived from the JTAG TCK clock.

Table 8-14. JTAG Timing

Number	Parameter	Symbol	Min	Max	Units
	TCK Frequency			10	MHz
T1	TCK Period	Tthth	100		ns
T2	TCK low/high time	Tth	40	60	ns
T3	TCK to TDO (Output) Delay Time	Tskl	2	7	ns
T4	TDI, TMS (Input) to TCK Setup Time	Tsks	5		ns
T5	TDI, TMS (Input) from TCK Hold Time	Tcs	5		ns
T6	non-test input Setup time to TCK	Tcs	5		ns
T7	non-test input Hold time from TCK	Tch	5		ns
T8	TCK to non-test outputs Delay Time	Tdvth	2	7	ns

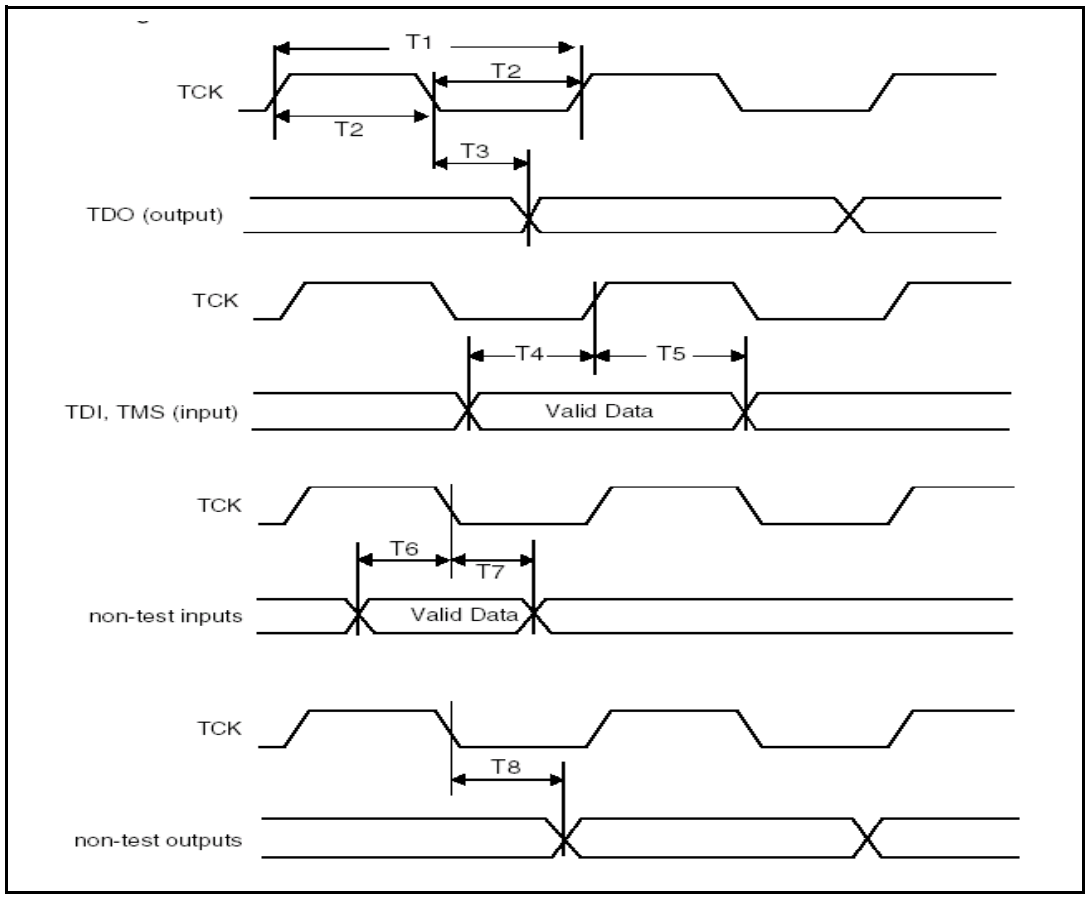


Figure 8-14. JTAG Timing

9 Pinout and Mechanical Description

9.1 8450 Numeric Pin List

Table 9-1. 8450 pin list (numeric) - first half

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	vss	B11	vddr	D3	vdda_ddr_pll	E13	dq[10]	G5	ba[2]
A2	sdclk_diff_n	B12	dq[11]	D4	a[1]	E14	vss	G6	we_n
A3	sdclk_diff_p	B13	dq[8]	D5	a[0]	E15	ecc[3]	G7	cas_n
A4	vss	B14	vddr	D6	dq[30]	E16	ecc_dm	G8	vddi
A5	odt	B15	dq[2]	D7	vddr	E17	eccs	G9	vddi
A6	vref_ddr[2]	B16	dq[1]	D8	dq[25]	E18	ecc[2]	G10	vddi
A7	vss	B17	vss	D9	dm[2]	F1	a[11]	G11	vddi
A8	dq[24]	B18	vref_ddr[0]	D10	vddr	F2	a[9]	G12	dq[14]
A9	dq[21]	C1	sdclk_fb_i	D11	dq[15]	F3	vddr	G13	h0_ctrl_0
A10	vss	C2	a[3]	D12	dqs[1]	F4	a[10]	G14	h0_clk_0
A11	vref_ddr[1]	C3	a[2]	D13	vddr	F5	a[12]	G15	h0_bus0[5]
A12	dm[1]	C4	vddr	D14	dq[7]	F6	vddr	G16	h0_bus0[6]
A13	vss	C5	a[4]	D15	dq[4]	F7	dq[27]	G17	h0_bus0[7]
A14	dq[9]	C6	vss	D16	vddr	F8	dq[23]	G18	vss
A15	dq[6]	C7	dq[29]	D17	ecc[5]	F9	vddr	H1	vss
A16	dm[0]	C8	dq[26]	D18	ecc[4]	F10	dqs[2]	H2	ras_n
A17	dqs[0]	C9	vss	E1	vddr	F11	dq[16]	H3	cs_n
A18	vss	C10	dq[17]	E2	a[7]	F12	vddr	H4	host_config[0]
B1	sdclk_fb_o	C11	dq[13]	E3	vssa_ddr_pll	F13	h0_bus0[8]	H5	vddr
B2	vddr	C12	vss	E4	a[8]	F14	h0_bus0[9]	H6	host_config[1]
B3	vss	C13	dq[5]	E5	vss	F15	vddh	H7	host_config[2]
B4	a[5]	C14	dq[3]	E6	dq[28]	F16	ecc[1]	H8	vss
B5	vddr	C15	vss	E7	dqs[3]	F17	vddr	H9	vss
B6	dq[31]	C16	dq[0]	E8	vss	F18	ecc[0]	H10	vss
B7	dm[3]	C17	ecc[6]	E9	dq[22]	G1	a[13]\cke	H11	vss
B8	vddr	C18	vddr	E10	dq[19]	G2	ba[0]	H12	vddi
B9	dq[20]	D1	a[6]	E11	vss	G3	vss	H13	h0_bus0[0]
B10	dq[18]	D2	vss	E12	dq[12]	G4	ba[1]	H14	vss

Table 9-2. 8450 pin list (numeric) - second half

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
H15	h0_bus0[1]	K17	h0_ctrl_1	N1	jtag_rst_n	R3	n0_bus0[3]	U5	n1_bus1[0]
H16	h0_bus0[2]	K18	vss	N2	vssa_pll	R4	vddn	U6	n1_clk_1
H17	h0_bus0[3]	L1	esc_gpio[6]	N3	jtag_tck	R5	n1_bus0[2]	U7	vss

Table 9-2. 8450 pin list (numeric) - second half

H18	h0_bus0[4]	L2	vss	N4	jtag_tdo	R6	vss	U8	n0_bus0_p
J1	dpu_gpio[4]	L3	esc_gpio[4]	N5	jtag_tms	R7	srefclk_p	U9	n1_bus0_p
J2	dpu_gpio[3]	L4	esc_gpio[5]	N6	testmode	R8	vss	U10	serdes_rref
J3	vdde	L5	vdd_reserved	N7	n1_bus1[1]	R9	vss	U11	h0_bus0_p
J4	dpu_gpio[2]	L6	esc_gpio[2]	N8	n0_bus1_n	R10	vss	U12	h1_bus0_p
J5	dpu_gpio[1]	L7	esc_gpio[3]	N9	n1_bus1_n	R11	vss	U13	3.3V (vdde)
J6	dpu_gpio[5]	L8	vddi	N10	vtth_serdes	R12	vss	U14	rmii_bus0[2]
J7	dpu_gpio[0]	L9	vss	N11	h0_bus1_n	R13	rmii_ref_clk	U15	rmii_bus1[1]
J8	vddi	L10	vss	N12	h1_bus1_n	R14	h1_bus0[6]	U16	h1_bus0[8]
J9	vss	L11	vss	N13	h1_ctrl_1	R15	vddh	U17	vddh
J10	vss	L12	vddi	N14	h1_clk_1	R16	h1_bus0[3]	U18	h1_bus0[2]
J11	vss	L13	h0_bus1[2]	N15	h1_bus1[5]	R17	h1_bus0[1]	V1	vss
J12	vddi	L14	vss	N16	h1_bus1[7]	R18	vss	V2	n1_ctrl_0
J13	h0_clk_2	L15	h0_bus1[0]	N17	h1_bus1[6]	T1	vref_netw	V3	n1_clk_0
J14	h0_bus1[9]	L16	h0_bus1[1]	N18	vss	T2	n0_bus1[1]	V4	n1_ctrl_1
J15	vddh	L17	h1_bus1[0]	P1	n0_ctrl_0	T3	n0_bus1[0]	V5	n1_bus1[2]
J16	h0_bus1[8]	L18	vref_host	P2	n0_bus0[1]	T4	n1_bus0[0]	V6	n1_bus1[3]
J17	vddh	M1	esc_gpio[7]	P3	n0_clk_0	T5	n1_bus0[3]	V7	vddn
J18	h0_bus1[7]	M2	vdda_pll	P4	n0_bus0[0]	T6	vddn	V8	n0_bus0_n
K1	esc_gpio[0]	M3	vdde	P5	n0_ctrl_1	T7	srefclk_n	V9	n1_bus0_n
K2	net_config[1]	M4	prefclk	P6	n0_clk_1	T8	vdds	V10	vss
K3	net_config[0]	M5	pll_bypass	P7	vddn	T9	vdds	V11	h0_bus0_n
K4	por_n	M6	jtag_tdi	P8	n0_bus1_p	T10	vdda_serdes	V12	h1_bus0_n
K5	dpu_gpio[7]	M7	pll_mode[1]	P9	n1_bus1_p	T11	vdds	V13	vss
K6	esc_gpio[1]	M8	vddi	P10	vttn_serdes	T12	vdds	V14	rmii_bus0[0]
K7	dpu_gpio[6]	M9	vddi	P11	h0_bus1_p	T13	rmii_bus0[1]	V15	rmii_bus1[0]
K8	vddi	M10	vddi	P12	h1_bus1_p	T14	rmii_bus1[2]	V16	h1_bus0[9]
K9	vss	M11	vddi	P13	h1_bus0[5]	T15	h1_bus0[7]	V17	h1_clk_0
K10	vss	M12	vss	P14	vss	T16	h1_ctrl_0	V18	vss
K11	vss	M13	h1_bus1[1]	P15	h1_bus1[9]	T17	h1_bus0[4]		
K12	h0_bus1[6]	M14	h1_bus1[2]	P16	h1_clk_2	T18	h1_bus0[0]		
K13	h0_bus1[5]	M15	vddh	P17	vddh	U1	n0_bus1[2]		
K14	h0_bus1[3]	M16	h1_bus1[4]	P18	h1_bus1[8]	U2	vddn		
K15	h0_clk_1	M17	vddh	R1	n0_bus0[2]	U3	n0_bus1[3]		
K16	h0_bus1[4]	M18	h1_bus1[3]	R2	vss	U4	n1_bus0[1]		

9.2 8450 Pin List by Signal Name

Table 9-3. 8450 pin list (by signal name) - first half

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
D5	a[0]	C14	dq[3]	F16	ecc[1]	J16	h0_bus1[8]	T16	h1_ctrl_0
D4	a[1]	D15	dq[4]	E18	ecc[2]	J14	h0_bus1[9]	N13	h1_ctrl_1
C3	a[2]	C13	dq[5]	E15	ecc[3]	G14	h0_clk_0	N12	h1_bus1_n
C2	a[3]	A15	dq[6]	D18	ecc[4]	K15	h0_clk_1	P12	h1_bus1_p
C5	a[4]	D14	dq[7]	D17	ecc[5]	J13	h0_clk_2	V12	h1_bus0_n
B4	a[5]	B13	dq[8]	C17	ecc[6]	G13	h0_ctrl_0	U12	h1_bus0_p
D1	a[6]	A14	dq[9]	E16	ecc_dm	K17	h0_ctrl_1	H4	host_config[0]
E2	a[7]	E13	dq[10]	E17	eccs	N11	h0_bus1_n	H6	host_config[1]
E4	a[8]	B12	dq[11]	K1	esc_gpio[0]	P11	h0_bus1_p	H7	host_config[2]
F2	a[9]	E12	dq[12]	K6	esc_gpio[1]	V11	h0_bus0_n	N1	jtag_rst_n
F4	a[10]	C11	dq[13]	L6	esc_gpio[2]	U11	h0_bus0_p	N3	jtag_tck
F1	a[11]	G12	dq[14]	L7	esc_gpio[3]	T18	h1_bus0[0]	M6	jtag_tdi
F5	a[12]	D11	dq[15]	L3	esc_gpio[4]	R17	h1_bus0[1]	N4	jtag_tdo
G1	a[13]\cke	F11	dq[16]	L4	esc_gpio[5]	U18	h1_bus0[2]	N5	jtag_tms
G2	ba[0]	C10	dq[17]	L1	esc_gpio[6]	R16	h1_bus0[3]	P4	n0_bus0[0]
G4	ba[1]	B10	dq[18]	M1	esc_gpio[7]	T17	h1_bus0[4]	P2	n0_bus0[1]
G5	ba[2]	E10	dq[19]	H13	h0_bus0[0]	P13	h1_bus0[5]	R1	n0_bus0[2]
G7	cas_n	B9	dq[20]	H15	h0_bus0[1]	R14	h1_bus0[6]	R3	n0_bus0[3]
H3	cs_n	A9	dq[21]	H16	h0_bus0[2]	T15	h1_bus0[7]	T3	n0_bus1[0]
A16	dm[0]	E9	dq[22]	H17	h0_bus0[3]	U16	h1_bus0[8]	T2	n0_bus1[1]
A12	dm[1]	F8	dq[23]	H18	h0_bus0[4]	V16	h1_bus0[9]	U1	n0_bus1[2]
D9	dm[2]	A8	dq[24]	G15	h0_bus0[5]	L17	h1_bus1[0]	U3	n0_bus1[3]
B7	dm[3]	D8	dq[25]	G16	h0_bus0[6]	M13	h1_bus1[1]	P3	n0_clk_0
J7	dpu_gpio[0]	C8	dq[26]	G17	h0_bus0[7]	M14	h1_bus1[2]	P6	n0_clk_1
J5	dpu_gpio[1]	F7	dq[27]	F13	h0_bus0[8]	M18	h1_bus1[3]	P1	n0_ctrl_0
J4	dpu_gpio[2]	E6	dq[28]	F14	h0_bus0[9]	M16	h1_bus1[4]	P5	n0_ctrl_1
J2	dpu_gpio[3]	C7	dq[29]	L15	h0_bus1[0]	N15	h1_bus1[5]	N8	n0_bus1_n
J1	dpu_gpio[4]	D6	dq[30]	L16	h0_bus1[1]	N17	h1_bus1[6]	P8	n0_bus1_p
J6	dpu_gpio[5]	B6	dq[31]	L13	h0_bus1[2]	N16	h1_bus1[7]	V8	n0_bus0_n
K7	dpu_gpio[6]	A17	dqs[0]	K14	h0_bus1[3]	P18	h1_bus1[8]	U8	n0_bus0_p
K5	dpu_gpio[7]	D12	dqs[1]	K16	h0_bus1[4]	P15	h1_bus1[9]	T4	n1_bus0[0]
C16	dq[0]	F10	dqs[2]	K13	h0_bus1[5]	V17	h1_clk_0	U4	n1_bus0[1]
B16	dq[1]	E7	dqs[3]	K12	h0_bus1[6]	N14	h1_clk_1	R5	n1_bus0[2]
B15	dq[2]	F18	ecc[0]	J18	h0_bus1[7]	P16	h1_clk_2	T5	n1_bus0[3]

Table 9-4. 8450 pin list (by signal name) - second half

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
U5	n1_bus1[0]	M2	vdda_pll	E1	vddr	L14	vss	N10	vtth_serdes
N7	n1_bus1[1]	T10	vdda_serdes	D10	vddr	R18	vss	G6	we_n
V5	n1_bus1[2]	J3	vdde	D13	vddr	N18	vss		
V6	n1_bus1[3]	M3	vdde	D16	vddr	K11	vss		
V3	n1_clk_0	R15	vddh	C4	vddr	K18	vss		
U6	n1_clk_1	M17	vddh	D7	vddr	G18	vss		
V2	n1_ctrl_0	M15	vddh	F12	vddr	H10	vss		
V4	n1_ctrl_1	P17	vddh	F3	vddr	E11	vss		
N9	n1_bus1_n	U17	vddh	F6	vddr	A10	vss		
P9	n1_bus1_p	J15	vddh	F9	vddr	C9	vss		
V9	n1_bus0_n	J17	vddh	H5	vddr	A7	vss		
U9	n1_bus0_p	F15	vddh	T8	vdds	H9	vss		
K3	net_config[0]	M11	vddi	T9	vdds	E8	vss		
K2	net_config[1]	L12	vddi	T11	vdds	C6	vss		
A5	odt	J12	vddi	T12	vdds	A4	vss		
M5	pll_bypass	H12	vddi	B18	vref_ddr[0]	H8	vss		
M7	pll_mode[1]	G11	vddi	A11	vref_ddr[1]	J9	vss		
K4	por_n	G10	vddi	A6	vref_ddr[2]	A1	vss		
M4	prefclk	G9	vddi	L18	vref_host	B3	vss		
H2	ras_n	G8	vddi	T1	vref_netw	E5	vss		
V14	rmii_bus0[0]	J8	vddi	J11	vss	D2	vss		
T13	rmii_bus0[1]	K8	vddi	B17	vss	G3	vss		
U14	rmii_bus0[2]	L8	vddi	J10	vss	H1	vss		
V15	rmii_bus1[0]	M8	vddi	H11	vss	L2	vss		
U15	rmii_bus1[1]	M9	vddi	E14	vss	R2	vss		
T14	rmii_bus1[2]	M10	vddi	A18	vss	K9	vss		
R13	rmii_ref_clk	R4	vddn	C15	vss	V1	vss		
U13	3.3V (vdde)	T6	vddn	R10	vss	R6	vss		
A2	sdclk_diff_n	U2	vddn	R11	vss	L9	vss		
A3	sdclk_diff_p	V7	vddn	L10	vss	U7	vss		
C1	sdclk_fb_i	P7	vddn	V13	vss	R8	vss		
B1	sdclk_fb_o	B11	vddr	R12	vss	R9	vss		
U10	serdes_rref	B14	vddr	K10	vss	V10	vss		
T7	srefclk_n	B2	vddr	L11	vss	P14	vss		
R7	srefclk_p	F17	vddr	V18	vss	H14	vss		
N6	testmode	B5	vddr	M12	vss	E3	vssa_ddr_pll		
L5	vdd_reserved	B8	vddr	A13	vss	N2	vssa_pll		
D3	vdda_ddr_pll	C18	vddr	C12	vss	P10	vttn_serdes		

9.3 Physical Specifications

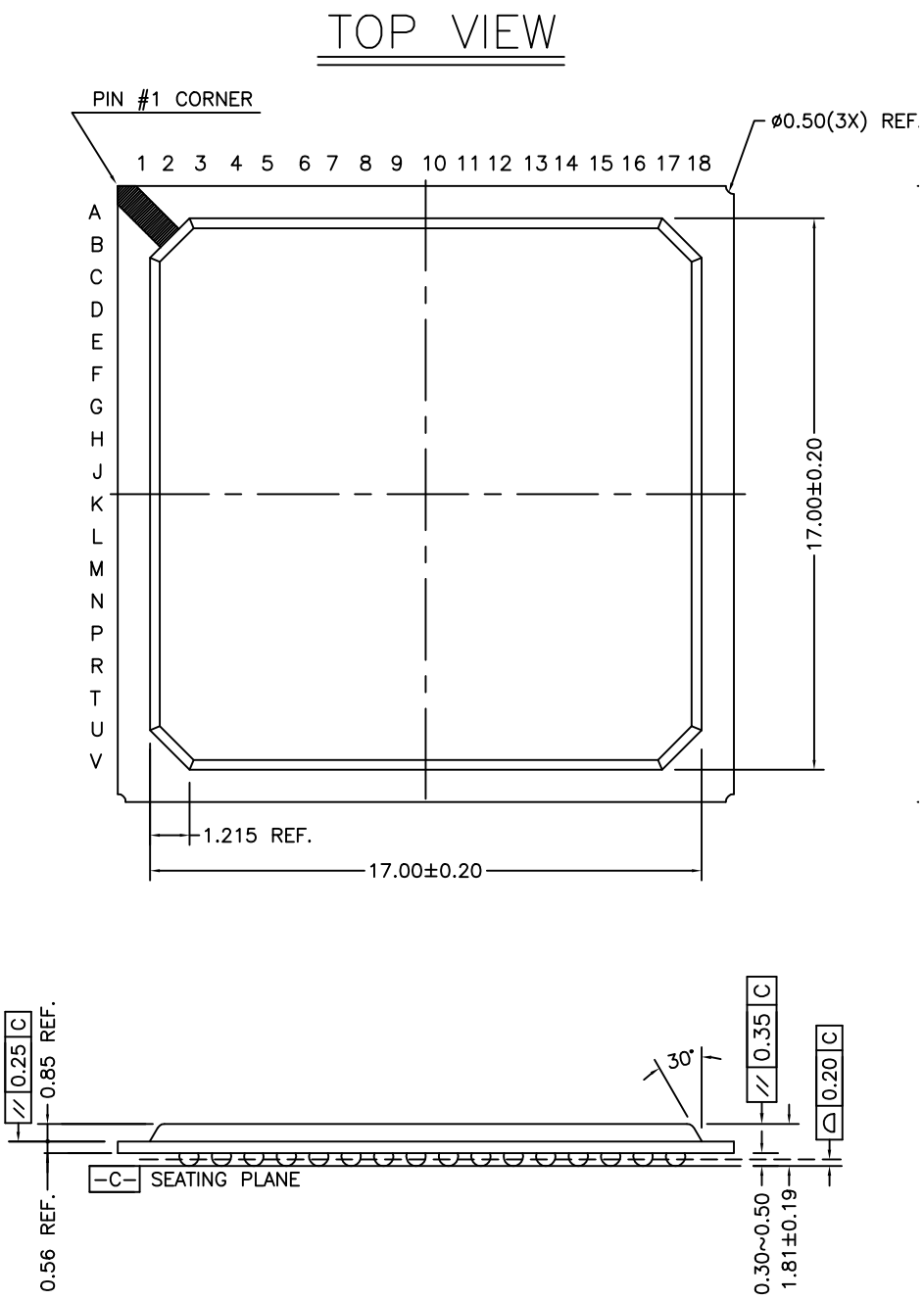


Figure 9-1. Physical Dimensions - Top View

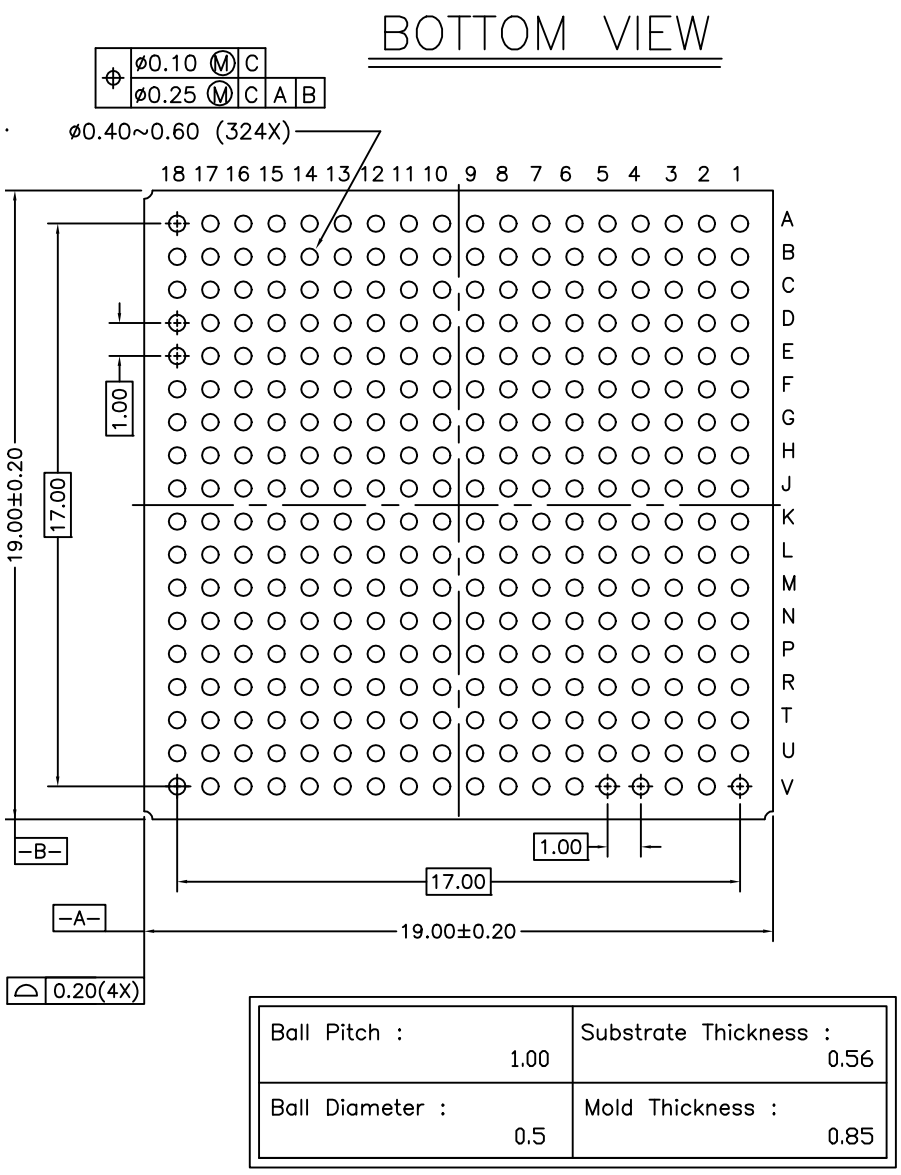


Figure 9-2. Physical Dimensions - Bottom View

I Document Changes/Revisions

Documentation Changes include additions, deletions, and modifications made to this document. This section identifies the changes made in each release of the document.

I.1 Document Revision A

Initial Release.

I.2 Document Revision B

Update 1. All sections: removed references to optional DDR memory.

Update 2. Acronym Section: Deleted duplicate acronyms, added TLS.

Update 3. Chapter 1: Slight revision and clean-up. Changed SA support from 300 to 250.

Update 4. Chapter 2: Minor editorial revisions. Changed SA support from 300 to 250 in Section 2.2.

Update 5. Chapter 3 Section 3.1: Changed IPSec Performance from 2.1 to 2.0.

Update 6. Chapter 4: Slight revision and clean-up. Added details on Post Crypto Processor to Table 5. Section 4.4 updated to more accurately reflect clock domains.

Update 7. Section 4.1 Chip Architecture: replaced Block Diagram.

Update 8. Chapter 5: Minor editorial revisions.

Update 9. Chapter 6: Major update. Added connection diagrams for each GMAC and SDRAM interface. Updated details on GPIO functionality and pin usage.

Update 10. Section 6.2.1.2 Connection drawings: added signal names to Host Side and moved hx_clk_0.

Update 11. Section 6.2.2 GMAC RGMII/RTBI Interface Usage (Host/Network) separated into Section 6.2.2 GMAC RGMII/RTBI Interface Usage (Host) and 6.2.2 GMAC RGMII/RTBI Interface Usage (Network) to correct signal name error.

Update 12. Section 6.4 DDR2 SDRAM Interface: updated description for pins sdclk_fb_i and sdclk_fb_o.

Update 13. Section 6.7 General Purpose Pins, Table 22: changed reset function of dpu_gpio[4] and dpu_gpio[3] to ddr_config1 and ddr_config0; assigned primary use values to dpu_gpio[6:1]. DDR Configuration section rewritten to reflect changes in DDR memory. Added Table 24 DDR2 Memory Configuration Sizing. Added sub-section Fiber PHY Control Signals.

Update 14. Section 6.9 Power and Ground Pins: removed 2.5V(DDR1) from vddr; added vdds, corrected vref_ddr[2:0] to 0.9V for DDR2; added description for vttn_serdes and vtth_serdes; deleted vdda_srefbuf.

Update 15. Section 6.5 PLL Interface, Table 21: Description for pll_ref_clk added "or 125MHz ref clock"; pll_mode[1] now only selects between the 25 and 125MHz input ref clock.

Update 16. Chapter 7: Major update. Modified DC Characteristics for each interface, GMAC, SDRAM, GPIO.

Update 17. Section 7.5 Power Sequencing: added second paragraph further describing the required power sequence.

Update 18. Section 8.1 AC Operating Conditions, Table 33: changed tolerance for core supply voltage (vddi, vdda_pll) to 3%; tolerance for vdde, vddh and vddn to 5%; removed 2.5V for DDR1 for vddr and changed tolerance to 5%; added vdds specs.

Update 19. Section 8.2 PLL Ref Intf Clock Timing, Table 34 125MHz PLL_REF Clock: changed PLL lock time. Table 34 25MHz PLL_REF Clock: changed PLL lock time.

Update 20. Section 8.3 RMII Timing: new timing diagram and table.

Update 21. Section 8.4 GMII Timing(Host Intf): new table.

Update 22. Section 8.5 TBI Timing(Host Intf): new table.

Update 23. Section 8.6 RTBI Timing: added content to this section.

Update 24. Section 8.7 RGMII Timing: added content to this section.

Update 25. Section 8.8 SGMII Timing: added content to this section.

Update 26. Section 8.9 SerDes Timing: added content to this section.

Update 27. Section 8.10 SDRAM Timing: modified text to reflect DDR2 SDRAM only.

Update 28. Chapter 9: Modified a[13] to a[13]\cke and ba[2] to ba[2]\cke.

Update 29. Section 9.1 Pin Lists: undated to reflect pinout changes.

I.3 Document Revision C

Update 1. Section 6.4.1 SDRAM Connection Diagrams: removed the 39-ohm series terms on the data signals.

Update 2. Section 7.2 Package Thermal Specs: added data for 4 and 8 layer PCB boards.

Update 3. Section 7.3 Recommended Operating Conditions: added Table 32 Operating temp derating factor.

Update 4. Section 7.4 DC Characteristics Table 35 GPIO Interface: removed low and high level input current specification. Added low and high level output current. Table 33 GMAC Interface: removed low and high level input current specification.

Update 5. Chapter 8 Timing: updated timing parameters for the DRAM, GMII, TBI, RGMII, RTBI, and RMII interfaces.

I.4 Document Revision 00

Update 1. Changed SA support from 250 to 200. Removed support for MACsec and changed support for SRTP as a future release.

Update 2. Section 1 Integrated Public-Key Processing: changed support for 8192 public key modules to 4096.

Update 3. Section 2.1 VPN Processing: changed on-chip policy support to 256 instead of 512.

Update 4. Section 2.4 Mult Host Intf: Removed RMII mode for the four GMAC interfaces in 10/100 mode.

Update 5. Section 2.8 Ordering Info: updated part numbers.

Update 6. Section 3.1 IPsec Perf: changed small packet performance to 550 Kpps.

Update 7. Section 4.2 Packet Proc Operation, Table 4: corrected number of policies supported for Embedded TCAM memory.

Update 8. Section 5.4 Security Policy and SAD Management: corrected number of security policies supported.

Update 9. Section 6.1 Signal Overview, Fig 6: renamed r_ref to serdes_rref, h_vtt to vtth_serdes and n_tt to vttn_serdes.

Update 10. Section 6.2.4 GMAC SERDES and SGMII Interface: added description of SERDES_RREF signal.

Update 11. Sections 6.2.4.2: replaced r_ref with SERDES_RREF in all connection diagrams. Renamed vttn with vttx_serdes, where x = host or network.

Update 12. Section 6.2.4.3 GMAC SERDES and SGMII Interface Usage: described how to terminate unused interfaces.

Update 1. Section 6.3 RMII Interface: added ref to RMII_VDD ball number.

Update 2. Section 6.4.4 No SDRAM Configuration: added this new section.

Update 3. Section 6.5 PLL Interface: corrected signal named PLL_REF_CLK to PREFCLK. Clarified that PLL interface signals are referenced to VDDE.

Update 4. Section 6.6 JTAG Interface: Clarified that JTAG interface signals are referenced to VDDE.

Update 5. Section 6.7 GPIO Interface: Clarified that GPIO interface signals are need to be terminated and are referenced to VDDE. Removed Optional in heading for Device ID, RMII/RTBI Voltage Select, Boot Rate Select, RMII MAC/PHY Select, DDR2 Config sections.

Update 6. Section 6.9 Power and Ground Pins: qualified vdd_reserved as test pin. Added option of connecting vddn and vddh to 3.3V if the host and network ports are configured for SERDES/GMII.

Update 7. Section 7.1 Absolute Max Ratings: changed max for vddn to 2.5v from 1.65v. Removed ref to vdda_srefbuf.

Update 8. Section 7.3 Recommended Operating Conditions: removed ref to vdda_srefbuf. Replaced Operating Temp with Ambient Operating Temp (0-70C). Removed Temperature Derating information.

Update 9. Corrected duplicate entry for ball G18 in table 54.

I.5 Document Revision 01

Update 1. Preface: added reference to the Product Release Notes.

Update 2. Section 2.2 Features: corrected policy lookup performance and added ref to Perf App Note.

Update 3. Section 3 Perf Summary: added ref to Perf App Note.

Update 4. Section 3.1 IPsec Perf: updated small packet size perf.

Update 5. Section 6.4.4 No SDRAM Config: corrected connection for VREF_DDR[2:0].

I.6 Document Revision 02

Update 1. Section 6.2.4.2 GMAC SerDes Connection Diagrams: Corrected drawings Fig 6-15 through 6-18.

I.7 Document Revision 03

Update 1. Section 2.7 Other Features: added part number for rev 3.

I.8 Document Revision 04

Update 1. Section 2.7 Other Features: corrected part number for rev 3.

I.9 Document Revision 05

Update 1. Chapter 1: added reference to Release Notes for the number of supported SAs.

Update 2. Removed all references to the Boot Flash workaround as this is fixed in Rev 3 of the device.

Update 3. Section 4.2 Packet Processing: added reference to Release Notes for the number of supported SAs.

Update 4. Corrected some performance specifications to reflect actual test results.

Update 5. Section 6.6 JTAG Interface: added JTAG ID table.

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