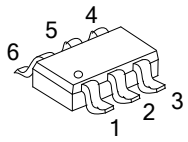
LOW QUIESCENT CURRENT PROGRAMMABLE-DELAY SUPERVISORY CIRCUIT



SOT-23-6
(JDEDE TO-236)

■ DESCRIPTION

The **84NXX** can monitor and provide reset function for system voltages from 0.4V which is the microprocessor supervisory circuit. If the SENSE voltage falls below its threshold (V_{IT}), the voltage of manual reset ($\overline{MR}$) is pulled to a logic low, the $\overline{RESET}$ signal will be asserted. The reset voltage can be factory-set from 0.9V to 5V, while the **84NXX** reset voltage is adjustable with an external resistor divider. When SENSE voltage and $\overline{MR}$ exceed their thresholds, $\overline{RESET}$ is driven to a logic high after a user-programmable delay time.

The **84NXX** has a very low quiescent, which makes it ideal suitable for battery-powered applications. It provides a precision reference to achieve ±1% threshold accuracy. A capacitor is connected between C_{DELAY} and GND which determined reset delay time, allowing the user to select any delay time from 2.1ms to 10s. When the C_{DELAY} pin connected to V_{CC}, the delay time is selected 380ms ,while leaving the C_{DELAY} pin float, the delay time is selected 24ms.

■ FEATURES

* Standard Voltage Rails From 0.9V to 5V and Adjustable Voltage From 0.4V are Available
* Low Quiescent Current: 1.6uA (typ.)
* Delay Time: 2.1ms to 10s
* High Threshold Accuracy: ±1% (typ.)
* Manual Reset ($\overline{MR}$) Input
* Open-Drain $\overline{RESET}$ Output
* Immune to Short Negative SENSE voltage
* Guaranteed Reset Valid to V_{CC}: 0.8V

■ ORDERING INFORMATION

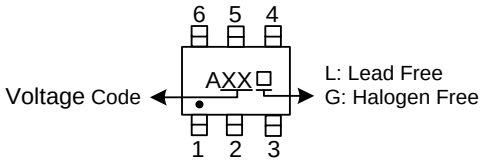
Ordering Number		Package	Packing
Lead Free	Halogen Free		
84NXXL-AE6-R	84NXXG-AE6-R	SOT-23-6	Tape Reel

84NXXG-AE6-R

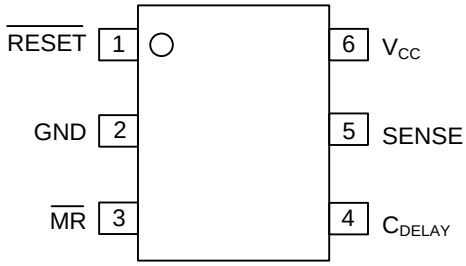
(1)Packing Type
(2)Package Type
(3)Green Package
(4)Output Voltage Code

(1) R: Tape Reel
(2) AE6: SOT-23-6
(3) G: Halogen Free and Lead Free, L: Lead Free
(4) XX: refer to Marking Information

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-23-6	04: ADJ	

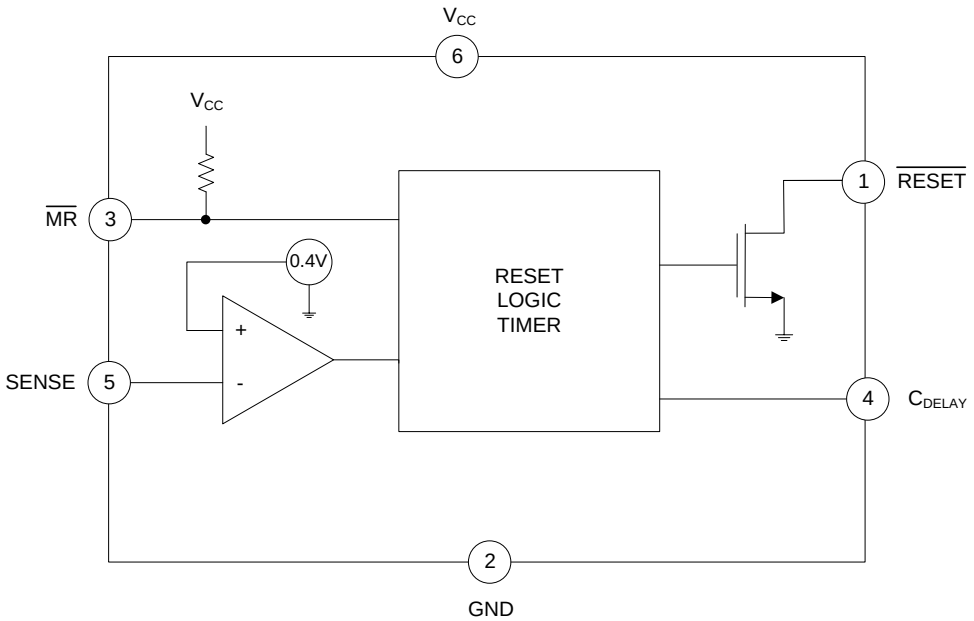
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	PIN NAME	Description
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is an open drain signal which will be asserted when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin drops to a logic low.
2	GND	Ground.
3	$\overline{\text{MR}}$	The manual reset ($\overline{\text{MR}}$) can introduce another logic signal to control the $\overline{\text{RESET}}$.
4	C_{DELAY}	Programmable reset delay time pin.
5	SENSE	SENSE pin is connected to the monitored system voltage.
6	V_{CC}	Supply voltage. A 0.1uF decoupling ceramic capacitor should be put close to this pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	6.5	V
C_{DELAY} Voltage	V_{CDELAY}	V_{CC} + 0.3	V
SENSE Voltage	V_{SENSE}	6	V
All Other Pins		6.5	V
$\overline{\text{RESET}}$ Current	$I_{\overline{\text{RESET}}}$	5	mA
Power Dissipation (Note 3)	P_D	0.57	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Exceeding these ratings may damage the device.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{IN}	1.8 ~ 6	V
Junction Temperature	T_J	-40 ~ +125	°C

Note: The device is not guaranteed to function outside of its operating conditions.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	220	°C/W
Junction to Case	θ_{JC}	110	°C/W

■ ELECTRICAL CHARACTERISTICS

(1.8V≤V_{CC}≤6V, R_3=100kΩ , C_3=47pF, T_A= -40°C~+85°C, Typical values are at T_A=25°C, unless otherwise specified.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{CC}		1.8		6	V
Supply Current (Current Into V_{CC} Pin)	I_{CC}	V_{CC}= 3.3V, $\overline{RESET}$ not asserted. $\overline{MR}$, $\overline{RESET}$, C_{DELAY} open		1.6	3.5	μA
		V_{CC}= 6V, $\overline{RESET}$ not asserted. $\overline{MR}$, $\overline{RESET}$, C_{DELAY} open		1.85	12	μA
Low-level Output Voltage	V_{OL}	1.3V ≤ V_{CC}< 1.8V, I_{OL}= 0.4mA			0.3	V
		1.8V ≤ V_{CC}≤ 6V, I_{OL}= 1.0mA			0.4	V
Power-Up Reset Voltage (Note 1)		V_{OL_MAX} = 0.2V, $I_{\overline{RESET}}$ =15uA $T_{Rise(Vcc)}$≥ 15μs/V			0.8	V
Negative-going Input Threshold Accuracy	V_{IT}	V_{SENSE} falling slowly		±1.0	±2.0	%
Hysteresis on V_{IT} Pin	V_{HYS}			1.5	3.5	V_{IT}%
$\overline{MR}$ Internal Pull-up Resistance	$R_{\overline{MR}}$		50	110		kΩ
Input Current at SENSE Pin	I_{SENSE}	84N04 V_{SENSE}= V_{IT}	-25		+25	nA
		Fixed versions, V_{SENSE}=6V		2.4		μA
$\overline{RESET}$ Leakage Current		V_{SENSE}=6V, $\overline{RESET}$ not asserted			300	nA
$\overline{MR}$ Logic Low Input	V_{IL}				0.25V_{CC}	V
$\overline{MR}$ Logic High Input	V_{IH}		0.7V_{CC}			V
SENSE Maximum Transient Duration	t_w	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		17.5		μs
$\overline{RESET}$ Delay Time	t_d	C_{DELAY}= Open	15	24	34	ms
		C_{DELAY} = V_{CC} (Note 2)	230	380	530	ms
		C_{DELAY}= 150pF	1.3	2.1	3	ms
		C_{DELAY} = 10nF (Note 2)	61	102	142	ms
$\overline{MR}$ to $\overline{RESET}$ Propagation Delay	t_{pHL1}	V_{IH}= 0.7 V_{CC}, V_{IL}= 0.25 V_{CC}		160		ns
High to Low Level $\overline{RESET}$ Delay, SENSE to $\overline{RESET}$	t_{pHL2}	V_{IH}= 1.05 V_{IT}, V_{IL}= 0.95 V_{IT}		17.5		μs

Notes: 1. The lowest supply voltage (V_{CC}) at which $\overline{RESET}$ becomes active.
2. Guaranteed by design.

■ STANDARD VERSIONS

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})
84N04	Adjustable	0.4V

■ FUNCTIONAL DESCRIPTION

$\overline{\text{RESET}}$ Output Function

The **84NXX** $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pull up resistor must be connected to hold this signal high, when $\overline{\text{RESET}}$ is not asserted. If the voltage is below 0.8V, $\overline{\text{RESET}}$ output is undefined. This condition can be ignored generally because that most microprocessors do not function at this state. When both SENSE and $\overline{\text{MR}}$ are higher than their threshold voltage, $\overline{\text{RESET}}$ output holds logic high. Once either of the two drops below their threshold, $\overline{\text{RESET}}$ will be asserted.

From the point that $\overline{\text{MR}}$ is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), $\overline{\text{RESET}}$ will be driven to a logic high after a reset delay time. The reset delay time is programmable by C_{DELAY} pin.

Monitor Multiple System Voltages

The manual reset ($\overline{\text{MR}}$) can introduce another logic signal to control the $\overline{\text{RESET}}$. When $\overline{\text{MR}}$ is a logic low (0.25*V_{CC}), $\overline{\text{RESET}}$ will be asserted. After both SENSE and $\overline{\text{MR}}$ are above their thresholds, $\overline{\text{RESET}}$ will be a logic high after a reset delay time. The $\overline{\text{MR}}$ is internally connected to V_{CC} through a 90kΩ resistor so this pin can float. If the signal on $\overline{\text{MR}}$ isn't up to V_{CC}, there will be an additional current through the 90k Ω pull up resistor. A logic-level FET can be used to minimize the leakage.

Monitor a Voltage

The SENSE input pin is connected to the monitored system or through a resistor network. When the voltage on the pin is below V_{IT}, $\overline{\text{RESET}}$ will be asserted. A threshold hysteresis will prevent the chip from responding perturbation on SENSE pin. A 1nF to 10nF bypass capacitor should be put on this pin. A typical application of the **84NXX** is shown in Figure 2. Two external resistors form a voltage divider from monitored voltage to GND. Its tap connects to the SENSE pin. The circuit can be used to monitor any voltage higher than 0.4V.

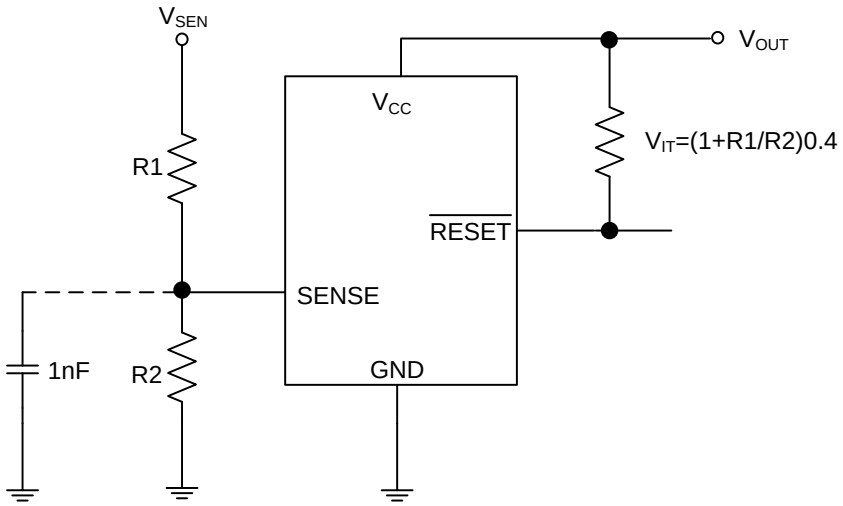


Figure 2. 84N04 MonitorIng a User- Defined Voltage

■ FUNCTIONAL DESCRIPTION (Cont.)

Programmable Reset Delay Time

The reset delay time can be programmed by C_{DELAY} configure. When C_{DELAY} is connected to V_{CC} through a resistor between 50k Ω and 200kΩ, the delay time is 380ms. When C_{DELAY} floated, the delay time is 24ms. A capacitor connected C_{DELAY} to GND could be used to get the user's programmable delay time from 2.1ms to 10s. The three configures can be found in Figure 3. (a)(b)(c).

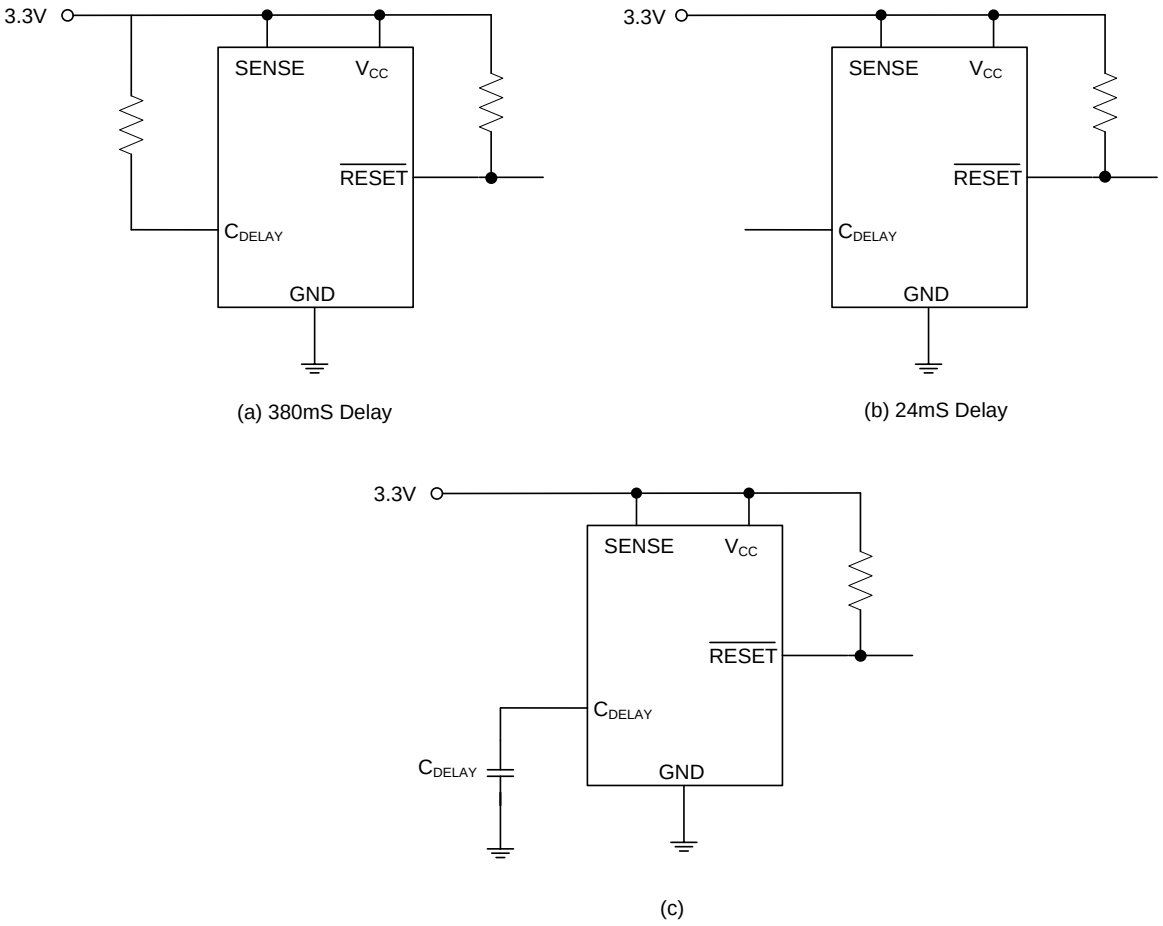


Figure 3. Programmable Configurations to the Reset Delay Time

SENSE Voltage Transients Immunity

The **84NXX** can be immune to SENSE pin short negative transient. The maximum immune duration is 17us while overdrive is 5%. A shorter negative transient can not assert the $\overline{RESET}$ output. The effective duration is relative to the threshold overdrive.

■ TYPICAL APPLICATION CIRCUIT