

# MOS FIELD EFFECT TRANSISTOR

## 84N06CLD, NP84N06DLD, NP84N06ELD

### SWITCHING

#### N-CHANNEL POWER MOS FET

#### INDUSTRIAL USE

#### DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance  
 $R_{DS(on)1} = 6.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 42 \text{ A)}$   
 $R_{DS(on)2} = 9.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 35 \text{ A)}$
- Built-in gate protection diode

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
NP84N06CLD	TO-220AB
NP84N06DLD	TO-262
NP84N06ELD	TO-263

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) <sup>Note1</sup>	$I_{D(DC)}$	$\pm 84$	A
Drain Current (Pulse) <sup>Note2</sup>	$I_{D(pulse)}$	$\pm 280$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T1}$	1.8	W
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T2}$	185	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	<b>Figure4</b>	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	<b>Figure4</b>	mJ
Repetitive Avalanche Current <sup>Note4</sup>	$I_{AR}$	70	A
Repetitive Avalanche Energy <sup>Note4</sup>	$E_{AR}$	490	mJ

- Notes**
1. Package Limit =  $\pm 75 \text{ A}$
  2.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1 \%$
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$
  4.  $T_{ch} \leq 175^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$ , Duty cycle  $\leq 3\%$

#### THERMAL RESISTANCE

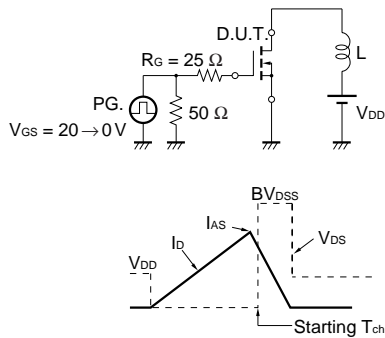
Channel to Case	$R_{th(ch-C)}$	0.81	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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**Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

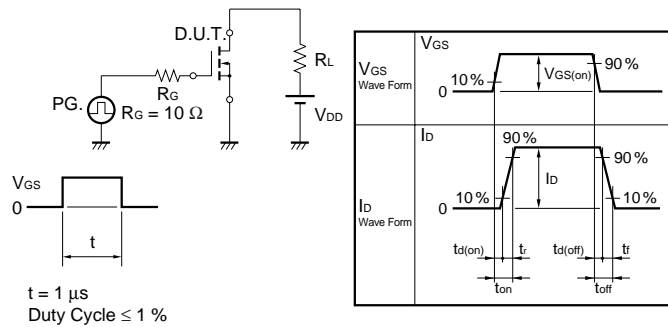
**ELECTRICAL CHARACTERISTICS (TA = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 42 A		5.5	6.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 35 A		6.4	9.5	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 35 A		7.0	10.5	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 35 A	20	94		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		7200	10900	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		2000	3000	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		700	1300	pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 35 A		50	110	ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		650	1700	ns
Turn-off Delay Time	T <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		450	900	ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		800	2000	ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 70 A		150	230	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 48 V		19		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		40		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 70 A, V <sub>GS</sub> = 0 V		0.97		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 70A, V <sub>GS</sub> = 0 V		80		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs		256		nC

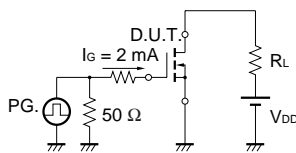
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**



TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

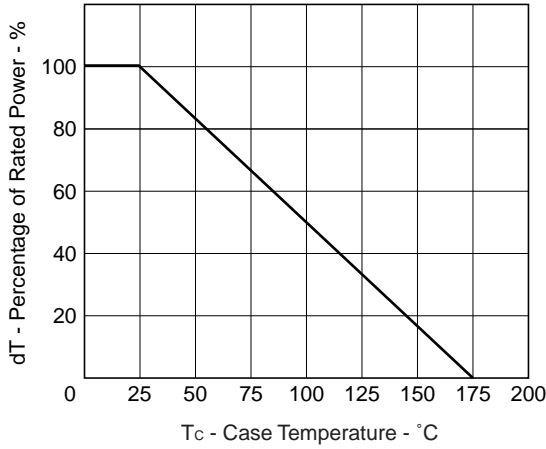


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

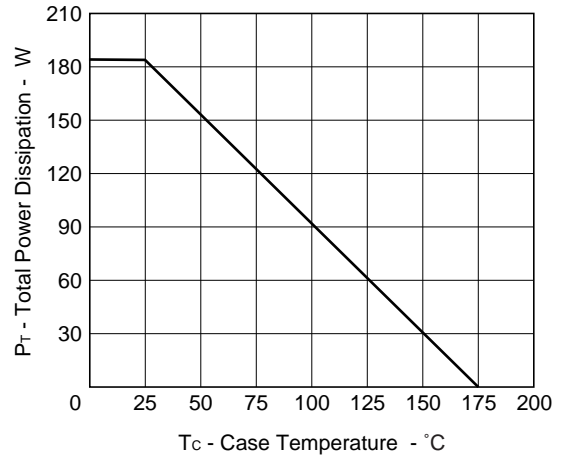


Figure3. FORWARD BIAS SAFE OPERATING AREA

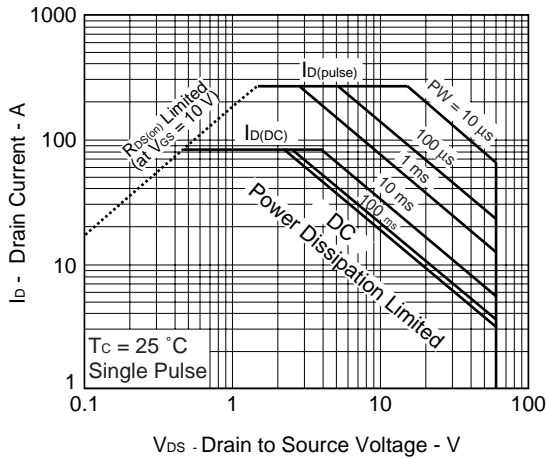


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

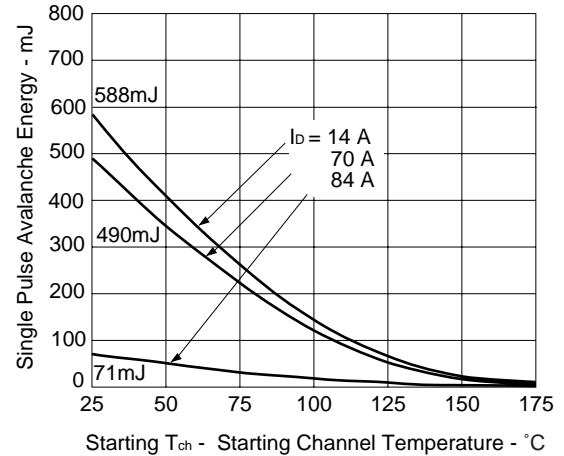


Figure5. FORWARD TRANSFER CHARACTERISTICS

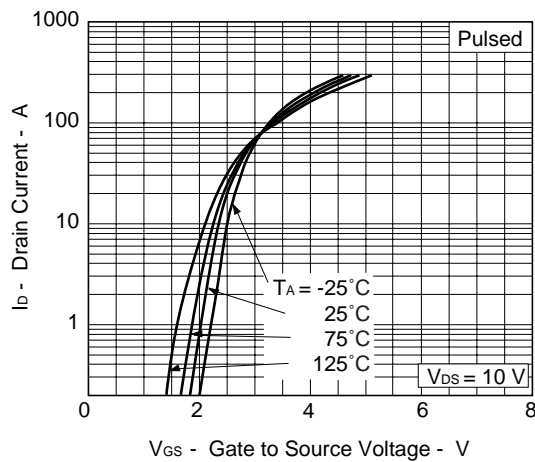


Figure6. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

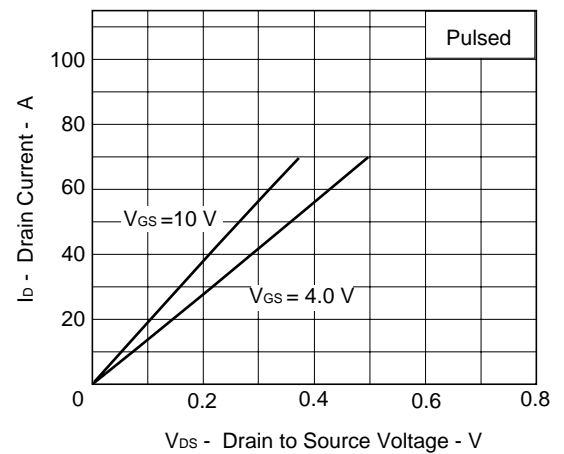


Figure7. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

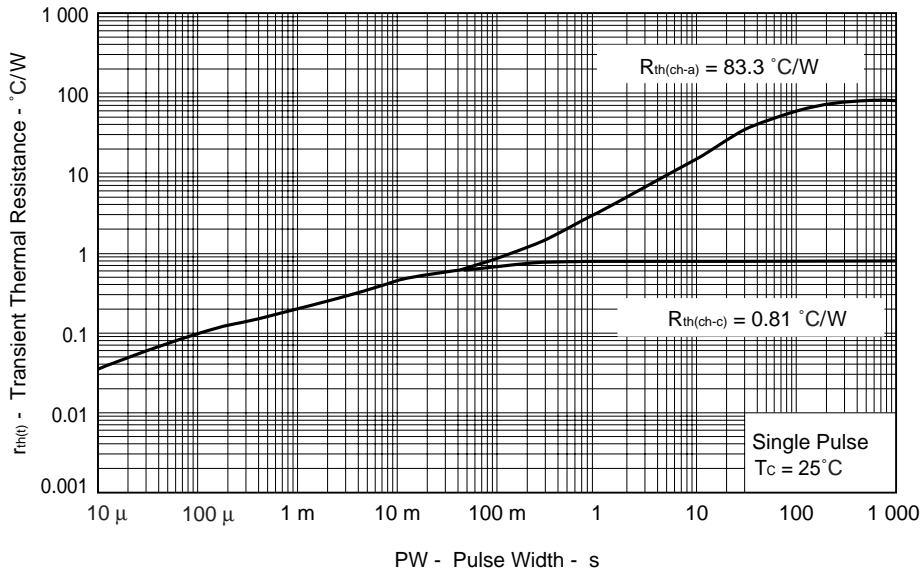


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

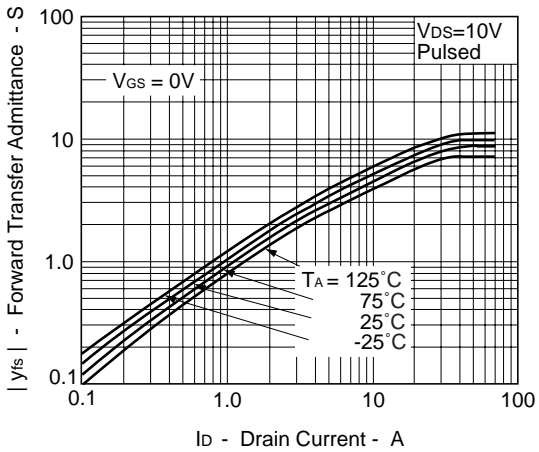


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

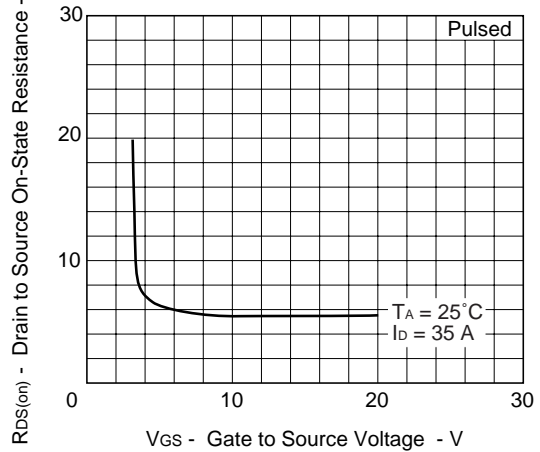


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

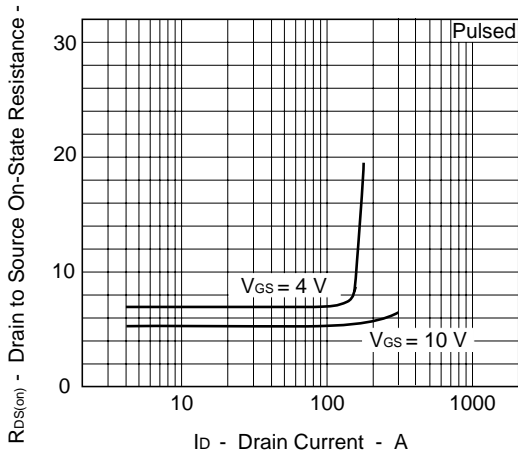


Figure11. GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

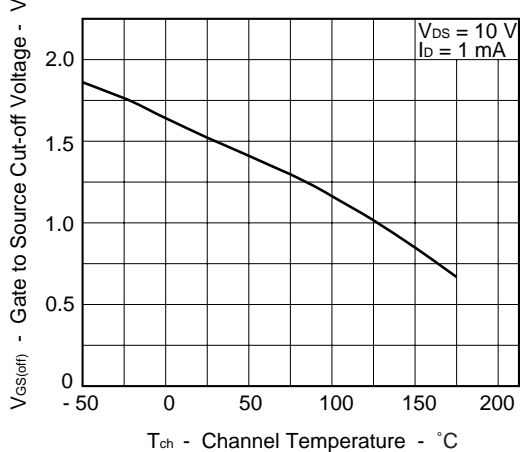


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

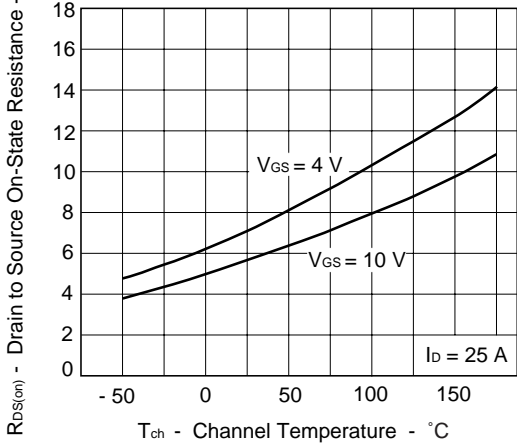


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

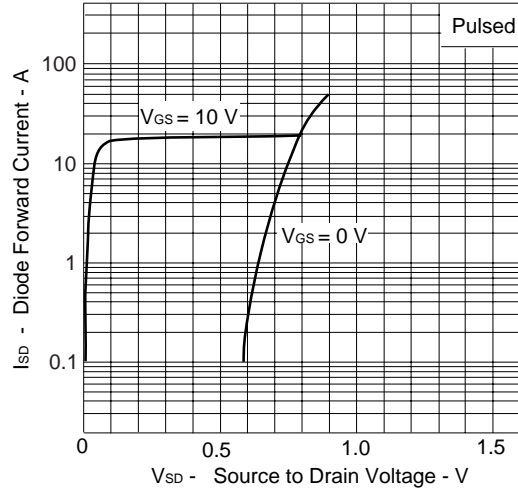


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

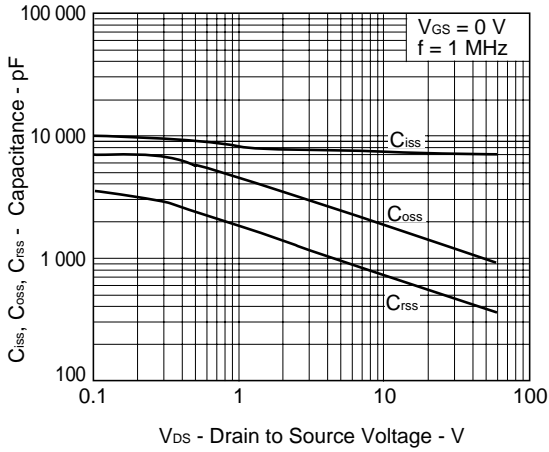


Figure15. SWITCHING CHARACTERISTICS

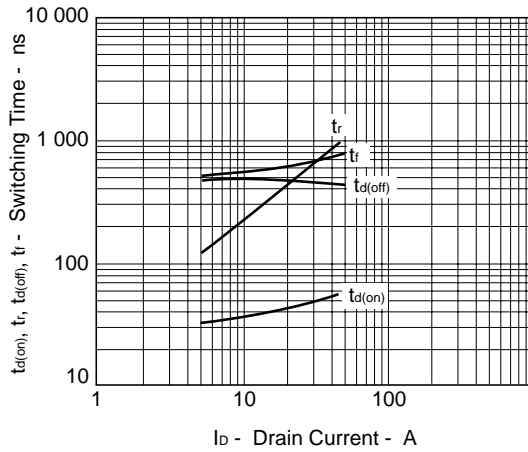


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

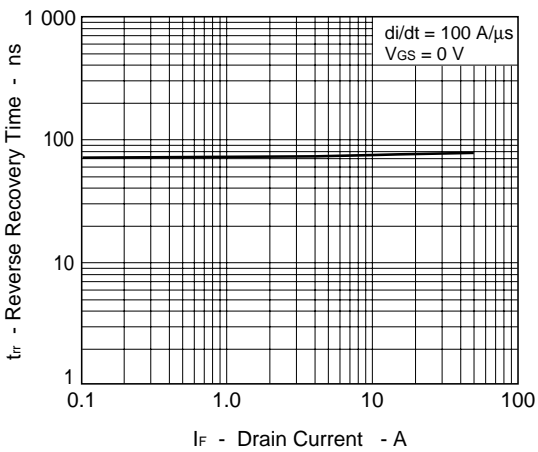
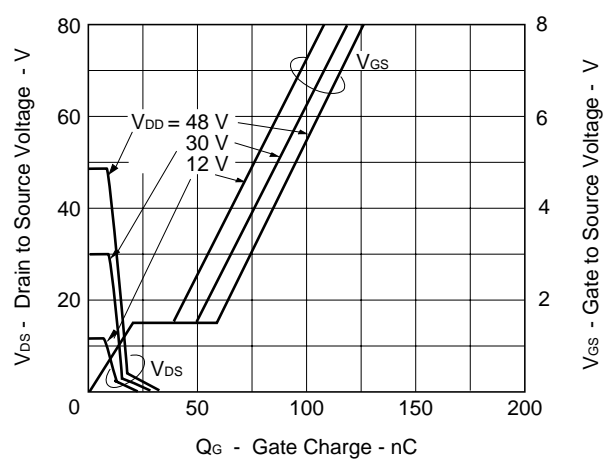
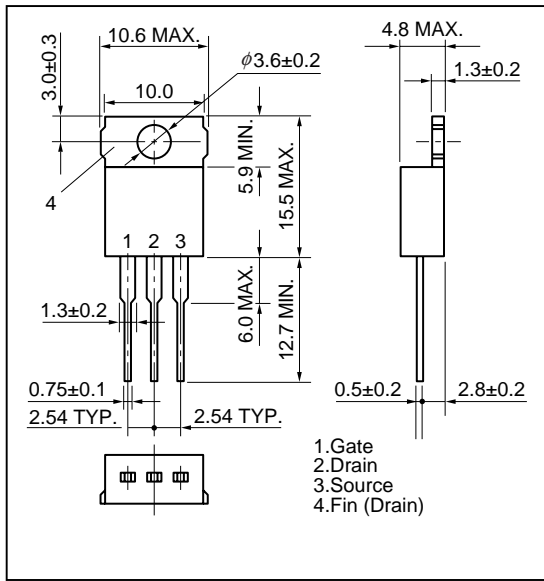


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

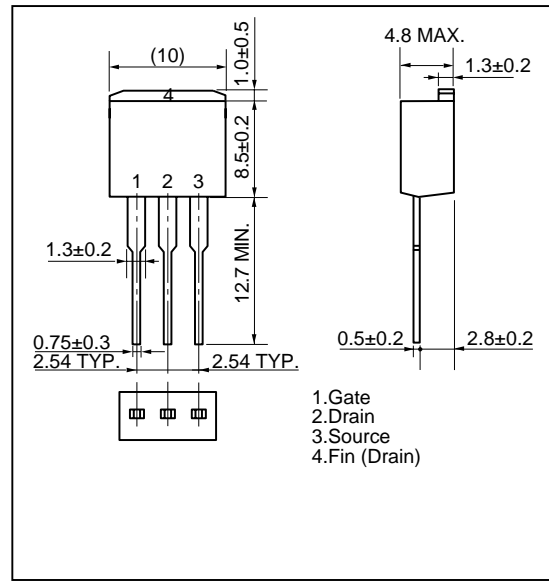


PACKAGE DRAWINGS (Unit : mm)

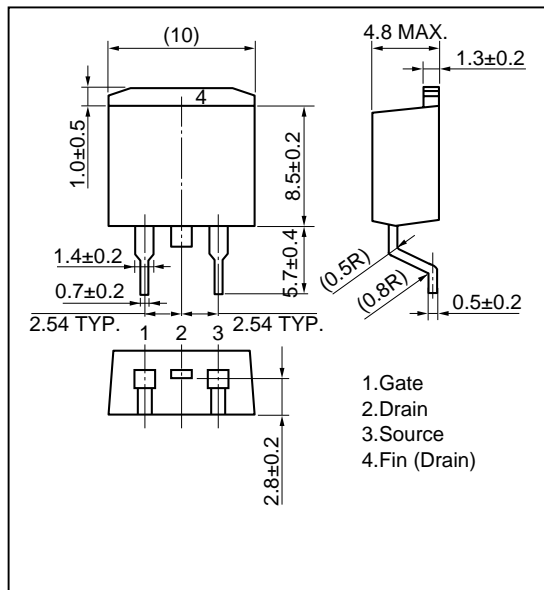
1)TO-220AB (MP-25)



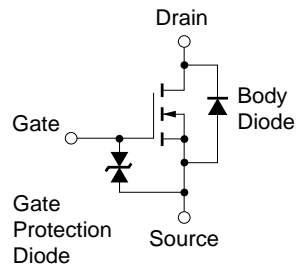
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (JEDEC TYPE:MP-25ZJ)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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