Low Skew, 1-to-8, Differential-to-0.7V HCSL Clock Distribution Chip

85108

DATA SHEET

General Description

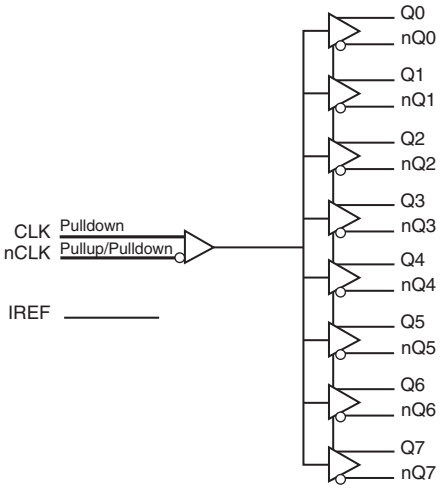
The 85108 is a low skew, high performance 1-to-8 Differential-to-0.7V HCSL Clock Distribution Chip. The 85108 CLK, nCLK pair can accept most differential input levels and translates them to 3.3V HCSL output levels. The 85108 provides a low power, low noise, low skew, point-to-point solution for distributing HCSL clock signals.

Guaranteed output and part-to-part skew specifications make the 85108 ideal for those applications demanding well defined performance and repeatability.

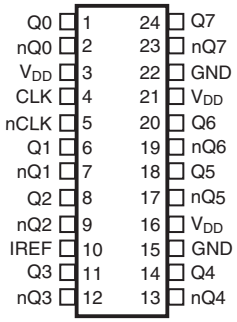
Features

- Eight 0.7V differential HCSL clock output pairs
- CLK/nCLK input pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 500MHz
- Additive phase jitter, RMS: 0.09ps (typical)
- Output skew: 80ps (maximum)
- Part-to-part skew: 400ps (maximum)
- Propagation delay: 3ns (maximum)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



85108

24-Lead TSSOP, 173-MIL
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. HCSL interface levels.
3, 16, 21	V_{DD}	Power		Power supply pins.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input.
6, 7	Q1, nQ1	Output		Differential output pair. HCSL interface levels.
8, 9	Q2, nQ2	Output		Differential output pair. HCSL interface levels.
10	IREF			External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx/nQx clock outputs.
11, 12	Q3, nQ3	Output		Differential output pair. HCSL interface levels.
13, 14	nQ4, Q4	Output		Differential output pair. HCSL interface levels.
15, 22	GND	Power		Power supply ground.
17, 18	nQ5, Q5	Output		Differential output pair. HCSL interface levels.
19, 20	nQ6, Q6	Output		Differential output pair. HCSL interface levels.
23, 24	nQ7, Q7	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistors			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistors			51		kΩ

Function Tables

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q[0:7]	n[0:7]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section *Wiring the Differential Input to Accept Single Ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	87.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current				27	mA

Table 4B. Differential DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.63V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.63V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.635V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

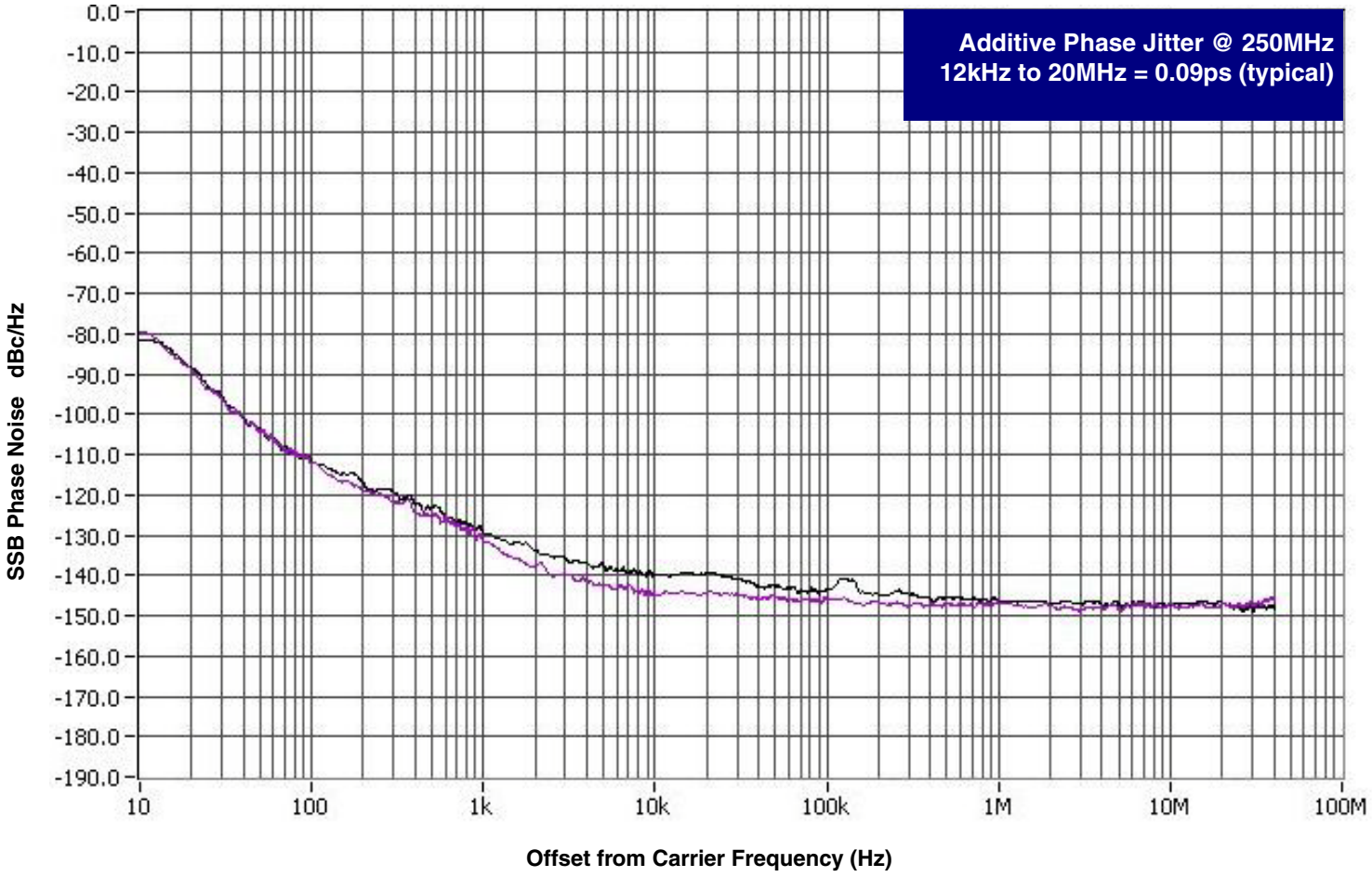
Table 5. HCSL AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay; NOTE 1		1.5		3	ns
tsk(o)	Output Skew; NOTE 2, 3				80	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				400	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	250MHz, Integration Range: 12kHz – 20MHz		0.09		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 5, 6		500			ps
V_{MAX}	Absolute Maximum Output Voltage; NOTE 7, 8				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 7, 9		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12				140	mV
	Rise/Fall Edge Rate; NOTE 5, 13	Measured between -150mV to +150mV	0.6		5.5	V/ns
odc	Output Duty Cycle; NOTE 14		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq 250$MHz unless noted otherwise.
NOTE 1: Measured from the differential input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range. See Parameter Measurement Information Section.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 12: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 14: Input duty cycle must be 50%.

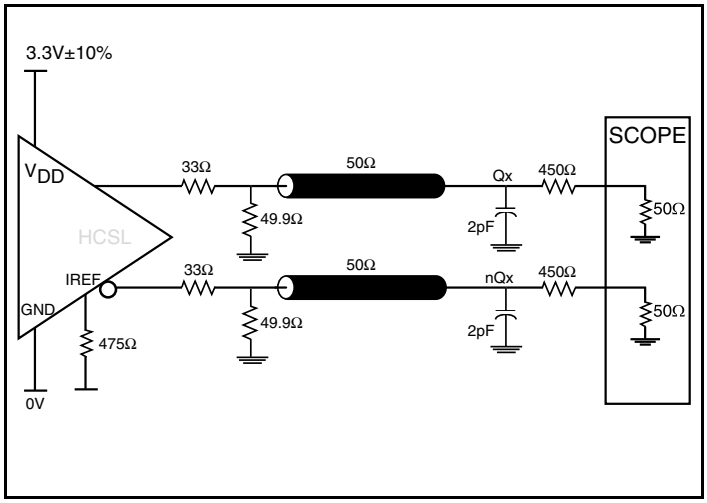
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

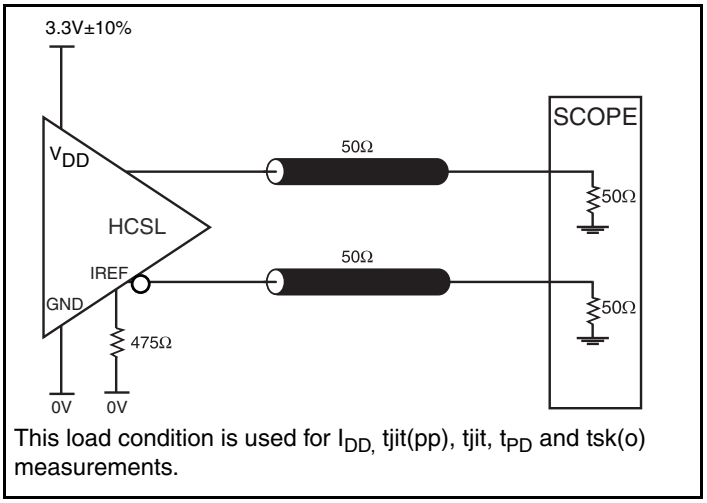


As with most timing specifications, phase noise measurements hase issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Parameter Measurement Information

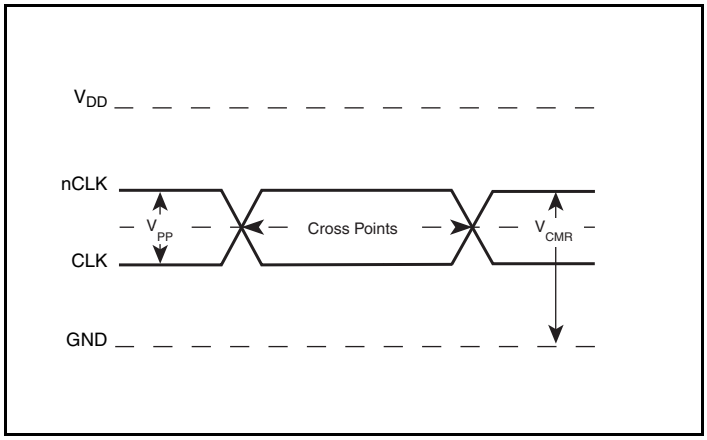


Output Load AC Test Circuit

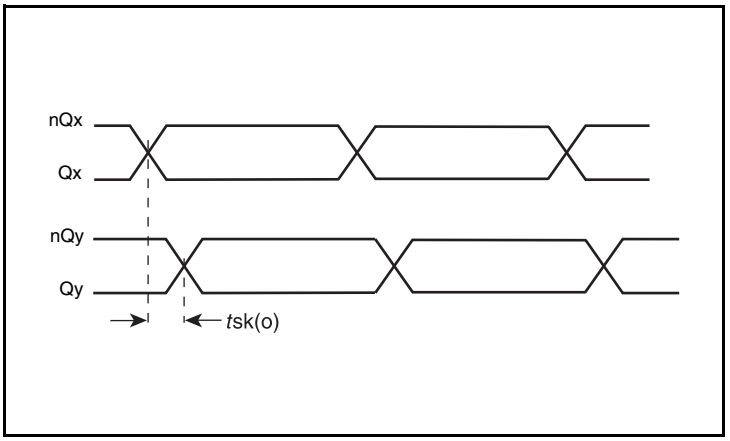


This load condition is used for I_{DD}, tjit(pp), tjit, t_{PD} and tsk(o) measurements.

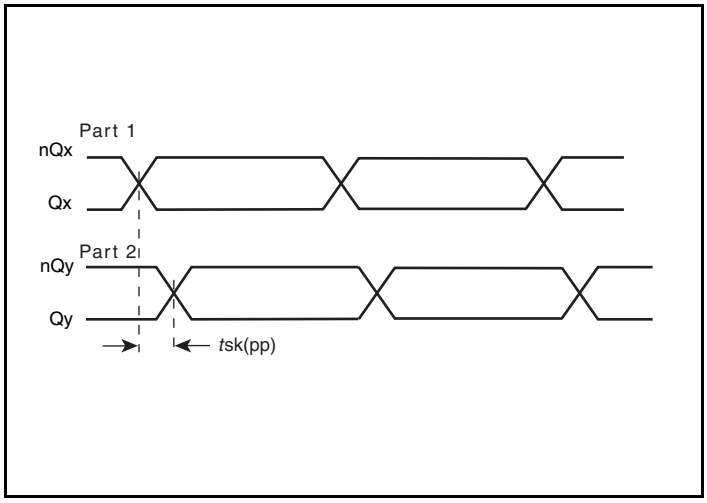
Output Load AC Test Circuit



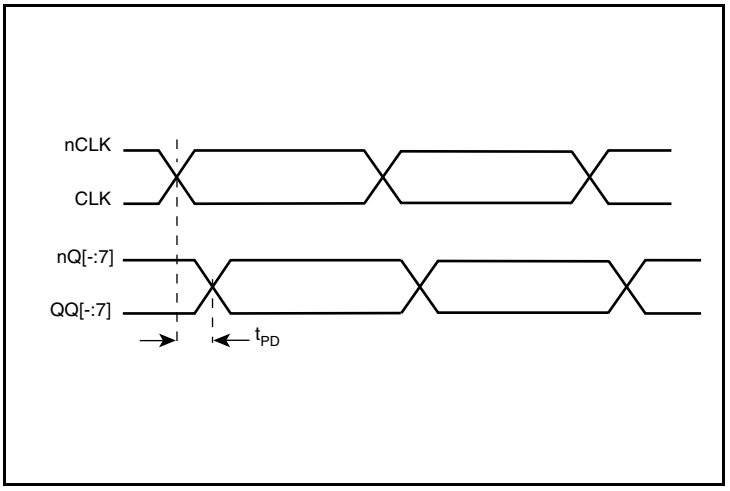
Differential Input Level



Output Skew

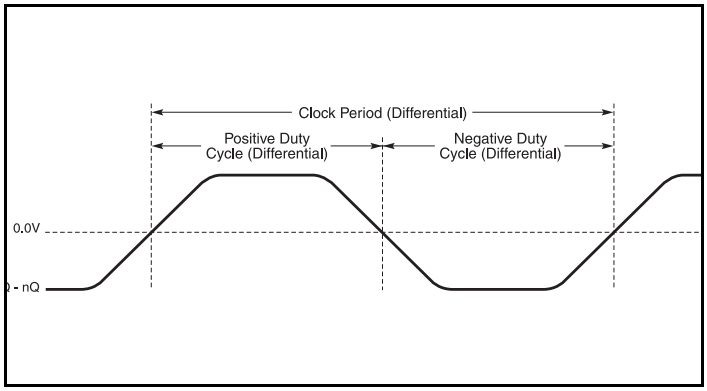


Part-to-Part Skew

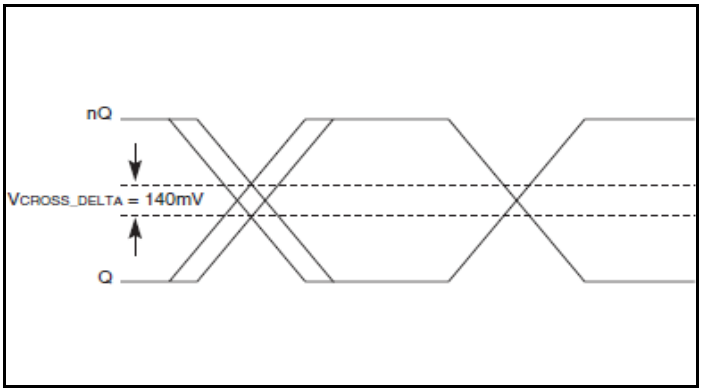


Propagation Delay

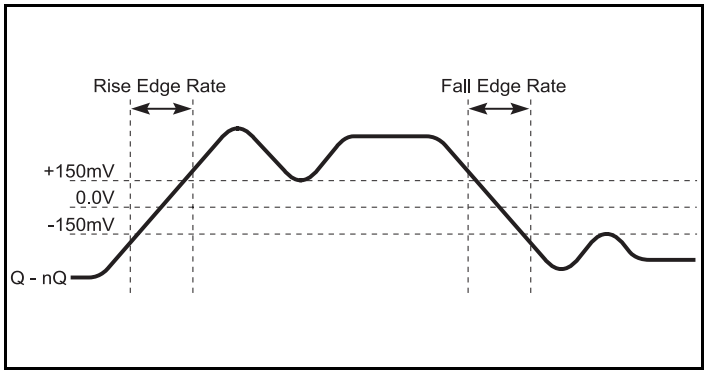
Parameter Measurement Information, continued



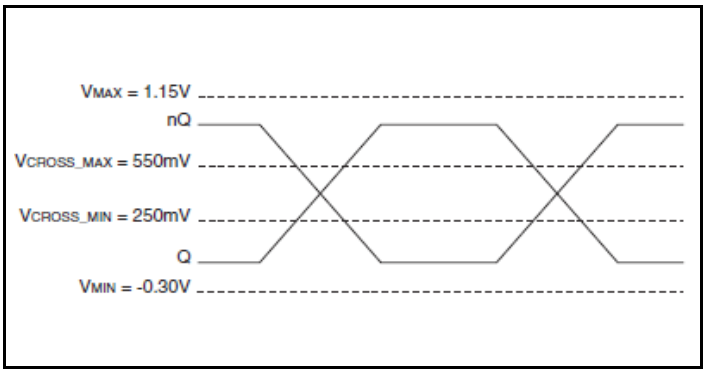
Differential Measurement Points for Duty Cycle/Period



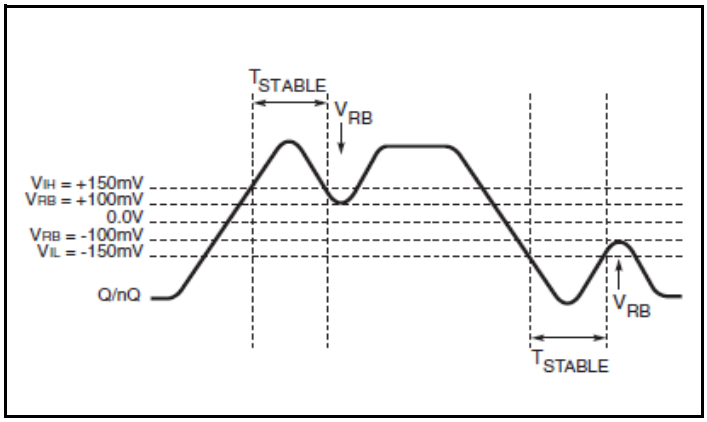
Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Rise/Fall Edge Rate



Single-ended Measurement Points for Absolute Cross Point/Swing



Differential Measurement Points for Ringback

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

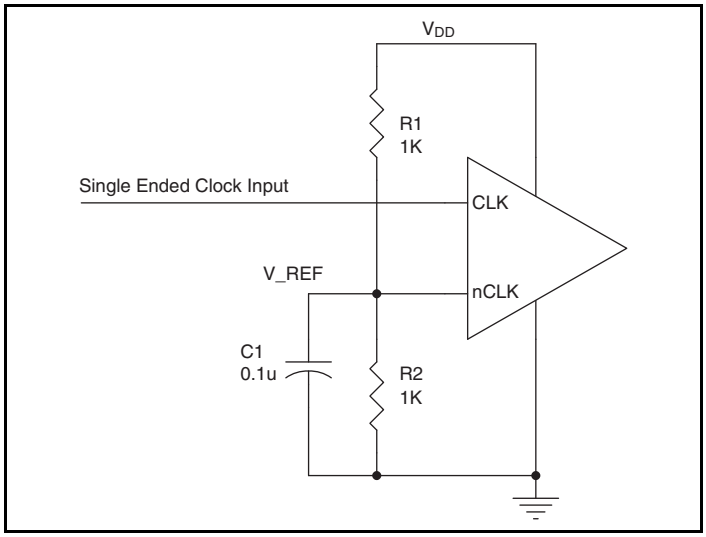


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Output Pins

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. The differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

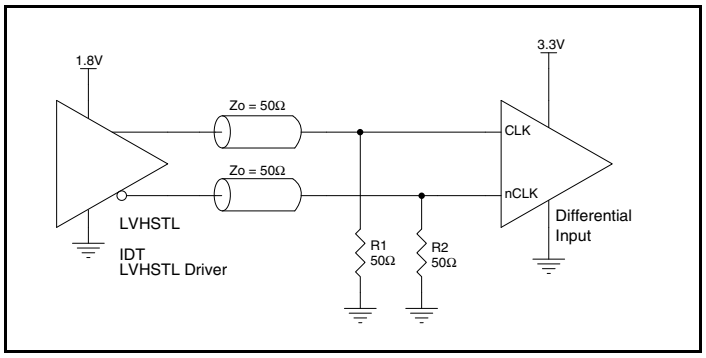


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

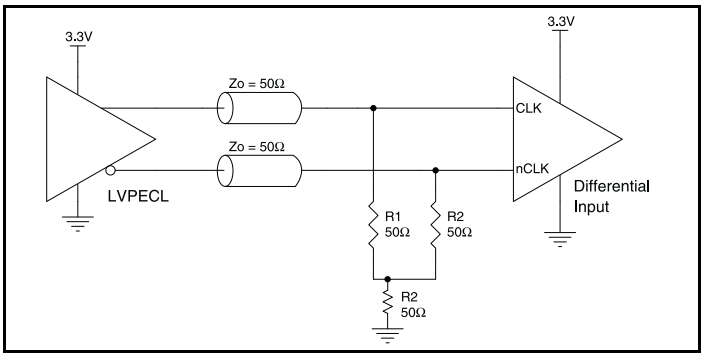


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

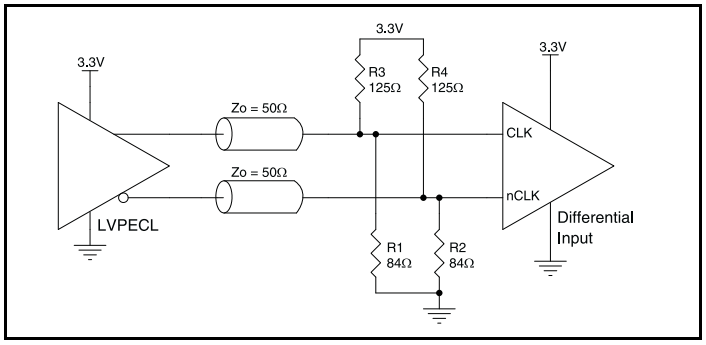


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

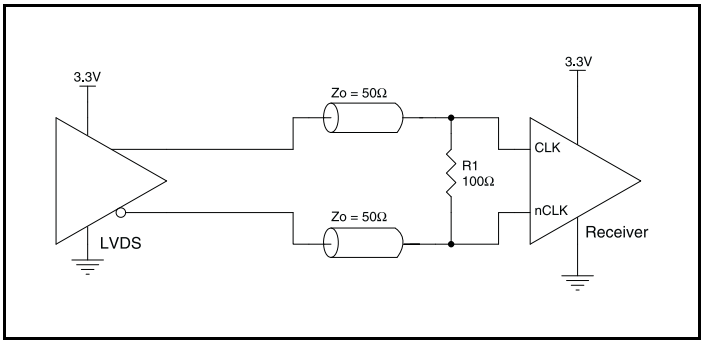


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

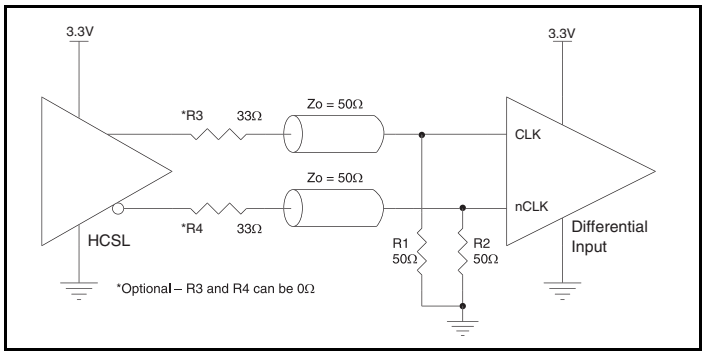


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

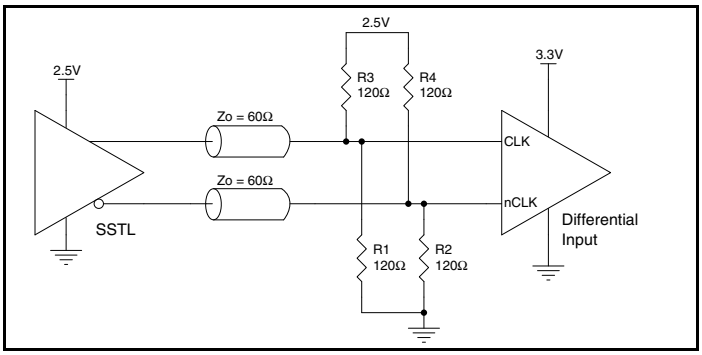


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommended Termination

Figure 3A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

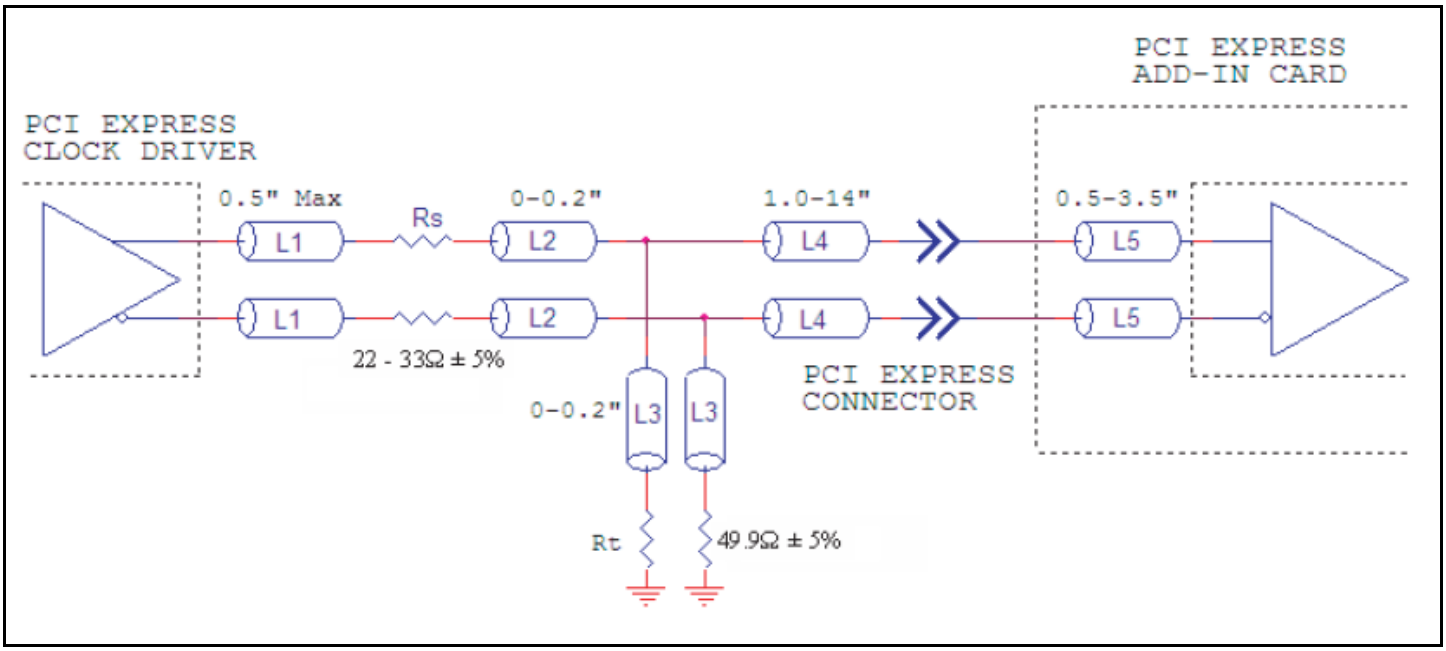


Figure 3A. Recommended Termination

Figure 3B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

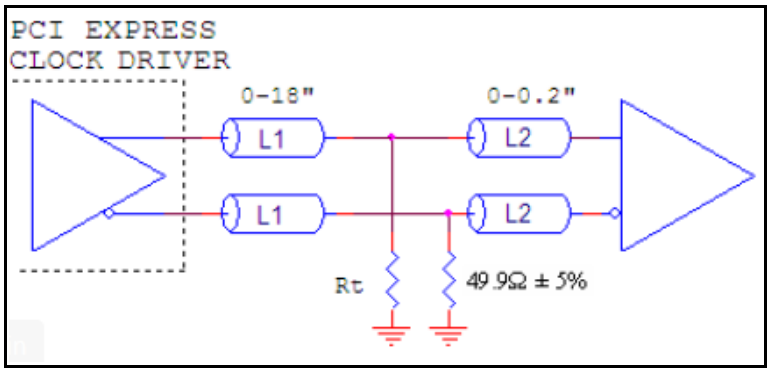


Figure 3B. Recommended Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 85108.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 85108 is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.63V * 27mA = **98.01mW**
- Power $(outputs)_{MAX}$ = **47.3mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 8 * 47.3mW = **378.4mW**

Total Power_MAX = (3.465V, with all outputs switching) = 98.01mW + 378.4mW = **476.41mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 1 meter per second and a multi-layer board, the appropriate value is 83.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.476W * 83.5°C/W = 124.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} Vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4.*

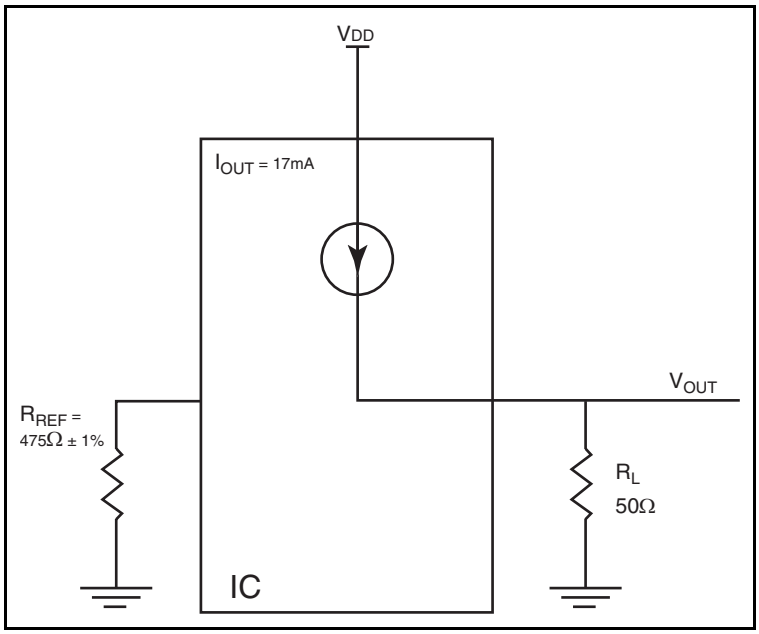


Figure 4. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DD–MAX}$.

Power = $(V_{DD\_MAX} – V_{OUT}) * I_{OUT}$,

since $V_{OUT} = I_{OUT} * R_L$

= $(V_{DD\_MAX} – I_{OUT} * R_L) * I_{OUT}$

= (3.63V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **47.3mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

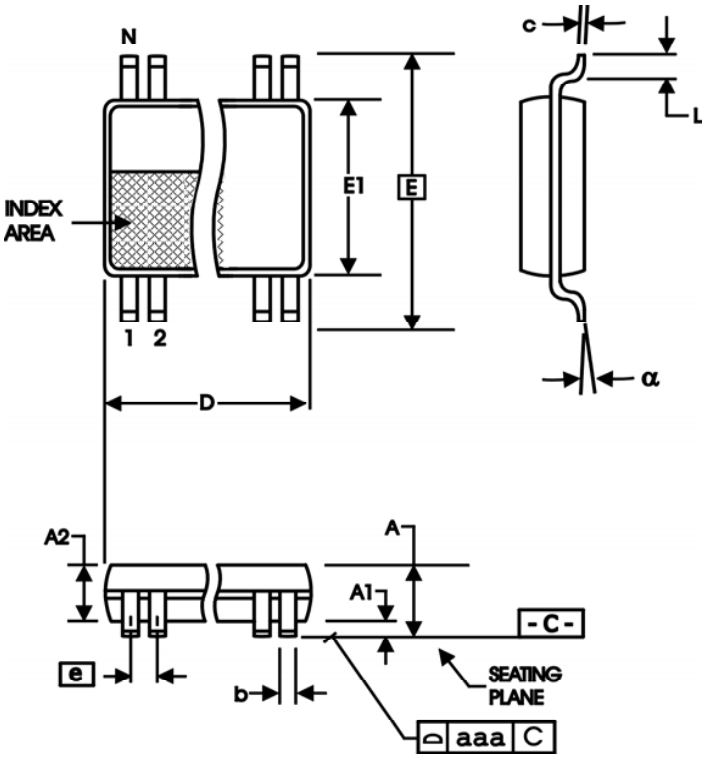
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.8°C/W	83.5°C/W	81.3°C/W

Transistor Count

The transistor count for 85108 is: 583

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP



All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85108AGILF	ICS85108AGILF	“Lead-Free” 24 Lead TSSOP	Tray	-40°C to 85°C
85108AGILFT	ICS85108AGILF	“Lead-Free” 24 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T1	2	Pin Description Table - corrected sequence of pin names to correspond to Pin Assignment. Pin 13 should be nQ4 and pin 14 should be Q4.	10/22/09
A	T1	2	Pin Description Table - corrected sequence of pin names to correspond to Pin Assignment. Pins 17 - 20 and pins 23 - 24 are in reverse order of Pin Assignment.	10/23/09
A	T9 1	14 1	Ordering information - removed leaded devices. Features section - removed reference to leaded devices. Updated data sheet format.	6/11/15

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