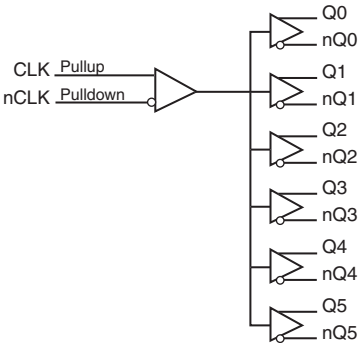
General Description

The 854S006I is a low skew, high perfor- mance 1-to-6 Differential-to-LVDS Fanout Buffer. The CLK, nCLK pair can accept most standard differential input levels. The 854S006I is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output skew characteristics make the 854S006I ideal for those clock distribution applications demanding well defined performance and repeatability.

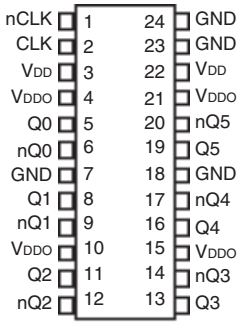
Features

- Six differential LVDS outputs
- One differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 1.7GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLK input
- Output skew: 55ps (maximum)
- Propagation delay: 850ps (maximum)
- Additive phase jitter, RMS: 0.067ps (typical)
- Full 3.3V or 2.5V power supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



854S006I
24-Lead TSSOP
4.40mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	nCLK	Input	Pulldown	Inverting differential clock input.
2	CLK	Input	Pullup	Non-inverting differential clock input.
3, 22	V_{DD}	Power		Positive supply pins.
4, 10, 15, 21	V_{DDO}	Power		Output supply pins.
5, 6	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
7, 18, 23, 24	GND	Power		Power supply ground.
8, 9	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
11, 12	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
13, 14	Q3, nQ3	Output		Differential output pair. LVDS interface levels.
16, 17	Q4, nQ4	Output		Differential output pair. LVDS interface levels.
19, 20	Q5, nQ5	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q5	nQ0:nQ5		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, “Wiring the Differential Input to Accept Single Ended Levels”.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				55	mA
I_{DDO}	Output Supply Current				105	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA
I_{DDO}	Output Supply Current				102	mA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			10	µA
		nCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V			150	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V	-150			µA
		nCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		326		526	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.28		1.44	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		305		505	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.
NOTE: Maximum value is a design target spec.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				1.7	GHz
t_{PD}	Propagation Delay; NOTE 1		300		850	ps
*t*sk(o)	Output Skew; NOTE 2, 3				55	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	622.08MHz, Integration Range: 12kHz – 20MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤ 1.2GHz	47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

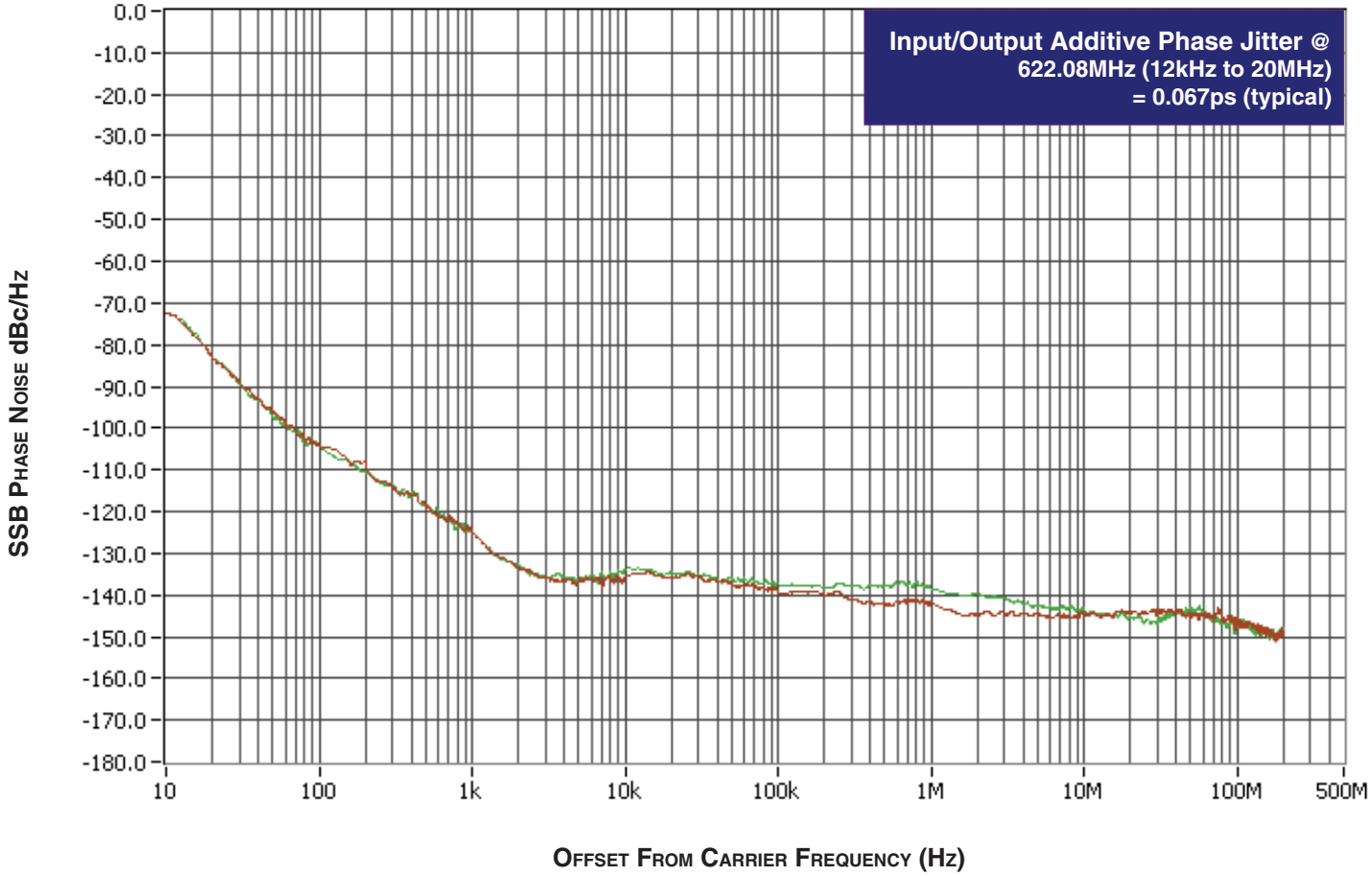
TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				1.7	GHz
t_{PD}	Propagation Delay; NOTE 1		300		800	ps
*t*sk(o)	Output Skew; NOTE 2, 3				55	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	622.08MHz, Integration Range: 12kHz – 20MHz		0.067		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤ 1.2GHz	47		53	%

For NOTES, see Table 5A.

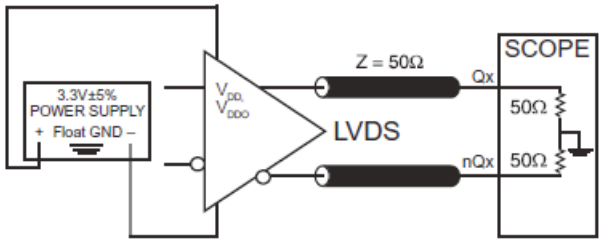
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

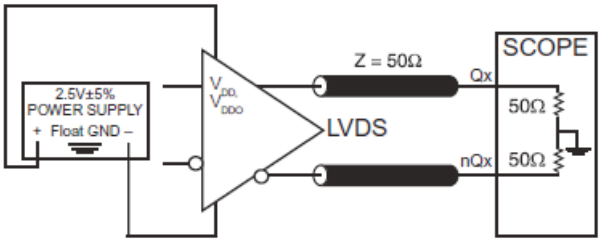


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

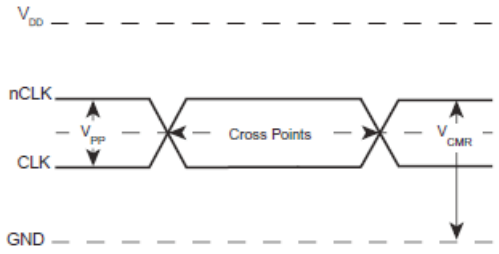
Parameter Measurement Information



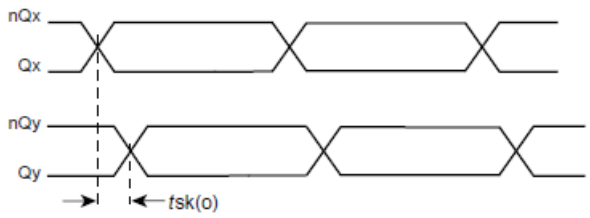
3.3V Core/3.3V Output Load AC Test Circuit



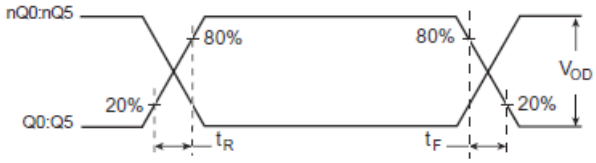
2.5V Core/2.5V Output Load AC Test Circuit



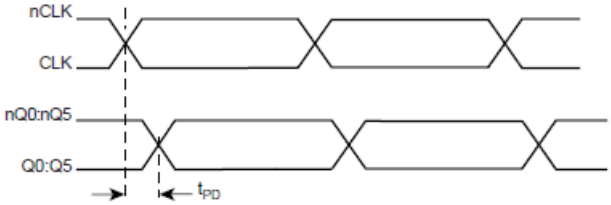
Differential Input Level



Output Skew

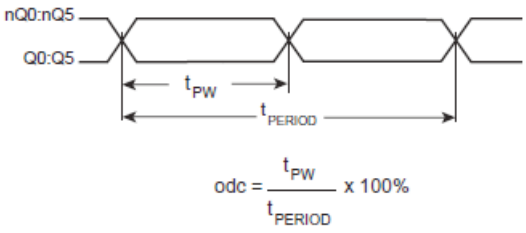


Output Rise/Fall Time

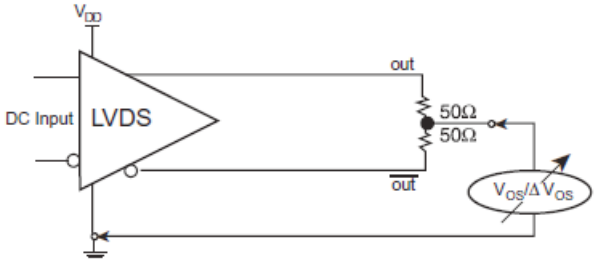


Propagation Delay

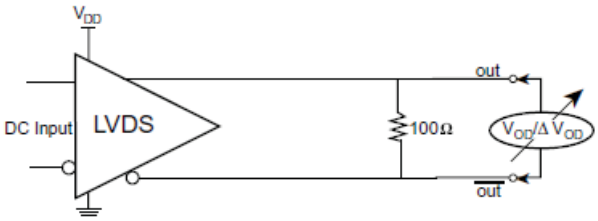
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

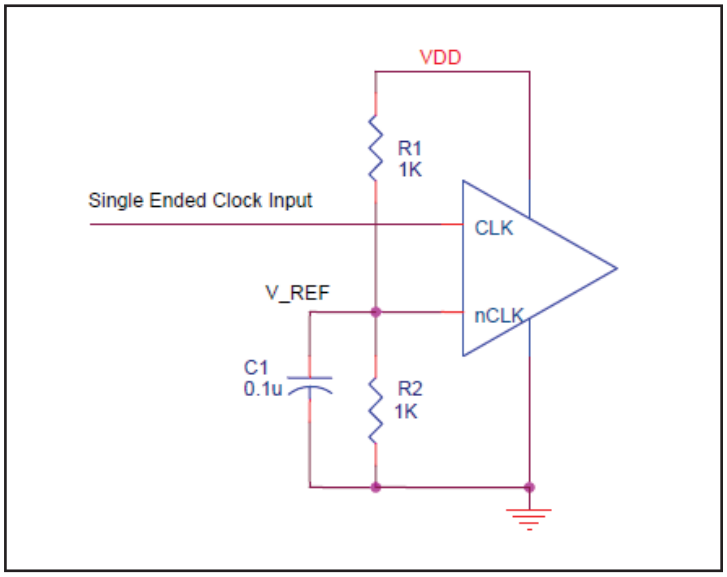


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Output Pins

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

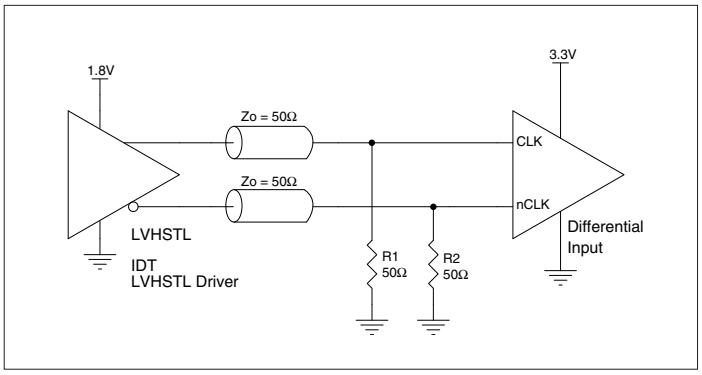


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

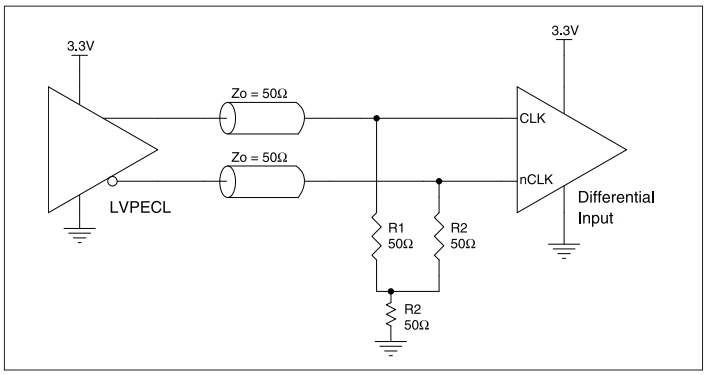


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

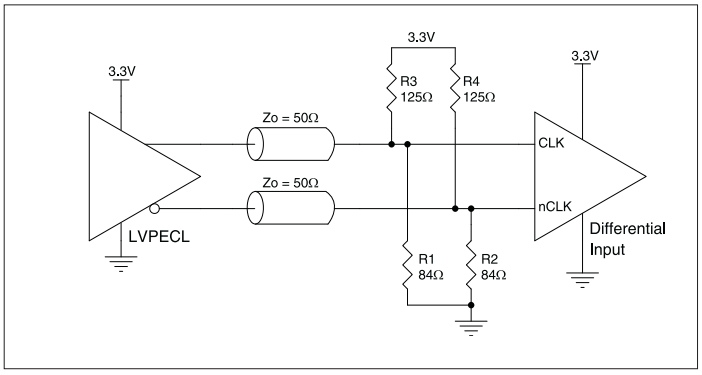


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

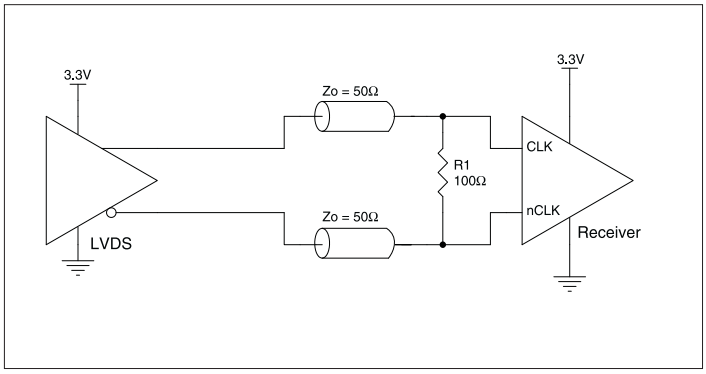


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

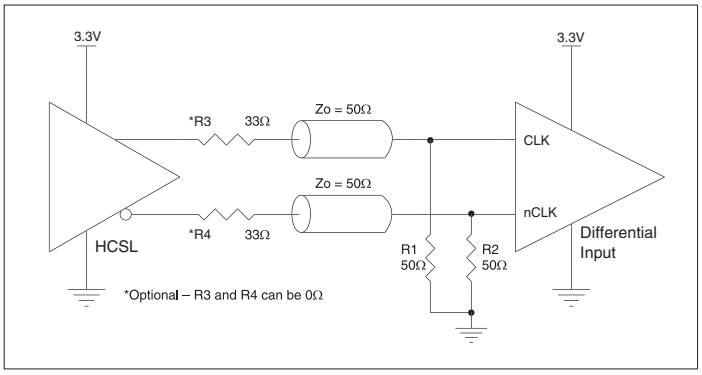


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

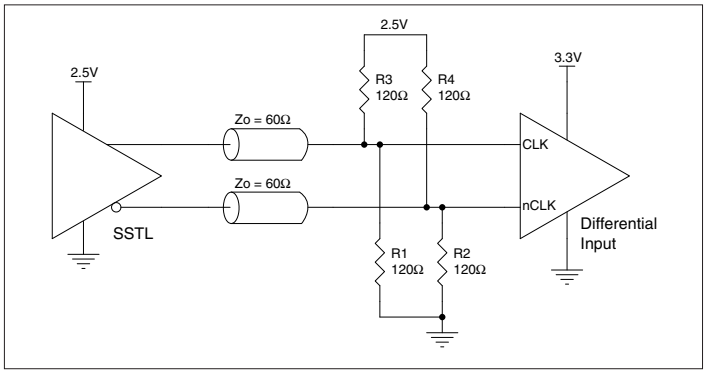


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

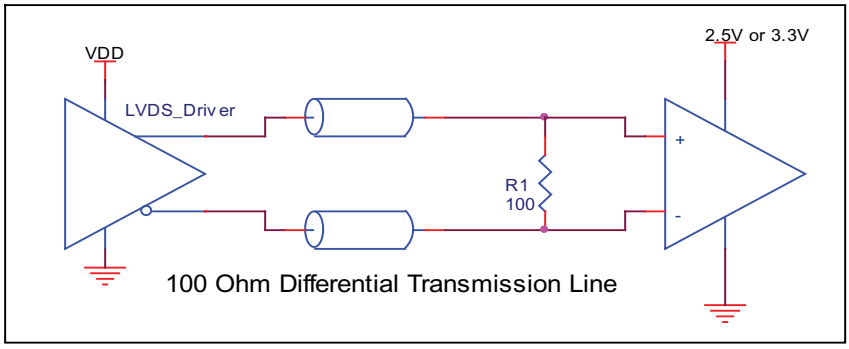


Figure 3. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 854S006I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 854S006I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 55mA = **190.575mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 105mA = **363.825mW**

Total Power$_{_MAX}$ = 190.575mW + 363.825mW = **554.4mW**

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.554W * 70°C/W = 123.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24-Lead TSSOP, Forced Convection

θ_{JA} by Velocity (Meters per Second)	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

The transistor count for 854S006I is: 293

Package Outline & Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

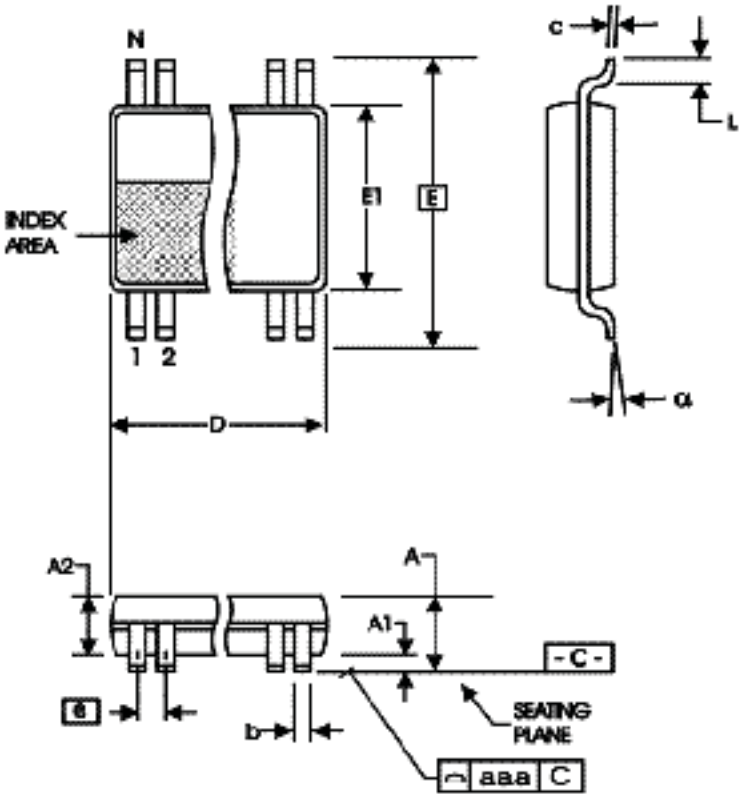


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S006AGILF	ICS854S006AIL	24 lead “Lead Free” TSSOP	Tray	-40°C to +85°C
854S006AGILFT	ICS854S006AIL	24 lead “Lead Free” TSSOP	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T4D, T4E T9	4 13	LVDS DC Characteristics Table - changed VOD units from V to mV. Ordering Information Table - deleted “ICS” prefix from Part/Order column. Changed style of header/footer.	7/20/09
B	 T1 T4C T5A, T5B	1 2 3 4 9	Block Diagram - changed CLK to “pullup” and nCLK to “pulldown”. Pin Descriptions - changed CLK and nCLK “Type” to reflect block diagram. Differential DC Characteristics Table - IIH parameters, changed CLK levels from 150uA max. to 10uA max.; nCLK levels from 5uA max. to 150uA max. IIL parameters, changed CLK levels from -5uA min. to -150uA min.; nCLK levels from -150uA min. to -10uA min. Added thermal note. Updated Differential Clock Input Interface section.	1/18/10
B	 T9	 1 12	Removed ICS from the part numbers where needed. General Description - removed ICS chip. Ordering Information - removed quantity from tape and reel. Deleted the LF note below the table. Updated header and footer.	1/19/16

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