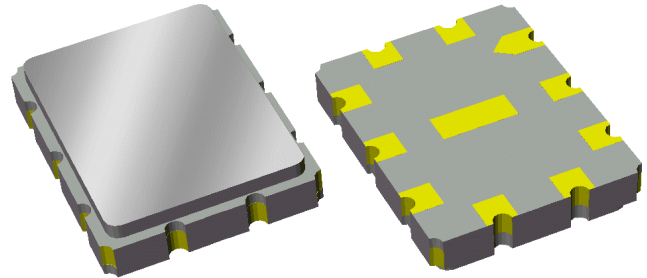


# Preliminary Data Sheet

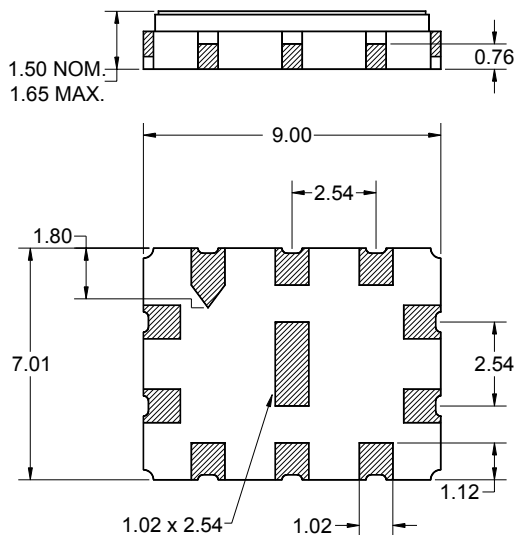
## Features

- For broadband applications
- Typical 3dB bandwidth of 33.2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Small size
- Replaces Sawtek P/N 851937 (BW 3dB=32 MHz)



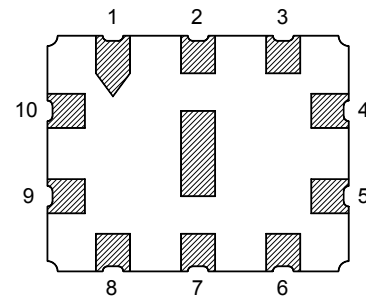
## Package

Surface Mount 9.00 x 7.01 x 1.50 mm



## Pin Configuration

Bottom View



Pin No.	Description
4	Output
5	Output return
9	Input
10	Input return
1,2,3,6,7,8	Case ground

Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15$ mm except overall  
length and width  $+0.10$ mm/ $-0.15$ mm

Body:  $Al_2O_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0  $\mu$ m,  
over a 2 - 6  $\mu$ m Ni plating

# Preliminary Data Sheet

## Electrical Specifications <sup>(1)</sup>

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

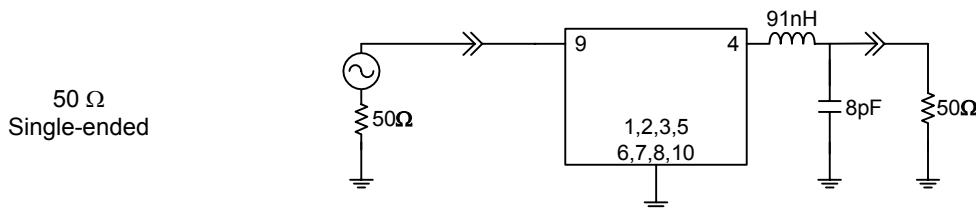
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	21.7	22.5	dB
Lower 1 dB Bandedge <sup>(4)</sup>	-	124.29	125.15	MHz
Upper 1 dB Bandedge	154.85	155.88	-	
Lower 3 dB Bandedge <sup>(4)</sup>	-	123.42	124.2	MHz
Upper 3 dB Bandedge	155.8	156.64	-	
Lower 40 dB Bandedge <sup>(4)</sup>	119.65	120.31	-	MHz
Upper 40 dB Bandedge	-	159.58	160.35	
Amplitude Variation 125.15 - 154.85 MHz	-	0.46	1.10	dB p-p
Phase Linearity 125.15 - 154.85 MHz	-	2.75	6.0	deg p-p
Group Delay Variation 125.15 - 154.85 MHz	-	15.46	30	ns p-p
Absolute Delay	-	0.905	-	μsec
Relative Attenuation <sup>(4)</sup>				
15 - 60 MHz	45	56	-	dB
60 - 115 MHz	43	54	-	dB
165 - 200 MHz	42	52	-	dB
200 - 300 MHz	47	58	-	dB
Terminating Source Impedance: <sup>(5)</sup>	-	50	-	Ω
Terminating Load Impedance: <sup>(5)</sup>	-	50	-	Ω
Substrate Material	-	128 LiNbO <sub>3</sub>	-	-
Temperature Coefficient of Frequency	-	-74	-	ppm/°C

### Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

### Test Circuit:

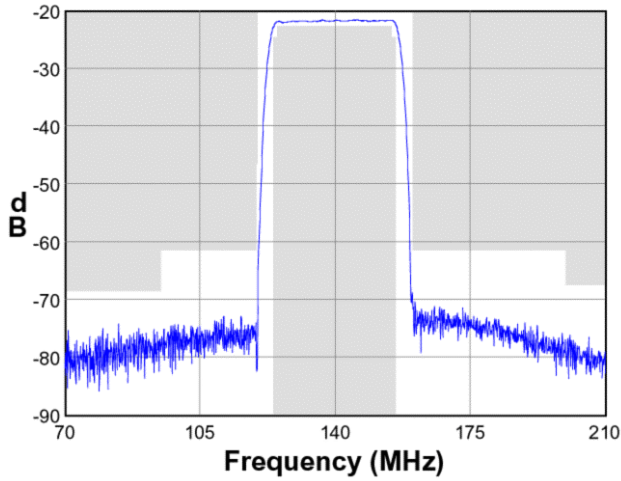
Actual matching values may vary due to PCB layout and parasitics



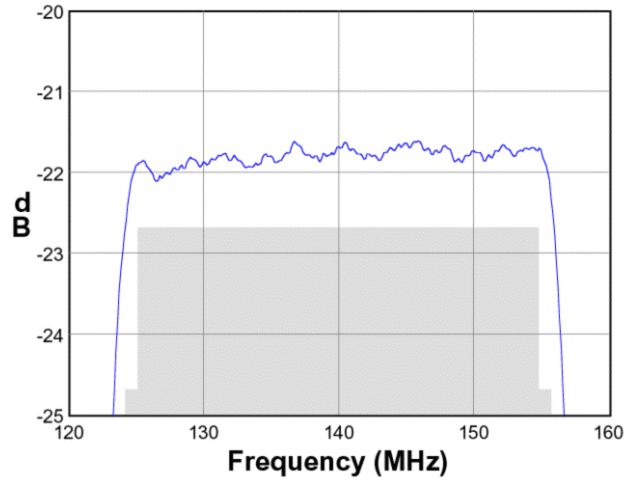
**Preliminary Data Sheet**

**Typical Performance (at +25°C)**

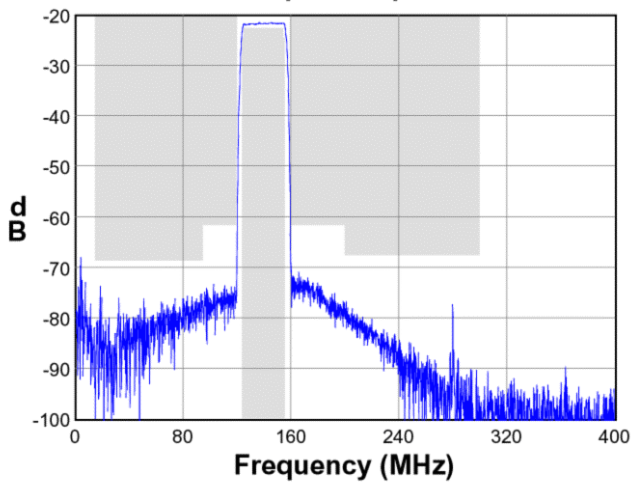
**Frequency Response**



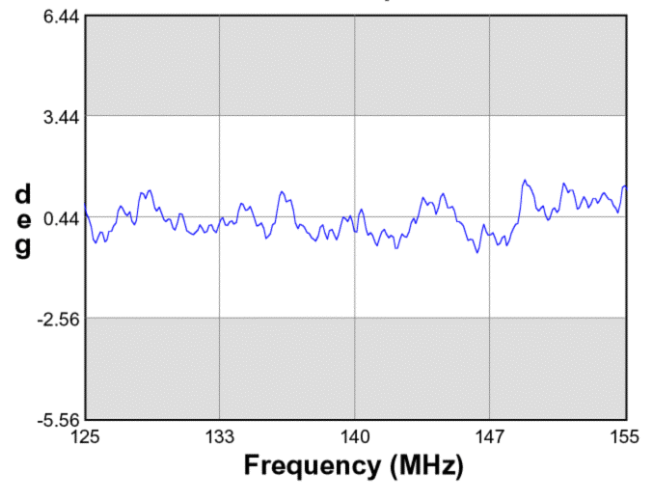
**Passband Response**



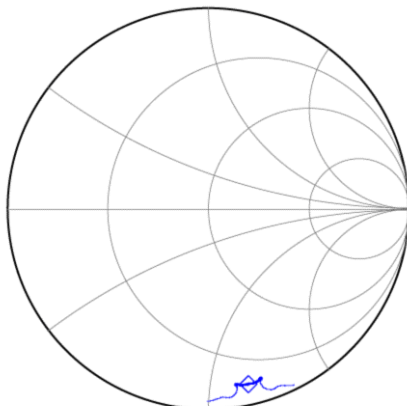
**Widespan Response**



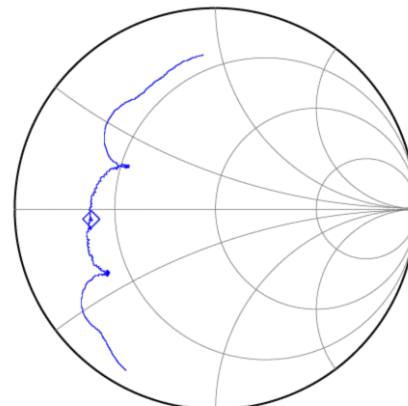
**Phase Response**



**Input Smith Chart**



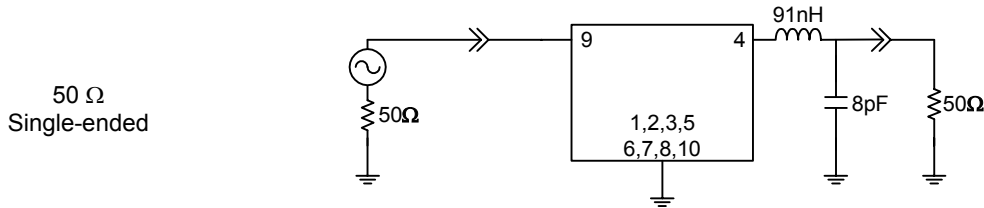
**Output Smith Chart**



**Preliminary Data Sheet**

**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

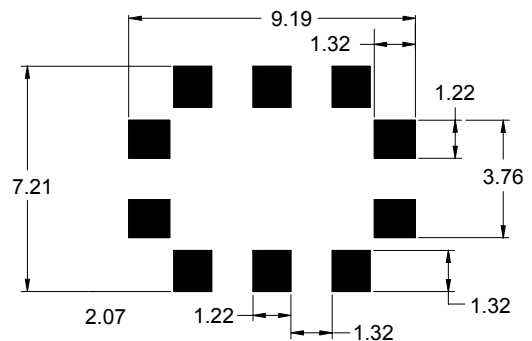


**Marking**



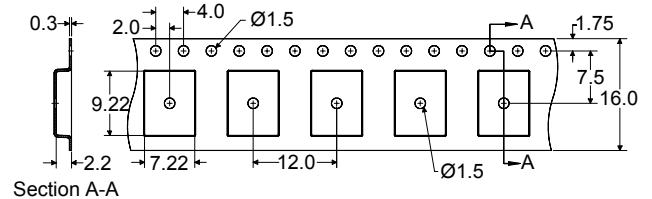
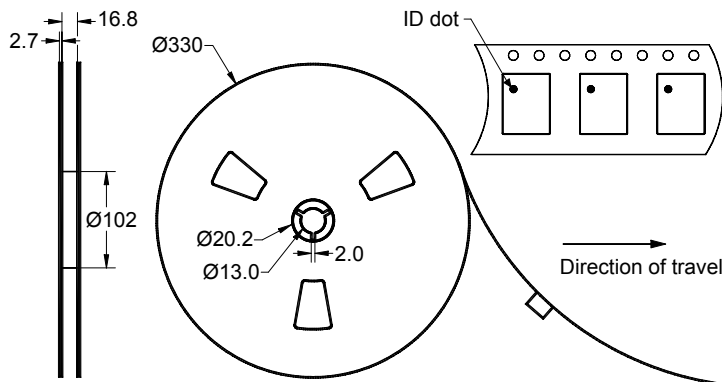
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**




Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel

# Preliminary Data Sheet

## Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	-	+85	°C

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

## Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[Reel and Packaging Label](#)

[Other Technical Information](#)

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