Vision964

Graphics

Accelerator

January 1995

S3 Incorporated
2770 San Tomas Expressway
Santa Clara, CA 95051-0968

DB009-B

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department, 2770 San Tomas Expressway, Santa Clara, CA 95051-0968.

Telephone: 408-980-5400, Fax: 408-980-5444

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Section 1: Introduction

The S3™ Vision964™ 64-bit VRAM-based graphics accelerator (hereinafter referred to as the Vision964) provides high resolutions, true color and multimedia capabilities to multiple PC hardware and software platforms. It supports Intel®, PowerPC™, Alpha™ and MIPS™ hardware platforms and a range of operating environments such as Windows™, Windows NT™, OS/2®, Solaris™ and SCO® OpenDesktop®.

The pixel data bus to the frame buffer is 64 bits wide. When combined with support for the fast page and extended data out (EDO) modes of the latest VRAMs, this provides a pixel data band-width up to 240 MBytes/second. Maximum screen refresh band-width using a 128-bit SID RAMDAC is 720 MBytes/second.

The Vision964 is register-level compatible with standard VGA and provides fast operation in both text and graphics modes. It supports the VESA® extended VGA modes. It also provides a set of enhanced modes for accelerated operation with higher resolutions and pixel depths.

1.1 BUS INTERFACES

The PCI bus interface is fully compliant with revision 2.0 of the PCI specification and requires no external glue logic. This interface is shown Figure 1-1. The VESA local bus interface requires external buffers. The Vision964 provides all required control signals for these buffers.

1.2 VRAM/RAMDAC SUPPORT

High performance Vision964-based systems can be designed with 1 MByte of VRAM and a 32-bit SID RAMDAC. Very high performance systems can be configured with up to 8 MBytes of faster VRAM and a 64- or 128-bit SID RAMDAC. VRAM sizes supported are 256Kx4/8/16.

1.3 RESOLUTIONS SUPPORTED

Table 1-1. Video Resolutions Supported

Resolution	1 MB	2 MB	4 MB	8 MB
640x480x4	✔	✔	✔	✔
640x480x8	✔	✔	✔	✔
640x480x16	✔	✔	✔	✔
640x480x24	✔	✔	✔	✔
640x480x32		✔	✔	✔
800x600x4	✔	✔	✔	✔
800x600x8	✔	✔	✔	✔
800x600x16	✔	✔	✔	✔
800x600x32		✔	✔	✔
1024x768x4	✔	✔	✔	✔
1024x768x8	✔	✔	✔	✔
1024x768x16		✔	✔	✔
1024x768x32			✔	✔
1280x1024x4	✔	✔	✔	✔
1280x1024x8		✔	✔	✔
1280x1024x16			✔	✔
1280x1024x32				✔
1600x1200x4	✔	✔	✔	✔
1600x1200x8		✔	✔	✔
1600x1200x16			✔	✔
1600x1200x32				✔

Extended VGA text modes up to 132 columns by 43 rows are possible as well.

1.4 ADVANCED ARCHITECTURE

The 64-bit Graphics Engine accelerates common graphics operations such as bit block transfers (BitBLTs) and rectangle fills. The Vision964 processes two 32 bits/pixel (bpp) (true color) operations, four 16 bpp operations (high color) or eight 8 bpp operations (pseudo-color) per clock cycle. Other architectural features enhancing performance include linear addressing of video memory, memory-mapped I/O and write posting of CPU writes to video memory.

1.5 MULTIMEDIA SUPPORT

The Vision964 supports several types of multimedia operations. It provides a request/grant protocol and associated signals to allow a video coprocessor to share the video frame buffer. In addition, the Vision964 contains built-in genlock circuitry to synchronize the RAMDAC output with an external NTSC/PAL video signal. This feature provides support for multimedia-type applications such as video superposition and chroma key control.

1.6 GREEN PC SUPPORT

For low power consumption designs (Green PC), the Vision964 allows software manipulation of its horizontal and vertical sync signals to control the power state of monitors.

1.7 SOFTWARE SUPPORT

S3 provides drivers for operating systems such as Microsoft Windows and IBM® OS/2 Presentation Manager™ and graphics-intensive applications such as AutoCAD®. S3 also provides video BIOS support for RAMDACs covering a large performance range. In addition, third party developers provide drivers for numerous applications.

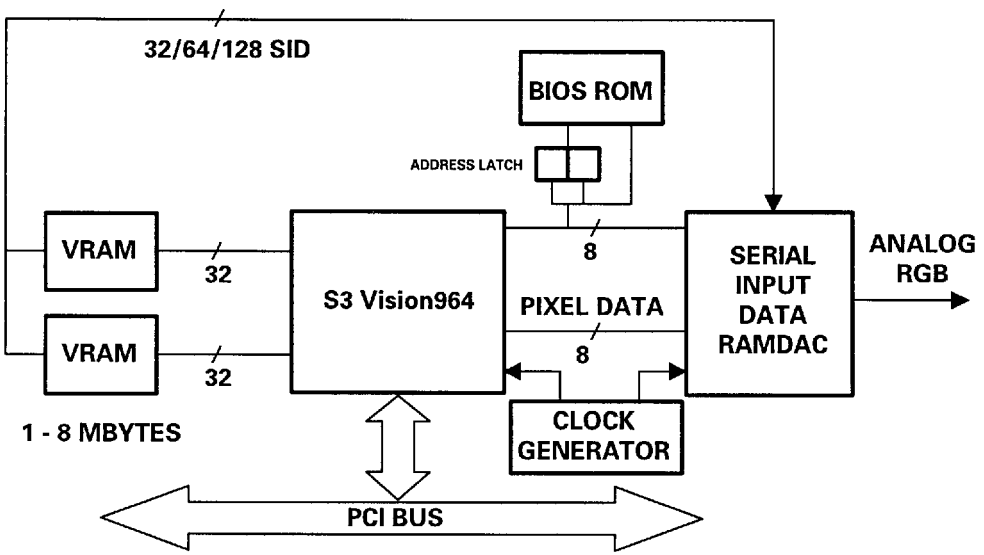


Figure 1-1. PCI-bus System Block Diagram

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		8		°C/W
Thermal Resistance Θ_{JA} (Still Air)		37		°C/W
Power Dissipation			1.75	W
Junction Temperature			125	°C

2.2 MECHANICAL DIMENSIONS

The Vision964 comes in a 208-pin PQFP package. The mechanical dimensions are given in Figure 2-1.

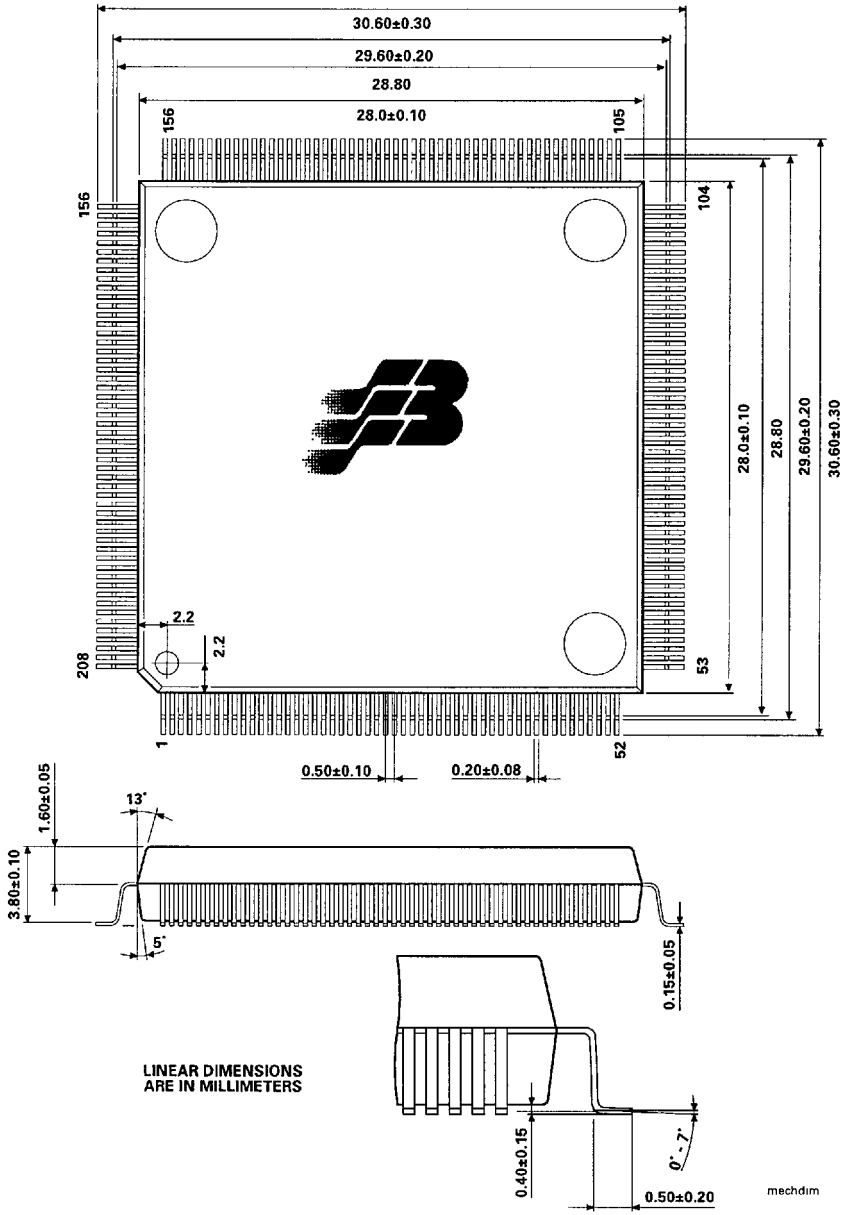


Figure 2-1. 208-pin PQFP Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

The Vision964 comes in a 208 pin PQFP package. The PCI bus pinout is shown in Figure 3-1. The pinout for the VESA local bus configuration is shown in Figure 3-2. Active low signals are indicated by an overbar.

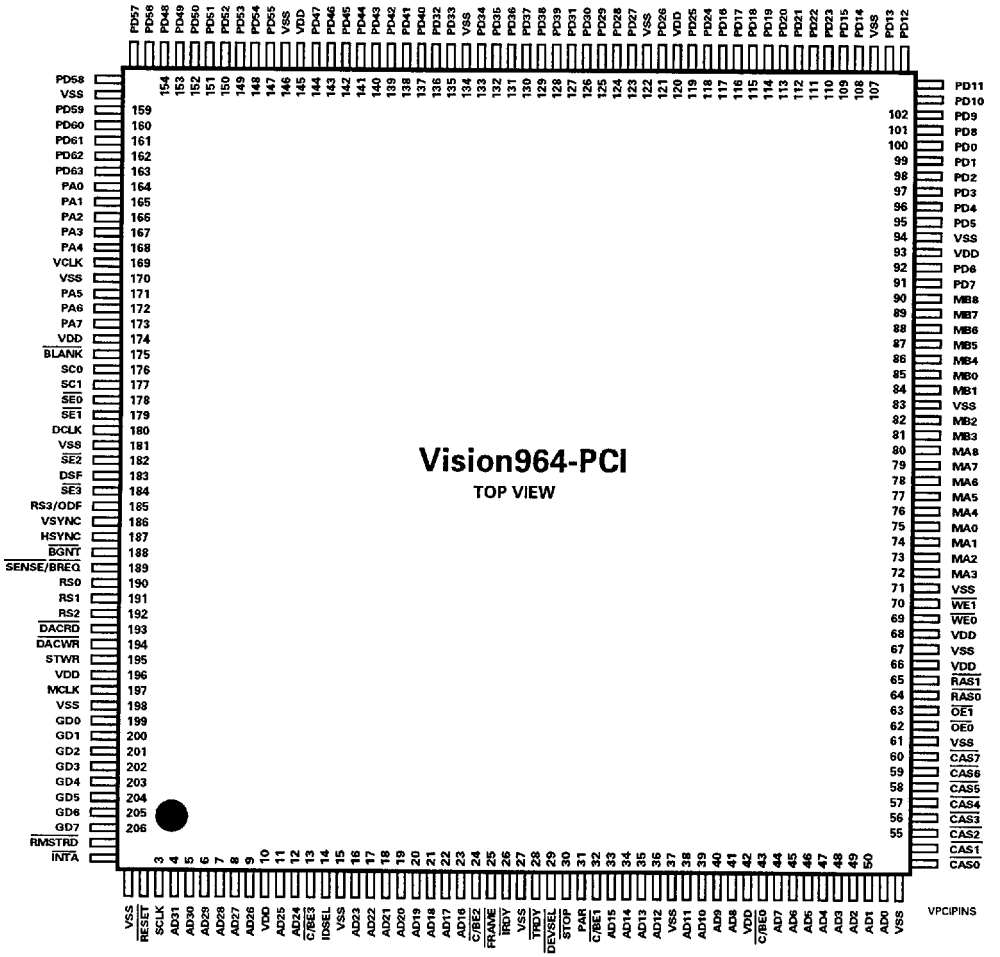


Figure 3-1. PCI Bus Configuration Pinout

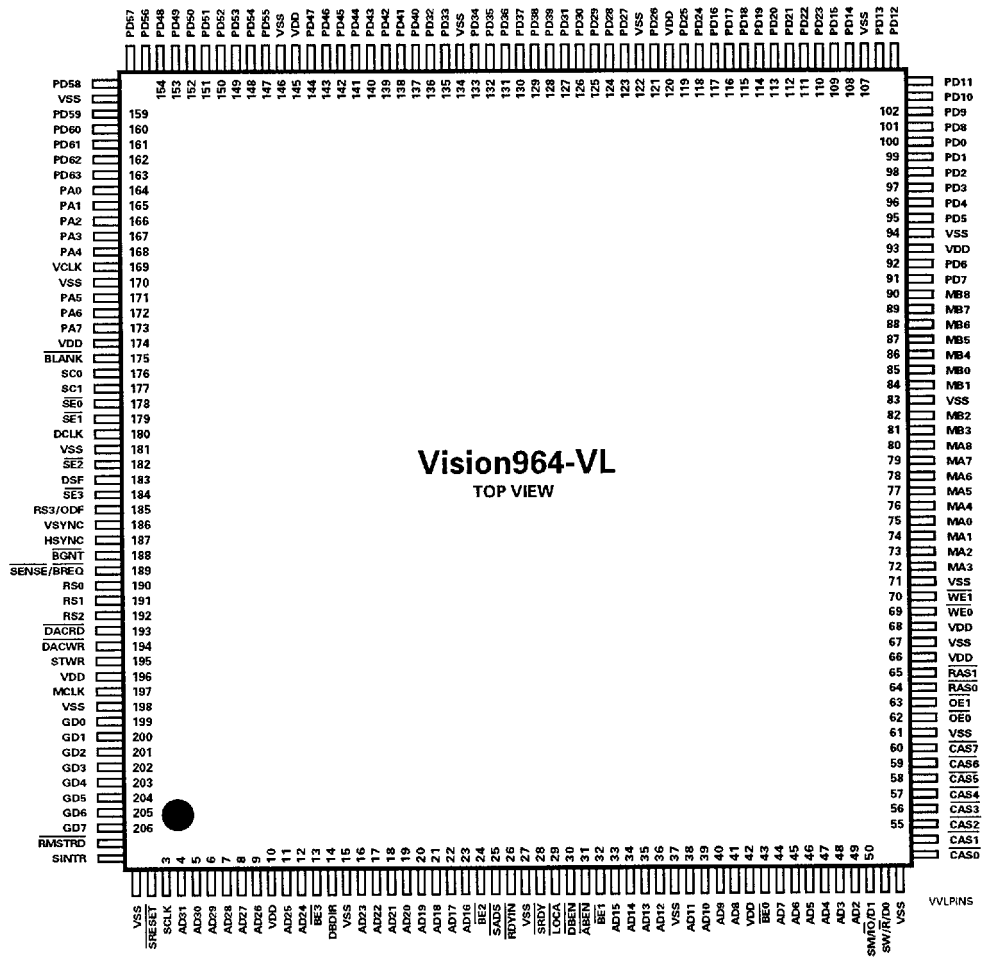


Figure 3-2. VESA Local Bus Configuration Pinout

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on the Vision964 for its VESA local bus and PCI bus configurations. The following definitions are used in these descriptions:

I - Input signal
O - Output signal
B - Bidirectional signal

Some pins have multiple names. This reflects the different functions performed by those pins depending on the bus configuration selected by power-on-strapping. The pin definitions and functions are given for each possible case.

Table 3-1. Vision964 Pin Descriptions

Symbol	Type	Pin Number(s)	Description
BUS INTERFACES			
Address and Data			
AD[31:2]	B	4-9, 11-12, 16-23, 33-36, 38-41, 44-49	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
AD1 SM/$\overline{IO}$/D1	B I	50	(PCI) Multiplexed Address/Data Bit 1. (VL) Memory/I/O Cycle Indicator/Data 1. The M/$\overline{IO}$ status is latched during the address phase and D1 is latched during the data phase.
AD0 SW/$\overline{R}$/D0	B I	51	(PCI) Multiplexed Address/Data Bit 0. (VL) Write/Read Cycle Indicator/Data 0. The W/$\overline{R}$ status is latched during the address phase and D0 is latched during the data phase.
$\overline{C/BE[3:0]}$ $\overline{BE[3:0]}$	I	13, 24, 32, 43	(PCI) Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase. (VL) Data Byte Enables.
Bus Control			
SCLK	I	3	System Clock.
$\overline{INTA}$ SINTR	O	208	(PCI) Interrupt Request. (VL) Interrupt Request.
$\overline{IRDY}$ $\overline{RDYIN}$	I	26	(PCI) Initiator Ready. A bus data phase is completed when both $\overline{IRDY}$ and $\overline{TRDY}$ are asserted on the same cycle. (VL) Local Bus Cycle End Acknowledge. The Vision964 holds read data valid on the bus until this input is asserted.

Table 3-1. Vision964 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
TRDY SRDY	O	28	(PCI) Target Ready. A bus data phase is completed when both IRDY and TRDY are asserted on the same cycle. (VL) Local Bus Cycle End.
DEVSEL LOCA	O	29	(PCI) Device Select. The Vision964 drives this signal active when it decodes its address as the target of the current access. (VL) Local Bus Access Cycle Indicator. This signal is output during local bus cycles to allow system logic chip sets to prevent concurrent EISA/ISA cycle generation.
IDSEL DBDIR	I O	14	(PCI) Initialization Device Select. This input is the chip select for Vision964 PCI configuration register reads/writes. (VL) Data Buffer Direction Control. This output is high for a data write and low for a data read.
RESET SRESET	I	2	(PCI) System Reset. Asserting this signal forces the Vision964 registers and state machines to a known state. (VL) System Reset.
FRAME SADS	I	25	(PCI) Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction. It is deasserted during the final data phase of a bus transaction. (VL) System Address Strobe.
PAR ABEN	O	31	(PCI) Parity. The Vision964 asserts this signal to verify even parity during reads. (VL) Address Buffer Enable. This signal enables the address buffers to drive the address, SM/IO and SW/R onto the AD[31:0] lines.
STOP DBEN	O	30	(PCI) Stop. The Vision964 asserts this signal to indicate a target disconnect. (VL) Data Buffer Enable. This output enables the data buffers to transfer data between the CPU data bus and the AD[31:0] lines.

Table 3-1. Vision964 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
CLOCK CONTROL			
MCLK	I	197	Master (Memory) Clock. This input is provided by the clock chip. It controls the pixel data transfer rate between the Vision964 and display memory.
DCLK	I	180	Dot Clock. This input is provided by the clock chip. It controls the pixel rate to the RAMDAC as well as the sync and blank timings.
DISPLAY MEMORY INTERFACE			
Address and Data			
PD[63:0]	B	163-159, 157-155, 147-154, 144-137, 128-133, 135-136, 127-123, 121, 119-118, 110-117, 109-108, 106-101, 91-92, 95-100	Display Memory Pixel Data Bus. PD[23-0] are also used as the system configuration strapping bits, providing system configuration and setup information upon power-on or reset.
MA[8.0]	O	80-76, 72-75	Memory Address Bus A.
MB[8:0]	O	90-86, 81-82, 84-85	Memory Address Bus B.
Memory Control			
$\overline{\text{RAS}}$[1:0]	O	65-64	Row Address Strobes.
$\overline{\text{CAS}}$[7.0]	O	60-53	Column Address Strobes.
$\overline{\text{WE}}$[1:0]	O	70-69	Write Enables.
$\overline{\text{OE}}$[1:0]	O	63-62	Output Enables.
SC[1:0]	O	177-176	Serial Clocks.
$\overline{\text{SE}}$[3:0]	O	184, 182, 179-178	Serial Enables.
DSF	O	183	Special VRAM Function Control.
RAMDAC INTERFACE			
Address and Data			
PA[7:0]	O	173-171, 168-164	RAMDAC Pixel Address Bus. This bus is used for VGA pixel data.
GD[7:0]	B	206-199	General Data Bus. These signals carry RAMDAC register read/write data. They also carry clock select outputs, General Output Port output and General Input Port input.

Table 3-1. Vision964 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
RS[2:0]	B	192-190	RAMDAC Register Select. These signals select the RAMDAC register to be read/written. For General Input Port (GOP) reads, RS2 low and $\overline{\text{RMSTRD}}$ asserted combine to provide the buffer output enable.
RS3/ODF	O	185	RAMDAC Register Select 3/Odd Frame Control. If bit 5 of CR45 is cleared to 0, this is the RS3 signal. If bit 5 of CR45 is set to 1, this is the ODF signal for the Bt9485 RAMDAC.
RAMDAC Control			
VCLK	O	169	Video/Pixel Clock. This signal latches pixel data into the RAMDAC.
$\overline{\text{DACRD}}$	O	193	RAMDAC Read. This signal is asserted to indicate a data read from the RAMDAC.
$\overline{\text{DACWR}}$	O	194	RAMDAC Write. This signal is asserted to indicate a data write to the RAMDAC.
$\overline{\text{BLANK}}$	O	175	Video Blank. Asserting this signal turns off the video output.
$\overline{\text{SENSE}}$/$\overline{\text{BREQ}}$	I	189	Video Level Sense/Bus Request. When bit 2 of CR50 is cleared to 0, this is the $\overline{\text{SENSE}}$ input. The RAMDAC drives this signal low when it detects a video voltage level exceeding 335 mV on any of the analog outputs. This is used by the video BIOS to detect the existence and type of the monitor connected to the system. The sense status is read from bit 4 of I/O port 3C2H. When bit 2 of CR50 is set to 1, this is the Bus Request input from another display memory master. This supports shared frame buffer operation. The appropriate input signal must be selected by external hardware.
HSYNC	O	187	Horizontal Sync. This signal is an output to the monitor.
VSYNC	B	186	Vertical Sync. When bit 0 of CR56 is cleared to 0 (default), this is an output to the monitor. When bit 0 of CR56 is set to 1, this is an input from a master video source. This provides the basis for genlocking the video output of the Vision964 with the master video source.
MISCELLANEOUS FUNCTIONS			
General Data Port			
GD[7:0]	B	206-199	General Data Bus. These signals carry data for RAMDAC reads/writes, clock select outputs, General Output Port output and General Input Port input

Table 3-1. Vision964 Pin Descriptions (Continued)

Symbol	Type	Pin Number(s)	Description
$\overline{\text{RMSTRD}}$	O	207	ROM/General Input Port Read Strobe. This signal provides the chip output enable input for ROM BIOS reads and is combined with RS0 for the enable to the General Input Port register.
STWR	O	195	General Output Port Write Strobe. Write strobe for the General Output Port (CR5C) latch and the clock select strobe input to the clock chip.
Bus Master Control			
$\overline{\text{SENSE}}/\overline{\text{BREQ}}$	I	189	Video Level Sense/Bus Request. When bit 2 of CR50 is cleared to 0, this is the $\overline{\text{SENSE}}$ input. The RAMDAC drives this signal low when it detects a video voltage level exceeding 335 mV on any of the analog outputs. This is used by the video BIOS to detect the existence and type of the monitor connected to the system. The sense status is read from bit 4 of I/O port 3C2H. When bit 2 of CR50 is set to 1, this is the Bus Request input from another display memory master. This supports shared frame buffer operation. The appropriate input signal must be selected by external hardware.
$\overline{\text{BGNT}}$	O	188	Bus Grant. The Vision964 asserts this signal in response to a $\overline{\text{BREQ}}$ input to notify another display memory master that it can take control of the display memory bus. The bus will not be not be granted if the termination position programmed into the Bus Grant Termination position register (CR5F) and its extension (bit 7 of CR5D) has been exceeded. The Vision964 raises this signal to reclaim bus control.
POWER AND GROUND			
V_{DD}	I	10, 42, 66, 68, 93, 120, 145, 174, 196	Power supply
V_{SS}	I	1, 15, 27, 37, 52, 61, 67, 71, 83, 94, 107, 122, 134, 146, 158, 170, 181, 198	Ground

3.3 PIN LISTS

Table 3-2 lists all Vision964 pins alphabetically. The pin number(s) corresponding to each pin name are given in the appropriate bus interface type column. Table 3-3 lists all Vision964 pins in numerical order. The pin name corresponding to each pin number is given in the appropriate bus interface column.

Table 3-2. Alphabetical Pin Listing

	PIN(S)	
Name	**PCI**	**VL**
$\overline{\text{ABEN}}$		31
AD[31:2]	4-9, 11-12, 16-23, 33-36, 38-41, 44-49	4-9, 11-12, 16-23, 33-36, 38-41, 44-49
AD[1:0]	50-51	
$\overline{\text{BE[3:0]}}$		13, 24, 32, 43
$\overline{\text{BGNT}}$	188	188
$\overline{\text{BLANK}}$	175	175
$\overline{\text{BREQ}}$	189	189
$\overline{\text{CAS[7:0]}}$	60-53	60-53
$\overline{\text{C/BE[3:0]}}$	13, 24, 32, 43	
$\overline{\text{DACRD}}$	193	193
$\overline{\text{DACWR}}$	194	194
DBDIR		14
$\overline{\text{DBEN}}$		30
DCLK	180	180
DSF	183	183
$\overline{\text{DEVSEL}}$	29	
$\overline{\text{FRAME}}$	25	
GD[7:0]	206-199	206-199
HSYNC	187	187
IDSEL	14	
$\overline{\text{INTA}}$	208	
$\overline{\text{IRDY}}$	26	
$\overline{\text{LOCA}}$		29
MA[8.0]	80-76, 72-75	80-76, 72-75
MB[8:0]	90-86, 81-82, 84-85	90-86, 81-82, 84-85
MCLK	197	197
ODF	185	185
$\overline{\text{OE[1:0]}}$	63-62	63-62
PA[7:0]	173-171, 168-164	173-171, 168-164
PAR	31	
PD[63:0]	163-159, 157-155, 147-154, 144-137, 128-133, 135-136, 127-133, 121, 119-118, 110-117, 109-108, 106-101 91-92, 95-100	163-159, 157-155, 147-154, 144-137, 128-133, 135-136, 127-133, 121, 119-118, 110-117, 109-108, 106-101 91-92, 95-100

Table 3-2. Alphabetical Pin Listing (Continued)

	PIN(S)	
Name	**PCI**	**VL**
$\overline{RAS[1:0]}$	65-64	65-64
$\overline{RESET}$	2	
$\overline{RDYIN}$		26
RS[2:0]	192-190	192-190
$\overline{RMSTRD}$	207	207
$\overline{SADS}$		25
SC[1:0]	177-176	177-176
SCLK	3	3
$\overline{SE[3:0]}$	184, 182, 179-178	184, 182, 179-178
$\overline{SENSE}$	189	189
SINTR		208
SM/$\overline{IO}$		50
SRDY		28
$\overline{SRESET}$		2
$\overline{STOP}$	30	
STWR	195	195
SW/$\overline{R}$		51
$\overline{TRDY}$	28	
VCLK	169	169
VDD	10, 42, 66, 68, 93, 120, 145, 174, 196	10, 42, 66, 68, 93, 120, 145, 174, 196
VSS	1, 15, 27, 37, 52, 61, 67, 71, 83, 94, 107, 122, 134, 146, 158, 170, 181, 198	1, 15, 27, 37, 52, 61, 67, 71, 83, 94, 107, 122, 134, 146, 158, 170, 181, 198
VSYNC	186	186
$\overline{WE[1:0]}$	70-69	70-69

Table 3-3. Numerical Pin Listing

	Name	
Number	**PCI**	**VL**
1	**VSS**	**VSS**
2	RESET	SRESET
3	SCLK	SCLK
4	AD31	AD31
5	AD30	AD30
6	AD29	AD29
7	AD28	AD28
8	AD27	AD27
9	AD26	AD26
10	**VDD**	**VDD**
11	AD25	AD25
12	AD24	AD24
13	C/BE3	BE3
14	IDSEL	DBDIR
15	**VSS**	**VSS**
16	AD23	AD23
17	AD22	AD22
18	AD21	AD21
19	AD20	AD20
20	AD19	AD19
21	AD18	AD18
22	AD17	AD17
23	AD16	AD16
24	C/BE2	BE2
25	FRAME	SADS
26	IRDY	RDYIN
27	**VSS**	**VSS**
28	TRDY	SRDY
29	DEVSEL	LOCA
30	STOP	DBEN
31	PAR	ABEN
32	C/BE1	BE1
33	AD15	AD15
34	AD14	AD14
35	AD13	AD13
36	AD12	AD12
37	**VSS**	**VSS**
38	AD11	AD11
39	AD10	AD10
40	AD9	AD9
41	AD8	AD8
42	**VDD**	**VDD**

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**PCI**	**VL**
43	C/BE0	BE0
44	AD7	AD7
45	AD6	AD6
46	AD5	AD5
47	AD4	AD4
48	AD3	AD3
49	AD2	AD2
50	AD1	SM/IO/D1
51	AD0	SW/R/D0
52	**VSS**	**VSS**
53	CAS0	CAS0
54	CAS1	CAS1
55	CAS2	CAS2
56	CAS3	CAS3
57	CAS4	CAS4
58	CAS5	CAS5
59	CAS6	CAS6
60	CAS7	CAS7
61	**VSS**	**VSS**
62	OE0	OE0
63	OE1	OE1
64	RAS0	RAS0
65	RAS1	RAS1
66	**VDD**	**VDD**
67	**VSS**	**VSS**
68	**VDD**	**VDD**
69	WE0	WE0
70	WE1	WE1
71	**VSS**	**VSS**
72	MA3	MA3
73	MA2	MA2
74	MA1	MA1
75	MA0	MA0
76	MA4	MA4
77	MA5	MA5
78	MA6	MA6
79	MA7	MA7
80	MA8	MA8
81	MB3	MB3
82	MB2	MB2
83	**VSS**	**VSS**
84	MB1	MB1

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**PCI**	**VL**
85	MB0	MB0
86	MB4	MB4
87	MB5	MB5
88	MB6	MB6
89	MB7	MB7
90	MB8	MB8
91	PD7	PD7
92	PD6	PD6
93	**VDD**	**VDD**
94	**VSS**	**VSS**
95	PD5	PD5
96	PD4	PD4
97	PD3	PD3
98	PD2	PD2
99	PD1	PD1
100	PD0	PD0
101	PD8	PD8
102	PD9	PD9
103	PD10	PD10
104	PD11	PD11
105	PD12	PD12
106	PD13	PD13
107	**VSS**	**VSS**
108	PD14	PD14
109	PD15	PD15
110	PD23	PD23
111	PD22	PD22
112	PD21	PD21
113	PD20	PD20
114	PD19	PD19
115	PD18	PD18
116	PD17	PD17
117	PD16	PD16
118	PD24	PD24
119	PD25	PD25
120	**VDD**	**VDD**
121	PD26	PD26
122	**VSS**	**VSS**
123	PD27	PD27
124	PD28	PD28
125	PD29	PD29
126	PD30	PD30

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**PCI**	**VL**
127	PD31	PD31
128	PD39	PD39
129	PD38	PD38
130	PD37	PD37
131	PD36	PD36
132	PD35	PD35
133	PD34	PD34
134	**VSS**	**VSS**
135	PD33	PD33
136	PD32	PD32
137	PD40	PD40
138	PD41	PD41
139	PD42	PD42
140	PD43	PD43
141	PD44	PD44
142	PD45	PD45
143	PD46	PD46
144	PD47	PD47
145	**VDD**	**VDD**
146	**VSS**	**VSS**
147	PD55	PD55
148	PD54	PD54
149	PD53	PD53
150	PD52	PD52
151	PD51	PD51
152	PD50	PD50
153	PD49	PD49
154	PD48	PD48
155	PD56	PD56
156	PD57	PD57
157	PD58	PD58
158	**VSS**	**VSS**
159	PD59	PD59
160	PD60	PD60
161	PD61	PD61
162	PD62	PD62
163	PD63	PD63
164	PA0	PA0
165	PA1	PA1
166	PA2	PA2
167	PA3	PA3
168	PA4	PA4

Table 3-3. Numerical Pin Listing (Continued)

	Name	
Number	**PCI**	**VL**
169	VCLK	VCLK
170	**VSS**	**VSS**
171	PA5	PA5
172	PA6	PA6
173	PA7	PA7
174	**VDD**	**VDD**
175	$\overline{\text{BLANK}}$	$\overline{\text{BLANK}}$
176	SC0	SC0
177	SC1	SC1
178	$\overline{\text{SE0}}$	$\overline{\text{SE0}}$
179	$\overline{\text{SE1}}$	$\overline{\text{SE1}}$
180	DCLK	DCLK
181	**VSS**	**VSS**
182	$\overline{\text{SE2}}$	$\overline{\text{SE2}}$
183	DSF	DSF
184	$\overline{\text{SE3}}$	$\overline{\text{SE3}}$
185	RS3/ODF	RS3/ODF
186	VSYNC	VSYNC
187	HSYNC	HSYNC
188	$\overline{\text{BGNT}}$	$\overline{\text{BGNT}}$
189	$\overline{\text{SENSE}}$/$\overline{\text{BREQ}}$	$\overline{\text{SENSE}}$/$\overline{\text{BREQ}}$
190	RS0	RS0
191	RS1	RS1
192	RS2	RS2
193	$\overline{\text{DACRD}}$	$\overline{\text{DACRD}}$
194	$\overline{\text{DACWR}}$	$\overline{\text{DACWR}}$
195	STWR	STWR
196	**VDD**	**VDD**
197	MCLK	MCLK
198	**VSS**	**VSS**
199	GD0	GD0
200	GD1	GD1
201	GD2	GD2
202	GD3	GD3
203	GD4	GD4
204	GD5	GD5
205	GD6	GD6
206	GD7	GD7
207	$\overline{\text{RMSTRD}}$	$\overline{\text{RMSTRD}}$
208	$\overline{\text{INTA}}$	SINTR

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Table 4-2. DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.4		V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	V_{DD} - 0.5		V
I_{OL1}	Output Low Current	4 (Note 1)		mA
I_{OH1}	Output High Current	-2		mA
I_{OL2}	Output Low Current	8 (Note 2)		mA
I_{OH2}	Output High Current	-4		mA
I_{OL3}	Output Low Current	16 (Note 3)		mA
I_{OH3}	Output High Current	-8		mA
I_{OL4}	Output Low Current	24 (Note 4)		mA
I_{OH4}	Output High Current	-10		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current		350	mA

Notes for Table 4-2

1. I_{OL1}, I_{OH1} for pins $\overline{\text{BLANK}}$, $\overline{\text{CAS}}$[7:0], $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$, GD[7:0], HSYNC, $\overline{\text{INTA}}$ (SINTR) $\overline{\text{MA}}$[8:0], MB[8:0], PA[7:0], PD[63:0], RS[2:0], RS3/ODF, $\overline{\text{RMSTRD}}$, STWR, VSYNC, SC[1:0], $\overline{\text{SE}}$[3:0], DSF
2. I_{OL2}, I_{OH2} for pins VCLK, AD[31:0]
3. I_{OL3}, I_{OH3} for pins $\overline{\text{OE}}$[1:0], $\overline{\text{RAS}}$[1:0]
4. I_{OL4}, I_{OH4} for pins PAR ($\overline{\text{ABEN}}$), $\overline{\text{STOP}}$ ($\overline{\text{DBEN}}$). $\overline{\text{DEVSEL}}$ ($\overline{\text{LOCA}}$), $\overline{\text{TRDY}}$ ($\overline{\text{SRDY}}$), $\overline{\text{WE}}$[1:0]

Note

Pin names for VL-Bus configurations are shown in parentheses.

4.3 AC SPECIFICATIONS

Notes

1. All AC timings are based on an 80 pF test load.
2. Functional timing diagrams are found in the appropriate functional description section, i.e, System Bus Interfaces, Display Memory or Miscellaneous Functions.

4.3.1 Clock Timing

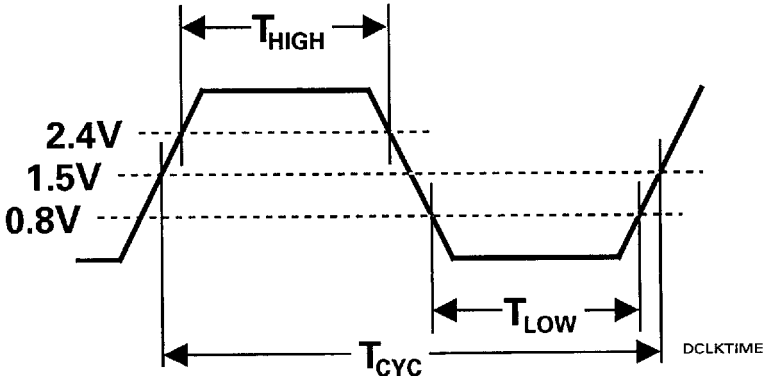


Figure 4-1. Clock Waveform Timing

Table 4-3. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	SCLK Cycle Time (VL-Bus)	20	125	ns	1
	SCLK Cycle Time (PCI)	30	125	ns	1
	MCLK Cycle Time	16.7	25	ns	
	DCLK Cycle Time (VGA Mode)	25	100	ns	1
	DCLK Cycle Time (Enhanced Mode)	10.5	100	ns	1
T_{HIGH}	SCLK High Time (VL-Bus)	8	80	ns	
	SCLK High Time (PCI)	12	80	ns	
	MCLK High Time	6	10	ns	
	DCLK High Time (VGA Mode)	10	65	ns	
	DCLK High Time (Enhanced Mode)	4	65	ns	
T_{LOW}	SCLK Low Time (VL-Bus)	8	80	ns	
	SCLK Low Time (PCI)	12	80	ns	
	MCLK Low Time	6	10	ns	
	DCLK Low Time (VGA Mode)	10	65	ns	
	DCLK Low Time (Enhanced Mode)	4	65	ns	
	SCLK Slew Rate	1	4	V/ns	2
	MCLK Slew Rate	1	4	V/ns	2
	DCLK Slew Rate	1	4	V/ns	2

Notes:

1. $f_{DCLK} \geq 1/2\ f_{SCLK}$ to ensure valid writes to the clock chip.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to peak portion of the clock waveform.

4.3.2 Input/Output Timing

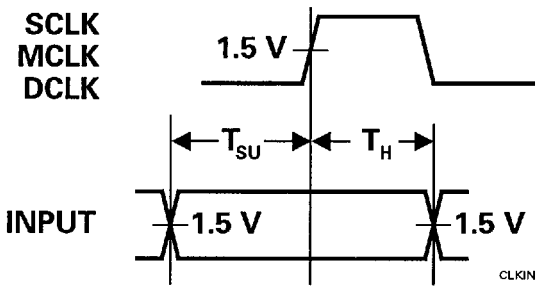


Figure 4-2. Input Timing

Table 4-4. SCLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:0], C/BE[3:0] , FRAME, IRDY, IDSEL setup	7	ns
T_H	AD[31:0] hold	1	ns
T_H	C/BE[3:0] , FRAME, IRDY, IDSEL hold	0	ns
VL-Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:2], BE[3:0] , SM/IO, SW/R, SADS (address phase) setup	6	ns
T_H	AD[31:2], BE[3:0] , SM/IO, SW/R, SADS (address phase) hold	0	ns
T_{SU}	AD[31:2], BE[3:0], D1, D0, SADS (data phase) setup	2	ns
T_H	AD[31:2], BE[3:0] , D1, D0, SADS (data phase) hold	0	ns
T_{SU}	RDYIN setup	6	ns
T_H	RDYIN hold	1	ns
Miscellaneous			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	ROM Data GD[7:0] Setup (PCI)	5	ns
T_H	ROM Data GD[7:0] Hold (PCI)	7	ns
T_{SU}	General Input Port GD[7:0] setup	5	ns
T_H	General Input Port GD[7:0] hold	7	ns

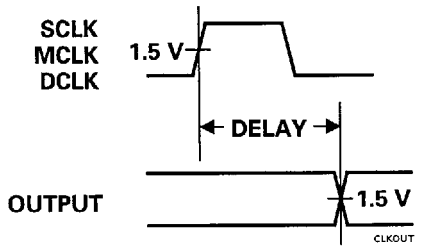


Figure 4-3. Output Timing

Table 4-5. SCLK-Referenced Output Timing

PCI Bus				
Parameter	**T_{MIN}**	**T_{MAX}**	**Units**	**Notes**
AD[31.0] valid delay	2	16	ns	1
$\overline{\text{DEVSEL}}$, PAR delay	2	11	ns	Medium $\overline{\text{DEVSEL}}$ timing used
$\overline{\text{STOP}}$ delay	2	11	ns	
$\overline{\text{TRDY}}$ delay	2	11	ns	
$\overline{\text{INTA}}$ delay	2	11	ns	
VL-Bus				
Parameter	**T_{MIN}**	**T_{MAX}**	**Units**	**Notes**
AD[31:2], D1, D0 valid delay	7	16	ns	
SINTR delay	5	30	ns	
$\overline{\text{SRDY}}$ delay	5	11	ns	
$\overline{\text{LOCA}}$ active delay	5	15	ns	
$\overline{\text{LOCA}}$ inactive delay	5	20	ns	
DBDIR delay	5	16	ns	
$\overline{\text{ABEN}}$, $\overline{\text{DBEN}}$ active delay (min non-overlap)	5	12	ns	
$\overline{\text{ABEN}}$, $\overline{\text{DBEN}}$ active delay (max non-overlap)	5	15	ns	
$\overline{\text{ABEN}}$, $\overline{\text{DBEN}}$ inactive delay	5	13	ns	
Miscellaneous				
Parameter	**T_{MIN}**	**T_{MAX}**	**Units**	**Notes**
RS[3:0] delay	5	20	ns	
$\overline{\text{RMSTRD}}$	3	15	ns	
ROM Address valid delay (PCI)	5	30	ns	
AD[7.0] ROM Data valid delay (PCI)	5	30	ns	

Note

1. Due to the timing for $\overline{\text{TRDY}}$ for read cycles, data is not sampled on the clock edge immediately following its becoming valid. This guarantees the PCI 2.0 specification time of 11 ns.

Table 4-6. MCLK-Referenced Input Timing

Symbol	Parameter	Min	Units
T_{SU}	PD[63:0] setup (EDO memory)	0	ns
T_H	PD[63:0] hold (EDO memory)	10	ns
T_{SU}	General Input Port GD[7:0] setup	5	ns
T_H	General Input Port GD[7:0] hold	7	ns

Table 4-7. MCLK-Referenced Output Timing

Parameter	T_{MIN}	T_{MAX}	Units
$\overline{RAS}$[1:0] active delay	4	12	ns
$\overline{RAS}$[1:0] inactive delay	4	10	ns
$\overline{CAS}$[7:0], $\overline{OE}$[1:0], $\overline{WE}$[1:0] active delay	5	12	ns
$\overline{CAS}$[7:0], $\overline{OE}$[1:0], $\overline{WE}$[1:0] inactive delay (min stretch)	4	8	ns
$\overline{CAS}$[7:0], $\overline{OE}$[1:0], $\overline{WE}$[1:0] inactive delay (max stretch)	6	17	ns
MA[8:0], MB[8:0] valid delay	5	24	ns
PD[63:0] valid delay	5	27	ns
$\overline{DACRD}$, $\overline{DACWR}$ delay	3	20	ns
SC[1:0] valid delay	8	20	ns
DSF valid delay	5	12	ns

Table 4-8. DCLK-Referenced Output Timing

Parameter	T_{MIN}	T_{MAX}	Units
$\overline{BLANK}$, HSYNC, VSYNC	3	17	ns
PA[15:0] valid delay	5	14	ns
STWR delay	3	15	ns
General Output Port Data GD[7:0] delay	5	20	ns
SC[1:0] valid delay	8	20	ns
$\overline{SE}$[3:0] valid delay	8	20	ns
VCLK delay	5	16	ns

Table 4-9. Fast Page Mode Memory Input Timing

Symbol	Parameter	Min	Units
T_{SU}	PD[63:0] setup to $\overline{CAS}$[7:0] inactive	0	ns
T_H	PD[63:0] hold from $\overline{CAS}$[7:0] inactive	5	ns

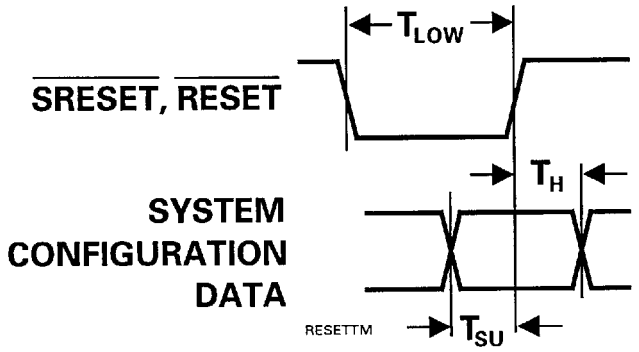


Figure 4-4. Reset Timing

Table 4-10. Reset Timing

Symbol	Parameter	Min	Units
T_{LOW}	SRESET (VL) or RESET (PCI) active pulse width	400	ns
T_{SU}	PD[23:0] setup to SRESET (VL) or RESET (PCI) inactive	20	ns
T_H	PD[23:0] hold from SRESET (VL) or RESET (PCI) inactive	10	ns

4.4 POWER ISOLATION CONSIDERATIONS

Because of electrical noise considerations, each power (VDD) pin must be isolated as shown in Figure 4-5. The layout with each power pin properly isolated is shown in Figure 4-6.

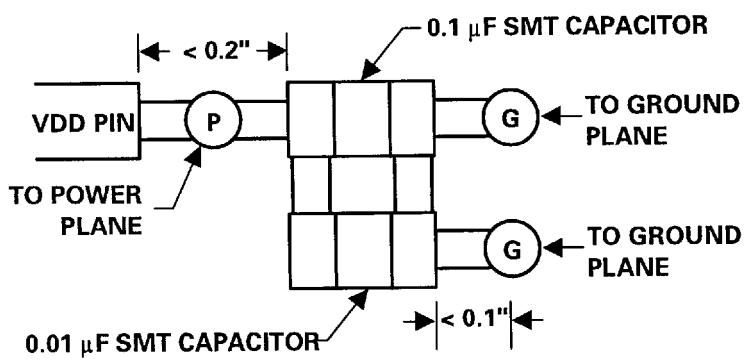


Figure 4-5. Power Pin Isolation Detail

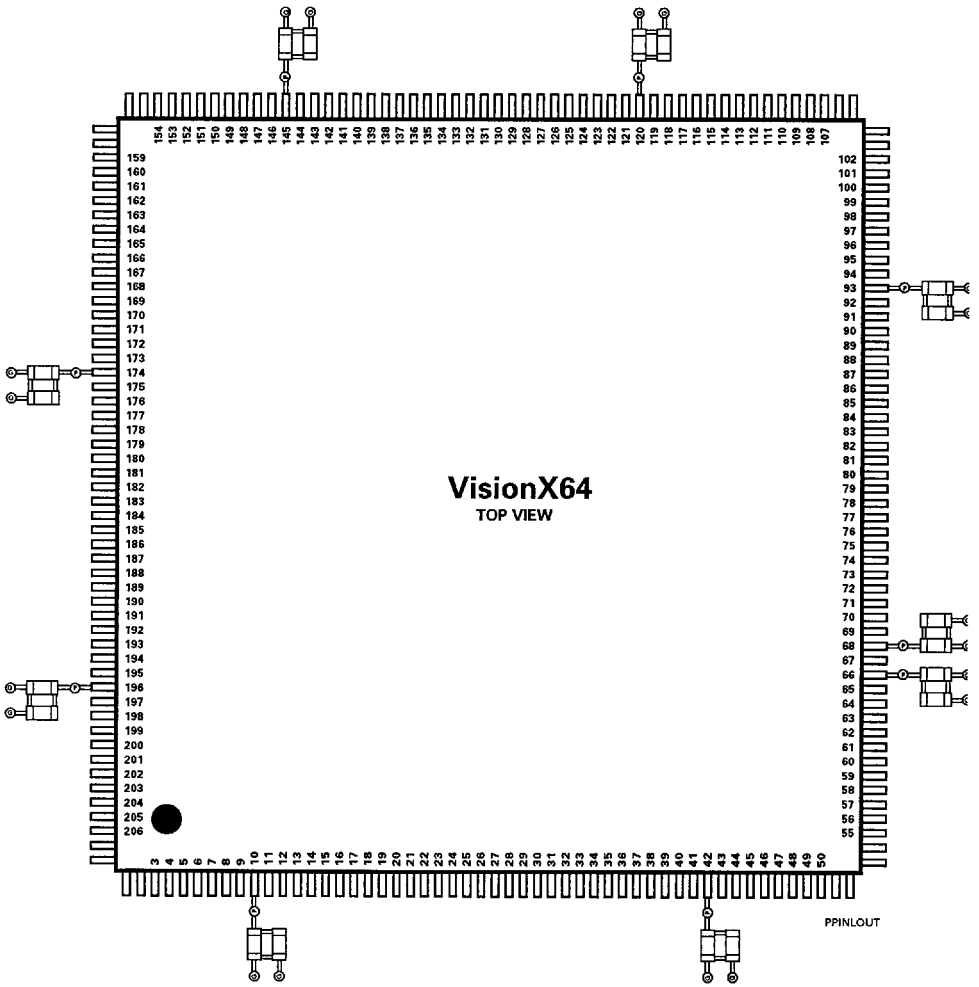


Figure 4-6. Power Pin Connection Requirements

Section 5: Reset and Initialization

The reset signal ($\overline{\text{RESET}}$ for PCI, $\overline{\text{SRESET}}$ for VL-Bus) is clocked into the Vision964 by the DCLK input. This resets the internal state machines in the Vision964 and places all registers in their power-on default states. It also initiates several configuration actions, as described in this section.

5.1 CONFIGURATION STRAPPING

The PD[23:0] pins can be individually pulled either high or low through 47 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins as part of the pixel data bus, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled and the data loaded into the CR36, CR37 and CR68 registers. The data is used for system configuration, such as system bus and memory parameter selection. The definitions of the PD[23:0] strapping bits at the rising edge of the reset signal are shown in Table 5-1.

Strapping bits 7-5 define the display memory size. However, the S3 BIOS determines this value directly and writes it to CR36 bits 7-5 after reset. Therefore, systems using the S3 BIOS do not need to strap the PD[7-5] pins. Other pins may also not require strapping, depending on the design and bus type.

Strapping bits 15-13 provide monitor information. The interpretation of the bit values is dependent on the video BIOS.

5.2 GENERAL DATA BUS AT RESET

At power-on reset, the GD[3:0] lines are all zeros and the STWR signal is asserted to latch them into the clock chip. See the Clock Generator discussion in the Miscellaneous Interfaces section of this data book for more details.

The GD[7:5] lines are input at reset and the values on these lines are latched into bits 6-4 of the 42E8H register. These are user-definable bits. An external source (such as monitor ID lines) can be connected to the General Input Port bits 7-5 and these will be captured on reset. Alternately, GD[7:5] can be strapped high or low through 47 KΩ resistors to set bits 6-4 of 42E8H to a fixed value on reset.

The GD4 pin is tri-stated on reset.

5.3 PREVENTING BUS LOADS DURING RESET

The VL-Bus specification requires that the address and data busses not be driven during reset. To ensure this, the $\overline{\text{ABEN}}$ and $\overline{\text{DBEN}}$ pins should be pulled high through 10 KΩ resistors. This prevents them from floating low during reset and allowing the busses to be driven.

Table 5-1. Definition of PD[23:0] at the Rising Edge of the Reset Signal

CR Bits	PD Bits	Value	Function
	System Bus Select		
CR36_1-0	1-0	00	Reserved
		01	VESA local bus
		10	PCI local bus
		11	Reserved
	Memory Page Mode Select		
CR36_3-2	3-2	00	Reserved
		01	Reserved
		10	Extended Data Out (EDO) mode
		11	Fast page mode
	Enable BIOS ROM (VL-Bus)		
CR36_4	4	0	Disable BIOS ROM access (system BIOS contains video BIOS)
		1	Enable BIOS ROM access
	Display Memory Size		
CR36_7-5	7-5	000	4 MBytes
		001	Reserved
		010	Reserved
		011	8 MBytes
		100	2 MBytes
		101	Reserved
		110	1 MByte
		111	Reserved
	Setup Select (VL-Bus)		
CR37_0	8	0	Disable Vision964 except for BIOS ROM accesses
		1	Enable Vision964
	Test Mode		
CR37_1	9	0	All outputs except $\overline{OE}$ tri-stated and all bi-directional pins become inputs
		1	Normal operation. Certain outputs required for the reset process are not tri-stated during reset
	BIOS ROM Size (VL-Bus)		
CR37_2	10	0	64-KByte BIOS
		1	32-KByte BIOS
	Dual $\overline{CAS}$ Select		
CR37_3	11	0	Dual $\overline{WE}$ byte select
		1	Dual $\overline{CAS}$ byte select
	RAMDAC Write Snooping (VL-Bus)		
CR37_4	12	0	Disable $\overline{LOCA}/\overline{SRDY}$ for RAMDAC Writes
		1	Enable $\overline{LOCA}/\overline{SRDY}$ for RAMDAC Writes

Table 5-1. Definition of PD[23:0] at the Rising Edge of the Reset Signal (Continued)

CR Bits	PD Bits	Value	Function
	Monitor Identification		
CR37_7-5	15-13		The S3 BIOS uses these bits for monitor information
	$\overline{CAS}$/$\overline{OE}$ Low Stretch		
CR68_1-0	17-16	00	6.5 ns delay (nominal)
		01	5 ns delay (nominal)
		10	3.5 ns delay (nominal)
		11	No delay
	Memory Address Depth Select		
CR68_3-2	19-18	00	Reserved
		01	Reserved
		10	Reserved
		11	256 K (512 rows x 512 columns)
	$\overline{RAS}$ Low Timing Select		
CR68_5-4	21-20	00	6.5 MCLKs
		01	5.5 MCLKs
		10	4.5 MCLKs
		11	3.5 MCLKs
	$\overline{RAS}$ Pre-Charge Timing Select		
CR68_7-6	23-22	00	Reserved
		01	4.5 MCLKs
		10	3.5 MCLKs
		11	2.5 MCLKs

5.4 TEST MODE

Upon power-on reset, most Vision964 output pins are tri-stated. However, some must be kept active to support the reset process. To facilitate bed-of-nails testing at the PCB level, the Vision964 incorporates a test mode that tri-states all output pins except $\overline{OE}$[1:0] (which are driven high) and makes all bi-directional pins inputs. To enter this mode, power-on strapping bit 9 (CR37, bit 1) must be pulled low at reset. The outputs that are normally not tri-stated on reset but which are tri-stated in test mode are shown in Table 5-2. The Vision964 remains in test mode as long as the reset signal is held low.

Table 5-2. Signals Tri-Stated by Test Mode

Signal Name
VCLK
HSYNC
VSYNC
$\overline{BLANK}$
STWR
GD[3:0]
$\overline{RAS0}$
$\overline{CAS}$[7:0]
$\overline{WE}$[1:0]

Section 6: System Bus Interfaces

The Vision964 interfaces to either a PCI bus or a VESA local bus (VL-Bus). This section describes the connections and functional characteristics of these interfaces.

6.1 PCI BUS INTERFACE

The Vision964 provides a complete PCI interface. Power-on strapping bits 1-0 must be set to 10b to enable this interface. The pinout and other specifications are in conformance with Revision 2 of the the PCI specification. No glue logic is required.

6.1.1 PCI CONFIGURATION

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 88D0H to specify the Vision964. Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium $\overline{\text{DEVSEL}}$ timing. Bit 0 of the Programming Interface register (Index 0AH) is hardwired to 1 to specify that the Vision964 supports the standard VGA programming interface. Bits 3-0 of the Base Address 0 register (Index 10H) are hardwired to 00H. This indicates that the "prefetchable" bit is cleared to 0, that the base register can be located anywhere in a 32-bit address space and that the base register is located in memory space.

6.1.2 PCI Bus Cycles

Figures 6-1 and 6-2 show the basic PCI read and write cycles respectively. Bit 1 of the PCI Command register (Index 04H) must be set to 1 to allow memory space access. Bit 0 of the PCI Command register must be set to 1 to allow I/O space access.

Figures 6-3 and 6-4 show two examples of PCI bus disconnection. These examples show cases where data is transferred after $\overline{\text{STOP}}$ is asserted. In example A, data is transferred after $\overline{\text{FRAME}}$ is deasserted because the master was not ready ($\overline{\text{IRDY}}$ deasserted on clock 2). In example B, data is transferred before $\overline{\text{FRAME}}$ is deasserted. See the *PCI Local Bus Specification* for a complete explanation of disconnects. Bit 7 of the CR66 register must be set to 1 to enable PCI disconnects.

The PCI configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. Figures 6-5 and 6-6 show the configuration read and write cycles respectively. The Vision964 supports or returns 0 for the first 64 bytes of configuration space.

The Vision964 drives even parity information onto the PAR line during read transactions. This operation is depicted in Figure 6-7.

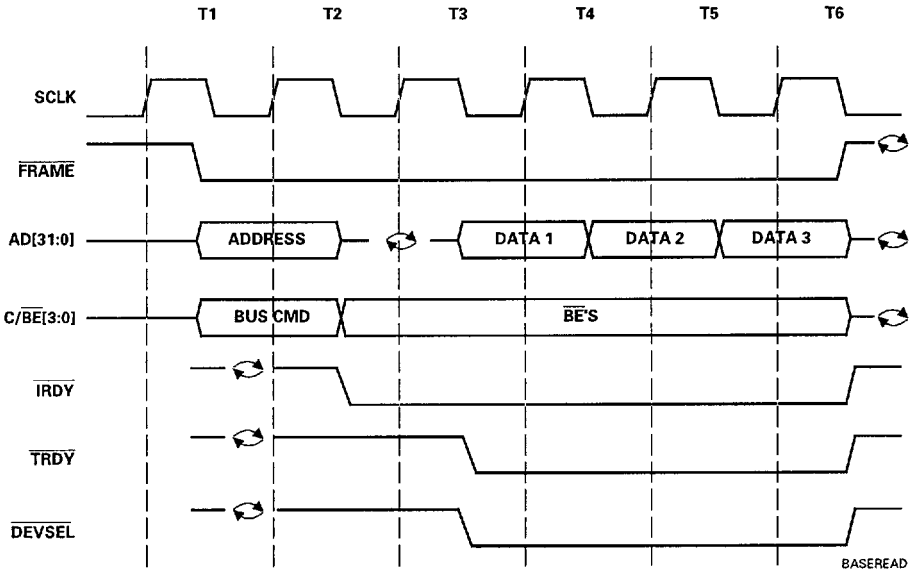


Figure 6-1. Basic PCI Read Cycle

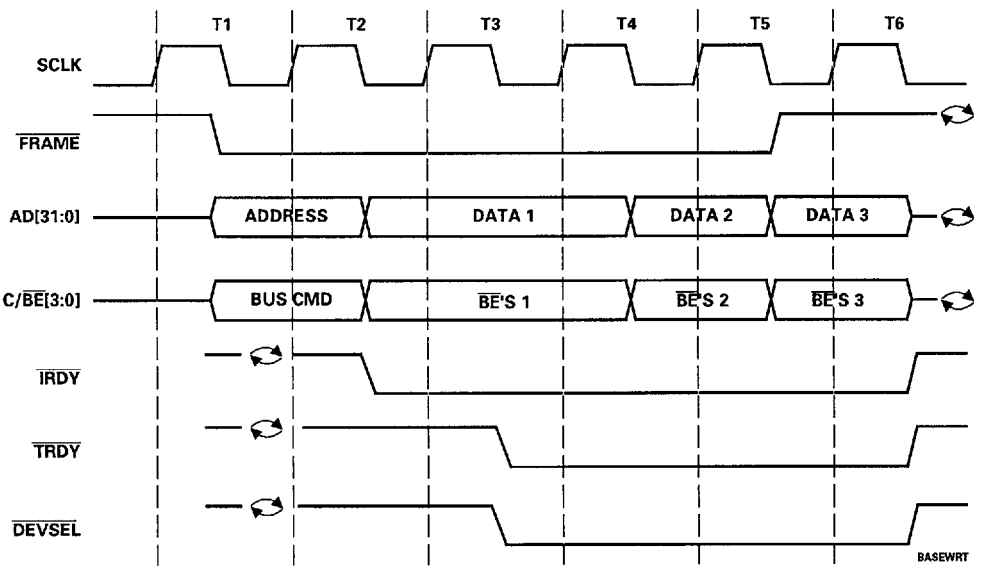


Figure 6-2. Basic PCI Write Cycle

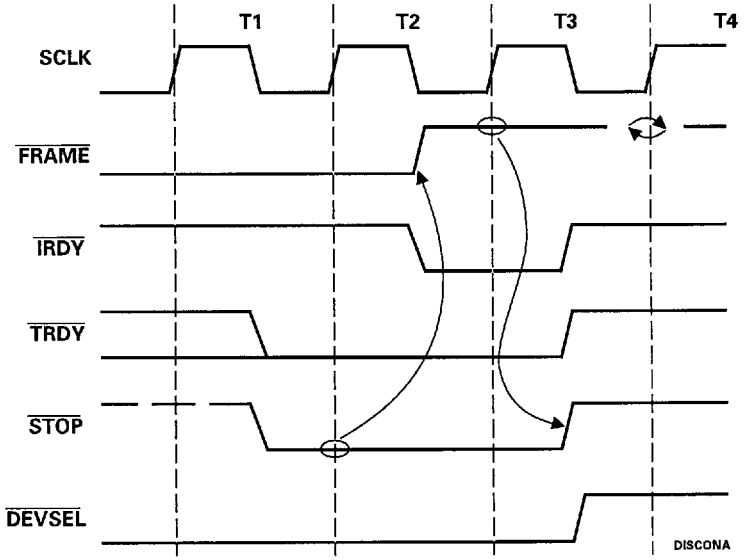


Figure 6-3. PCI Disconnect Example A

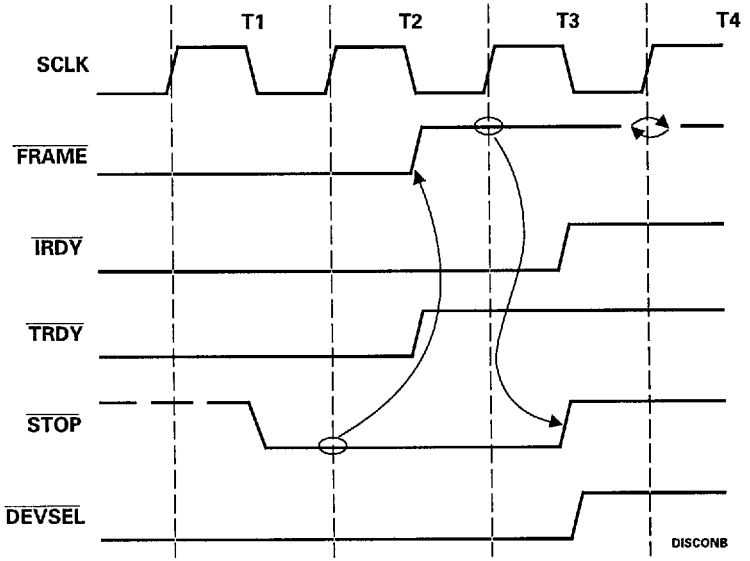


Figure 6-4. PCI Disconnect Example B

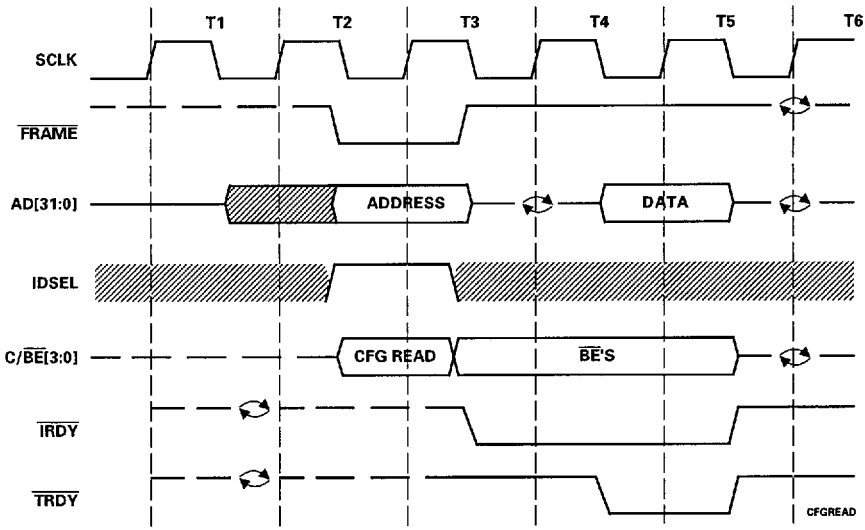


Figure 6-5. PCI Configuration Read Cycle

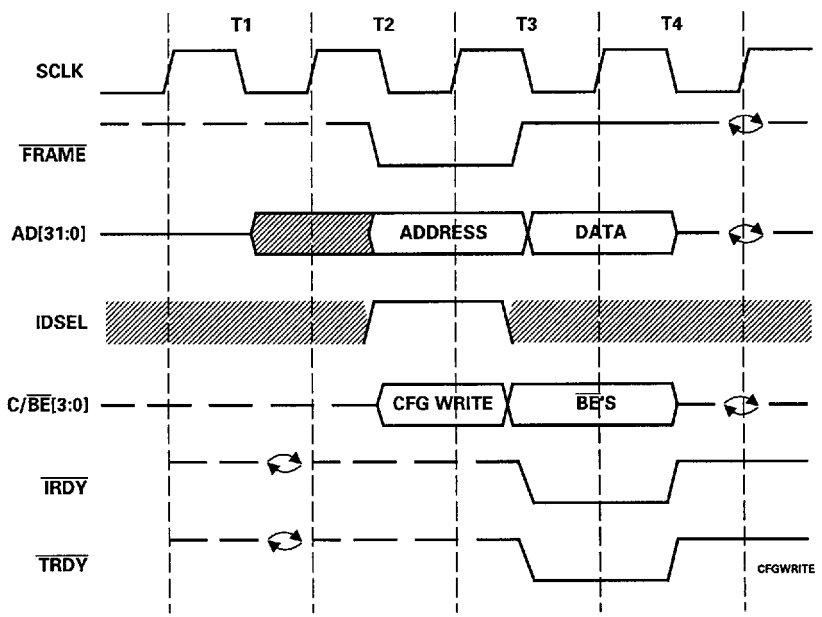


Figure 6-6. PCI Configuration Write Cycle

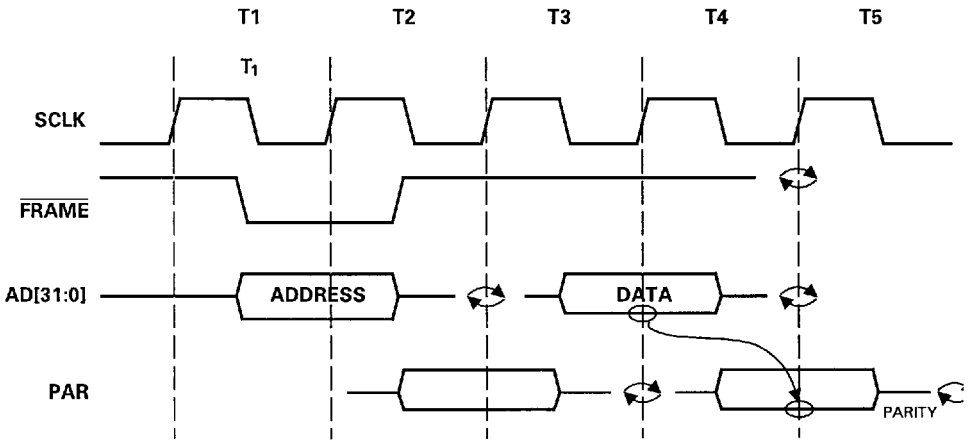


Figure 6-7. Read Parity Operation

6.2 VL-BUS INTERFACE

Power-on strapping bits 1-0 must be set to 01b to enable VL-Bus operation. Because the address and data busses are multiplexed on the same pins, a VL-Bus interface requires glue logic to provide the correct bus information and direction. Figure 6-8 shows how eight F245-type devices are configured to provide the necessary control. One or more specialized ASICs are available to reduce the number of chips required to provide this interface. The buffer enables ($\overline{ABEN}$ and $\overline{DBEN}$) and the data buffer direction signal (DBDIR) are provided by the Vision964.

6.2.1 VL-Bus Cycles

The basic VL-Bus read cycle is shown in Figure 6-10. Note that the A[31:2], M/$\overline{IO}$ and W/$\overline{R}$ inputs from the VL-Bus must first pass through the interface buffers, which in turn feed AD[31:2], SM/$\overline{IO}$ and SW/$\overline{R}$ to the Vision964. The address is latched by the Vision964 on one of two rising SCLK edges as shown in Figure 6-10 and explained in Note 1. The programmability of the gap between $\overline{ABEN}$ deasserted and $\overline{DBEN}$ asserted and vice versa is also indicated in Figure 6-10 and explained by Note 2. During this gap, the address/data bus is tri-stated and switches from address input to data output. The progress of the data back through the interface buffers to the VL-Bus is not shown on the diagram.

The basic VL-Bus write cycle is shown in Figure 6-11. The cycle is similar to a read cycle except there is no bus turnaround when the direction of the interface buffers is reversed. The single wait-state is the default configuration. This can be changed to 0 wait-states ($\overline{SRDY}$ asserted one cycle earlier) by clearing bit 4 of CR40 to 0. The address is latched at the end of T1. By default, write data is latched on the first rising SCLK edge after the assertion of $\overline{RDYIN}$. This can be changed to the first rising SCLK edge after the assertion of $\overline{SRDY}$ by setting bit 5 of CR40 to 1.

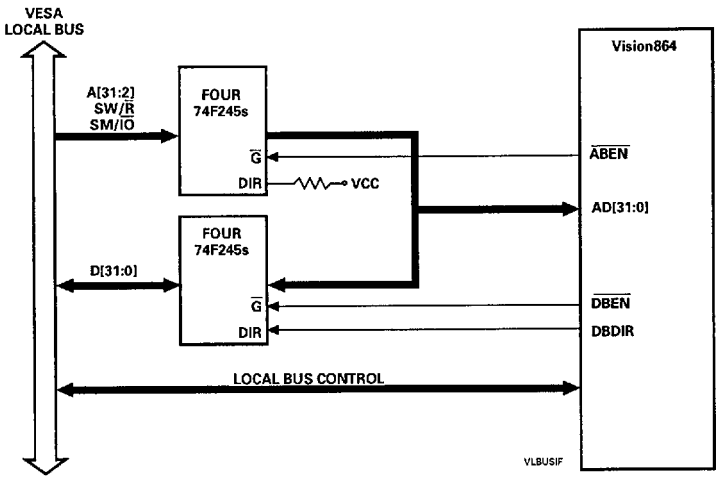


Figure 6-8. VL-Bus Interface

6.2.2 SRDY Generation

For a VL-Bus configuration, the Vision964 raises its SRDY output early in the T_1 cycle and then tri-states it. It then asserts SRDY to signal the end of the cycle. Some systems synchronize or otherwise delay this signal and then assert RDY to the processor. If this is done, this RDY signal should also be fed to the RDYIN input of the Vision964 (see Note 3 of Figure 6-10). The Vision964 holds read data active until RDYIN is asserted. If the SRDY signal is not intercepted, it should be fed to both the processor RDY input and the Vision964 RDYIN input.

6.3 LOCAL BUS CLOCKING

The Vision964 expects a 1X SCLK like that used in a 486 system. Figure 6-9 shows one possible circuit for building such a 1X clock from the 386 2X clock. Since the Vision964 requires a clock during reset, any circuit used to generate a synchronized 1X clock must be free-running during reset.

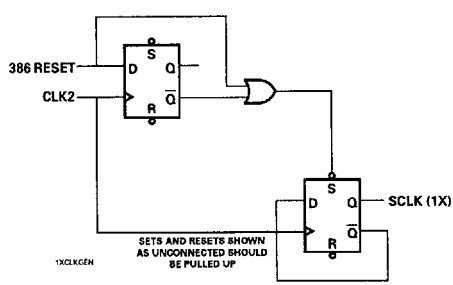


Figure 6-9. 1X Clock Generation

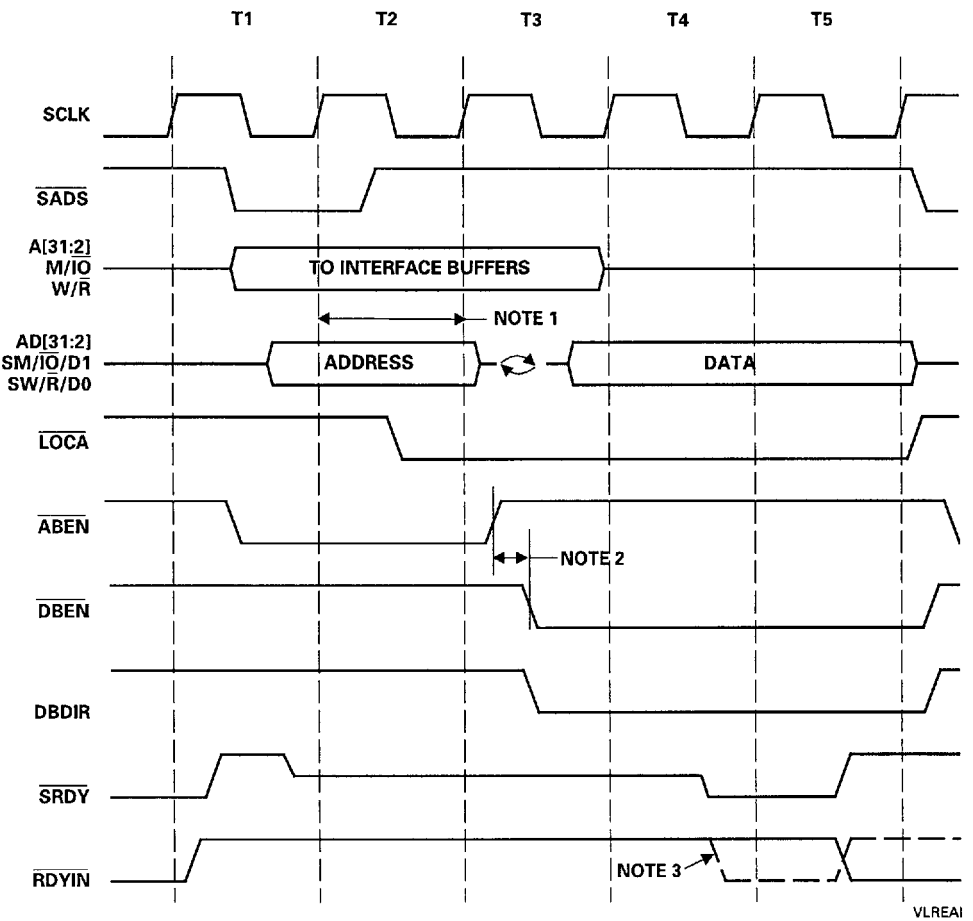


Figure 6-10. VL-Bus Read Cycle

Notes

1. The address is latched on the first clock edge indicated here if bit 3 of CR58 is set to 1. If this bit is cleared to 0, the address is latched on the second clock edge indicated.
2. The non-overlap time between $\overline{\text{ABEN}}$ deasserted and $\overline{\text{DBEN}}$ asserted (and vice versa) is programmable via bits 7-6 of CR40.
3. The system chip set can delay the $\overline{\text{RDYIN}}$ input by 1 or more cycles. This example assumes a 1 cycle delay, as indicated by the solid line. Note that read data is held valid an extra cycle.

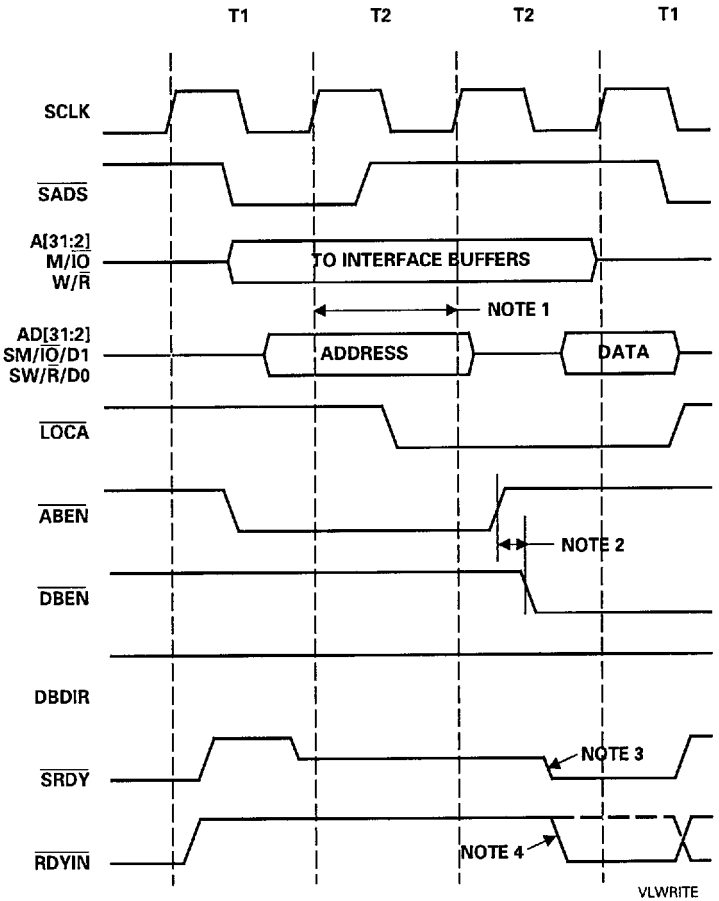


Figure 6-11. 1 Wait-state VL-Bus Write Cycle

Notes

1. For one decode wait state (bit 4 of CR40 set to 1), the address is latched on the first clock edge indicated here if bit 3 of CR58 is set to 1. If this bit is cleared to 0, the address is latched on the second clock edge indicated.
2. The non-overlap time between $\overline{ABEN}$ deasserted and $\overline{DBEN}$ asserted (and vice versa) is programmable via bits 7-6 of CR40
3. The wait-state is inserted by setting bit 4 of CR40 to 1 to delay $\overline{SRDY}$ assertion by 1 cycle from the assertion of $\overline{SADS}$. This is the default value.
4. Data is normally latched on the rising SCLK edge following assertion of $\overline{RDYIN}$. This can be changed to the rising clock edge following the assertion of $\overline{SRDY}$ by setting bit 5 of CR40 to 1.

Section 7: Display Memory

The Vision964 supports a VRAM-based video frame buffer. This section describes the various configurations supported, the functional timing for memory accesses and the operation of various register bits that affect memory timing and operation. It also describes how access to display memory is controlled to maximize graphics performance in VGA modes and how the Vision964 can share the frame buffer with a secondary memory controller for multimedia applications.

7.1 DISPLAY MEMORY CONFIGURATIONS

The Vision964 provides direct support for 1-, 2-, 4- and 8- MByte VRAM configurations. 256Kx4, x8 or x16 VRAMs can be used.

The Vision964 has a dual-$\overline{CAS}$ mode for x16 VRAMs with two $\overline{CAS}$es and one $\overline{WE}$. It also has a dual-$\overline{WE}$ mode for x16 VRAMs with two $\overline{WE}$s and one $\overline{CAS}$. Power-on strapping bit 11 is pulled high on reset to select dual-$\overline{CAS}$ mode and low to select dual-$\overline{WE}$ mode. Dual-$\overline{CAS}$ mode should be selected for x4 or x8 VRAMs, which have only one $\overline{CAS}$ and one $\overline{OE}$ input.

In dual-$\overline{CAS}$ mode, the Vision964's $\overline{CAS}$ lines connect to the $\overline{CAS}$ lines on the VRAMs and select which bytes are accessed. The $\overline{WE0}$/$\overline{OE0}$ lines select the first and third 2-MByte banks, and the $\overline{WE1}$/$\overline{OE1}$ lines select the second and fourth 2-MByte banks. The $\overline{RAS0}$ line selects the first 4 MBytes and the $\overline{RAS1}$ line selects the second 4 MBytes.

On the serial out (SID) side of the VRAM, the SC[1:0] and $\overline{SE}$[3:0] lines control the output. How these lines are connected depends on the memory size, SID bus size and whether serial, (non-interleaved) or parallel. (interleaved) addressing is used. Bits 5-4 of CR66 define the addressing mode as a function of SID bus size. For 128-bit SID bus operation, bit 5 of CR53 and bits 7-6 of CR65 must also be appropriately set.

Figure 7-1 shows a 4-MByte configuration using 256Kx8 VRAMs and a 32-bit SID RAMDAC. Memory above 1 MByte is optional. If bits 5-4 of CR66 are set to 11b, this configuration uses serial addressing. Figure 7-12 shows the functional timing for this mode of operation (only SID[31:0] are applicable). Note that SC0 and SC1 are identical signals and consecutive 4-byte outputs come from the same memory bank unless the address changes to another bank (selected by $\overline{SE}$, as shown by the 4th data out unit). If bits 5-4 of CR66 are set to 01b, this configuration uses parallel addressing. (At least 2 MBytes of memory are required.) SC0 and SC1 are 180° out of phase and drive 4-byte outputs to the 32-bit SID bus from alternating (even and odd) memory banks. Figure 7-11 provides the functional timing for this mode of operation. With sufficient memory, parallel addressing is recommended because it automatically uses 1/2 the SC frequency of serial addressing and allows the use of slower memory and/or supports higher resolutions.

Figure 7-2 shows a 4-MByte configuration using 256Kx8 VRAMs and a 64-bit SID RAMDAC. At least 2 MBytes are required to support the 64-bit SID bus. The second two MBytes are optional. This configuration is connected for serial addressing. Bits 5-4 of CR66 must be cleared to 00 to support this configuration. Figure 7-12 provides the functional timing for this mode of operation.

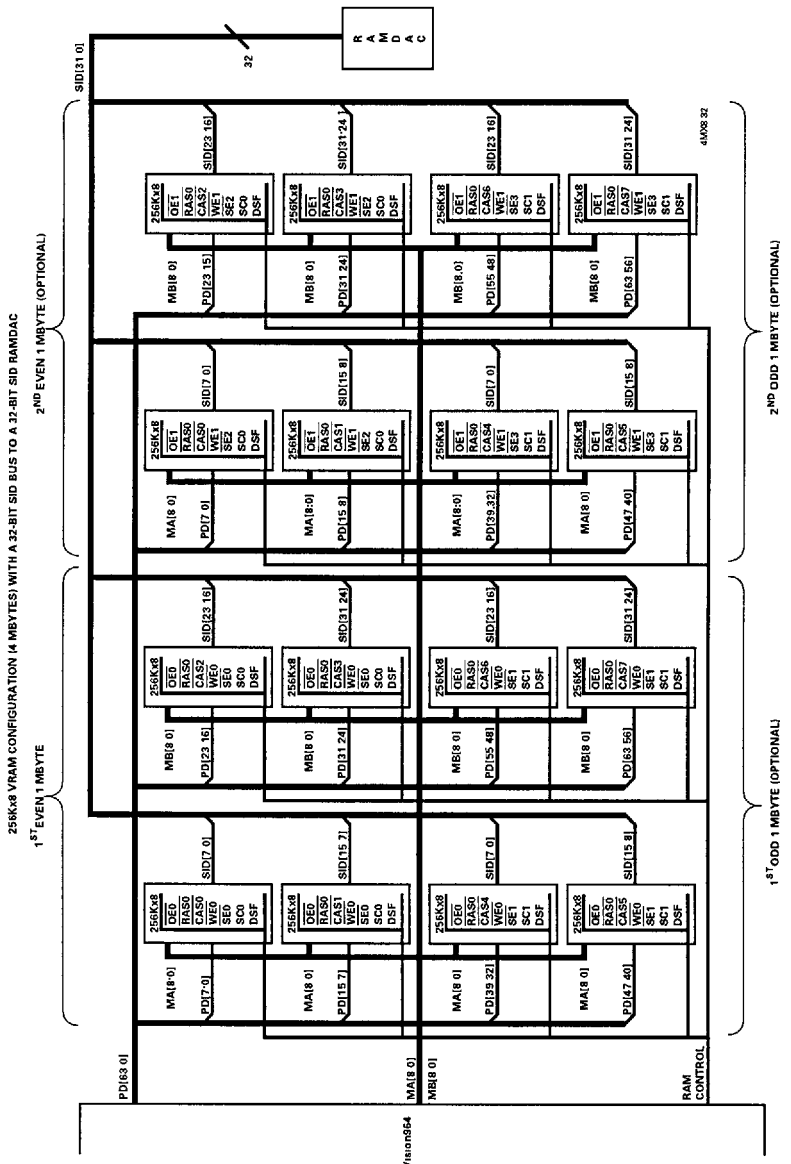


Figure 7-1. 4-MByte DRAM Configuration (32-Bit SID)

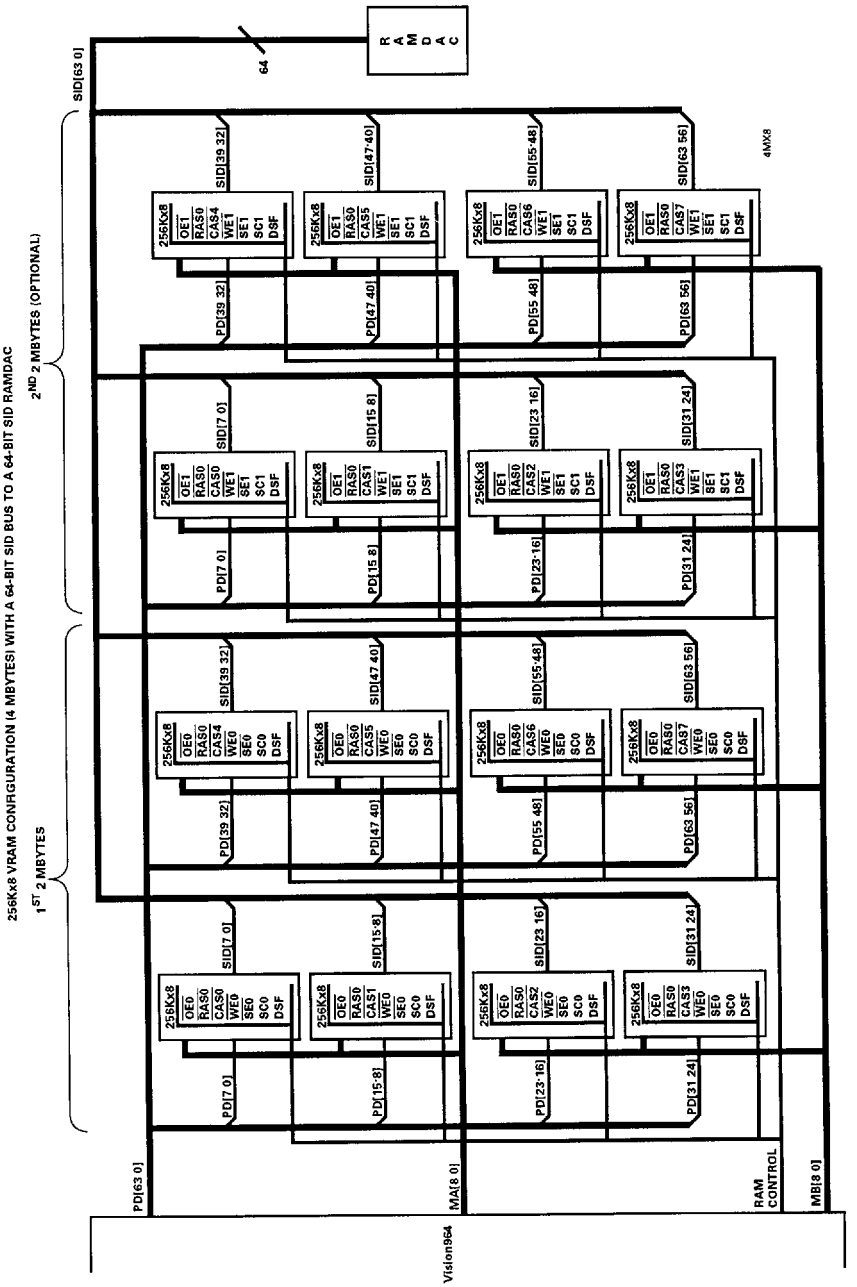


Figure 7-2. 4-MByte DRAM Configuration (64-bit SID)

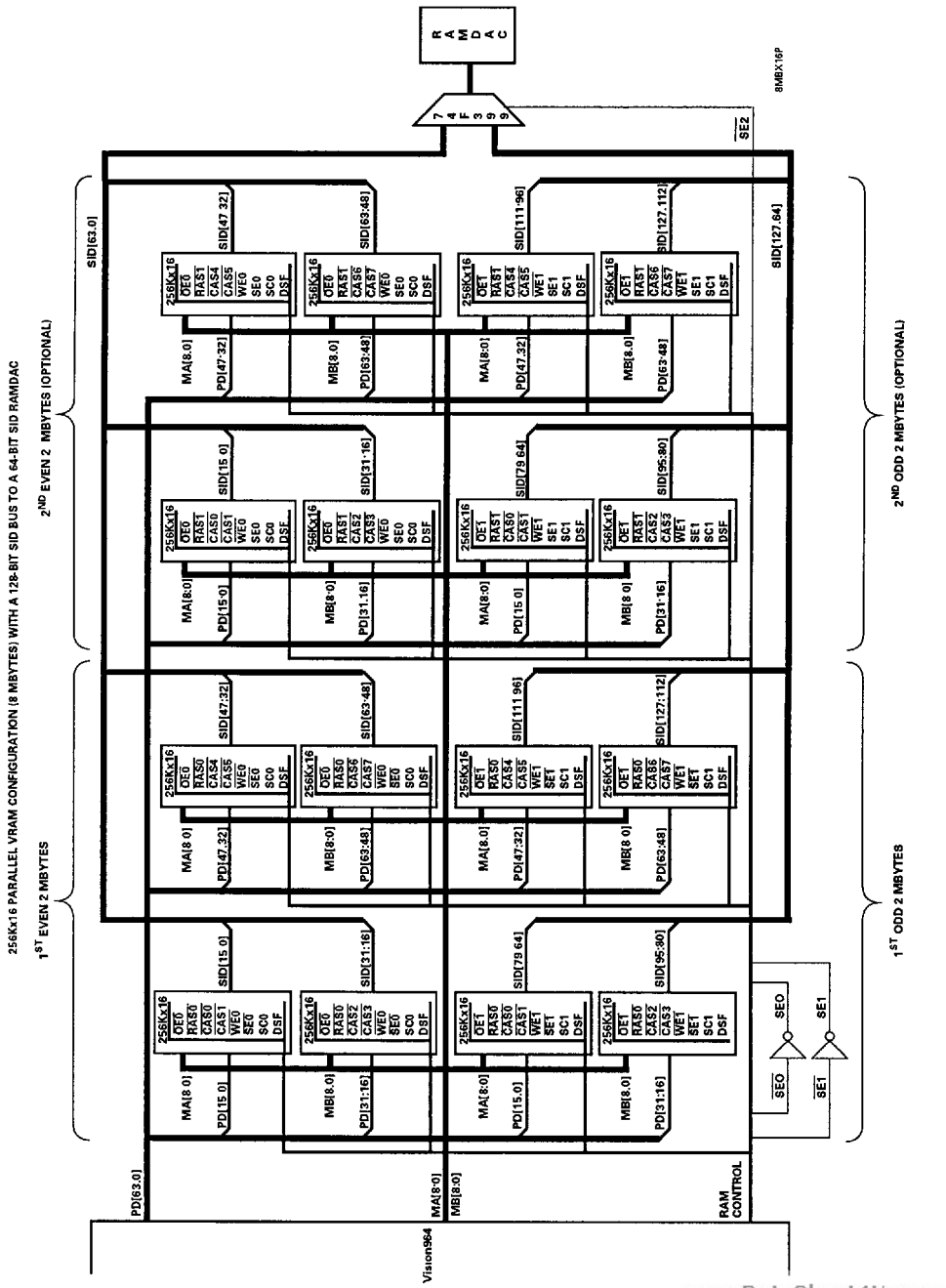


Figure 7-3. 8-MByte Parallel VRAM Configuration

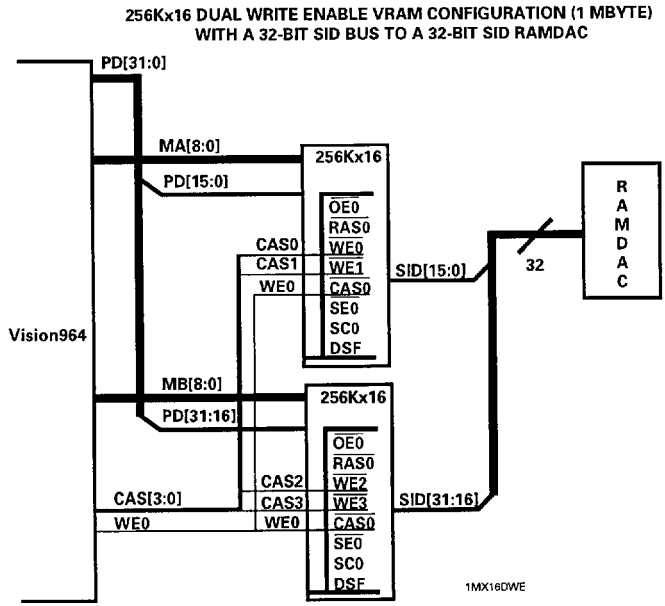


Figure 7-4. 1-MByte Dual-WE VRAM Configuration

Figure 7-3 shows an 8-MByte configuration using 256Kx16 VRAMs, a 64-bit SID RAMDAC and parallel addressing. Bits 5-4 of CR66 must be set to 10b to support this configuration. In addition, bit 5 of CR53 must be set to 1 and bits 7-6 of CR65 must be set appropriately, depending on the type of VRAM used. Figure 7-13 provides the functional timing for this mode of operation. Note that the $\overline{SE0}$ and $\overline{SE1}$ lines are inverted before they are connected to the second odd and even 2 MBytes. This is indicated by the removal of the overbars on these inputs. $\overline{SE2}$ is the selector input to the MUX.

All the configurations described above use dual-$\overline{CAS}$ mode. In dual-$\overline{WE}$ mode, the $\overline{CAS}$ and $\overline{WE}$ lines are swapped. That is, the eight $\overline{CAS}$ lines are connected to the $\overline{WE}$ inputs on the VRAMs and the two $\overline{WE}$ lines are connected to the $\overline{CAS}$ inputs on the VRAMs. This is illustrated in Figure 7-4 for a 1-MByte 256Kx16 configuration using a 32-bit SID RAMDAC. Note that only PD[31:0] are used for 1-MByte configurations. The unconnected VRAM signals shown on this figure tie directly to the corresponding signals on the Vision964. The swapping of $\overline{CAS}$ and $\overline{WE}$ is required for x4 and x8 VRAMs if the Vision964 is placed in dual-$\overline{WE}$ mode on reset. However, this use is not recommended.

Two memory address busses (MA[8:0] and MB[8:0]) are provided. MA[8:0] control PD[15:0] and PD[47:32]. MB[8:0] control PD[31:16] and PD[63:48].

7.2 DISPLAY MEMORY REFRESH

The Vision964 uses the standard $\overline{CAS}$ before $\overline{RAS}$ RAM refresh method. The functional timing for this can be found in any standard VRAM data book.

The number of refresh cycles performed per horizontal line is determined by bit 6 of CR11. If bit 2 of CR3A is set to 1, the number of refresh cycles per horizontal line is determined by the setting of bits 1-0 of CR3A.

7.3 DISPLAY MEMORY FUNCTIONAL TIMING

Figure 7-5 shows the functional timing for a fast page mode read cycle. This also shows how certain parameters for various control signals can be adjusted to meet the access time requirements of a variety of VRAMs. Bits 1-0 of CR68 allow the pulse widths of the $\overline{CAS}$ and $\overline{OE}$ signals to be adjusted. Bits 5-4 of CR68 allow adjustment of the $\overline{RAS}$ low time. Bits 7-6 of CR68 allow adjustment of the $\overline{RAS}$ precharge (high) time. All of these settings in CR68 can be made by power-on strapping of PD[23:16] at reset or by programming after reset.

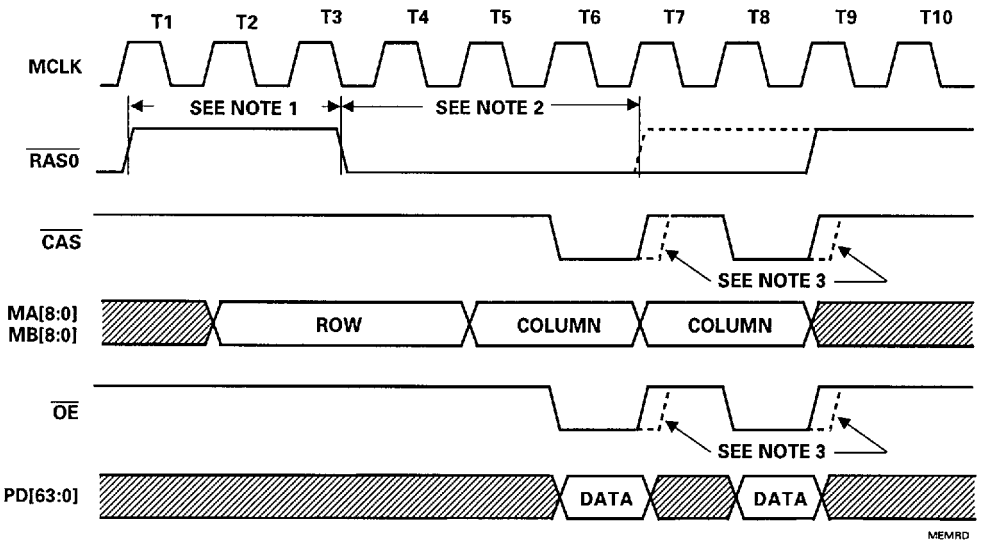


Figure 7-5. Fast Page Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 4.5 MCLKs via bits 7-6 of CR68.
2. The minimum $\overline{RAS}$ low time for a single column access is 3.5 MCLKs as shown in this figure. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This minimum $\overline{RAS}$ active time can be lengthened to 4.5, 5.5 or 6.5 MCLKs via bits 5-4 of CR68.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

Figure 7-6 shows the functional timing for a fast page mode write cycle. The $\overline{RAS}$ and $\overline{CAS}$ signals can be adjusted as explained for the read cycle above. The $\overline{WE}$ and $\overline{CAS}$ signals are equally stretched via bits 1-0 of CR68.

The write-per-bit feature provided by VRAMs is supported by the Vision964 if bit 0 of CR53 is set to 1. This is indicated by the WPB Mask in Figure 7-5.

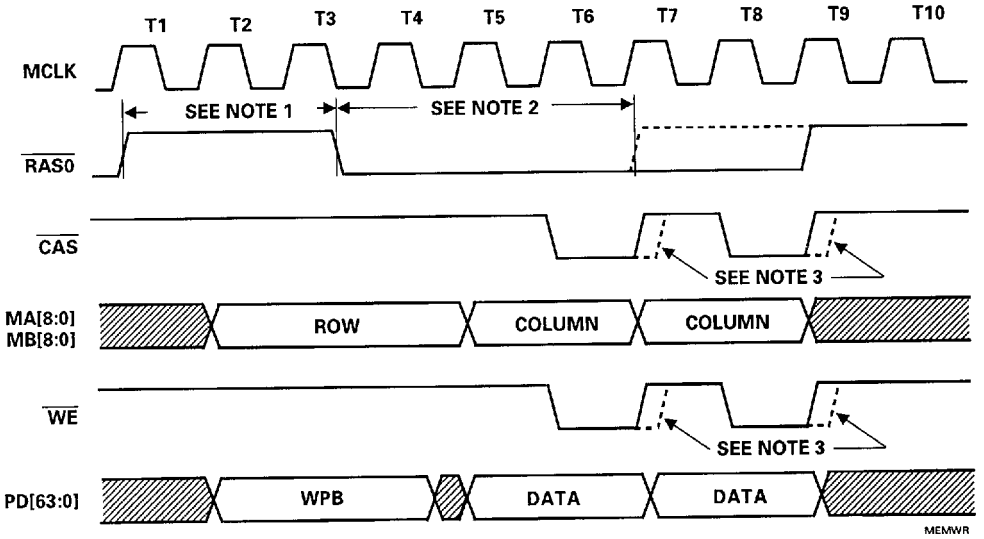


Figure 7-6. Fast Page Mode Write Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 4.5 MCLKs via bits 7-6 of CR68.
2. The minimum $\overline{RAS}$ low time for a single column access is 3.5 MCLKs as shown in this figure. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This minimum $\overline{RAS}$ active time can be lengthened to 4.5, 5.5 or 6.5 MCLKs via bits 5-4 of CR68.
3. The $\overline{CAS}$ and $\overline{WE}$ active (low) times can be stretched via bits 1-0 of CR68.

Figure 7-7 shows the functional timing for an Extended Data Out (EDO) mode read cycle. One difference between an EDO read cycle and a fast page mode read cycle is that since EDO memory holds the data valid after $\overline{CAS}$ is deactivated, it allows the data to be latched one cycle later (rising edges of T8 and T10). This allows the use of slower access time memory or a faster MCLK. However, the last page access (or first for a single access) must be stretched one MCLK to allow the data to be latched because EDO memory does not keep data valid after $\overline{OE}$ goes inactive. Note that $\overline{RAS}$ and $\overline{OE}$ are all stretched one MCLK. With EDO, $\overline{OE}$ is held low for the entire cycle instead of being pulsed as in a fast page mode cycle.

The timing adjustments for $\overline{RAS}$ and for $\overline{CAS}$/$\overline{OE}$/$\overline{WE}$ as described above for a fast page mode read cycle also apply to EDO cycles. Note that if the minimum RAS active time is specified as 3.5 MCLKs, the actual minimum for a single EDO read cycle will be 4.5 MCLKs.

An EDO write cycle is functionally the same as a fast page mode write cycle.

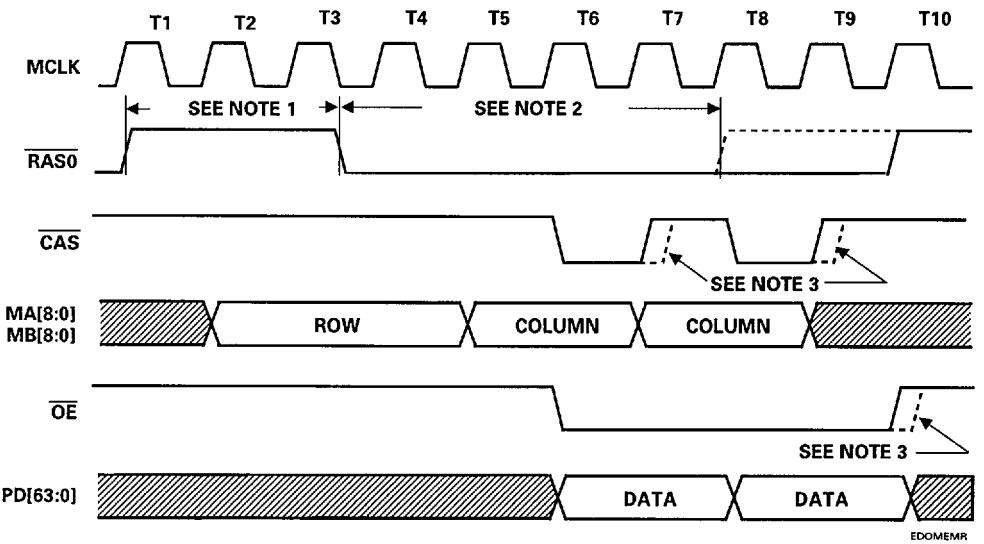


Figure 7-7. EDO Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 4.5 MCLKs via bits 7-6 of CR68.
2. The minimum $\overline{RAS}$ low time for a single column access is 4.5 MCLKs as shown in this figure. This is achieved by specifying 3.5 MCLKs in bits 5-4 of CR68. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This minimum $\overline{RAS}$ active time can be lengthened by 1, 2 or 3 MCLKs via bits 5-4 of CR68.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

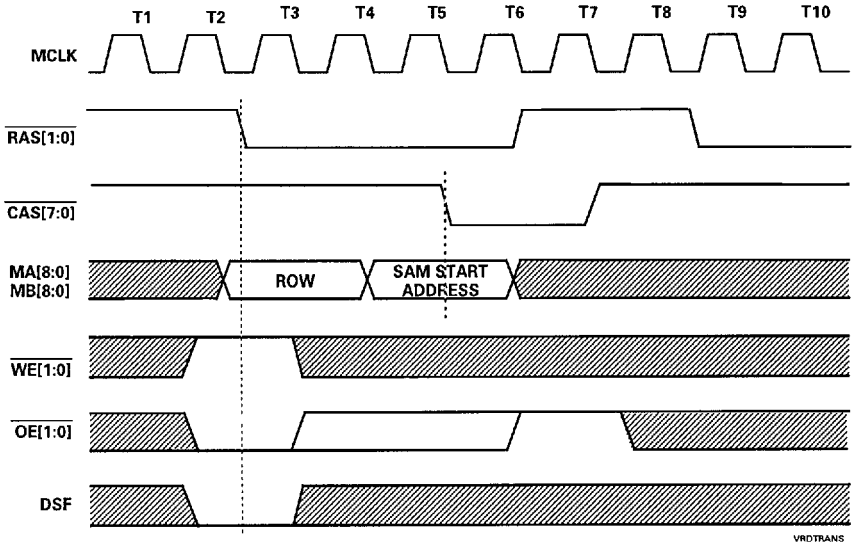


Figure 7-8. Full Read Transfer Cycle Timing

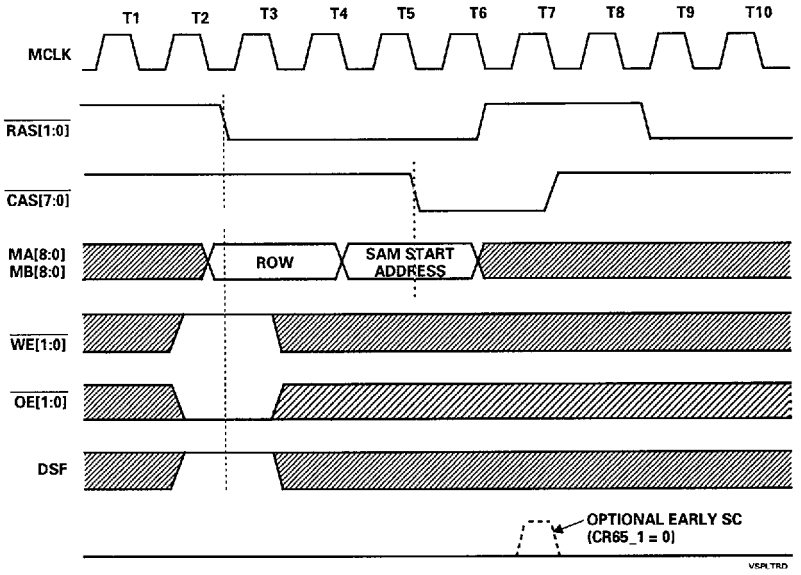


Figure 7-9. Split Read Transfer Cycle Timing

Figure 7-8 shows the functional timing for a read transfer cycle. This cycle is defined by $\overline{CAS}$ and $\overline{WE}$ being high and $\overline{OE}$ and $\overline{DSF}$ being low at the falling edge of RAS. This operation loads the data from one row of the DRAM side of the VRAM into the SAM (serial access memory) register on the serial out side of the VRAM. The address latched on the falling edge of $\overline{RAS}$ specifies the DRAM row to be transferred. The SAM start address (the starting point for serial output) is latched on the falling edge of $\overline{CAS}$. The transfer is complete by the rising edge of $\overline{OE}$.

The amount of data transferred each cycle is a function of the VRAM design. Each VRAM type will specify a SAM size, either 256 or 512. This is the number of "words" per transfer, with the "word" size being equal to the width of the DRAM. For example, a x8 VRAM with a 512 SAM size transfers 512x8 bits per VRAM chip. With 64-bit operation, a total of 4096 bytes are transferred each cycle, assuming serial addressing. This is doubled for parallel addressing. Bit 6 of CR58 specifies the SAM size as either 512 (=0) or 256 (=1). If the designer is unsure of the SAM size to be used, this bit should be set for 256. A setting of 512 can enhance performance if the VRAM can support it.

The Vision964 always performs a full transfer cycle during each horizontal blanking period. CR3B plus bit 6 of CR5D define the horizontal character position where this transfer begins. This specification is enabled by setting bit 4 of CR34 to 1. Split transfers are enabled by default. They can be disabled by setting bit 6 of CR51 to 1, but this is not recommended for any mode.

Figure 7-9 shows the functional timing for a split transfer cycle. The cycle specification is the same as for a full transfer except that DSF is high on the falling edge of $\overline{RAS}$. During a split transfer, only 1/2 the data is transferred from the DRAM to the SAM as would be transferred for a full transfer.

For a split transfer, the SAM is divided into an A half and a B half. Immediately after the full transfer during blanking, the A half of the SAM is replaced (A1 in Figure 7-10). When enough data has been shifted out to reach the midpoint of the A half of the SAM (the small s point in the A1 block of Figure 7-10), the data in the B half (B1 in

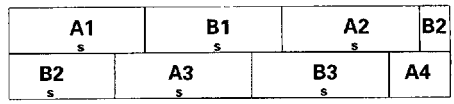


Figure 7-10. Split Transfers

Figure 7-10) of the SAM is replaced concurrently with the shifting out of the rest of the data in the A half. Similarly, when half the data has been shifted out of the B half of the SAM (the small s in the B1 block of Figure 7-10), a split transfer to replace the data in the A half (A2) is initiated. B2 is then filled when the midpoint of A2 is reached.

In this example, the end of the active screen period for the first line is reached when some part of B2 has been shifted out. The Vision964 then performs another full transfer and another split transfer into the A half of the SAM during the horizontal blanking period. When blanking ends, screen refreshing for the next line is continued from the point (in B2) where it was stopped on the previous line. The rest of the line is then refreshed (A3, B3, part of A4) and the full transfer, split transfer sequence is repeated.

A full transfer during the active screen period will cause screen corruption. Split transfers allow even the longest screen lines (which contain more data than can be held in one SAM) to be refreshed without causing this problem.

Certain older VRAMs require an SC pulse between the full and split transfers during blanking. This pulse is indicated in Figure 7-9. The extra SC is provided as a default. This can be disabled via bit 1 of CR65. The first SC pulse for the next line should then be generated just prior to the end of the horizontal period, providing the first pixel for the next line. If this is not the case, SC[1:0] can be delayed by the number of VCLKs specified in bits 6-4 of CR6D. $\overline{BLANK}$ can be delayed by the number of DCLKs specified in bits 2-0 of CR6D. Together, these allow coordination of the relationship between SC and $\overline{BLANK}$ to provide the required pixel setup for the next line.

Figure 7-11 shows the serial out functional timing for a 32-bit parallel (interleaved) SID bus operation. As explained earlier in this section, the configuration in Figure 7-1 can be operated in this

manner. Setting bit 0 of CR65 to 1 delays the falling edge of all SC pulses. This is indicated in Figure 7-11 and produces a reduced risk of contention from two memory banks driving data onto the same SID bus.

Figure 7-12 shows the serial out functional timing for a 64-bit SID serial (non-interleaved) operation. The configuration in Figure 7-1 can be operated in this manner and the configuration in Figure 7-2 must be operated in this manner.

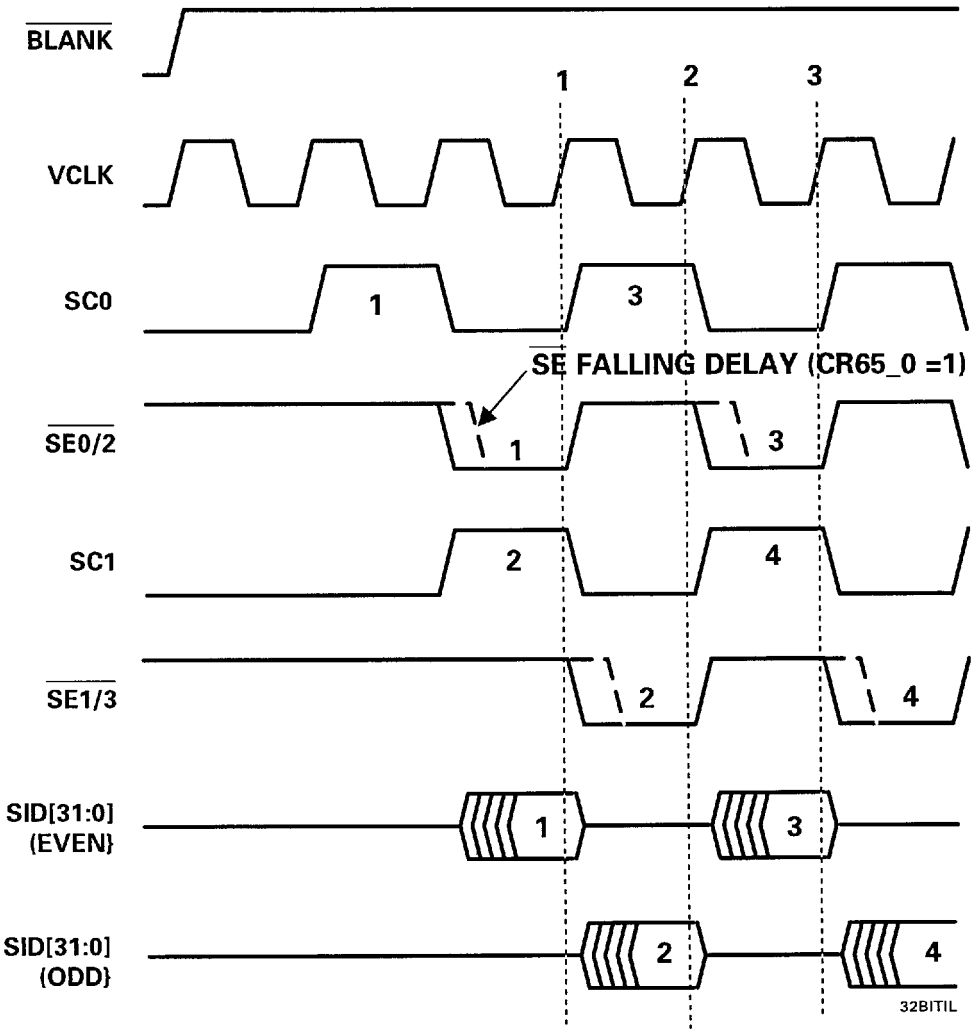


Figure 7-11: 32-bit Parallel Addressing Timing

Figure 7-13 shows the serial out functional timing for a 64-bit parallel (interleaved) SID bus operation. This is equivalent to a 128-bit SID bus. The configuration in Figure 7-3 is operated in this manner.

The frequency requirement for SC, $\overline{SE}$ and VCLK are affected by the number of pixels transferred to the RAMDAC each SC. With a 64-bit SID bus and serial addressing, 64 bits are transferred each SC. This represents 2, 4, 8 or 16 pixels for 32-, 16-, 8- and 4-bits/pixel operation respectively. SC, $\overline{SE}$ and VCLK must then be divided down (from DCLK) by 2, 4, 8 or 16 respectively. The required division is specified via bits 2-0 of CR66. For parallel addressing, which doubles the pixel output rate, SC is further divided by 2. This is done automatically when bits 5-4 of CR66 are set to specify interleaved operation. If these bits specify a 128-bit SID bus, bit 5 of CR53 must also be set to 1 to specify parallel addressing.

If bit 3 of CR66 is set to one, SC0 = VCLK frequency and SC1 = inverted VCLK frequency. This can be used to support a 128-bit RAMDAC.

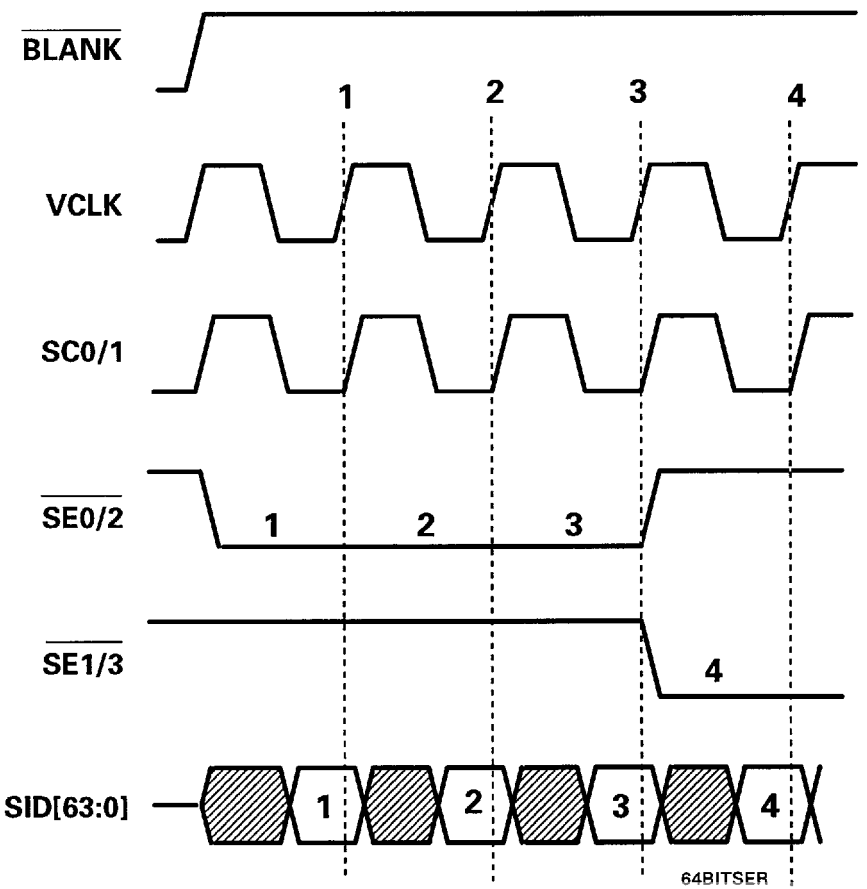


Figure 7-12. 64-bit Serial Addressing Timing

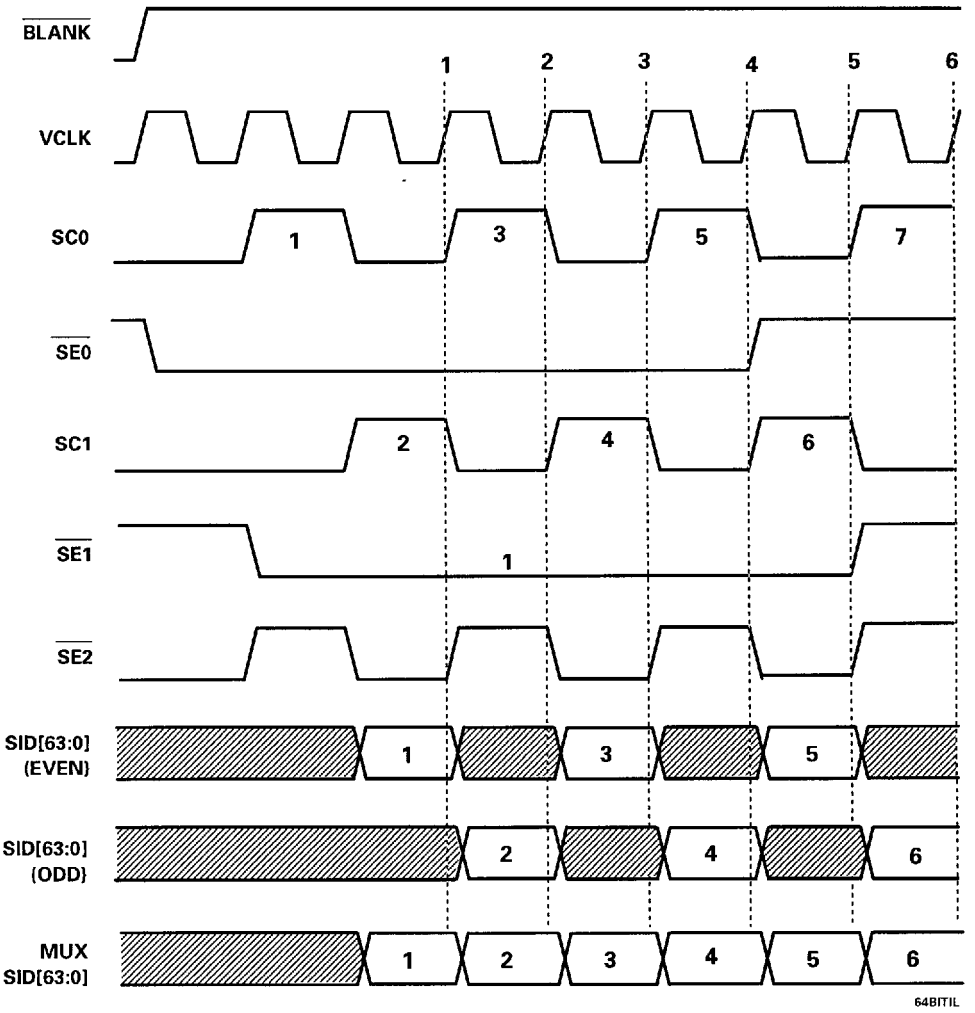


Figure 7-13. 64-bit Parallel Addressing Timing

7.4 DISPLAY MEMORY ACCESS CONTROL

Figure 7-7 shows that a number of processes compete for access to the DRAM side of display memory. These are (in decreasing order of access priority):

- RAM refresh (not explicitly shown)
- Full/split transfers
- Display FIFO writes (VGA modes only)
- CPU accesses
- Graphics Engine accesses

The display FIFO is 32 bits wide by 16 positions deep with 1 MByte of display memory or 64 bits wide by 16 positions deep for 2 or 4 MBytes of display memory. This FIFO provides the display refresh data to the RAMDAC in VGA modes and must never underrun, i.e., output more data than has been input to it from display memory. If an underrun occurs, the display may be corrupted. Note that the Vision964 is normally operated in a mode using the SID VRAM output for display refresh data (bypassing the display FIFO). The following discussion is only relevant for operation in a standard VGA (non-accelerated) mode.

The Vision964 provides a patented technique for maximizing video performance while preventing display FIFO underrun. This involves programming of three parameters. These are the L parameter (bits 2-0 of CR61 and bits 7-0 of CR62), M parameter (bits 7-3 of CR54) and N parameter (bits 7-0 of CR60).

When the Vision964 transfers data from display memory to the FIFO, the N parameter specifies one less than the number of 4-byte (1 MByte of memory) or 8-byte (2 or 4 MBytes of memory) units to write. When N units have been written or the FIFO is filled, whichever comes first, the Vision964 then allows the other display memory processes access to memory. Filling of the FIFO also stops at the end of active display as defined by the L parameter. FIFO filling cannot begin again until the scan line position defined by the Start Display FIFO register (CR3B), which is nor-

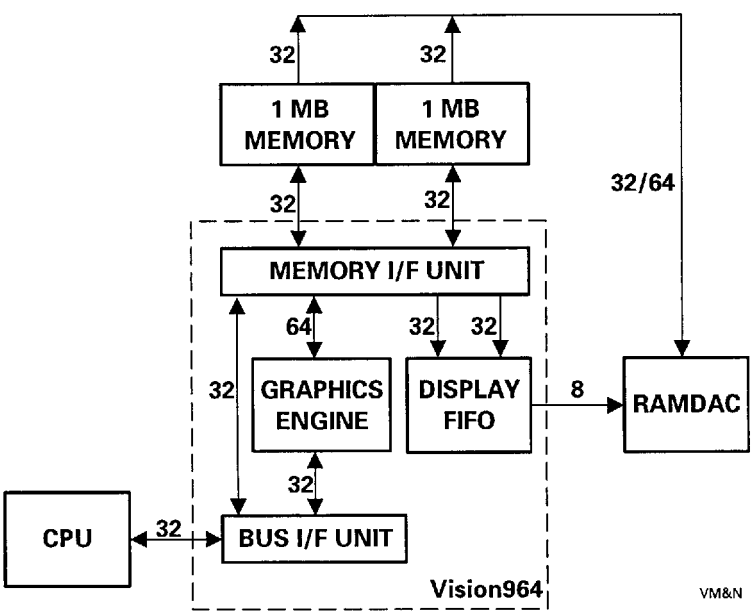


Figure 7-14. Display Memory Access Sources

mally programmed with a value 5 less than the value programmed in CR0 (horizontal total). This provides time during the horizontal blanking period for necessary activities such as RAM refresh and hardware cursor fetch.

The M parameter specifies the number of 8-byte memory access cycles less one that can be performed for reasons other than display FIFO filling. When this number of access cycles has been performed, memory control is returned for FIFO filling. For example, a value of 01010b (10 decimal) specifies that 11 8-byte memory cycles are available to the CPU, Graphics Engine, etc., before FIFO filling restarts. If during the processing period controlled by the M parameter there is time when there are no memory access requests and the M value has not been reached, control is immediately returned to FIFO filling as specified by the N parameter.

M should be maximized for maximum graphics performance. The maximum value of M possible without causing a FIFO underrun is dependent on the pixel data bandwidth required for the particular mode in question. The calculation is based on a FIFO filling bandwidth of 120 (1 MByte) or 240 (2 or 4 MBytes) MBytes/second. The maximum value is also possibly dependent on the N parameter value if the FIFO is not filled each cycle.

The above discussion assumes that the Vision964 has control of the memory bus. The next section describes the implications of allowing a secondary memory controller to take control of the display memory bus.

7.5 SHARED FRAME BUFFER

The Vision964 can share the video frame buffer (display memory) with a secondary controller. This is especially useful for multimedia applications. At all times, the Vision964 serves as the primary display memory controller. As the primary controller, the Vision964 takes responsibility for screen management functions such as RAM refresh cycles and the arbitration of frame buffer requests from a secondary controller.

The Vision964 has two pins that are used for the frame buffer arbitration. These pins implement a Bus REQuest ($\overline{BREQ}$) and Bus GraNT ($\overline{BGNT}$) protocol. $\overline{BREQ}$ is an input to the Vision964 and $\overline{BGNT}$ is an output. When the Vision964 grants the bus to the secondary controller, it also floats its memory control output signals so that the secondary controller has full access to the memory. With full access to memory, the secondary controller can operate at its optimum speed for memory accessing.

The shared frame buffer function is enabled via bit 2 of CR50. The Bus Grant Termination Position register CR5F) and its extension bit (bit 7 of CR5D) must be programmed with a value less than the value programmed in CR0 (horizontal total). Only between the start of a horizontal scan and this value can the Vision964 give up control of the pixel bus. This prevents conflict with Vision964 control functions such as RAM refreshing and VRAM read transfers that occur during the horizontal blanking period.

When operating in a standard VGA mode, the Vision964 will not pre-empt the secondary controller when filling the display FIFO is required for screen refreshing or when RAM refreshing is required. Therefore, the secondary controller must retain control of the bus for a very limited time each time it gains control or it will cause screen corruption. How long the secondary controller can retain control without causing problems in a standard VGA mode is a function of many variables, including the L, M and N parameter settings, the pixel data bandwidth of the RAMDAC and the needs of the CPU and Graphics Engine to access display memory. In general, the secondary controller should retain control for a period less than the time specified by the M parameter. See Section 7.4, Display Memory Access Control for more information on this subject. In non-VGA (Enhanced) modes, screen refresh is handled by the serial output side of the VRAM and can occur simultaneously with a secondary controller in control of the DRAM side of the frame buffer.

For most cases, the Vision964 will be operating in Enhanced mode during shared frame buffer operation. This means that screen refresh data is provided by the SID side of the VRAM and the DRAM bandwidth available to the secondary controller is greatly increased. Normally, the secondary controller can control the bus for most of the active video time.

The timing diagram shown in Figure 7-15 illustrates the arbitration handshake between the Vision964 and the secondary controller. This figure is explained in the following paragraphs.

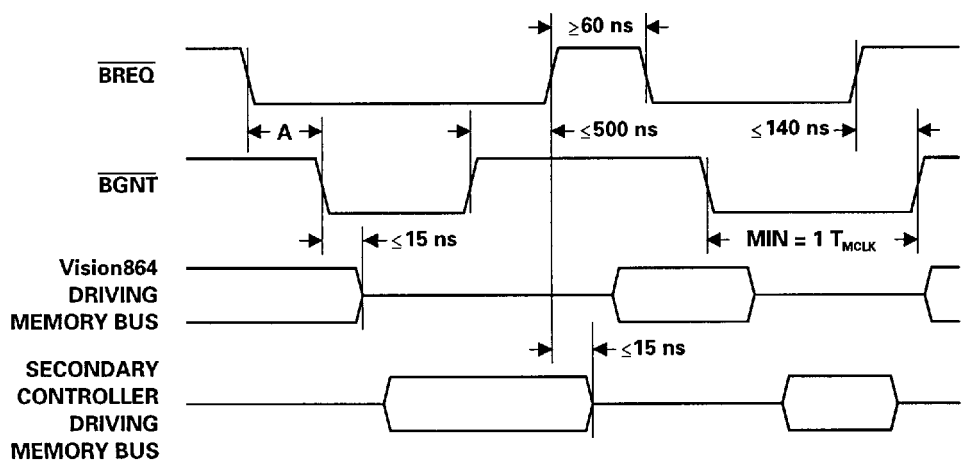
The secondary controller asserts the $\overline{\text{BREQ}}$ signal to the Vision964 to request the bus. This asynchronous input is internally synchronized by the Vision964. If the bus grant termination position value has not been reached and the Vision964 is not performing a memory cycle, the Vision964 grants control of the pixel bus and memory control signals to the secondary controller by asserting $\overline{\text{BGNT}}$ and tri-stating the memory bus signals within 15 ns of this assertion. As indicated by "A" in Figure 7-15, assertion of $\overline{\text{BGNT}}$ after assertion of $\overline{\text{BREQ}}$ occurs within the larger of 1.2 µs or the value of the formula shown in the figure. This formula subtracts the bus grant termination position (CR5F) from the horizontal total (CR0), resulting in some number of character clocks. This is multiplied by 8 to convert to dot clocks and then by the dot clock period to generate a time.

If the bus grant termination position value has been reached, the Vision964 will wait until the start of the next scan line before granting control of the bus. If the Vision964 is performing a memory cycle when the secondary controller requests the bus, it completes that cycle before asserting $\overline{\text{BGNT}}$. If the Vision964 is filling the display FIFO (in standard VGA modes), it will continue to do so until the FIFO is full or the amount of data specified by the N parameter is transferred to the FIFO. In other words, the Vision964 will only grant control of the bus in standard VGA modes during the memory access time controlled by the M parameter.

When control has been granted to the secondary controller, it keeps the $\overline{\text{BREQ}}$ signal active and is then able to perform read and write cycles to the display memory. Return of control to the Vision964 can be initiated by either the Vision964 or the secondary controller.

At the bus grant terminate position or when the Vision964 needs the bus, the Vision964 raises $\overline{\text{BGNT}}$ high. The secondary controller must then raise $\overline{\text{BREQ}}$ high within 500 ns, tri-state its memory bus signals within 15 ns of raising $\overline{\text{BREQ}}$ and give up the bus for at least 60 ns. The secondary controller can then reassert $\overline{\text{BREQ}}$ at any time. Note that the Vision964 can remove its bus grant in as little as one MCLK period.

The secondary controller can give up the bus by raising $\overline{\text{BREQ}}$ and tri-stating its memory bus sig-



A≤ LARGER OF 1.2 µs OR (CR0-CR5F)* 8* T_{DCLK}

Figure 7-15. Shared Frame Buffer Protocol Timing

nals. The Vision964 then raises its $\overline{\text{BGNT}}$ signal within 140 ns and begins to drive the memory bus signals. This sequence is shown in the second bus grant cycle depicted in Figure 7-15.

When the Vision964 regains control of the memory bus in standard VGA modes, it will immediately begin display FIFO filling as specified by the N parameter. The complete FIFO fill cycle will be completed even if the start of filling has been delayed by the secondary controller's control of the bus.

Section 8: Miscellaneous Functions

This section explains how the Vision964 interfaces to the video BIOS ROM, RAMDAC and clock generator. The General I/O Ports and genlocking are also described.

8.1 VIDEO BIOS ROM INTERFACE

The video BIOS ROM contains power-on initialization, mode setup, and video data read/write routines. The video BIOS can be part of the system ROM or it can be implemented separately.

8.1.1 Disabling BIOS ROM Accesses

If the video BIOS is integrated with the system BIOS in a VL-Bus configuration, then power-on strapping bit 4 (CR36, bit 4) must be pulled low to disable BIOS accesses. For PCI configurations, bit 0 of the BIOS ROM Base Address register (Index 30H) is cleared to 0 to disable BIOS accesses.

8.1.2 BIOS ROM Hardware Interface

A separate implementation of the video BIOS for a PCI configuration is shown in Figure 8-1. The implementation for a VL-Bus configuration is

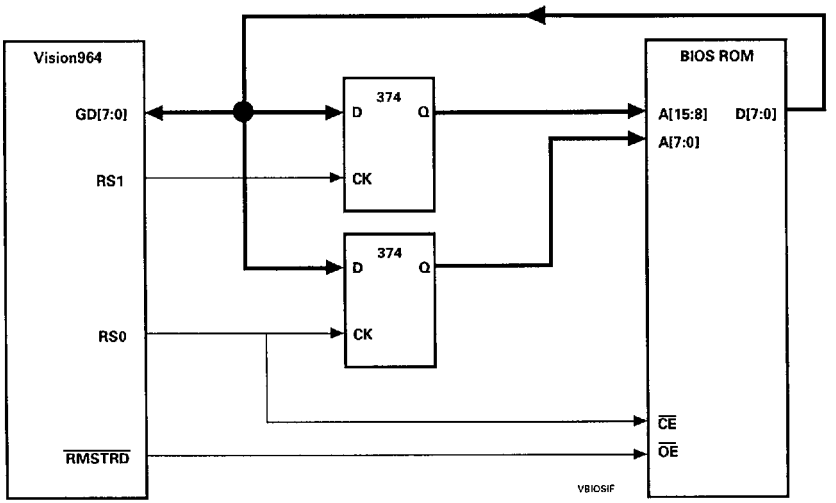


Figure 8-1. BIOS ROM PCI Configuration Interface

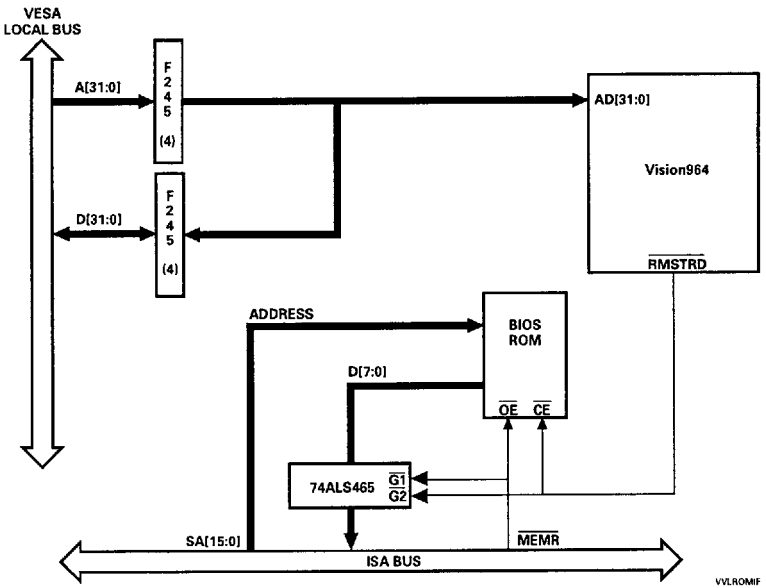


Figure 8-2. BIOS ROM VL-Bus Configuration Interface

shown in Figure 8-2. The ROM is accessed via the ISA bus. This allows a shadowed BIOS to be accessed by a CPU memory read without also generating data directly from the physical ROM. Only 8-bit ROMs are supported.

8.1.3 BIOS ROM Read Functional Timing

Figure 8-3 depicts the PCI configuration functional timing for reading one byte from the ROM. The upper 8 bits of the address are placed on the General Data Bus and are latched into an external register by the rising edge of RS1. The lower 8 bits of the ROM address are then placed on the General Data Bus and latched into a second external register by the rising edge of RS0. RS0 goes low to enable the ROM chip and RMSTRD is asserted to drive the byte of read data to the General Data Bus. The Vision964 latches the data one clock before deassertion of RMSTRD. The transparent latch in the Vision964 then drives this data onto the AD bus.

The Vision964 also supports 16- and 32-bit ROM reads, as defined by the states of the byte enables. For a 16-bit read, the Vision964 automatically increments the lower address once and generates the second byte of read data. For a 32-bit read, the Vision964 automatically increments the lower address three times and generates the remaining three bytes of read data. In both cases, TRDY is delayed until all the required data is available on the AD bus.

For a VL-Bus configuration, a BIOS ROM read is a standard ISA bus read cycle with the Vision964 providing its RMSTRD output as a second buffer enable (see Figure 8-2). RMSTRD is asserted during the time the ROM address is valid and therefore will be active when the chipset asserts the ISA MEMR signal.

8.1.4 BIOS ROM Address Mapping

The Vision964 maps the CPU memory address spaces for the video BIOS ROM into physical

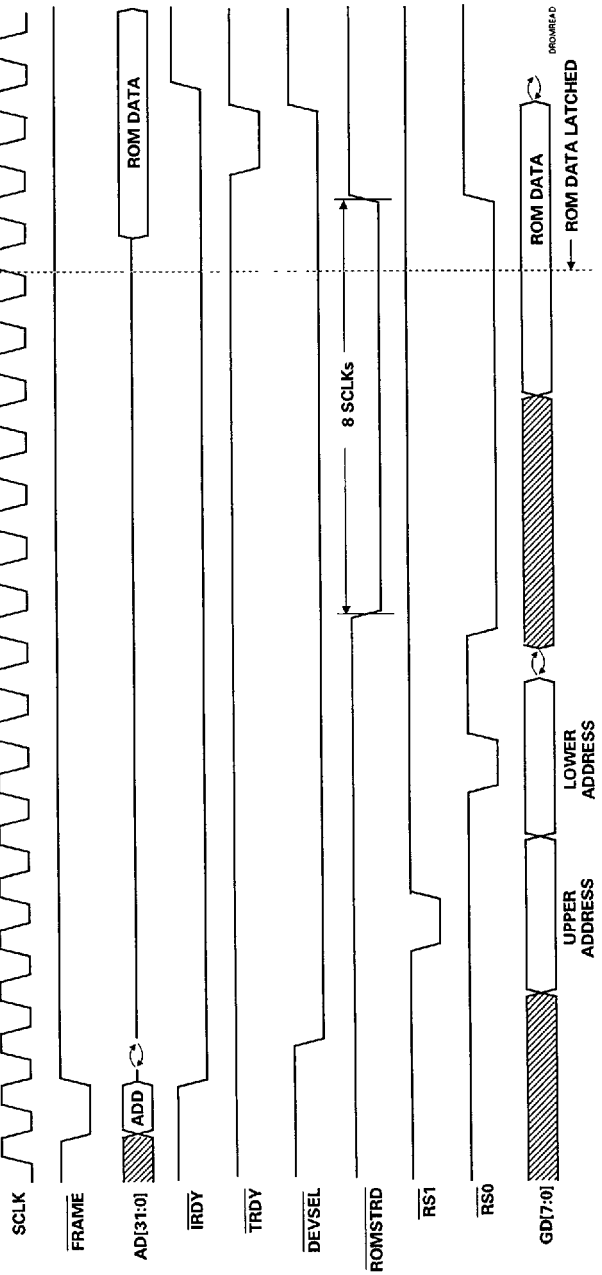


Figure 8-3. BIOS ROM Read Functional Timing - PCI

ROM addresses. If implemented separately for a VL-Bus system, the video BIOS normally uses the standard address range C0000H–C7FFFH (32 KBytes). If power-on strapping bit 10 (CR37, bit 2) is strapped low or if bit 2 of CR37 is cleared to 0 in a VL-Bus system, the video BIOS address range becomes C0000H-CFFFFH (64 KBytes). PCI systems support a relocatable 64-KByte video BIOS address range via the BIOS ROM Base Address configuration register (Index 30H).

8.2 RAMDAC/DISPLAY INTERFACE

The Vision964 decodes all CPU accesses to the RAMDAC registers. It has an 8-bit pixel address bus for standard VGA operation and supports both 32- and 64-bit SID RAMDACs.

8.2.1 RAMDAC Hardware Interface

The Vision964 provides all required control signals. The hardware interface is shown in Figure 8-4. The various serial data interfaces with the VRAM and the register bits controlling their operation are described in Section 7.

8.2.2 PA Bus Tri-State

Some SID RAMDACs multiplex the VGA and SID ports. Setting bit 6 of CR66 to 1 tri-states the PA[7:0] outputs to allow serial input to these pins on the RAMDAC.

8.2.3 RAMDAC Functional Timing

Figure 8-5 depicts the functional timing for RAMDAC internal register accesses. Read data is latched by the Vision964 on the rising edge of $\overline{\text{DACRD}}$ and appears immediately after that on the proper byte lane of AD[31:0].

8.2.4 VCLK Control

Figure 8.6 shows how various register bits and internal logic elements affect the DCLK input in

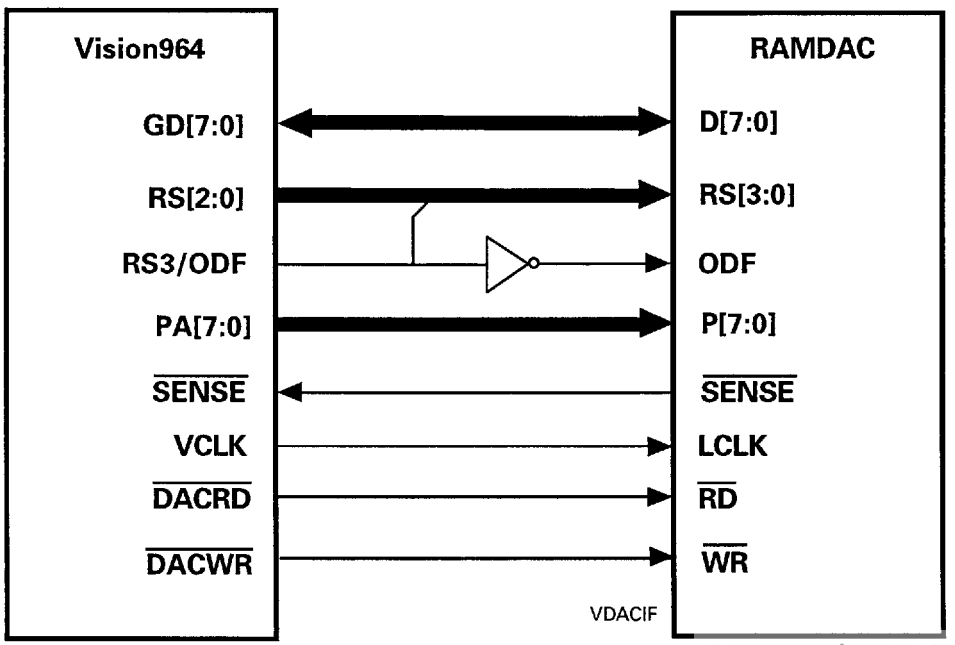


Figure 8-4. RAMDAC Interface

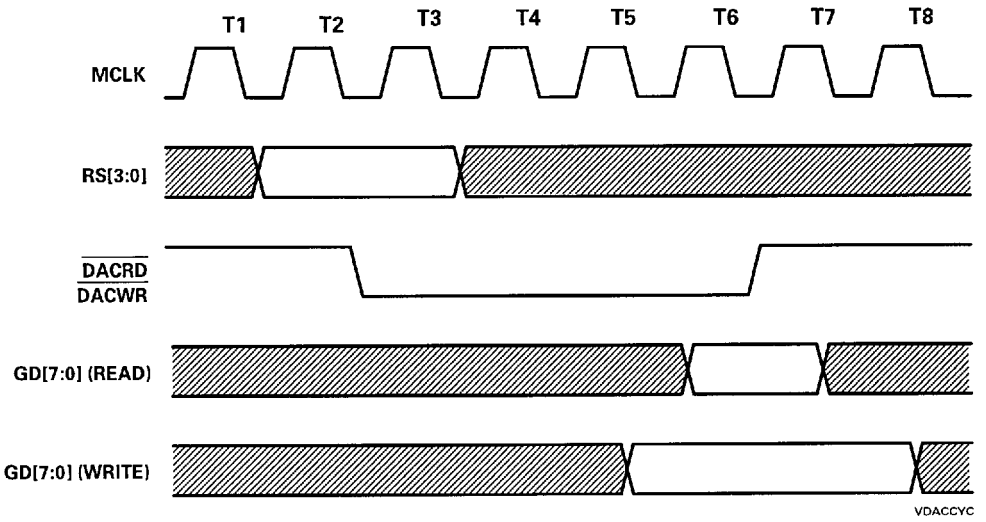


Figure 8-5. RAMDAC Access Functional Timing

the process of generating the VCLK output. In general:

1. CR67, bit 0, either leaves DCLK unchanged or inverts it. Since it is always inverted later (after CR33), this means that inverting it here results in a VCLK with the same phase as DCLK.
2. SR1, bit 3, is used for VGA modes. It selects between DCLK and DCLK/2. Its output is called the internal dot clock.
3. CR33, bit 0, selects the internal dot clock or bypasses it.
4. CR66, bits 2-0, divide the clock by 1, 2, 4, 8, 16 or 32. This is used with serial addressing to adjust for the varying number of pixels shifted out each SC depending on the color depth. For example, at 32 bits/pixel, two pixels are shifted each SC, so SC, $\overline{SE}$ and VCLK must be divided by 2.

8.2.5 Generating Register Select Signals

The Vision964 has four RAMDAC register select outputs. The RS[1:0] signals are generated by accesses to standard VGA RAMDAC register addresses according to the following table.

Table 8-1 RS[1:0] Generation

Address	RS[1:0]
3C8H	00
3C9H	01
3C6H	10
3C7H	11

The RS2 output is controlled by the state of bit 0 of CR55. This should be programmed to the desired value before the RAMDAC register is accessed to generate RS[1:0]. In older software, bit

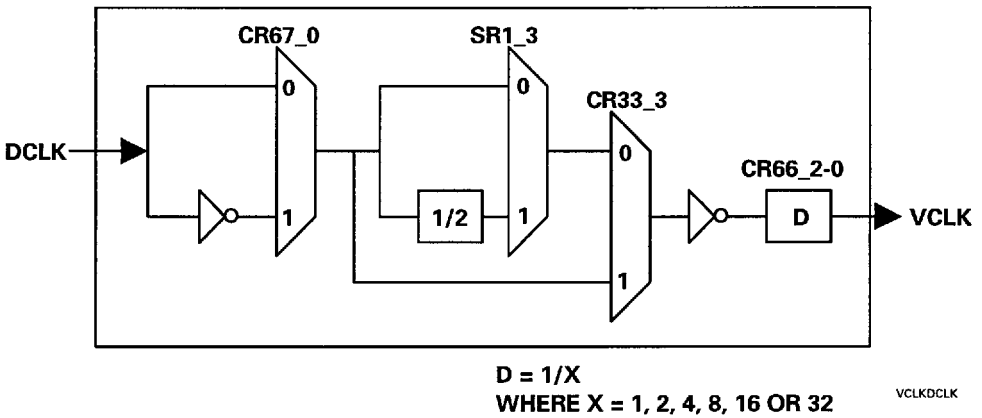


Figure 8-6. VCLK Selection

2 of CR43 is used to generate RS2. This function is retained for backward compatibility. RS3 is multiplexed with the ODF signal. The RS3 function is selected by clearing bit 5 of CR45 to 0. The RS3 output is controlled by the state of bit 1 of CR55. This should be programmed to the desired value before the RAMDAC register is accessed to generate RS[1:0].

8.2.6 Green PC Support

The Vision964 provides support for the VESA Display Power Management Signaling (DPMS) protocol by allowing independent control of the HSYNC and VSYNC signals. To use this capability, the bit pattern xxxx0110b must be written to the SR8 register to unlock access to the SRD register. Bits 5-4 of SRD then control the state of HSYNC and bits 7-6 of SRD control the state of VSYNC.

8.2.7 $\overline{\text{SENSE}}$ Input Utilization

The $\overline{\text{SENSE}}$ output of the RAMDAC is used by the S3 BIOS to detect the existence and type of monitor connected to the system. The BIOS sequentially drives the three analog outputs (red, green, blue) and determines whether or not the $\overline{\text{SENSE}}$ signal is driven active. If no monitor is present, $\overline{\text{SENSE}}$ will never go active. If a monochrome monitor is present, $\overline{\text{SENSE}}$ will go active only when the green output is driven. If a color monitor is present, $\overline{\text{SENSE}}$ will go active when each of the outputs is driven. DOS uses special palette colors when in monochrome mode. No S3 enhanced mode drivers use monochrome palettes.

8.2.8 RAMDAC Write Snooping (VL-Bus)

If power-on strapping bit 12 (CR37, bit 4) is pulled low at reset for a VL-Bus configuration, $\overline{\text{LOCA}}$ and $\overline{\text{SRDY}}$ are not generated by the Vision964 for RAMDAC write accesses. The Vision964 generates write cycles to the local RAMDAC and the ISA controller also generates cycles to an off-board RAMDAC (mirroring). RAMDAC reads are always from the local RAMDAC.

8.2.9 Disabling RAMDAC Register Access (PCI)

For PCI bus configurations, setting bit 5 of the Command configuration space register (Index 04H) to 1 disables Vision964 response to

RAMDAC register accesses. This is used when a second video card is present and its RAMDAC registers require updating.

8.3 CLOCK GENERATOR INTERFACE

The Vision964 receives its memory clock (MCLK) and dot clock (DCLK) inputs from an external clock generator. The allowable values of SCLK and DCLK are interdependent, as defined in the clock waveform timing table of the AC Specifications. System designers must consider these interdependencies when choosing a clock generator, especially if the SCLK frequency is to be varied.

8.3.1 Clock Generator Hardware Interface

Figure 8-7 shows one type of hardware interface to the clock generator. Four clock select signals are provided, which allow selection of up to 16 DCLK frequencies. If the clock generator allows selection of more than one MCLK frequency, this can be implemented by using the General Output port capability described in Section 8.4.

8.3.2 Clock Generator Access Functional Timing

The Vision964 drives the DCLK select signals onto the GD[3:0] lines, which in turn connect to the clock select pins on the clock chip. The clock chip then latches these signals on the falling edge of STWR. The functional timing for this is the same as for the General Output Port as shown in Figure 8-9.

Some clock chips use a serial programming technique to select a DCLK or MCLK frequency or program a register. In this case, the clock and serial data bits are transferred by repeated writes to bits 1-0 of CR42.

STWR is asserted and then deasserted when the Mode Control register (CR42) bits 3-0, the Miscellaneous Output register (3C2H) bits 3-2 or the General Output Port register (CR5C) bits 7-4 are written to.

8.3.3 DCLK Selection

The values of the bits written to CR42 or 3C2H determine the value automatically written to the General Output Port register (CR5C) bits 3-0 and

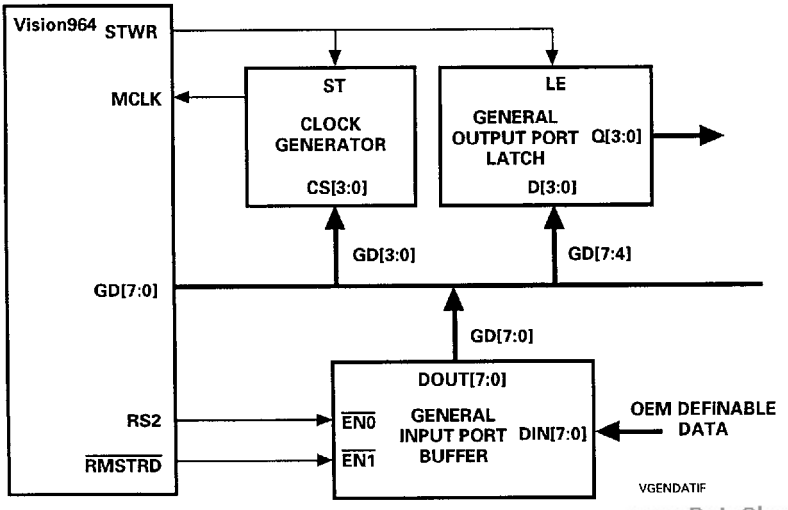


Figure 8-7. General Data Bus Interfaces

then driven onto the GD[3:0] lines to be latched by STWR. This is shown in Table 8-2.

Table 8-2. DCLK Select Values

3C2H, Bits 3-2	GD[3:0]
00	0000
01	0001
10	0010
11	CR42, Bits 3-0

The coding for these signals is dependent upon the clock generator capabilities.

8.4 GENERAL INPUT PORT

The Vision964 provides an 8-bit General Input Port (GIP). The block diagram showing how this is implemented is shown in Figure 8-7.

Bit 2 of the Extended DAC Control register (CR55) is set to 1 to enable the GIP read function. The data is read from an external buffer by an I/O read of port 3C8H (the same as the DAC Write Index off-chip register). When RS2 is low and $\overline{\text{RMSTRD}}$ is asserted, this data is driven to the Vision964 via GD[7:0] and transparently latched by the rising edge of MCLK preceding deassertion of $\overline{\text{RMSTRD}}$. The data then appear almost immediately on AD[7:0]. The functional timing for this operation is shown in Figure 8-8.

Bits 7-5 of the GIP are input to the Vision964 via GD[7:5] during power-on reset and latched into bits 6-4 of 42E8H. One potential use of this capability is to input monitor ID information as provided by certain monitors.

8.5 GENERAL OUTPUT PORT

The Vision964 provides a 4-bit General Output Port (GOP). The block diagram showing how this is implemented is shown in Figure 8-7.

The General Output Port register (CR5C) bits 7-4 can be set to any value by a CPU write. The programmed values appear on GD[7:4] and are latched into the GOP external latch when STWR goes low. STWR is asserted and then deasserted when the Mode Control register (CR42) bits 3-0, the Miscellaneous Output register (3C2H) bits 3-2 or the General Output Port register (CR5C) bits 7-4 are written to. One use of the GOP is to provide programmable control of external logic.

The functional timing for the GOP is shown in Figure 8-9.

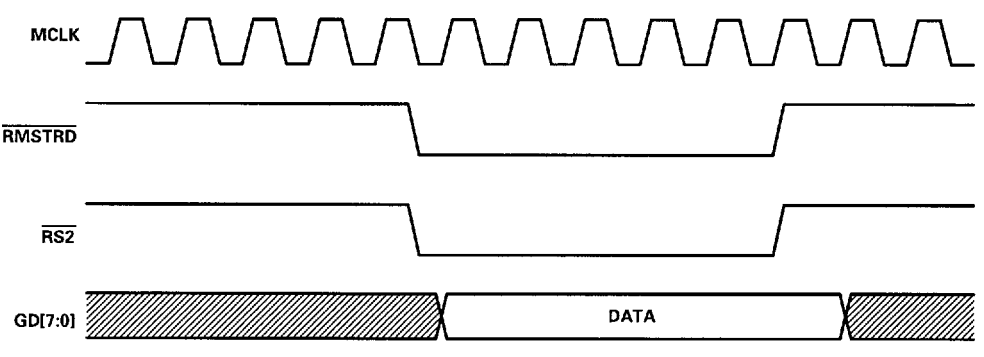


Figure 8-8. General Input Port Functional Timing

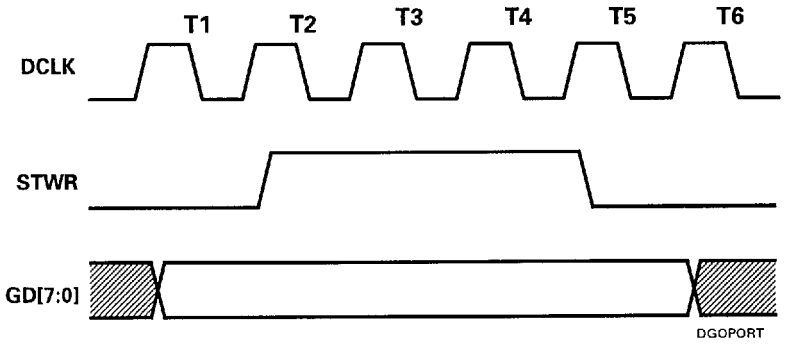


Figure 8-9. General Output Port Functional Timing

8.6 GENLOCKING

Genlocking allows two different video sources (one or both being an S3 accelerator) to contribute to the construction of a single frame of pixel data. The VSYNC output of a master video source is input to the slave video source to provide the basis for genlocking. This process ensures that each screen refresh cycle (frame) begins at exactly the same physical location on the screen.

The total time for each horizontal scan (screen active, blanking, retrace and front and back porches) is called the Horizontal Total. It is programmed in character clocks (minus 5) in the CR0 register. The internal horizontal character counter counts up from 0 (the first pixel on the line) until it reaches the Horizontal Total. It then resets to 0, signaling the start of a new line. HSYNC is typically deasserted several character clocks before the horizontal counter resets to 0. This is indicated by the Δ1 gap in Figure 8-10. Similarly, VSYNC is typically deasserted (ending the vertical retrace) some number of scan lines before the vertical counter resets to 0. This is the Δ2 depicted in Figure 8-10. Both the horizontal and vertical counters reset to 0 (times A and C in Figure 8-10) after VSYNC is deasserted (time B in Figure 8-10).

The total adjustment is indicated by the vector in Figure 8-11. The horizontal component of this vector (Δ1) is programmed into bits 7-4 of CR63 (high nibble) and bits 7-4 of CR57 (low nibble). The programmed value is the number of character clocks from deassertion of HSYNC to the horizontal counter reset (both for the master). This programmed value should never exceed the horizontal total programmed in CR0.

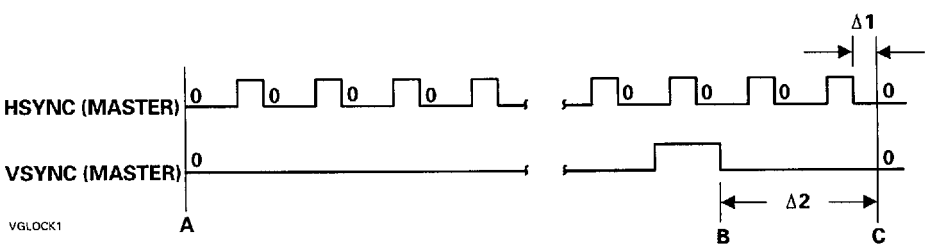


Figure 8-10. Genlocking Master Sync Timing

Bits 6-4 of CR64 allow fine turning of the horizontal adjustment in VCLK units instead of character clock (8 or 9 VCLK) units. This is required for signals such as those used for television. Bit 7 of CR64 must be set to 1 to enable this function.

The vertical component of this vector (Δ2) is programmed into bits 3-0 of CR63 (high nibble) and bits 3-0 of CR57 (low nibble). The programmed value is the number of scan lines from the deassertion of VSYNC to the vertical counter reset.

Note that this adjustment does not affect any of the CRT control timings other than to shift them in time. In other words, the lengths of the blanking period, HSYNC and VSYNC pulses, etc., do not change; their occurrences are all delayed by a fixed amount.

The result of these adjustments is that both video sources use the same starting point as a reference for pixel data written to the frame buffer. As long as both use the same VCLK frequency and have the same CRT control parameters (H and V Total, etc.), pixels contributed by either source should appear in the proper places on the screen. One additional problem is that the character clocks of the master and slave will probably not be exactly in phase after the horizontal and vertical counter reset adjustment. To rectify this, bits 6-4 of the CR64 register are programmed with a value equal to the number of VCLKs (dot clocks) the character clock of the slave must be delayed from the rising edge of the master's VSYNC rising edge to bring the character clocks in phase. Bit 7 of this register must be set to 1 to enable this function.

In general, genlocking programming should be performed during the vertical sync period to avoid screen jitter.

See the *Genlocking* Tech Note for several implementation examples, including one describing how to genlock to a television-style (NTSC, PAL) external source.

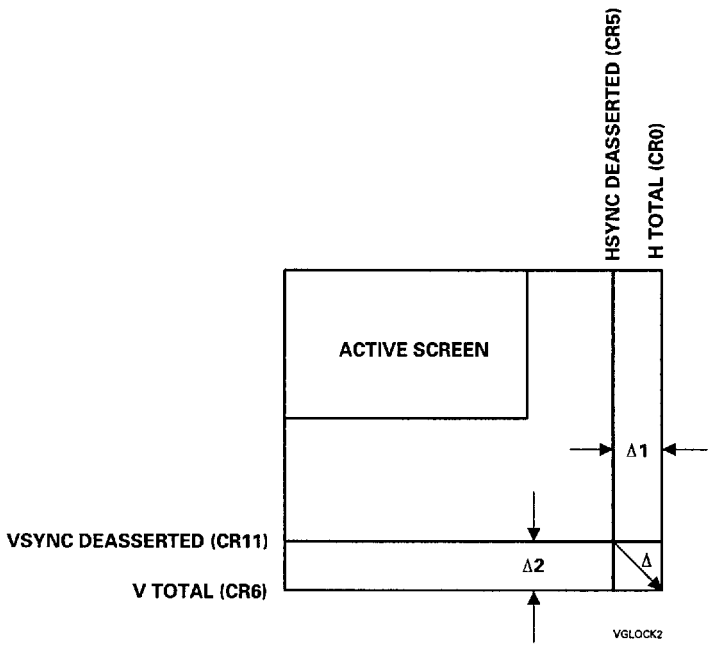


Figure 8-11. Genlocking Timing Adjustments

Section 9: Software Setup

This section describes the basic operations required to set up the Vision964.

9.1 CHIP WAKEUP

The following program wakes up the Vision964.

```
;Program runs as COM file
;Program enables S3 chips
code    segment
        assume   CS:code, DS:code
        ORG      100h
start:
        mov dx,46E8h        ; Video Subsystem Enable register address
        mov al,10h          ; bit 3 = 0, disable I/O and memory decoders
                            ; bit 4 = 1; place video subsystem in setup mode
        out dx,al           ; write new bit values to 46E8H
        mov dx,102h         ; Setup Option Select register address
        mov al,01h          ; Video subsystem responds to commands,
                            ; addresses& data
        out dx,al           ; Write new bit value to 102H

        mov dx,46E8h        ; Video Subsystem Enable register address
        mov al,08h          ; Bit 3 = 1, enable I/O and memory decoders
                            ; Bit 4 = 0, return to operational mode
        out dx,al           ; Write new bit values to 46E8H
        mov dx,4AE8h        ;
        xor al,al           ; Enable standard VGA functions and screen size
        out dx,al           ; Write new bit values to 4AE8h
        mov dx, 3C2h        ;
        mov al, 23h         ; Enable memory, color base, page 0,
                            ; clock @ 28.322 MHz
        out dx, al          ; Write new bit values to 3C2h
        mov ah,4Ch
        int 21h             ; return to DOS
code    ENDS
        END  start
```

9.2 REGISTER ACCESS

9.2.1 Unlocking the S3 Registers

The S3 registers (CR30 and higher plus the Enhanced Commands registers) must be unlocked before they can be accessed by the CPU. The code to do this is:

```
; Write code to CR38 to provide access to the S3 VGA registers (CR30-CR3F)
;
   mov dx,3d4h        ; copy index register address into dx
   mov al,38h         ; copy index for CR38 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   mov al,48h         ; copy unlocking code (01xx10xxb, x=don't care) to al
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
;
; Write code to CR39 to provide access to the System Control and System Extension
; registers (CR40-CRFF)
;
; dx is already loaded with 3D4h because of the previous instruction
;
   mov al,39h         ; copy index for CR39 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   mov al,0a5h        ; copy unlocking code to al (the code a5H also unlocks
                      ; access to configuration registers CR36, CR37 and CR68
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
;
; Set bit 0 in CR40 to enable access to the Enhanced Commands registers.
;
; dx is already loaded with 3D4h because of previous instruction
   mov al,40h         ; copy index for CR40 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   in al,dx           ; read register data for read/modify/write operation
   or al,1            ; set bit 0 to 1
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
```

9.2.2 Locking the S3 Registers

Relocking the S3 registers is done by repeating the code used to unlock the registers except:

1. The values written to the CR38 and CR39 registers must change at least one of the significant bits in the valid code pattern. For example, 00h will always accomplish this.

2. After first verifying that the Graphics Engine is not busy (bit 9 of 9AE8H is 0), bit 0 of CR40 must be cleared to 0. A read-modify-write cycle must be used instead of the code used above to prevent overwriting of any changes made to bits [7:1] in CR40 since reset.

```
mov dx,3d4h        ; copy index register address into dx
mov al,40h         ; copy index for CR40 register into al
out dx,al          ; write index to index register
inc dx             ; increment dx to 3D5h (data register address)
in al,dx           ; read content of CR40 into al
and al,0feh        ; clear bit 0 to 0
out dx,al          ; write to CR40 to lock the Enhanced Commands registers
dec dx             ; restore the index register address to dx
```

9.2.3 Unlocking/Locking Other Registers

The Extended Sequencer register (SRD) has been added to the standard VGA sequencer register set to provide display power management (Green PC) control. To gain access to this register, write xxxx0110b (x = don't care) to SR8. Writing a bit pattern that changes one of the significant bits re-locks access to the SRD register.

In addition to the standard VGA register access controls, the Vision964 provides a number of bits extending the control of access to these registers. These are listed in Table 9-1.

Table 9-1. VGA Register Access Control Extensions

Register Bit	Controls Access To:
CR33, bit 1	CR7, bits 1 and 6 (1 = disable write protect setting of CR11, bit 7)
CR33, bit 4	RAMDAC register (1 = disable writes)
CR33, bit 6	Palette/Overscan registers (1 = lock)
CR34, bit 5	SR1, bit 5 (1 = lock)
CR34, bit 7	3C2H, bits 3-2 (1 = lock)
CR35, bit 4	Vertical Timing registers (1 = lock)
CR35, bit 5	Horizontal Timing registers (1 = lock)

9.3 TESTING FOR THE PRESENCE OF A Vision964 CHIP

After unlocking, a code identifying the Vision964 and its revision level can be read via CR30. The following code aborts the driver program and returns to DOS if a Vision964 chip is not found.

```
    mov dx,3d4h         ; copy index register address into dx
    mov al,30h          ; copy index for CR30 register into al
    out dx,al           ; write index to index register
    inc dx              ; increment dx to 3D5h (data register address)
    in al,dx            ; read content of CR30 into al
    and al,0f0h         ; mask out revision status (lower nibble)
    cmp al,0d0h         ; compare chip ID to the desired chip ID (D0h for Vision964)
    jne not_D0x         ; jump to a label if chip ID does not match desired ID
    .
    .
    .
not_D0x:
    mov ax,4c00h        ; terminate with a return code of zero
    int 21h             ; return to DOS
```

9.4 GRAPHICS MODE SETUP

The Vision964 provides a number of standard VGA, VESA Super VGA and S3 Enhanced graphics modes. The particular modes supported depend on the RAMDAC used and can vary. See the *S3 Video BIOS and Utilities OEM Guide* for a complete listing of the RAMDACs and modes supported by the S3 BIOS for the Vision964.

9.4.1 Backward Compatibility Modes Setup

The Vision964 is hardware compatible with CGA, MDA, and Hercules Graphics Card (HGC) standards which are based on the Motorola 6845 CRT controller. These standards are designed to run on TTL (digital) monitors, however, the Vision964 uses analog displays for all modes. To emulate the 6845, the following additional setup is required before relinquishing control to 6845-based applications.

1. Character Generator Locking. The VGA BIOS reloads the character generator each time an alphanumeric mode is set whereas non-VGA modes (CGA, MDA, and Hercules) do not. Therefore the character table must be loaded onto plane 2 when the controller is still in the VGA mode.

2. Video DAC color compatibility. Non-VGA modes use 6-bit video output. Therefore, only the first 64 video DAC addresses need to be programmed and locked. Locking is done using bit 4 of the Backward Compatibility 2 register (CR33).

3. Program default parameters. The Vision964 should be programmed for a 640 × 200 or 320 × 200 programming table for CGA, whereas MDA uses a 350-line programming table (Mode 7).

4. Set the S3 Registers for 6845 emulation by setting bit 3 of the Backward Compatibility 1 register (CR32) to 1 to select non-VGA operation. Force high rate horizontal timing, then lock horizontal and vertical timing. These and other backward compatibility setup capabilities are provided by the Backward Compatibility 1 (CR32), Backward Compatibility 2 (CR33) and Backward Compatibility 3 (CR34) registers.

At this point the Vision964 is hardware compatible with and can be programmed as a 6845. The program values will be inappropriate for VGA, but internal translation converts them to an equivalent value for analog monitors.

9.4.2 VGA Mode Setup

The Vision964 powers up into a standard VGA mode determined by the BIOS. The mode can then be altered by programming the standard VGA registers. All standard VGA and VESA modes are supported.

For each mode, the CRTC timing must be appropriately specified. Table 9-2 shows the required parameters, the relevant register bits for each and the value to be programmed for each. These parameters must also be programmed for the Enhanced modes discussed in the next section.

Table 9-2. CRTC Timing Specification Summary

Parameter	Register Bits	Value to be Programmed
Horizontal Total	CR5D_0, CR0_7-0	Character clocks per horizontal period (HSYNC active to next HSYNC active) - 5
Horizontal Display End	CR5D_1, CR1_7-0	Character clocks of active display - 1
Start Horizontal Blank	CR5D_2, CR2_7-0	Character clock counter value at which horizontal blanking begins
End Horizontal Blank	CR5_7, CR3_4-0	Least significant six bits of the character clock counter value at which horizontal blanking ends. The $\overline{\text{BLANK}}$ pulse width can be extended by 64 DCLKs via bit 3 CR5D.
Start Horizontal Sync	CR5D_4, CR4_7-0	Character clock counter value at which HSYNC becomes active
End Horizontal Sync	CR5_4-0	Least significant five bits of the character clock counter value at which HSYNC goes inactive. The HSYNC pulse width can be extended by 32 DCLKs via bit 5 of CR5D.
Vertical Total	CR5E_0, CR7_5, CR7_0, CR6_7-0	Number of scan lines from VSYNC active to next VSYNC active - 2
Vertical Retrace Start	CR5E_4, CR7_7, CR7_2, CR10_7-0	Number of scan lines at which VSYNC becomes active
Vertical Retrace End	CR12_3-0	Least significant 4 bits of the scan line counter value at which VSYNC goes inactive
Vertical Display End	CR5E_1, CR7_6, CR7_1, CR12_7-0	Scan lines of active display -1
Offset	CR51_5-4, CR13_7-0	This value multiplied by 2 (byte mode), 4 (word mode) or 8 (doubleword mode) specifies the difference between the starting byte addresses of two consecutive scan lines.
Start Vertical Blank	CR5E_2, CR9_5, CR7_3, CR15_7-0	Number of scan lines at which vertical blanking begins - 1
End Vertical Blank	CR16_7-0	Least significant eight bits of the scan line counter at which vertical blanking ends
Line Compare	CR5E_6, CR9_6, CR7_4, CR18_7-0	Number of scan lines at which the screen is split into screen A and screen B

See standard VGA and VESA-compliant documentation for the other setup steps.

9.4.3 S3 Enhanced Mode Setup

The Enhanced Graphics Command register group is unlocked by setting bit 0 of the System Configuration register (CR40) to 1. After that, bit 0 of 4AE8H must be set to 1 to enable Enhanced mode functions. Bit 2 of 4AE8H is also programmed at this time for the desired mode as explained in Table 9-3. A screen refresh rate is selected. The CRTC timing registers are programmed as explained in the previous section. The Enhanced mode setup bits are then programmed. Table 9-4 shows register bit values for a particular mode for the bitmap specification bits described in Table 9-3. This assumes a 32-bit RAMDAC with parallel (interleaved) SID operation. Some modes may require programming of bits not mentioned in this example.

Table 9-3. Register Bits Affecting the Bitmap Definition

Register Bits	Description
CR13	Specifies the logical screen width (pitch). Bits 5-4 of CR51 are extension bits 9-8 for this value.
CR31_1	This is set to 1 to enable a 2Kx1Kx4 map for 1024x768 or 800x600 resolutions, or a 2Kx512x8 map for 640x480 resolution.
CR31_3	This bit must be set to 1 to enable Enhanced mode memory mapping. This forces operation in doubleword mode.
CR3A_4	0 = 4-bit modes 1 = 8/16/24/32-bit modes
CR42_5	0 = Non-interlaced operation 1 = Interlaced operation
CR50_0,7,6	Screen Width Definition 000 = 1024 (or 2048 if bit 1 of CR31 =1) (Default) 001 = 640 010 = 800 (or 1600x1200x4 if bit 2 of 4AE8H = 1) 011 = 1280 100 = 1152 101 = Reserved 110 = 1600 111 = Reserved
CR50_5-4	Pixel Color Depth Definition 00 = 1 byte. Bit 2 of 4AE8H selects between 4 (=0) and 8 (=1) bits/pixel. 01 = 2 bytes (16 bits/pixel) 10 = Reserved 11 = 4 bytes (32 bits/pixel). True color (24 bits/pixel) is handled by this setting, with the upper byte unused.
4AE8H_2	If bits 0,7,6 of CR50 are 010b, this bit is set to 1 for 1600x1200x4 mode. If bits 5,4 of CR50 are 00b, this bit is set to 1 for 4 bits/pixel modes.

Table 9-4. Enhanced Mode Setup for 1024x768x8 Resolution at 75 Hz Refresh

Register	Value (Hex)	Description
CR31	09	Enables use of a CPU base address offset. Enables use of Enhanced mode memory mappings.
CR34	10	Enables CR3B (VRAM data transfer position).
CR3A	15	Enables RAM refresh count specification and specifies 1 RAM refresh cycle per horizontal line. Configures attribute controller shift registers for 8 bits/pixel.
CR3B	9D	Specifies the time from the start of display active until the start of data transfer from the DRAM side of the VRAM to the SAM side.
CR3C	00	Not used for this non-interlaced mode.
CR40	See Description	Bit 0 must be set to 1 early in the setup process to enable Enhanced mode register access. Bits 7-4 select 0 or 1 wait state and latching of write data on $\overline{SRDY}$ or $\overline{RDYIN}$. These bits default to 1 wait state and latching on $\overline{RDYIN}$, which will almost always be required for proper VL-Bus operation of the Vision964. Consequently, the S3 BIOS protects these bits from being overwritten during the normal setup process.
CR42	See Description	Bits 3-0 specify the DCLK rate selection output to the clock generator. 80 MHz is required for this mode, but the actual value programmed will depend on the clock generator.
CR50	00	Bits 0,7,6 specify the screen width of 1024 pixels. Bits 5,4 specify a pixel length of 8 bits/pixel.
CR51	00	Split transfers are enabled (default)
CR53	00	Setting bit 5 enables parallel addressing and divides the SC frequency by 2 when a 128-bit SID bus is being used. This is not required for this mode of operation.
CR5C	See Description	The General Output Port is not used during the setup of this mode unless the clock generator requires serial input for DCLK selection or frequency programming.
CR65	00	No address adjustments are required for split transfers for this mode (bits 7-6).
CR66	12	Bits 2-0 specify that SC, $\overline{SE}$ and VCLK are divided down to 1/4 the DCLK rate. This is because each SAM transfer involves 4 pixels. Bits 5-4 specify a 32-bit SID bus with parallel (interleaved) operation. This invokes parallel addressing and divides the SC frequency by an additional factor of 2.
CR67	00	VCLK is inverted with respect to DCLK.
CR6D	01	Delays $\overline{BLANK}$ by 1 DCLK to meet a design-related timing requirement

9.4.4 Memory Mapping of Enhanced Mode Registers

For improved performance, the Enhanced mode registers can be memory-mapped (MMIO). This function is enabled by setting bit 4 of CR53 or bit 5 of 4AE8H to 1. Image writes normally made by accessing I/O addresses E2E8H and E2EAH (the Pixel Data Transfer registers) are made instead by accessing any memory location in the 32-KByte address space from A0000H to A7FFFH. Accesses to the Enhanced command registers (write only) are made to particular locations in the A8000H to AFFFFH address range as shown in Table 9-5. The only exception is the Read Register Select register (BEE8H, Index 0FH), which cannot be accessed as a memory-mapped register.

Table 9-5. Memory-Mapped I/O Addresses for Enhanced Mode Registers

I/O Address	Memory Address
8xE8H	A8xE8H
9xE8H	A9xE8H
AxE8H	AAxE8H
BxE8H	ABxE8H

9.4.5 Hardware Graphics Cursor Setup

Use of the 64x64 bits hardware graphics cursor is enabled by setting bit 0 of the Hardware Graphics Cursor Mode register (CR45) to 1. The hardware cursor only works in Enhanced mode (bit 1 of 4AE8H = 1). See the Programmable Hardware Cursor section of the Enhanced Mode Programming section for more information.

Section 10: VGA/Backward Compatibility Support

This section describes the Vision964's support for standard VGA, VESA Super VGA and older graphics standards.

10.1 VGA COMPATIBILITY

The Vision964 is compatible with the VGA standard. These modes are not accelerated using the Graphics Engine. However, other design features including a multi-modal FIFO provide excellent VGA performance.

Several of the standard VGA registers have been modified or extended in the Vision964. Table 10-1 describes these changes.

Table 10-1. Standard VGA Registers Modified or Extended in the Vision964

Register	Change to Standard VGA Definition
3C2H (Write)	VCLK selection via bits 3-2 has been modified as follows: 00 = 25.175 MHz (standard) 01 = 28.322 MHz (standard) 10 = Reserved 11 = VCLK frequency is selected by bits 3-0 of CR42 Access to these bits can be controlled via bit 7 of CR34.
3C2H (Read)	Reading this bit reports the state of the $\overline{\text{SENSE}}$/$\overline{\text{BREQ}}$ input to the Vision964.
3C4H	The sequencer address has been extended from 3 to 4 bits to support the new SR8 and SRD registers.
SR1	Access to bit 0 of this register is controlled by bit 5 of CR34. Bits 1-0 of CR32 allow selection of 7 and 9 dot characters in addition to the 8/9 dot section provided by bit 0 of this register.
SR8	This new register unlocks/locks access to the new SRD register.
SRD	This new register provides the HSYNC and VSYNC controls required for VESA DPMS (Display Power Management) support.
CR0	Extension bit 8 is bit 0 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR1	Extension bit 8 is bit 1 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.

CR2	Extension bit 8 is bit 2 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR3	The length of the blanking pulse defined in this register can be extended by 64 DCLKs via bit 3 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR4	Extension bit 8 is bit 4 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR5	The length of the HSYNC pulse defined in this register can be extended by 32 DCLKs via bit 5 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR6	In addition to the standard VGA extensions (bit 8 is bit 0 of CR7, bit 9 is bit 5 of CR47), bit 10 is bit 0 of CR5E. Bit 4 of CR35 controls access to this register.
CR7	Bit 4 of CR35 controls access to bits 0, 2, 3, 5 and 7 of this register.
CR9	Bit 4 of CR35 controls access to bit 5 of this register.
CRC	The display start address is a 20-bit value for the Vision964. The extension bits (20-16) are bits 4-0 of CR69.
CRE	The cursor location address is a 20-bit value for the Vision964. The extension bits (20-16) are bits 4-0 of CR69. When using a 4/8 bits/pixel color depth in Enhanced mode and an 8-bit RAMDAC, this register contains the hardware cursor foreground color.
CRF	When using a 4/8 bits/pixel color depth in Enhanced mode and an 8-bit RAMDAC, this register contains the hardware cursor background color.
CR10	In addition to the standard VGA extensions (bit 8 is bit 2 of CR7, bit 9 is bit 7 of CR7), bit 10 is bit 4 of CR5E. Bit 4 of CR35 controls access to this register.
CR11	Bit 4 of CR35 controls access to bits 3-0 of this register. Bit 6 (3/5 refresh cycles per line) can be overridden by CR3A_2-0. The actions of bits 4 and 5 on vertical interrupts are controlled by the setting of bit 4 of CR32 or the setting of bit 8 of 42E8H. Setting bit 1 of CR33 to 1 disables the write protect effect of bit 7 of this register on bits 1 and 6 of CR7.
CR12	In addition to the standard VGA extensions (bit 8 is bit 1 of CR7, bit 9 is bit 6 of CR7), bit 10 is bit 1 of CR5E.
CR13	Bit 2 of CR43 is the old extension bit (bit 8) of this register. Bits 5-4 of CR51 are the new extension bits (bits 9-8) of this register.
CR15	In addition to the standard VGA extensions (bit 8 is bit 3 of CR7, bit 9 is bit 5 of CR9), bit 10 is bit 2 of CR5E. Bit 4 of CR35 controls access to this register.
CR16	Bit 4 of CR35 controls access to this register.
CR17	Bit 5 of CR35 controls access to bit 2 of this register.
CR18	In addition to the standard VGA extensions (bit 8 is bit 4 of CR7, bit 9 is bit 6 of CR9), bit 10 is bit 6 of CR5E.
AR00-AR0F	Bit 6 of CR33 controls access to these registers.
46E8H	If bit 2 of CR65 is set to 1, the setup address is 3C3H instead of this address.
3C6H-3C9H	Bit 4 of CR33 controls writes to these registers.

For a detailed discussion of VGA programming, see *Programming Guide to the EGA and VGA Cards, Second Edition* by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc.).

10.2 VESA SUPER VGA SUPPORT

The Vision964 supports the extended (Super) VGA modes defined by VESA. All modes can be accelerated by the Vision964's graphics Engine except for the planar (4 bits/pixel) ones.

10.3 BACKWARD COMPATIBILITY SUPPORT

The Vision964 supports CGA, MDA and HGC-compatible modes. None of these modes can be accelerated.

Section 11: Enhanced Mode Programming

Enhanced mode provides a level of performance far beyond what is possible with the VGA architecture. Hardware line drawing, BitBlt, rectangle fill, and image transfers between CPU memory and display memory are implemented. Also implemented are data manipulation functions, such as data extension, data source selection, and read/write bitplane control. Hardware clipping is supported by 4 registers that define a rectangular clipping area. While in enhanced mode, the display memory bit map can be updated in two ways. One is to have the CPU write directly to memory. (This is also possible in non-Enhanced modes via paging.) The other is to have the CPU issue commands to the Graphics Engine, which then controls pixel updating. This section explains these two methods and provides a comprehensive set of Enhanced mode programming examples.

11.1 DIRECT BITMAP ACCESSING—LINEAR ADDRESSING

Linear addressing is useful when software requires direct access to display memory. In general, large image transfers to display memory can be performed faster using the Graphics Engine and memory-mapped I/O transfers. Linear addressing should not be enabled concurrently with memory-mapped I/O, which is described in the Software Setup section.

Enhanced mode operation must be enabled before linear addressing is enabled. This means that bit 0 of 4AE8H is set to 1 to enable Enhanced mode functions and bit 3 of CR31 is set to 1 to specify Enhanced mode memory mapping.

The Vision964 provides linear addressing of up to 8 MBytes of display memory. Linear addressing of more than 64 KBytes requires that the CPU be operated in 386 protected mode.

The Graphics Engine busy flag, bit 9 of 9AE8H, should be verified to be 0 (not busy) before linear addressing is enabled by setting bit 4 of CR58 or bit 4 of 4AE8H to 1. The size of the linear address window is set via bits 1-0 of CR58. The base address for the linear addressing window is set via CR59 and CR5A (or via the Base Address 0 (Index 10H) PCI configuration register for PCI systems).

The linear addressing window size can be set to 64 KBytes. The base address for the window is set by programming bits 31-16 of the window position in CR59-CR5A. This allows the CPU to be operated in real mode. If bit 0 of CR31 is set to 1, the memory page offset (64K bank) specified in bits 5-0 of CR6A is added to the linear addressing window position base address, allowing access to up to 8 MBytes of display memory through a 64-KByte window.

11.2 BITMAP ACCESS THROUGH THE GRAPHICS ENGINE

When updating the display bitmap through the Graphics Engine, all CPU data moves through the Pixel Data Transfer registers (E2E8H and E2EAH). These registers can be memory mapped as explained in Memory Mapping of Enhanced Mode Registers in the Software Setup section.

The Graphics Engine manipulates the bits for each pixel to assign a color index or true color value, which is then translated via a programmable RAMDAC before being displayed on a CRT. Selected bits in a pixel can be masked off from being displayed by programming the DAC Mask register (3C6H). The Vision964 can manipulate 64 bits each clock cycle, from two 32-bit pixels to eight 8-bit pixels.

Figure 11-1 is a flowchart for the process of updating the color of each pixel. Start at the block labeled 'New Color' in the middle of Figure 11-1. At this stage, a color has been determined that may or may not be used to update a pixel in the bitmap. How this color is determined will be covered later.

The first hurdle for the new color is the color compare process. If this is turned off (bit 8 of BEE8H, Index 0EH = 0), the new color is passed to the Write Mask register (AAE8H). If the plane to which the pixel update is directed has been masked off in this register, no update occurs. Otherwise, the new color value is written to the bitmap.

If color compare is enabled (bit 8 of BEE8H, Index 0EH = 1), the new color value (source) is compared to a color value programmed into the Color Compare (B2E8H) register. The sense of the color comparison is determined by the SRC NE (source not equal) bit (bit 7) of BEE8H, Index 0EH. If this bit is 0, the new pixel color value is passed to the write mask only when the source color does not match the color in the Color Compare register. If this bit is 1, the new pixel color value is passed to the write mask only when the source color matches the color in the Color Compare register. If the new pixel color value is not passed to the write mask, no update occurs. Notice that the source color is used for the comparison, as opposed to the destination (bitmap) color used by the standard VGA color compare operation.

The new color is the result of a logical mix performed on a color source and the current color in the bitmap. For example, the color source could be XORed with the bitmap color. The new color can also be selected by operating on only the color source or the bitmap color, e.g., NOT color source. Both the color source and the logical mix operation are specified in either the Background Mix register (B6E8H) or the Foreground Mix register (BAE8H). Which of these two registers is used is determined by the settings of bits [7:6] of the Pixel Control register (BEE8H, Index 0AH).

To set up the pixel color updating scheme, the programmer specifies one of four color sources by writing bits 6-5 of the Background Mix and Foreground Mix registers. The color sources are:

- Background Color register (A2E8H)
- Foreground Color register (A6E8H)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Current display bitmap color index

One of 16 logical operations is chosen by writing bits 3-0 of the Background Mix and Foreground Mix registers. Examples of logical operations are making the new pixel color index equal to the NOT of the current bitmap color index or making the new index equal to the XOR of the source and current bitmap indices.

When the logical operation and color source have been specified in the Background and Foreground Mix registers, bits 7-6 of the Pixel Control register are written to specify the source of the mask bit

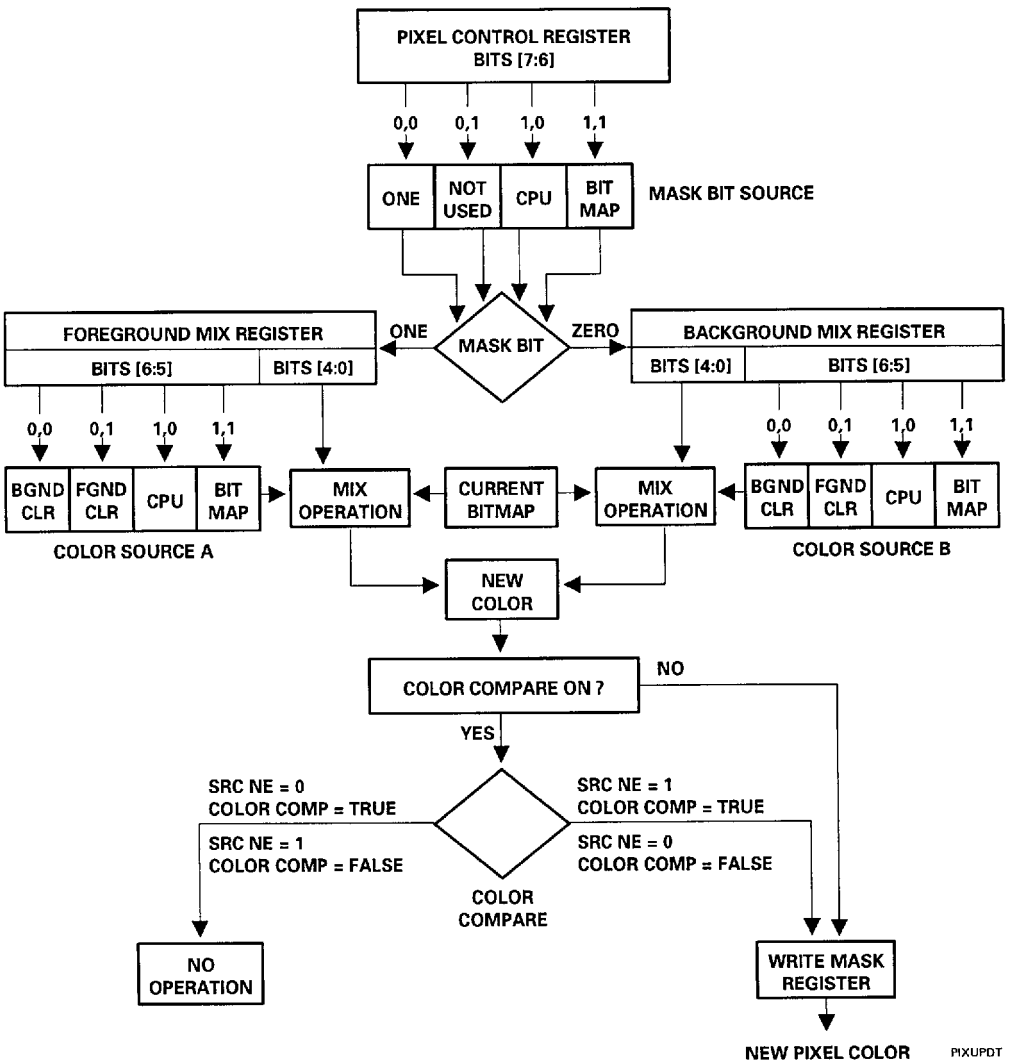


Figure 11-1. Pixel Update Flowchart

value. If the resulting mask bit is a 'ONE', the Foreground Mix register is used to determine the color source and mix. If the mask bit is a 'ZERO', the Background Mix register is used to determine the color source and mix. There are three sources for the mask bit value:

- Always ONE (Foreground Mix register used)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Bitmap

Setting bits 7-6 to 00b sets the mask bit to 'ONE'. All drawing updates to the video bitmap use the Foreground Mix register settings. This setup is used to draw solid lines, through-the-plane image transfers to display memory and BitBLTs.

If bits 7-6 are set to 10b, the mask bit source is the CPU. After the draw operation command is issued to the Drawing Command register (9AE8), a mask bit corresponding to every pixel drawn on the display must be provided via the Pixel Data Transfer register(s). If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the CPU, the mask bit source cannot also be the CPU, and vice versa. This setup is used to transfer monochrome images such as fonts and icons to the screen.

If bits 7-6 are set to 11b, the current display bit map is selected as the mask bit source. The Read Mask register (AAE8H) is set up to indicate the active planes. When all bits of the read-enabled planes for a pixel are a 1, the mask bit 'ONE' is generated. If any one of the read-enabled planes is a 0, then a mask bit 'ZERO' is generated. If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the bitmap, the mask bit source cannot also be the bitmap, and vice versa. This setting is used to BitBLT patterns and character images.

11.3 PROGRAMMING

This section provides programming examples of Enhanced mode features provided by the Vision964.

11.3.1 Notational Conventions

The REGMNEMONIC on the left hand side of the arrow is the register mnemonic of the I/O port being written into. Text following a ';' is a comment.

```
REGMNEMONIC ⇐ XXXXH                ; Load a hexadecimal value into the register.
REGMNEMONIC ⇐ XXXXD                ; Load a decimal value into the register.
REGMNEMONIC ⇐ XXXX                 ; Load a decimal value into the register
REGMNEMONIC ⇐ XXXXXXXXXXXXXXXXB   ; Load a binary value into the register.
```

The programming examples often contain the following step:

wait for FIFO X empty

where X is some number between 1 and 13. This number equals the number of commands to follow that may need to be stored in the command FIFO before execution. The number of empty command FIFO entries is determined by reading the FIFO-STATUS bits of the Graphics Processor Status register (9AE8H, Read). See the register description for the interpretation of these bits.

11.3.2 Initial Setup

All examples assume the desired mode is selected. The RAMDAC must also be set up appropriately.

The Bitmap Access Through the Graphics Engine section earlier in this section explains in detail how the colors, mixes and the data extensions are set for each example. These registers need not be set repeatedly before a series of draw commands if they use the same colors, mixes and data extension.

All bitmap updates are affected by the settings in the clipping registers (BEE8H, Indices 1-4) and the choice of internal or external clipping (BEE8H, Index E, bit 5). These must be set up so they include the area being drawn into.

If color compare is to be used, it must be enabled by setting bit 8 of BEE8H, Index 0EH to 1. Bit 7 of this register determines whether a TRUE or FALSE comparison allows the pixel update to continue. The comparison color is programmed into the Color Compare register (B2E8).

All planes are enabled for writing unless explicitly set otherwise in an example. This is done via the Write Mask register (AAE8H).

11.3.3 Programming Examples

This section provides programming examples for the following Enhanced mode drawing operations:

- Solid Line
- Textured Line
- Rectangle
- Image Transfer—Through the Plane
- Image Transfer—Across the Plane
- BitBLT—Through the Plane
- BitBLT—Across the Plane
- Pattern Fill—Through the Plane
- Pattern Fill—Across the Plane
- Short Stroke Vectors

In addition, an example of the programming of the hardware cursor is provided.

A number of programming steps are repeated in multiple examples. They are explained in detail at their first occurrence. Therefore, readers are encouraged to work through the examples from first to last.

The register mnemonics used in the examples are listed in Table 11-1.

Table 11-1 Mnemonics Used in the Programming Examples

Mnemonic	Register
BKGD_COLOR	Background Color (A2E8)
BKGD_MIX	Background Mix (B6E8H)
CMD	Drawing Command (9AE8H)
CUR_X	Current X Position (86E8H)
CUR_Y	Current Y Position (82E8H)
DESTY_AXSTP	Destination Y-Position/Axial Step Constant (8AE8H)
DESTY_DIASTP	Destination X-Position/Diagonal Step Constant (8EE8H)
ERR_TERM	Error Term (92E8H)
FRGD_COLOR	Foreground Color (A6E8H)
FRGD_MIX	Foreground Mix (BAE8H)
MAJ_AXIS_PCNT	Major Axis Pixel Count (96E8H)
MIN_AXIS_PCNT	Minor Axis Pixel Count (BEE8H)
PIXEL_CNTL	Pixel Control (BEE8H)
PIX_TRANS	Pixel Data Transfer (E2E8H) - Also E2EAH for 32-bit transfers.
RD_MASK	Bitplane Read Mask (AEE8H)
SHORT_STROKE	Short Stroke Vector Transfer (9EE8H)
WRT_MASK	Bitplane Write Mask (AAE8H)

Mnemonic	Description
NEW	Mix = 00111b in bits 4-0 of BAE8H or B6E8H. This overwrites the present bitmap color value with a new value.
XOR	Mix = 00101b in bits 4-0 of BAE8H or B6E8H. The current bitmap color is XORed with the new color.

11.3.3.1 Solid Line

Draw a solid line using axial coordinates from x1,y1 to x2,y2 using the mix NEW and color index 2.

Setup:

Drawing a line using axial coordinates requires programming the axial step constant into the Destination Y-Position/Axial Step Constant (8AE8H) register (DESTY_AXSTP), the diagonal step constant into the Destination X-Position/Diagonal Step Constant (8EE8H) register (DESTX_DIASTP) and the error term into the Error Term (92E8H) register (ERR_TERM). Calculation of these three constants is based on the MAX and MIN parameters as calculated below.

MAX = maximum(ABS(x2–x1), ABS(y2–y1))
MIN = minimum(ABS(x2–x1), ABS(y2–y1))

where maximum means choose the largest of the two terms in parentheses and minimum means choose the smallest. ABS means take the absolute value of the expression.

Bits 7-5 of the Drawing Command (9AE8H) register (CMD) specify the drawing direction. Setting bit 7 to 1 means that the Y drawing direction is positive (y1 < y2). Clearing bit 7 to 0 means the Y drawing direction is negative (y1 > y2). Setting bit 6 to 1 means that Y is the major (longer) axis (ABS(x2–x1) > ABS(y2–y1)). Clearing bit 6 to 0 means that X is the major axis. Setting bit 5 to 1 means that the X drawing direction is positive (x1 < x2). Clearing bit 5 to 0 means that the X drawing direction is negative (x1 > x2). These values replace the DDD sequence in the write to the CMD register shown in the pseudocode below.

The mix NEW represents a setting of 0111b in bits 3-0 of the Foreground Mix (BAE8H) register (FRGD_MIX). This overwrites the present bitmap color value with a new value.

The remainder of the setup is:

```
Wait For FIFO 3 empty                ; Three commands to follow
FRGD_MIX ⇐ 0027H                     ; color source is FRGD_COLOR, mix type is NEW
FRGD_COLOR ⇐ 00000002H               ; color index
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX provides color source and mix type
```

Drawing Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ MAX - 1              ; length in pixels of the major axis - 1
DESTX_DIASTP ⇐ 2 * (MIX–MAX)         ; diagonal step constant
DESTY_AXSTP ⇐ 2 * MIN                ; axial step constant
If the X drawing direction is positive then
    ERR_TERM ⇐ 2 * MIN – MAX         ; error term
else if the X drawing direction is negative
    ERR_TERM ⇐ 2 * MIN – MAX – 1     ; error term
CMD ⇐ 00100000DDD10011b              ; Draw line command (bits 15-13), Draw (as opposed to
                                     ; just move current position)(bit 4), draw multiple pixels (bit 1),
                                     ; write (bit 0).
```

11.3.3.2 Textured Line

Draw a textured line from x1,y1 to x2,y2 using the mix NEW for the foreground mix, XOR for the background mix, foreground color index 2 and background color index 4. The 32-bit line texture/pattern (PATTERN) is 00110000111100110011000011110011b. When the pattern bit is a 1, the pixel is written with the foreground color and mix. When the bit is a 0, the pixel is written with the background color and mix.

Setup:

The XOR mix corresponds to a setting of 0101b in bits 3-0 of the Background Mix (B6E8H) register (BKGD_MIX). See the Solid Line example for an explanation of other parameters and registers used in this example.

```
Wait For FIFO 5 empty                ; 5 commands to follow
FRGD_MIX ⇐ 0027H                     ; color source is FRGD_COLOR, NEW mix type
FRGD_COLOR ⇐ 00000002H               ; color index
BKGD_MIX ⇐ 0005H                     ; color source BKGD_COLOR, XOR mix type
BKGD_COLOR ⇐ 00000004H               ; color index
PIXEL_CNTL ⇐ A080H                   ; mask data selecting mix register is provided by the CPU
```

Drawing Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ MAX - 1              ; length in pixels of major axis - 1
DESTX_DIASTP ⇐ 2 * (MIX–MAX)         ; diagonal step constant
DESTY_AXSTP ⇐ 2 * MIN                ; axial step constant
If the X drawing direction is positive then
    ERR_TERM ⇐ 2 * MIN – MAX         ; error term
else if the X drawing direction is negative
    ERR_TERM ⇐ 2 * MIN – MAX – 1     ; error term
CMD ⇐ 00100101DDD10011b              ; Draw line (bits 15-13), 32-bit bus (bits 10-9), wait for data from
                                     ; the Pixel Data Transfer register (bit 8), Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0),

COUNT (of PATTERN dwords) = (MAX + 31)/32 (See Note)
PIX_TRANS ⇐ 00110000111100110011000011110011b    ; Output PATTERN to Pixel Data Transfer
                                                 ; registers COUNT times
```

Note

The COUNT of the number of writes required by the CPU is a function of the number of bits to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)). The number of bits transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy bits to meet this requirement. For example, if the transfer width is 8 bits and nine bits are to be transferred for the line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (MAX+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a MAX = 11 transfer requires (11+7)/8 = 2 1/4 = 2 bytes. The formulas for all transfer widths are given below.

8-bit transfers: COUNT = (MAX+7)/8 bytes
16-bit transfers: COUNT = (MAX+15)/16 words
32-bit transfers: COUNT = (MAX+31)/32 dwords

11.3.3.3 Rectangle

Draw a rectangle with its top left corner at x1,y1, height = HEIGHT and width = WIDTH. Use the mix NEW and color index 2. The drawing direction (bits 7-5 in the write to the CMD register below) is set to X positive, X major and Y positive (101b).

Setup:

```
Wait For FIFO 3 empty                ; 3 commands to follow
FRGD_MIX ⇐ 0027H                     ; color source is FRGD_COLOR, NEW mix type
FRGD_COLOR ⇐ 00000002H               ; color index
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX specifies the color source and mix type
```

Draw Operation:

```
Wait For FIFO 5 empty                ; 5 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 0100000010110011b              ; Draw rectangle (bits 15-13), Draw (bit 4), Multi-pixel (bit 1),
                                     ; Write (bit 0)
```

Note

The rectangle can be defined by specifying any one of the four corners and setting bits 7-5 accordingly. Always select X as the major axis (bit 6 =0). No matter how the rectangle is defined, it always fills from left to right and top to bottom.

Corner	X direction (bit 5)	Y direction (bit 7)
top left	positive (1)	positive (1)
top right	negative (0)	positive (1)
bottom left	positive (1)	negative (0)
bottom right	negative (0)	negative (0)

11.3.3.4 Image Transfer—Through the Plane

A rectangular image is transferred from the CPU to the display memory through the plane. The image is stored as an array of pixels arranged in row major fashion. This example uses a mix type of NEW and x1,y1 is the top left corner of the rectangle on the display. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 6 empty                ; 6 commands to follow
FRGD_MIX ⇐ 0047H                     ; color source is the CPU, mix type is NEW
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX is the source for color source and mix type
```

Drawing Operation:

```
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
Wait for Graphics Engine not busy    ; loop till bit 9 of 9AE8H register is 0
CMD ⇐ 01010101D0110001b              ; Draw rectangle (bits 15-13), Swap ON (bit 12),
                                     ; 32-bit transfers (bits 10-9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Write (bit 0)
```

COUNT (of image pixel data to transfer) = (See Note)
PIX_TRANS ⇐ IMAGEDATA; Output image data to the Pixel Data Transfer registers for COUNT dwords.

Note

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred, the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)) and the color depth (bits/pixel). The number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, at 4 bits/pixel, each byte holds two pixels. If the transfer width is one byte and three pixels are to be transferred per line, two bytes must be written per line, with the upper nibble of the second byte a dummy pixel. If the transfer width is 16 bits, from one to three dummy pixels may be required to make the number of pixels per line an even multiple of 16. The number of word writes required per line can be determined from the formula n = (W+3)/4, with n being truncated to an integer if the result contains a fraction. Thus a six pixel transfer requires (6+3)/4 = 2.25 = 2 words. This is then multiplied by the height of the the image (in pixels) to determine the COUNT of words to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

COUNT for 4 bits/pixel modes

8-bit transfers: COUNT = (W+1)/2 * H bytes
16-bit transfers: COUNT = (W+3)/4 * H words
32-bit transfers: COUNT = (W+7)/8 * H dwords

COUNT for 8 bits/pixel modes

8-bit transfers: COUNT = W * H bytes
16-bit transfers: COUNT = (W+1)/2 * H words
32-bit transfers: COUNT = (W+3)/4 * H dwords

COUNT for 16 bits/pixel modes

8-bit transfers: Do not use this combination
16-bit transfers: COUNT = W * H words
32-bit transfers: COUNT = (W+1)/2 * H dwords

COUNT for 32 bits/pixel modes

8-bit transfers: COUNT = Do not use this combination
16-bit transfers: COUNT = 2W * H words
32-bit transfers: COUNT = W * H dwords

Note that in 32 bits/pixel modes, the upper byte is a dummy byte providing padding for a 24-bit pixel.

11.3.3.5 Image Transfer—Across the Plane

A rectangular image is transferred from the CPU to the display memory across the plane. The monochrome bit image is stored as an array of pixels arranged in row major fashion. A byte represents data for 8 pixels in a row. This example uses a mix type of NEW, and x1,y1 is the top left corner of the rectangle on the display. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. The monochrome image is translated so that pixels corresponding to a 1 in the bit image are given color index 4 and pixels corresponding to a 0 in the bit image are given color index 0.

Setup:

```
Wait For FIFO 5 empty                ; 5 commands to follow
FRGD_MIX ⇐ 0027H                     ; foreground color source, mix type NEW
FRGD_COLOR ⇐ 00000004H               ; foreground color index 4
BKGD_MIX ⇐ 0007H                     ; background color source, mix type NEW
BKGD_COLOR ⇐ 00000000H               ; background color index 0
PIXEL_CNTL ⇐ A080H                   ; selection of mix register is based on data from the CPU
```

Drawing Operation:

```
Wait For FIFO 4 empty                ; 4 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
Wait for Graphics Engine not busy    ; loop till bit 9 of 9AE8H register is 0
CMD ⇐ 01010011D0110011b              ; Draw rectangle (bits 15-13), Swap ON (bit 12),
                                     ; 16-bit transfers (bits 10-9), Wait for CPU data (bit 8),
                                     ; Always X Major (bit 6) & X Positive (bit 5), Draw (bit 4),
                                     ; Multiple pixel (bit 1), Write (bit 0)
```

COUNT (of image pixel data to transfer) = ((WIDTH +15)/16)*HEIGHT words
PIX_TRANS ⇐ IMAGEDATA; Output image data to Pixel Transfer register for COUNT words

Notes

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of 9AE8H). The number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, if the transfer width is 8 bits and nine pixels are to be transferred per line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (W+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a 13-bit pixel transfer requires (13+7)/8 = 2.5 = 2 bytes. This is then multiplied by the height of the image (in pixels) to determine the COUNT of bytes to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

8-bit transfers: COUNT = (W+7)/8 * H bytes
16-bit transfers: COUNT = (W+15)/16 * H words
32-bit transfers: COUNT = (W+31)/32 * H dwords

To write to a single plane, set the foreground mix to 'logical one' (0002H), the background mix to 'logical zero' (0001H), and the Write Mask register (AAE8H) to select the desired (single) plane for updates.

11.3.3.6 BitBLT—Through the Plane

A source rectangular area in display memory is transferred to a specified destination in display memory. The pixels are written into the destination rectangle using the current foreground mix. Assume x1,y1 is the top left corner of the source rectangle in display memory and x2,y2 is the top left corner of the destination rectangle. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

Case 2: Source and destination rectangles overlap

```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 + WIDTH –1, Desty = x2 + WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative

Wait For FIFO 2 empty                ; 2 commands to follow
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX is the source of color source and mix type
FRGD_MIX ⇐ 0067H                     ; color source is display memory and mix type is NEW
```

Draw Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ Srcx                         ; set starting horizontal position
CUR_Y ⇐ Srcy                         ; set starting vertical position
DESTX_DIASTP ⇐ Destx                 ; set destination horizontal position
DESTY_AXSTP ⇐ Desty                  ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11000000D0D10011b              ; BitBLT (bits 15-13), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

11.3.3.7 BitBLT—Across the Plane

A source rectangular area in display memory is transferred to a specified destination in display memory. The bits corresponding to a single plane specified by setting the Read Mask register (AEE8H) can be transferred. With more than 1 plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

Case 2: Source and destination rectangles overlap

```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 + WIDTH –1, Desty = x2 + WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative
```

```
Wait For FIFO 5 empty          ; 5 commands to follow
PIXEL_CNTL ⇐ A0C0H             ; data from display memory selects mix register
FRGD_MIX ⇐ 0002H               ; always 'logical 1'
BKGD_MIX ⇐ 0001H               ; always 'logical 0'
RD_MASK ⇐ 00000001H            ; Read from plane 0
WRT_MASK ⇐ 00000004H           ; plane 2 enabled for write
```

Draw Operation:

```
Wait For FIFO 7 empty          ; 7 commands to follow
CUR_X ⇐ Srcx                   ; set starting horizontal position
CUR_Y ⇐ Srcy                   ; set starting vertical position
DESTX_DIASTP ⇐ Destx           ; set destination horizontal position
DESTY_AXSTP ⇐ Desty            ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1        ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1       ; rectangle height
CMD ⇐ 11000000D0D10011b        ; BitBLT (bits 15-13), Always X Major (bit 6) , Draw (bit 4),
                               ; Multi-pixel (bit 1), Write (bit 0)
```

Note

It is possible to translate a monochrome image, e.g., text fonts, stored in a single plane in display memory into a 2-color image. This is accomplished by setting the mix registers differently and setting the desired background and foreground colors. If the source bit is a '1', then the corresponding pixel at the destination is colored with the foreground color index. The destination pixel is colored with the background color index if the corresponding source bit is a '0'. The setup for this is as follows:

```
WRT_MASK ⇐ FFFFFFFFH          ; enable all planes for writing
FRGD_MIX ⇐ 0027H              ; color source foreground, mix type NEW
BKGD_MIX ⇐ 0007H              ; color source background, mix type NEW
FRGD_COLOR ⇐ 00000004H        ; foreground color
BKGD_COLOR ⇐ 00000001H        ; background color
```

11.3.3.8 PatBLT—Pattern Fill Through the Plane

An 8x8 pixel pattern is initially copied into an off-screen area of display memory using an image transfer operation or a direct write. This source pattern is then repeatedly copied to a destination rectangle of arbitrary size. The destination rectangle must not overlap the source pattern. Each copy is aligned to an 8-pixel boundary (x coordinate = 0, 8, etc.). The pixels are written into the destination rectangle using the current foreground mix. Assume x1,y1 is the top left corner of the source rectangle on the display and x2,y2 is the top left corner of the destination rectangle. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 2 empty                ; 2 commands to follow
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX is the source of color source and mix type
FRGD_MIX ⇐ 0067H                     ; color source is display memory, mix type is NEW
```

Draw Operation

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
DESTX_DIASTP ⇐ x2                    ; set destination horizontal position
DESTY_AXSTP ⇐ y2                     ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11100000D0D10011b              ; Pattern Fill (bits 15-13), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

11.3.3.9 PatBLT—Pattern Fill Across the Plane

An 8x8 pixel pattern is initially copied into an off-screen area of display memory using an image transfer operation or by a direct write. This source pattern is then transferred to a specified destination in display memory. The destination rectangle must not overlap the source rectangle. The bits corresponding to a single plane specified by setting the Read Mask register (AEE8H) can be transferred. With more than 1 plane enabled for read, if all the bits in the planes enabled for read are '1's, then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The height and width of the rectangle are HEIGHT and WIDTH.

Setup:

```
Wait For FIFO 5 empty                ; 5 commands to follow
PIXEL_CNTL ⇐ A0C0H                   ; data from display memory selects mix register
FRGD_MIX ⇐ 0002H                     ; always 'logical 1'
BKGD_MIX ⇐ 0001H                     ; always 'logical 0'
RD_MASK ⇐ 00000001H                  ; read from plane 0
WRT_MASK ⇐ 00000004H                 ; plane 2 enabled for write
```

Draw Operation:

```
Wait For FIFO 7 empty                ; 7 commands to follow
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
DESTX_DIASTP ⇐ x2                    ; set destination horizontal position
DESTY_AXSTP ⇐ y2                     ; set destination vertical position
MAJ_AXIS_PCNT ⇐ WIDTH-1              ; rectangle width
MIN_AXIS_PCNT ⇐ HEIGHT-1             ; rectangle height
CMD ⇐ 11100000D0D10011b              ; Pattern Fill (bits 15-13), Always X Major (bit 6) , Draw (bit 4),
                                     ; Multi-pixel (bit 1), Write (bit 0)
```

Note

To expand the source mono pattern into a 2-color pattern, set the foreground mix to 27H, the background mix to 7H and the foreground and background colors as desired. Also set the write mask (AAE8H) to FFFFFFFFH.

11.3.3.10 Short Stroke Vectors

Using short stroke vectors, short lines up to 15 pixels in length can be drawn rapidly because it is not necessary to calculate and set the line constants. Such lines are constrained to one of the 8 directions at 45 degree increments starting at 0 degrees. The current point x1,y1 is set and a NOP command is issued to set all the desired drawing parameters without actually writing a pixel. For example, bit 2 (Last Pixel Off) would be set to 1 (OFF) for drawing connected lines until the last line is drawn. The short stroke vector parameters are then loaded in the Short Stroke Vector Transfer (9EE8H) register (SHORT_STROKE). Two vectors can be defined at a time, one in the low byte and one in the high byte. For the low byte, bits [7:5] define the direction, with bit 4 set to '1' for a draw operation or to '0' for a move current position operation. Bits 3-0 define the length of the short line. Let SSVD0, SSVD1, ...SSVDN–1 bytes be the short stroke vector data for N lines.

Setup:

```
Wait For FIFO 3 empty                ; 3 commands to follow
PIXEL_CNTL ⇐ A000H                   ; FRGD_MIX is the source of color source and mix type
FRGD_MIX ⇐ 0027H                     ; use the foreground color, mix type NEW
FRGD_COLOR ⇐ 00000004H               ; foreground color index 4
```

Draw Operation:

```
CUR_X ⇐ x1                           ; set starting horizontal position
CUR_Y ⇐ y1                           ; set starting vertical position
CMD ⇐ 00010010XXX11111b              ; NOP (bits 15-13), Byte Swap (bit 12), 16-bit transfers (bits 10-9),
                                     ; Draw (bit 4), RadialDir (bit 3), LPixelOff (bit 2), Multi-pixel (bit 1),
                                     ; Write (bit 0)
```

```
While space available in the FIFO
  SHORT_STROKE ⇐ SSVD1 SHL 8 + SSVD0     ; SSVD1 shifted to high byte, SSVD0 in low byte
  SHORT_STROKE ⇐ SSVD3 SHL 8 + SSVD2     ; Byte swap turned on to read vectors out in
                                         ; correct order
          .
          .
          .
  SHORT_STROKE ⇐ SSVDN-1 SHL 8 + SSVDN-2
```

11.3.3.11 Programmable Hardware Cursor

A programmable cursor is supported which is compatible with the Microsoft Windows (bit 4 of CR55 = 0) and X11 (bit 4 of CR55 = 1) cursor definitions. The cursor size is 64 pixels wide by 64 pixels high, with the cursor pattern stored in an off-screen area of display memory. Two monochrome images 64 bits wide by 64 bits high (512 bytes per image) define the cursor shape. The first bit image is an AND mask and the second bit image is an XOR mask. The following is the truth table for the cursor display logic.

AND Bit	XOR Bit	Displayed (Microsoft Windows)	Displayed (X11)
0	0	Cursor Background Color	Current Screen Pixel
0	1	Cursor Foreground Color	Current Screen Pixel
1	0	Current Screen Pixel	Cursor Background Color
1	1	NOT Current Screen Pixel	Cursor Foreground Color

The Cursor Location High register (CRE) holds the hardware cursor foreground color and the Cursor Location Low register (CRF) holds the hardware cursor background color when hardware cursor color depth is 4/8 bits/pixel (CR45, bits 3-2 = 00b) and an 8-bit RAMDAC is being used. For all other values of bits 3-2 of CR45 when using an 8-bit RAMDAC, the hardware cursor color is taken from the Hardware Graphics Cursor Foreground Stack (CR4A) and the Hardware Graphics Cursor Background Stack (CR4B) registers. Each of these is a stack of four 8-bit registers. The stack pointers are reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). The color value is then programmed by consecutive writes (low byte, second byte, third byte, fourth byte) to the appropriate (foreground or background) register. When using a 16-bit RAMDAC, the cursor colors are always taken from CR4A and CR4B.

Enabling/Disabling the Cursor

The hardware cursor is disabled when a VGA-compatible mode is in use. It can be enabled or disabled when in Enhanced mode (bit 0 of 4AE8H = 1), as follows.

```
CR39 ⇐ A0H          ; Unlock System Control registers
CR45_0 ⇐ 1          ; Enable hardware cursor
CR45_0 ⇐ 0          ; Disable hardware cursor
CR39 ⇐ 00H          ; Lock System Control registers
```

Positioning the Cursor

The cursor can be positioned at any point on the display, with the X,Y coordinates ranging from 0 to 2047. This enables the full cursor images to be displayed on the screen and partial cursor images to be displayed at the right edge and the bottom edge of the screen. The cursor offset OX,OY has to be set to 0,0 for a 1024x768 resolution. If X is > (1024 – 64) or Y is > (768 – 64), then a partial cursor is visible at the right edge or top edge of the screen respectively. Note that if Y ≥ 768 then the cursor is not visible; it is residing in the off-screen area.

A partial cursor image can be displayed at the left edge or the top edge of the screen. To enable partial cursor display at the top edge of the screen, Y is set to 0 and the Y offset register is set to OY (range from 0 to 63). This displays the bottom 64–OY rows of the cursor image at the currently set X position and the top edge of the screen. Similarly, a partial cursor can be displayed at the left edge of the screen by setting X to 0 and the X offset register to OX (range from 0 to 63). This displays the right 64–OX columns of the cursor image at the currently set X and the left edge of the screen. The following pseudocode illustrates cursor positioning.

```
CR39 ⇐ A0H                                  ; Unlock System Control registers
CR46_10-8 ⇐ MS 3 bits of X cursor position
CR47_7-0 ⇐ LS 8 bits of X cursor position
CR49_7-0 ⇐ LS 8 bits of Y cursor position
CR4E_5-0 ⇐ Cursor Offset X position
CR4F_5-0 ⇐ Cursor Offset Y position
CR48_10-8 ⇐ MS 3 bits of Y cursor position
CR39 ⇐ 00H                                  ; Lock System Control registers
```

The cursor position is updated by the hardware once each frame. Therefore, the programmer should ensure that the position is re-programmed no more than once for each vertical sync period.

Programming the Cursor Shape

The AND and the XOR cursor image bitmaps are 512 bytes each. These are stored in consecutive bytes of off-screen display memory, 512 AND bytes followed by 512 XOR bytes. The starting location must be on a 1024-byte boundary. This location is programmed into the Hardware Graphics Cursor Start Address registers (CR4C and CR4D) as follows:

```
CR39 ⇐ A0H                                  ; Unlock System Control registers
CR4C_11-8 ⇐ MS 4 bits of the cursor storage start 1024-byte segment
CR4D ⇐ LS 8 bits of the cursor storage start 1024-byte segment
CR39 ⇐ 0                                    ; Lock System Control registers
```

The value programmed is the 1024-byte segment of display memory at which the beginning of the hardware cursor bit pattern is located.

The 1024 bytes of cursor definition are then written directly to display memory by the CPU using linear addressing.

Note

If the cursor is not 64 bits by 64 bits, the given images should be padded to make the cursor image 64 bits by 64 bits. The padded area should be made transparent by padding the extra AND mask bits with '1's and the extra XOR bits by '0's.

11.4 RECOMMENDED READING

Graphics Programming for the 8514/A by Jake Richter and Bud Smith (M&T Publishing, Inc) provides extensive explanations and examples for programming most of the bits in the S3 Enhanced Registers.

Although not released at the time this data book was printed, the 3rd edition of *Programming Guide to the EGA and VGA Cards* by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc) is scheduled to include a section on programming for S3 accelerator chips.

Section 12: CGA-Compatible Register Descriptions

In the following register descriptions, "U" stands for undefined or unused and "R" stands for reserved (write = 0, read = U).

See Appendix A for a table listing each register in this section and its page number.

Light Pen High Register (LPENH)

Read Only Address: 3D5H, Index 10H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
U	U	Light Pen Strobe Address High					

Light Pen Low Register (LPENL)

Read Only Address: 3D5H, Index 11H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Light Pen Strobe Address Low							

These registers contain the 14 memory address bits at the time the light pen strobe signal was detected in CGA and HGC modes.

These registers are not available in VGA mode.

The light pen is not actually connected to most systems, but the LP set/reset flag can be used to read the video memory addresses at the vertical retrace interval. The CPU can read the video memory address through this register. The screen mode and the video memory address have a known ratio at the vertical retrace interval. Therefore, the CPU can guess the screen mode (ex: low or high resolution, and text or graphics) from the light pen detect address at the vertical retrace.

The mode register is a write-only register, except in VGA mode. The CPU cannot read any screen mode information directly. Therefore the light pen detect address at the vertical retrace interval is used as a mode indicator indirectly in CGA and HGC modes.

CGA Mode Control Register (CGA_MODE)

Read/Write
Power-On Default: 00H

Address: 3D8H

7	6	5	4	3	2	1	0
R	R	TEXT BLNK	HRES GRPH	DISP ENB	B/W MODE	GRPH MODE	HRES TEXT

Bit 0 HRES TEXT - Select High Resolution Text
0 = 40 x 25 alpha mode
1 = 80 x 25 alpha mode

Bit 1 GRPH MODE - Select Graphics Mode
0 = Alpha Mode
1 = Graphics Mode

Bit 2 B/W MODE - Select Black/White Mode
0 = Color enabled
1 = Color disabled. In 320 x 200 x 4 color mode, pixel bits represent:
00 = background
01 = cyan
10 = red
11 = white

Bit 3 DISP ENB - Enable Display
0 = Screen Blank
1 = Video Enabled

Bit 4 HRES GRPH - Select High Resolution Graphics
0 = all other modes
1 = Enable 640 x 200 graphics mode

Bit 5 TEXT BLNK - Enable Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bits 7–6 Reserved

CGA Color Select Register (CGA_COLOR)

Read/Write Address: 3D9H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	SEL CSET	SEL I-EN	BORDER/BKGR COLOR I	R	G	B

In 640 x 200 (2 color) mode, pixel bit = 0 corresponds to black and pixel bit = 1 corresponds to the foreground color specified by bits 3-0 of this register.

Bit 0 BORDER/BKGR COLOR - Select Blue Border
0 = Blue not selected
1 = Select blue border in alpha mode, select blue background and border color in 320 × 200 graphics mode, select blue foreground color in 640 × 200 graphics mode

Bit 1 BORDER/BKGR COLOR - Select Green Border
0 = Green not selected
1 = Select green border in alpha mode, select green background and border color in 320 × 200 graphics mode, select green foreground color in 640 × 200 graphics mode

Bit 2 BORDER/BKGR COLOR - Select Red Border
0 = Red not selected
1 = Select red border in alpha mode, select red background and border color in 320 × 200 graphics mode, select red foreground color in 640 × 200 graphics mode

Bit 3 BORDER/BKGR COLOR - Select Intensified Border
0 = No intensification
1 = Select intensified border in alpha mode, select intensified background and border color in 320 × 200 graphics mode, select intensified foreground color in 640 × 200 graphics mode

Bit 4 SEL I-EN - Select Alternate Color Set
0 = Alternate color set not enabled
1 = Background color in alpha mode. Enable alternate (high intensity) color set in graphics mode

Bit 5 SEL CSET - Select Color Set in 320x200 Mode
0 = Pixel Bits
00 = Background determined by bits 3-0
01 = Green
10 = Red
11 = Yellow
1 = Pixel Bits
00 = Background determined by bits 3-0
01 = Cyan
10 = Violet
11 = White

Bits 7–6 Reserved

CGA Status Register (CGA_STAT)

Read Only Address: 3DAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 1	= 1	= 1	= 1	VSY	= 1	LPF	DTM

Bit 0 $\overline{\text{DTM}}$ - Border/Blanking Active
0 = Active display
1 = Border/Blanking Active

Bit 1 LPF - Light Pen Flag
0 = Light Pen Latch cleared
1 = Light Pen Latch triggered

Bit 2 = 1
0 = Light Pen switch closed (not available)
1 = Light Pen switch open

Bit 3 VSY - Vertical Sync Active
0 = Inactive Vertical Sync
1 = Active Vertical Sync

Bits 7–4 Reserved = 1

Reset Light Pen Flag Register (RLPEN)

Write Only Address: 3DBH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Reset Light Pen Flag							

The CPU can control the light pen flag with I/O writes with any data to 3B9H or 3DCH to set, and 3BBH or 3DBH to reset. The CPU can guess the screen mode indirectly by reading the video memory address at the vertical retrace interval. When the light pen flag is set to 1, the video memory address at that time is stored in the Light Pen High and Low registers. The sequence to read the light pen detect address is:

1. Clear the light pen flag with an I/O write to 3BBH or 3DBH.
2. Wait for the vertical sync signal (VSY) to set.
3. Set light pen flag with an I/O write to 3B9H or 3DCH.
4. Read the light pen detect address.
5. Return to 1.

Set Light Pen Flag Register(SLPEN)

Write Only Address: 3DCH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Set Light Pen Flag							

A write of anything to this register sets the light pen flag. See the description for the Reset Lightpen Flag register above.

Section 13: MDA- and HGC-Compatible Register Descriptions

In the following register descriptions, "U" stands for undefined or unused and "R" stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

Light Pen High Register (LPENH)

Read Only Address: 3B5H, Index 10H
Power-On Default: Undefined

Refer to the description in Section 12.

Light Pen Low Register (LPENL)

Read Only Address: 3B5H, Index 11H
Power-On Default: Undefined

Refer to the description in Section 12.

MDA-Mode Control Register (MDA_MODE)

Read/Write Address: 3B8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	TXT BLK	R	DSP ENB	R	R	R

Bits 2–0 Reserved

Bit 3 DSP ENB - Enable Display
0 = (screen blank)
1 = Video enabled

Bit 4 Reserved

Bit 5 TXT BLK - Enable Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bits 7–6 Reserved

HGC-Mode Control Register (HGC_MODE)

Read/Write Address: 3B8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HGC PAGE	R	TXT BLK	R	DSP ENB	R	GRPPH MODE	R

Bit 0 Reserved

Bit 1 GRPH MODE - Enable Graphics Mode
0 = 80 x 25 alpha mode enabled
1 = 720 x 348 graphics mode enabled

Bit 2 Reserved

Bit 3 DSP ENB - Enable Display
0 = (screen blank)
1 = Video enabled

Bit 4 Reserved

Bit 5 TXT BLK - Enable Text Blinking
0 = Blinking disabled
1 = Blinking enabled

Bit 6 Reserved

Bit 7 HGC PAGE - Select Hercules Graphics Video Page 1
0 = graphics mode buffer displayed from B0000H (video page 0)
1 = graphics mode buffer displayed from B8000H (video page 1)

HGC-Set Light Pen Flag Register (HGC_SLPEN)

Write Only Address: 3B9H
Power-On Default: Undefined

Refer to the description in Section 12.

HGC Status Register (HGC_STS)

Read Only Address: 3BAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
$\overline{VSY}$	= 1	= 1	= 1	V-DT	= 1	LPF	HSY

Bit 0 HSY - Horizontal Sync Active
0 = Active display
1 = Border/Blanking Active

Bit 1 LPF - Light Pen Flag On
0 = Light Pen Flag off
1 = Light Pen Flag on

Bit 2 Reserved = 1

Bit 3 V-DT - Black/White Video Enabled
0 = B/W Video disabled
1 = B/W Video enabled

Bits 6–4 Reserved = 1

Bit 7 $\overline{VSY}$ - Vertical Sync Inactive
0 = Inactive Vertical Sync
1 = Active Vertical Sync

MDA Status Register (MDA_STS)

Read Only Address: 3BAH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 1	= 1	= 1	= 1	TEST	=1	= 1	HSY

Bit 0 HSY - Horizontal Sync Active
0 = Active display
1 = Border/Blanking Active

Bits 2–1 Reserved = 1

Bit 3 TEST
0 = B/W Video disabled
1 = B/W Video enabled

Bits 7–4 Reserved = 1

Reset Light Pen Flag Register (HGC_RLPEN)

Write Only Address: 3BBH
Power-On Default: Undefined

Refer to the description in Section 12.

HGC Configuration Register (CONFIG)

Write Only Address: 3BFH
Power-On Default: 00H

7	6	5	4	3	2	1	0
U	U	U	U	U	U	ENB PAGE	ENB GRPH

Bit 0 ENB PAGE - Enable Page
0 = Alpha mode is forced
1 = Allows graphics mode

Bit 1 ENB GRPH - Enable Graphics
0 = Bit 7 of Hercules Mode register can't be set, thus video memory occupies B0000H–B7FFFH, which allows the CGA to coexist
1 = Bit 7 of Hercules Mode register can be set, allowing upper memory page access

Section 14: VGA Standard Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation.

See Appendix A for a table listing each register in this section and its page number.

14.1 GENERAL REGISTERS

This section describes general input status and output control registers.

Miscellaneous Output Register (MISC)

Write Only — Address: 3C2H
Read Only — Address: 3CCH
Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
VSP	HSP	PGSL	= 0	CLK 1	SEL 0	ENB RAM	IOA SEL

Bit 0 IOA SEL - I/O Address Select
0 = Monochrome emulation. Address based at 3Bx
1 = Color emulation. Address based at 3Dx

Bit 1 ENB RAM - Enable CPU Display Memory Access
0 = Disable access of the display memory from the CPU
1 = Enable access of the display memory from the CPU

Bit 3–2 Clock Select - These two bits select the video clock source
00 = Selects 25.175 MHz clock for 640 horizontal pixels
01 = Selects 28.322 MHz clock for 720 horizontal pixels
10 = Reserved
11 = Enable dot clock select bits in the Mode Control register (CR42), bits 3-0. This is an enhanced function

Bit 4 Reserved = 0

Bit 5 PGSL - Select High 64K Page
0 = Select the low 64K page of memory
1 = Select the high 64K page of memory

Bit 6 $\overline{\text{HSP}}$ - Select Negative Horizontal Sync Pulse
0 = Select a positive horizontal retrace sync pulse
1 = Select a negative horizontal retrace sync pulse

Bit 7 $\overline{\text{VSP}}$ - Select Negative Vertical Sync Pulse
0 = Select a positive vertical retrace sync pulse
1 = Select a negative vertical retrace sync pulse

Feature Control Register (FCR_WT, FCR_AD)

Write Only Address: 3?AH
Read Only Address: 3CAH
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 VSSL - Vertical Sync Type Select
0 = Enable normal vertical sync output to the monitor
1 = The 'vertical sync' output is the logical OR of 'vertical sync' and 'vertical active display enable' (an internal signal).

Bits 7–4 Reserved = 0

Input Status 0 Register (STATUS_0)

Read Only Address: 3C2H
Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SENS	= 0	= 0	= 0	= 0

Bits 3–0 Reserved = 0

Bit 4 MON SENS - Monitor Sense Input Status
0 = The $\overline{\text{SENSE}}/\overline{\text{BREQ}}$ input is a logical 0
1 = The $\overline{\text{SENSE}}/\overline{\text{BREQ}}$ input is a logical 1

The $\overline{\text{SENSE}}/\overline{\text{BREQ}}$ input functions as $\overline{\text{BREQ}}$ (memory bus request from another memory master) when bit 2 of CR50 is set to 1.

Bits 6–5 Reserved = 0

Bit 7 CRT INTPE - CRT Interrupt Status
0 = Vertical retrace interrupt cleared
1 = Vertical retrace interrupt pending. Interrupt generation is enabled by bit 5 of CR11 for VGA modes and bit 8 of 42E8H for Enhanced modes.

Input Status 1 Register (STATUS_1)

Read Only Address: 3?AH
Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
= 0	= 0	TST-VDT 1	0	VSY	= 1	LPF	DTM

Bit 0 $\overline{\text{DTM}}$ - Display Mode Inactive
0 = The display is in the display mode.
1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active

Bit 1 LPF - Light Pen Flag Triggered
0 = Light pen has not been triggered
1 = Light pen has been triggered

Bit 2 Reserved = 1

Bit 3 VSY - Vertical Sync Active
0 = Display is in the display mode
1 = Display is in the vertical retrace mode

Bits 5–4 TST-VDT - Video Signal Test
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output observation.

Bits 7–6 Reserved = 0

14.2 SEQUENCER REGISTERS

The sequencer registers are located at two-byte address spaces. These registers are accessed by first writing the data to the index register of the sequencer at I/O address 3C4H and then writing to or reading from the data register at 3C5H.

Sequencer Index Register (SEQX)

Read/Write Address: 3C4H
Power-On Default: Undefined

This register is loaded with a binary value that indexes the sequencer register for read/write data. This value is referred to as the "Index Number" of the SR register in this document.

7	6	5	4	3	2	1	0
R	R	R	R	SEQ ADDRESS			

Bits 3–0 SEQ ADDRESS - Sequencer Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Sequencer Data Register (SEQ_DATA)

Read/Write Address: 3C5H
Power-On Default: Undefined

This register is the data port for the sequencer register indexed by the Sequencer Index register (3C4H).

7	6	5	4	3	2	1	0
SEQ DATA							

Bit 7–0 SEQ DATA - Sequencer Register Data
Data to the sequencer register indexed by the sequencer address index.

Reset Register (RST_SYNC) (SR0)

Read/Write Address: 3C5H, Index 00H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	SYN RST	ASY RST

Bit 0 $\overline{\text{ASY}}$ RST - Asynchronous Reset

This bit is for VGA software compatibility only. It has no function for the Vision964.

Bit 1 $\overline{\text{SYN}}$ RST - Synchronous Reset

This bit is for VGA software compatibility only. It has no function for the Vision964.

Bits 7–2 Reserved = 0

Clocking Mode Register (CLK_MODE) (SR1)

Read/Write Address: 3C5H, Index 01H
Power-On Default: 00H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCRN OFF	SHF 4	DCK 1/2	SHF LD	= 0	8DC

Bit 0 $\overline{8DC}$ - 8 Dot Clock Select
0 = Character clocks 9 dots wide are generated
1 = Character clocks 8 dots wide are generated

Bit 1 Reserved = 0

Bit 2 SHF LD - Load Serializers Every Second Character Clock
0 = Load the video serializer every character clock
1 = Load the video serializers every other character clock

Bit 3 DCK 1/2 - Internal Dot Clock is 1/2 DCLK
0 = Set the internal dot clock to the same frequency as the DCLK input
1 = Set the internal dot clock to 1/2 the frequency of the DCLK input

Bit 4 SHF 4 - Load Serializers Every Fourth Character Clock
0 = Load the serializers every character clock cycle
1 = Load the serializers every fourth character clock cycle

Bit 5 SCRN OFF - Screen Off
0 = Screen is turned on
1 = Screen is turned off

Bit 7–6 Reserved = 0

Enable Write Plane Register (EN_WT_PL) (SR2)

Read/Write Address: 3C5H, Index 02H
Power-On Default: 00H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

Bits 3–0 EN.WT.PL - Enable Write to a Plane
0 = Disables writing into the corresponding plane
1 = Enables the CPU to write to the corresponding color plane

Bits 7–4 Reserved = 0

Character Font Select Register (CH_FONT_SL) (SR3)

Read/Write Address: 3C5H, Index 03H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	SLA 2	SLB 2	SLA 1	SLA 0	SLB 1	SLB 0

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1–0 SLB - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

Bits 4,1,0	Font Table Location	Bits 4, 1,0	Font Table Location
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3–2 SLA - Select Font A
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select A.

Bits 7–6 Reserved = 0

Memory Mode Control Register (MEM_MODE) (SR4)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 04H

This register controls CPU memory addressing mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	CHN 4M	SEQ MODE	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access
0 = Memory access restricted to 16/32 KBytes
1 = Allows complete memory access to 256 KBytes. Required for VGA

Bit 2 SEQ MODE - Select Sequential Addressing Mode
This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3
1 = Directs the system to use a sequential addressing mode

Bit 3 CHN 4M - Select Chain 4 Mode
0 = Enables odd/even mode.
1 = Chain 4 Mode. This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bits 7–4 Reserved = 0

Unlock Extended Sequencer Register (UNLK_EXSR) (SR8)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 08H

Loading xxxx0110b (e.g., 06H) unlocks the Extended Sequencer register (SRD) for reading/writing. (x = don't care).

7	6	5	4	3	2	1	0
R	R	R	R	=0	=1	=1	=0

Extended Sequencer Register (EX_SR_D) (SRD)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 0DH

7	6	5	4	3	2	1	0
VSY-CTL		HSY-CTL		R	R	R	R
1	0	1	0				

This register provides independent control of the HSYNC and VSYNC signals, therefore supporting the VESA DPMS (Display Power Management Control) standard.

Bits 3–0 Reserved

Bits 5–4 HSY-CTL - HSYNC Control
00 = Normal operation
01 = HSYNC = 0
10 = HSYNC = 1
11 = Reserved

Bits 7–6 VSY-CTL - VSYNC Control
00 = Normal operation
01 = VSYNC = 0
10 = VSYNC = 1
11 = Reserved

14.3 CRT CONTROLLER REGISTERS

The CRT controller registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at I/O address 3?4H and the CRT Controller Data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H.

CRT Controller Index Register (CRTC_ADR) (CRX)

Read/Write Address: 3?4H
Power-On Default: 00H

This register is loaded with a binary value that indexes the CRT controller register where data is to be accessed. This value is referred to as the "Index Number" of the CR register (CR00–18). This register is also used as an index to the S3 VGA registers, the System Control Registers and the System Extension registers.

7	6	5	4	3	2	1	0
CRTC ADDRESS							

Bits 7–0 CRTC ADDRESS - CRTC Register Index
A binary value indexing the register where data is to be accessed.

CRT Controller Data Register (CRTC_DATA) (CRT)

Read/Write Address: 3?5H
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC DATA							

Bits 7–0 CRTC DATA - CRTC Register Data
Data to the CRT controller register indexed by the CRT controller address index.

Horizontal Total Register (H_TOTAL) (CR0)

Read/Write Address: 3?5H, Index 00H
Power-On Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active. In other words, it is the total time required for both the displayed and non-displayed portions of a singe scan line. Bit 8 of this value is bit 0 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bits 7–0 HORIZONTAL TOTAL.
9-bit Value = (number of character clocks in one scan line) - 5. This register contains the least significant 8 bits of this value.

Horizontal Display End Register (H_D_END) (CR1)

Read/Write Address: 3?5H, Index 01H
Power-On Default: Undefined

This register defines the number of character clocks for one line of the active display. Bit 8 of this value is bit 1 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END							

Bits 7–0 HORIZONTAL DISPLAY END
9-bit Value = (number of character clocks of active display) - 1. This register contains the least significant 8 bits of this value.

Start Horizontal Blank Register (S_H_BLNK) (CR2)

Read/Write Address: 3?5H, Index 02H
Power-On Default: Undefined

This register specifies the value of the character clock counter at which the $\overline{\text{BLANK}}$ signal is asserted. Bit 8 of this value is bit 2 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK							

Bits 7–0 START HORIZONTAL BLANK
9-bit Value = character clock value at which horizontal blanking begins. This register contains the least significant 8 bits of this value.

End Horizontal Blank Register (E_H_BLNK) (CR3)

Read/Write Address: 3?5H, Index 03H
Power-On Default: Undefined

This register determines the pulse width of the $\overline{\text{BLANK}}$ signal and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1	0	END HORIZONTAL BLANK				

Bits 4–0 END HORIZONTAL BLANK
6-bit Value = least significant 6 bits of the character clock counter value at which time horizontal blanking ends. To obtain this value, add the desired $\overline{\text{BLANK}}$ pulse width in character clocks to the Start Horizontal Blank value, which is also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 7 of CR5. This allows a maximum pulse width of 63 character clocks. This pulse width can be extended by 64 DCLKs via bit 3 of CR5D.

Bits 6–5 DSP-SKW - Display Skew
These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the HSYNC and VSYNC signals. The bit values and amount of skew are shown in the following table:
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved

Start Horizontal Sync Position Register (S_H_SY_P) (CR4)

Read/Write Address: 3?5H, Index 04H
Power-On Default: Undefined

This register is used to adjust the screen center horizontally and to specify the character position at which HSYNC becomes active. Bit 8 of this value is bit 4 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION							

Bits 7–0 START HORIZONTAL SYNC POSITION.
9-bit Value = character clock counter value at which HSYNC becomes active. This register contains the least significant 8 bits of this value.

End Horizontal Sync Position Register (E_H_SY_P) (CR5)

Read/Write Address: 3?5H, Index 05H
Power-On Default: Undefined

This register specifies when the HSYNC signal becomes inactive and the horizontal skew. The HSYNC pulse defined by this register can be extended by 32 DCLKs via bit 5 of CR5D.

7	6	5	4	3	2	1	0
EHB	HOR-SKW		END HORIZONTAL SYNC POS				
b5	1	0					

Bits 4–0 END HORIZONTAL SYNC POS
5-bit Value = 5 least significant bits of the character clock counter value at which time HSYNC becomes inactive. To obtain this value, add the desired HSYNC pulse width in character clocks to the Start Horizontal Sync Position value, also in character clocks. The 5 least significant bits of this sum are programmed into this field. This allows a maximum HSYNC pulse width of 31 character clocks. This pulse width can be extended by 32 DCLKs via bit 5 of CR5D.

Bits 6–5 HOR-SKW - Horizontal Skew
These bits control the skew of the HSYNC signal. A binary 00 equals no HSYNC delay. For some modes, it is necessary to provide an HSYNC signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the HSYNC signal. To guarantee the signals are latched properly, HSYNC is asserted before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew00

Bit 7 EHB b5
End Horizontal Blanking bit 5.

Vertical Total Register (V_TOTAL) (CR6)

Read/Write Address: 3?5H, Index 06H
Power-On Default: Undefined

This register specifies the number of scan lines from one VSYNC active to the next VSYNC active. The scan line counter resets to 0 at this point. Bit 8 is bit 0 of CR7. Bit 9 is bit 5 of CR7. Bit 10 is bit 0 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bits 7–0 VERTICAL TOTAL
11-bit Value = (number of scan lines from VSYNC active to the next VSYNC active) - 2.
This register contains the least significant 8 bits of this value.

CRTC Overflow Register (OVFL_REG) (CR7)

Read/Write Address: 3?5H, Index 07H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VRS 9	VDE 9	VT 9	LCM 8	SVB 8	VRS 8	VDE 8	VT 8

This register provides extension bits for fields in other registers.

Bit 0 Bit 8 of the Vertical Total register (CR6)

Bit 1 Bit 8 of the Vertical Display End register (CR12)

Bit 2 Bit 8 of the Vertical Retrace Start register (CR10)

Bit 3 Bit 8 of the Start Vertical Blank register (CR15)

Bit 4 Bit 8 of the Line Compare register (CR18)

Bit 5 Bit 9 of the Vertical Total register (CR6)

Bit 6 Bit 9 of the Vertical Display End register (CR12)

Bit 7 Bit 9 of the Vertical Retrace Start register (CR10)

Preset Row Scan Register (P_R_SCAN) (CR8)

Read/Write Address: 3?5H, Index 08H
Power-On Default: Undefined

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1	0	PRE-SET ROW SCAN COUNT				

Bits 4–0 PRE-SET ROW SCAN COUNT
Value = starting row within a character cell for the first character row displayed after vertical retrace. This allows a partial character row to be displayed at the top of the display and is used for scrolling.

Bits 6–5 BYTE-PAN
Value = number of bytes to pan. The number of pixels to pan is specified in AR13.

Bit 7 Reserved = 0

Maximum Scan Line Register (MAX_S_LN) (CR9)

Read/Write Address: 3?5H, Index 09H
Power-On Default: Undefined

This register specifies the number of scan lines per character row and provides one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4–0 MAX SCAN LINE
Value = (number of scan lines per character row) - 1

Bit 5 SVB 9
Bit 9 of the Start Vertical Blank Register (CR15)

Bit 6 LCM 9
Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN
0 = Normal operation
1 = Enables double scanning operation. Each line is displayed twice by repeating the row scan counter and video memory address. Vertical parameters in the CRT controller are not affected.

Cursor Start Scan Line Register (CSSL) (CRA)

Read/Write Address: 3?5H, Index 0AH
Power-On Default: Undefined

The cursor start register defines the row scan of a character line where the cursor begins.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4–0 CSR CURSOR START SCAN LINE
Value = (starting cursor row within the character cell) - 1. When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF
0 = Turns on the text cursor
1 = Turns off the text cursor

Bits 7–6 Reserved = 0

Cursor End Scan Line Register (CESL) (CRB)

Read/Write Address: 3?5H, Index 0BH
Power-On Default: Undefined

This register defines the row scan of a character line where the cursor ends.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1	0	CURSOR END SCAN LINE				

Bits 4–0 CURSOR END SCAN LINE
Value = ending scan line number within the character cell for the text cursor. If the value of the cursor start scan line is greater than the value of cursor end line, then no cursor is generated.

Bits 6–5 CSR-SKW - Cursor Skew
These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one character position on the screen.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved = 0

Start Address High Register (STA(H)) (CRC)

Read/Write Address: 3?5H, Index 0CH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
DISPLAY START ADDRESS (HIGH)							

20-bit Value = the first address after a vertical retrace at which the display on the screen begins on each screen refresh. These along with bits 4-0 of CR69 are the high order start address bits.

Start Address Low Register (STA(L)) (CRD)

Read/Write Address: 3?5H, Index 0DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Start address (low) contains the 8 low order bits of the address.

Cursor Location Address High Register (CLA(H)) (CRE)

Read/Write Address: 3?5H, Index 0EH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

20-bit Value = the cursor location address of the video memory where the text cursor is active. This register along with bits 4-0 of CR69 are the high order bits of the address. When using a 4/8 bits/pixel color depth and an 8-bit RAMDAC in Enhanced mode, this register contains the hardware cursor foreground color.

Cursor Location Address Low Register (CLA(L)) (CRF)

Read/Write Address: 3?5H, Index 0FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Cursor location address (low) contains the 8 low order bits of the address. When using a 4/8 bits/pixel color depth and an 8-bit RAMDAC in Enhanced mode, this register contains the hardware cursor background color.

Vertical Retrace Start Register (VRS) (CR10)

Read/Write Address: 3?5H, Index 10H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VERTICAL RETRACE START							

Bits 7–0 VERTICAL RETRACE START.
11-bit Value = number of scan lines at which VSYNC becomes active. These are the low-order 8 bits. Bit 8 is bit 2 of CR7. Bit 9 is bit 7 of CR7. Bit 10 is bit 4 of CR5E.

Vertical Retrace End Register (VRE) (CR11)

Read/Write Address: 3?5H, Index 11H
Power-On Default: 0xH

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	REF 3/5	DIS VINT	CLR VINT	VERTICAL RETRACE END			

Bits 3–0 VERTICAL RETRACE END
Value = least significant 4 bits of the scan line counter value at which VSYNC goes inactive. To obtain this value, add the desired VSYNC pulse width in scan line units to the CR10 value, also in scan line units. The 4 least significant bits of this sum are programmed into this field. This allows a maximum VSYNC pulse width of 15 scan line units.

Bit 4 $\overline{\text{CLR}}$ VINT - Clear Vertical Retrace Interrupt
0 = Vertical retrace interrupt cleared
1 = The flip-flop is able to catch the next interrupt request

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt
0 = Vertical retrace interrupt enabled
1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on

Bit 6 REF $\bar{3}$/5 - Refresh Cycle Select
0 = Three DRAM refresh cycles generated per horizontal line
1 = Five DRAM refresh cycles generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 KHz). This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on. This setting can be overridden via bits 1-0 of CR3A

Bit 7 LOCK R0-7 - Lock Writes to CRT Controller Registers
0 = Writing to all CRT Controller registers enabled
1 = Writing to all bits of the CRT Controller registers CR0–CR7 except bit 4 of CR7 (LCM8) disabled. This bit is set to 1 by the BIOS during a mode set, a reset or power-on

Vertical Display End Register (VDE) (CR12)

Read/Write Address: 3?5H, Index 12H
Power-On Default: Undefined

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends. Bit 8 and bit 9 are bits 1 and 6 of CR7. Bit 10 is bit 1 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7–0 VERTICAL DISPLAY END
11-bit Value = (number of scan lines of active display) - 1. This register contains the least significant 8 bits of this value.

Offset Register (SCREEN-OFFSET) (CR13)

Read/Write Address: 3?5H, Index 13H
Power-On Default: Undefined

This register specifies the logical line width of the screen and is sometimes called the screen pitch. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount. Bits 5-4 of CR51 are extension bits 9-8 of this register. If these bits are 00b, bit 2 of CR43 is extension bit 8 of this register.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

Bits 7–0 LOGICAL SCREEN WIDTH
10-bit Value = quantity that is multiplied by 2 (word mode), 4 (doubleword mode) or 8 (quadword mode) to specify the difference between the starting byte addresses of two consecutive scan lines. This register contains the least significant 8 bits of this value. The addressing mode is specified by bit 6 of CR14 and bit 3 of CR17. Setting bit 3 of CR31 to 1 forces doubleword mode.

Underline Location Register (ULL) (CR14)

Read/Write Address: 3?5H, Index 14H
Power-On Default: Undefined

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBWD MODE	CNT BY4	UNDER LINE LOCATION				

Bits 4–0 UNDER LINE LOCATION
5-bit Value = (scan line count of a character row on which an underline occurs) -1.

Bit 5 CNT BY4 - Select Count by 4 Mode
0 = The memory address counter depends on bit 3 of CR17 (count by 2)
1 = The memory address counter is incremented every four character clocks

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBLWD MODE - Select Doubleword Mode
0 = The memory addresses are byte or word addresses
1 = The memory addresses are doubleword addresses

Bit 7 Reserved = 0

Start Vertical Blank Register (SVB) (CR15)

Read/Write Address: 3?5H, Index 15H
Power-On Default: Undefined

This register specifies the scan line at which the vertical blanking period begins. Bit 8 is bit 3 of CR7. Bit 9 is bit 5 of CR9. Bit 10 is bit 2 of CR5E.

7	6	5	4	3	2	1	0
START VERTICAL BLANK							

Bits 7–0 START VERTICAL BLANK.
11-bit value = (scan line count at which $\overline{\text{BLANK}}$ becomes active) - 1. This register contains the least significant 8 bits of this value.

End Vertical Blank Register (EVB) (CR16)

Read/Write Address: 3?5H, Index 16H
Power-On Default: Undefined

This register specifies the scan line count value when the vertical blank period ends.

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7–0 END VERTICAL BLANK
Value = least significant 8 bits of the scan line counter value at which vertical blanking ends. To obtain this value, add the desired width of the vertical blanking pulse in scan lines to [(value in the Start Vertical Blank register)-1], also in scan lines. The 8 least significant bits of this sum are programmed into this field. This allows a maximum vertical blanking pulse of 63 scan line units.

CRTC Mode Control Register (CRT_MD) (CR17)

Read/Write Address: 3?5H, Index 17H
Power-On Default: 00H

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
RST	BYTE MODE	ADW 16K	= 0	WRD MODE	VT X2	4BK HGC	2BK CGA

Bit 0 $\overline{2BK}$ CGA - Select Bank 2 Mode for CGA Emulation
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1 $\overline{4BK}$ HGC - Select Bank 4 Mode for HGA Emulation
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2 VT X2 - Select Vertical Total Double Mode
0 = Horizontal retrace clock selected
1 = Horizontal retrace clock divided by two selected

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Bit 3 CNT BY2 - Select Word Mode
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected

Bit 4 Reserved = 0

Bit 5 $\overline{\text{ADW}}$ 16K - Address Wrap
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller

This bit is useful in implementing IBM CGA mode.

Bit 6 BYTE MODE - Select Byte Addressing Mode
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output
1 = Byte address mode

Bit 7 $\overline{\text{RST}}$ - Hardware Reset
0 = Vertical and horizontal retrace pulses cleared (always 0)
1 = Vertical and horizontal retrace pulses enabled

This bit does not reset any other registers or outputs.

Line Compare Register (LCM) (CR18)

Read/Write Address: 3?5H, Index 18H
Power-On Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset (CR13) register content. Bit 8 is bit 4 of CR7. Bit 9 is bit 6 of CR9. Bit 10 is bit 6 of CR5E.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION							

Bit 7–0 LINE COMPARE POSITION
11-bit Value = number of scan lines at which the screen is split into screen A and screen B. This register contains the least significant 8 bits of this value.

CPU Latch Data Register (GCCL) (CR22)

Read Only Address: 3?5H, Index 22H
Power-On Default: Undefined

This register is used to read the CPU latch in the Graphics Controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7–0 GRAPHICS CONTROLLER CPU LATCH - N
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

Attribute Index Register (ATC_F/I) (CR24)

Read Only Address: 3?5H, Index 24H, 26H
Power-On Default: Undefined

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF).

7	6	5	4	3	2	1	0
AFF	= 0	ENV	ATTRIBUTE CONTROLLER INDEX				

Bits 4–0 ATTRIBUTE CONTROLLER INDEX
This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 5 ENV- Enable Video Display
This is the setting of bit 5 of 3C0H, indicating video display enabled status (1 = enabled)

Bit 6 Reserved = 0

Bit 7 $\overline{\text{AFF}}$

14.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

Graphics Controller Index Register (GRC_ADR)

Read/Write Address: 3CEH
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0–6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3–0 GR CONT ADDRESS - Graphics Controller Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Graphics Controller Data Register (GRC_DATA)

Read/Write Address: 3CFH
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7–0 GRAPHICS CONTROLLER DATA
Data to the Graphics Controller register indexed by the graphics controller address.

Set/Reset Data Register (SET/RST_DT) (GR0)

Read/Write Address: 3CFH, Index 00H
Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3–0 SET/RESET DATA
These bits become the color value for CPU memory write operations. In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7–4 Reserved = 0

Enable Set/Reset Data Register (EN_S/R_DT) (GR1)

Read/Write Address: 3CFH, Index 01H
Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3–0 ENB SET/RST DATA
When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7–4 Reserved = 0

Color Compare Register (COLOR-CMP) (GR2)

Read/Write Address: 3CFH, Index 02H
Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3–0 COLOR COMPARE DATA
This value becomes the reference color used to compare each pixel. Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7–4 Reserved = 0

Raster Operation/Rotate Count Register (WT_ROP/RTC) (GR3)

Read/Write Address: 3CFH, Index 03H
Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
			RST-OP				
= 0	= 0	= 0	1	0	ROTATE-COUNT		

Bits 2–0 ROTATE-COUNT
These bits define a binary encoded value of the number of positions to right-rotate data during a CPU memory write. To write non-rotated data, the CPU must preset a count of 0.

Bits 4–3 RST-OP - Select Raster Operation
The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical functions are defined as follows:
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7–5 Reserved = 0

Read Plane Select Register (RD_PL_SL) (GR4)

Read/Write Address: 3CFH, Index 04H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
						RD-PL-SL	
= 0	= 0	= 0	= 0	= 0	= 0	1	0

The contents of this register represent the memory plane from which the CPU reads data in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored. Four memory planes are selected as follows:

Bits 1–0 RD-PL-SL - Read Plane Select
The memory plane is selected as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

Bits 7–2 Reserved = 0

Graphics Controller Mode Register (GRP_MODE) (GR5)

Read/Write Address: 3CFH, Index 05H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
	SHF-MODE		O/E	RD		WRT-MD	
= 0	256	O/E	MAP	CMP	= 0	1	0

This register controls the mode of the Graphics Controller as follows:

Bit 1–0 WRT-MD - Select Write Mode
These bits select the CPU write mode into video memory. The function of each mode is defined as follows:

00 = Write Mode 0. Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective

01 = Write Mode 1. Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective

10 = Write Mode 2. Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored

11 = Write Mode 3. Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern

Bit 2 Reserved = 0

Bit 3 RD CMP - Enable Read Compare

0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register. This is called read mode 0

1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1

Bit 4 O/E MAP - Select Odd/Even Addressing
0 = Standard addressing.
1 = Odd/even addressing mode selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU

Bit 5 SHF-MODE - Select Odd/Even Shift Mode
0 = Normal shift mode
1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes

Bit 6 SHF-MODE - Select 256 Color Shift Mode
0 = Bit 5 in this register controls operation of the video shift registers
1 = The shift registers are loaded in a manner that supports the 256 color mode

Bit 7 Reserved = 0

Memory Map Mode Control Register (MISC_GM) (GR6)

Read/Write Address: 3CFH, Index 06H
Power-On Default: Undefined

This register controls the video memory addressing.

7	6	5	4	3	2	1	0
				MEM-MAP		CHN	TXT
= 0	= 0	= 0	= 0	1	0	O/E	/GR

Bit 0 $\overline{\text{TXT}}$/GR - Select Graphics Mode
0 = Text mode display addressing selected
1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled

Bit 1 CHN O/E - Select Chain Odd/Even Planes
0 = A0 address bit unchanged
1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plane is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory

Bits 3–2 MEM-MAP - Memory Map Mode
These bits control the address mapping of video memory into the CPU address space. The bit functions are defined below.
00 = A0000H to BFFFFH (128 KBytes)
01 = A0000H to AFFFFH (64 KBytes)
10 = B0000H to B7FFFH (32 KBytes)
11 = B8000H to BFFFFH (32 KBytes)

Bits 7–4 Reserved = 0

Color Don't Care Register (CMP_DNTC) (GR7)

Read/Write Address: 3CFH, Index 07H
Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

Bits 3–0 COMPARE PLANE SEL - Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1
1 = The corresponding color plane is used for color comparison with the data in the Color Compare register

Bits 7–4 Reserved = 0

Bit Mask Register (BIT_MASK) (GR8)

Read/Write Address: 3CFH, Index 08H
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7–0 BIT MASK
A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

14.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

Attribute Controller Index Register (ATR_AD)

Read/Write Address: 3C0H
Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0–14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4–0 ATTRIBUTE ADDRESS
A binary value that points to the attribute controller register where data is to be written.

Bit 5 ENB PLT - Enable Video Display
0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU
1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0–ARF) cannot be accessed by the CPU

Bits 7–6 Reserved

Attribute Controller Data Register (ATR_DATA)

Read/Write Address: R: 3C1H/W: 3COH
Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7–0 ATTRIBUTE DATA
Data to the attribute controller register indexed by the attribute controller address.

Palette Registers (PLT_REG) (AR00-0F)

Read/Write Address: 3C1H/3C0H, Index 00H-0FH
Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
		SECONDARY			PRIMARY		
= 0	= 0	SR	SG	SB	R	G	B

Bits 5–0 PALETTE COLOR
The six bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B, respectively.

Bits 7–6 Reserved = 0

Attribute Mode Control Register (ATR_MODE) (AR10)

Read/Write
Power-On Default: 00H

Address: 3C1H/3C0H, Index 10H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MONO ATRB	TX /GR

Bit 0 $\overline{TX}$/GR - Select Graphics Mode
0 = Selects text attribute control mode
1 = Selects graphics control mode

Bit 1 MONO ATRB - Select Monochrome Attributes
0 = Selects color display text attributes
1 = Selects monochrome display text attributes

Bit 2 ENB LGC - Enable Line Graphics
0 = The ninth dot of a text character (bit 0 of SR1 = 0) is the same as the background
1 = Special line graphics character codes enabled

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking
0 = Selects the background intensity for the text attribute input
1 = Selects blink attribute in text modes

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

Bit 5 TOP PAN - Top Panning Enable
0 = Line compare has no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned

Bit 6 256 CLR - Select 256 Color Mode
0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle
1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock

Bit 7 SEL V54 - Select V[5:4]
0 = In VGA, mode, bits 5-4 of video output are generated by the attribute palette registers. Bits 7-6 of video output are always generated by bits 3-2 of AR14
1 = Bits 5-4 of video output are generated by bits 1-0 of AR14

Border Color Register (BDR_CLR) (AR11)

Read/Write
Address: 3C1H/3C0H, Index 11H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7–0 Border Color. This 8-bit register determines the border color displayed on the CRT screen. The border is an area around the screen display area.

Color Plane Enable Register (DISP_PLN) (AR12)

Read/Write
Address: 3C1H/3C0H, Index 12H
Power-On Default: 00H

This register enables the respective video memory color plane 3–0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
		VDT-SEL					
= 0	= 0	1	0	DISPLAY PLANE ENBL			

Bits 3–0 DISPLAY PLANE ENBL
A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

Bits 5–4 VDT-SEL - Video Test Select
These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7–6 Reserved = 0

Horizontal Pixel Panning Register (H_PX_PAN) (AR13)

Read/Write Address: 3C1H/3C0H, Index 13H
Power-On Default: 00H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

Bits 3–0 NUMBER OF PAN SHIFT
This register selects the number of pixels to shift the display data horizontally to the left. In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

	Number of pixels shifted in		
Bits 3–0	**9 pixel/char.**	**8 pixel/char.**	**256 color mode**
0000	1	0	0
0001	2	1	–
0010	3	2	1
0011	4	3	–
0100	5	4	2
0101	6	5	–
0110	7	6	3
0111	8	7	–
1000	0	–	–

Bits 7–4 Reserved = 0

Pixel Padding Register (PX_PADD) (AR14)

Read/Write
Power-On Default: 00H

Address: 3C1H/3C0H, Index 14H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
				PIXEL PADDING			
= 0	= 0	= 0	= 0	V7	V6	V5	V4

Bits 1–0 PIXEL PADDING V5, V4
These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3–2 PIXEL PADDING V7, V6
In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7–4 Reserved = 0

14.6 SETUP REGISTERS

This section describes the Video Subsystem Setup registers on the system board.

The I/O functions of the system board use POS information during the setup procedure. The I/O controllers on the system board are treated as a single device. Although the VGA is a part of the system board, POS treats it as a separate device. The Setup Enable register is used to place the system board or the Video Subsystem into setup. The Setup Enable register is read/write at I/O address 46E8H. The bit definitions are provided below.

Setup Option Select Register (SETUP_MD)

Read/Write Address: 102H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	SLP MODE

Bit 0 SLP MODE- Disable Sleep Mode
When in setup mode (I/O address 46E8H, bit 4 =1, the Vision964 responds to a single option select byte at I/O address 102H and treats this bit as the Video Subsystem sleep bit.
0 = Vision964 does not respond to commands, addresses, or data on the data bus. If the Vision964 was set up and is generating video output when this bit is cleared to 0, the output is still generated
1 = Vision964 responds to commands, addresses, or data on the data bus

The Vision964 responds only to address 102H when in the setup mode. No other addresses are valid at that time. The Vision964 ignores address 102H when in the enabled mode (I/O address 46E8H, bit 4 = 0, and decodes normal I/O and memory addresses.

If bit 2 of CR65 is set to 1, 3C3H is the address used for setup instead of 46E8H.

Bit 7–1 Reserved

Video Subsystem Enable Register (SETUP_MD)

Write Only Address: 46E8H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	EN SUP	AD DEC	R	R	R

Bits 2–0 Reserved

Bit 3 AD DEC - Vision964 Address Decoding
0 = Video I/O and memory address decoding are disabled
1 = Video I/O and memory address decoders are enabled

Bit 4 EN SUP - Enable Vision964 Setup
0 = The Vision964 is in operational mode
1 = The Vision964 is placed in setup mode

If bit 2 of CR65 is set to 1, 3C3H is the address used for setup instead of 46E8H.

Bits 7–5 Reserved

14.7 RAMDAC REGISTERS

Of all the RAMDAC registers described in this section, only the DAC Status Register (3C7H, Read Only) is physically located inside the Vision964. The others are located in the RAMDAC. The Vision964 decodes these addresses for RAMDAC data byte steering.

DAC Mask Register (DAC_AD_MK)

Read/Write Address: 3C6H
Power-On Default: Undefined

This register is the pixel read mask register to select pixel video output. The CPU can access this register at any time. An access to this register causes 10b to be driven to the RS[1:0] outputs to the RAMDAC.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7–0 DAC ADDRESS MASK
The contents of this register are bit-wise logically ANDed with the pixel select video output (PA[7:0]). This register is initialized to FFH by the BIOS during a video mode set.

DAC Read Index Register (DAC_RD_AD)

Write Only Address: 3C7H
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette. A write to this register causes 11b to be driven to the RS[1:0] outputs to the RAMDAC.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7–0 DAC READ ADDRESS
Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the RAMDAC data register at I/O address 3C9H. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (RAMDAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the RAMDAC data register at address 3C9H.
3. Three bytes are read back from the RAMDAC data register.
4. The contents of this register auto-increment by one.
5. Go to step 2.

The effects of writing to the RAMDAC data register during a three-byte read cycle or reading from the RAMDAC data register during a three-byte write cycle (i.e., interrupting the sequence) are undefined and may change the look-up table contents.

DAC Status Register (DAC_STS)

Read Only Address: 3C7H
Power-On Default: Undefined

A read of this register causes 11b to be driven to the RS[1:0] outputs to the RAMDAC.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1–0 DAC-STS - RAMDAC Cycle Status
The last executing cycle was:
00 = Write Palette cycle
11 = Read Palette cycle

Reads from the RAMDAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7–2 Reserved = 0

DAC Write Index Register (DAC_WR_AD)

Read/Write Address: 3C8H
Power-On Default: Undefined

An access to this register causes 00b to be driven to the RS[1:0] outputs to the RAMDAC.

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS/GIP READ DATA							

Bits 7–0 DAC WRITE ADDRESS/GIP READ DATA
This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. For 18-bit DACs, the least significant 6 bits of each byte are concatenated to form the value placed in the 18-bit data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.
3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.

If bit 2 of the Extended RAMDAC Control register (CR55) is set to 1 to enable the General I/O Port read function, a read of 3C8H retrieves data from an external input buffer.

RAMDAC Data Register (DAC_DATA)

Read/Write Address: 3C9H
Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers. An access to this register causes 01b to be driven to the RS[1:0] outputs to the RAMDAC.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7–0 DAC READ/WRITE DATA
To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the BLANK input to the RAMDAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking the Input Status 1 register to determine when retrace is occurring, or by using the screen-off bit in the Clocking Mode register of the sequencer.

Section 15: S3 VGA Register Descriptions

The Vision964 has additional registers to extend the functions of basic VGA. These registers are located in CRT Controller address space at locations not used by the IBM® VGA. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a changed key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by altering a significant bit.

In the following register descriptions, 'R' stands for reserved (write =0, read = undefined). See Appendix A for a table listing each register in this section and its page number.

Chip ID/REV Register (CHIP-ID/REV) (CR30)

Read Only Address: 3?5H, Index 30H
Power-On Default: DxH (x will change with the stepping)

7	6	5	4	3	2	1	0
CHIP ID				REVISION STATUS			

Bits 7–0 CHIP ID AND REVISION STATUS

Memory Configuration Register (MEM_CNFG) (CR31)

Read/Write Address: 3?5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HST DFF	OLD-DSAD 17	16	ENH MAP	VGA 16B	SCRN 2.PG	CPUA BASE

Bit 0 CPUA BASE - Enable Base Address Offset
0 = Address offset bits 3-0 of CR35 and bits 3-2 of the CR51 or the new address offset bits (6-0 of CR6A) are disabled
1 = Address offset bits 3-0 CR35 and bits 3-2 of CR51 or the new address offset bits (6-0 of CR6A) are enabled for specifying the 64K page of display memory. This allows access to up to 8 MBytes of display memory through a 64K window.

Bit 1 SCRN 2.PG - Enable Two-Page Screen Image
0 = Normal Mode
1 = Enable 2K x 1K x 4 map image screen for 1024 × 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution

Bit 2 VGA 16B - Enable VGA 16-bit Memory Bus Width
0 = 8-bit memory bus operation
1 = Enable 16-bit bus VGA memory read/writes

Bit 3 ENH MAP - Use Enhanced Mode Memory Mapping
0 = Force IBM VGA mapping for memory accesses
1 = Force Enhanced Mode mappings

Setting this bit to 1 overrides the settings of bit 6 of CR14 and bit 3 of CR17 and causes the use of doubleword memory addressing mode.

Bits 5–4 OLD-DSAD 17, 16 - Old Display Start Address Bits 17-16
Bits 17-16 of start address (CRC, CRD) and cursor location (CRE, CRF)

Bits 1-0 of CR51 are bits 19-18 of the address and enable access to up to 4 MBytes of display memory. If a value is programmed into bits 4-0 of the Extended System Control 3 register (CR69), this value becomes the upper 5 bits of the display start base address, enabling access to up to 8 MBytes of display memory, and bits 5-4 of CR31 and bits 1-0 of CR51 are ignored.

Bit 6 HST DFF - Enable High Speed Text Display Font Fetch Mode
0 = Normal font access mode
1 = Enable high speed text display

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz.

Bit 7 Reserved

Backward Compatibility 1 Register (BKWD_1) (CR32)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 32H

7	6	5	4	3	2	1	0
SRO-TRI	VGA FXPG	(R)	ENB VIRQ	BKWD MODE	FCHI CHCK	CH-CLK 1	0

Bits 1–0 CH-CLK - Set Character Clock Period
00 = Same as IBM VGA (8 or 9 dot clocks, as set via bit 0 of SR1)
01 = 7 dots (overrides 00 setting)
10 = 9 dots (overrides 00 setting)
11 = Reserved

This is used only for non-standard modes (not VGA or backwards compatible).

Bit 2 FCHI CHCK - Force Character Clock High
0 = Normal character clock
1 = Force character clock of horizontal timing to high rate (not 1/2 dot clock rate) for CGA and HGC emulations.

Bit 3 BKWD MODE - Enable Backward Compatibility Modes
0 = VGA
1 = All other backward compatibility modes

Bits 5-4 Reserved

Bit 6 VGA FXPG - Use Standard VGA Memory Wrapping
0 = Memory accesses extending past a 256K boundary do not wrap
1 = Memory accesses extending past a 256K boundary wrap at the boundary

The standard 256K VGA memory page always ends on a natural 256K boundary and accesses beyond this boundary will wrap. If the starting address is moved via bits 4-0 of CR69 (or bits 5-4 of CR31 and bits 1-0 of CR51), the 256K page may not end on a 256K boundary and accesses past the boundary will not wrap. This is the case when this bit is cleared to 0. For standard VGA compatibility when the page base address is moved, this bit is set to 1 to cause wrapping at a 256K boundary.

Bit 7 SRO-TRI Serial Out Tri-State Enable
0 = Serial Out tri-state disabled
1 = SC[1:0], $\overline{\text{SE}}$[3:0] pins are tri-stated

This can be used to allow another controller to share control of the VRAM serial port.

Backward Compatibility 2 Register (BKWD_2) (CR33)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 33H

7	6	5	4	3	2	1	0
DISA FLKR	LOCK PLTW	BDR SEL	LOCK DACW	VCLK= -DCK	R	DIS VDE	R

Bit 0 Reserved

Bit 1 DIS VDE - Disable Vertical Display End Extension Bits Write Protection
0 = VDE protection enabled
1 = Disables the write protect setting of the bit 7 of CR11 on bits 1 and 6 of CR7.

Bit 2 Reserved

Bit 3 VCLK = -DCK - VCLK is Inverted DCLK
0 = VCLK is the inverted internal dot clock (see bit 3 of SR1)
1 = VCLK is the inverted DCLK

Bit 4 LOCK DACW - Lock RAMDAC Writes
0 = Enable writes to RAMDAC registers
1 = Disable writes to RAMDAC registers

Bit 5 BDR SEL - Blank/Border Select
0 = $\overline{\text{BLANK}}$ active time is defined by CR2 and CR3
1 = $\overline{\text{BLANK}}$ is active during entire display inactive period (no border)

Bit 6 LOCK PLTW - Lock Palette/Border Color Registers
0 = Unlock Palette/Border Color registers
1 = Lock Palette/Border Color registers

Bit 7 DISA FLKR - Remove Flicker
0 = No effect
1 = Overrides the 3D8H video enable (bit 3). This eliminates flicker (CGA snow).

Backward Compatibility 3 Register (BKWD_3) (CR34)

Read/Write Address: 3?5H, Index 34H
Power-On Default: 00H

7	6	5	4	3	2	1	0
LOCK CKSL	R	LOCK 8/9D	ENB DTPC	R	R	R	R

Bits 3–0 Reserved

Bit 4 ENB DTPC - Enable Data Transfer Position Control
0 = Data transfer position defined by Horizontal Total Position (CR0) register
1 = Data transfer position defined by Data Transfer Execute Position register (CR3B)

This bit selects which registers define the timing of transfers of pixel data from the DRAM side of the VRAM to the serial output side.

Bit 5 LOCK 8/9D - Lock 8/9 Dots
0 = Bit 0 of the Clocking Mode register (SR1) is unlocked
1 = Bit 0 of the Clocking Mode register (SR1) is locked

When emulating EGA hardware, horizontal timing registers are programmed for an 8 dot character clock period (bit 0 of SR1) and these registers are locked. This prevents EGA software from modifying this bit. Writes to bits 1-0 of CR32 override this setting.

Bit 6 Reserved

Bit 7 LOCK CKSL - Lock Clock Select
0 = Bits 3-2 of the Miscellaneous Output register (3C2H) are unlocked
1 = Bits 3-2 of the Miscellaneous Output register (3C2H) are locked. This locks the DCLK frequency to a fixed value in VGA and backwards compatibility modes. If 11b is programmed in bits 3-2 of 3C2H, the DCLK frequency can still be changed via bits 3-0 of CR42.

CRT Register Lock Register (CRTR_LOCK) (CR35)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 35H

7	6	5	4	3	2	1	0
		LOCK	LOCK	OLD-CPU-BASE-ADDRESS			
R	R	HTMG	VTMG	17	16	15	14

Bits 3–0 OLD-CPU-BASE-ADDRESS
CPU Base Address bits 17-14. These four bits define the CPU address base in 64 KByte units of display memory. These bits are added with CPU address bit 17 (MSB of video memory addressing) to bit 14 for display buffer accesses.

Bits 3-2 of the Extended System Control 2 register (CR51) are bits 19-18 of the address and enable access to up to 4 MBytes of display memory. If a value is programmed into bits 6-0 of the Extended System Control 4 register (CR6A), this value becomes the upper 7 bits of the CPU base address, enabling access to up to 8 MBytes of display memory, and bits 3-0 of CR35 and bits 3-2 of CR51 are ignored.

Bit 4 LOCK VTMG - Lock Vertical Timing Registers
0 = Vertical timing registers are unlocked
1 = The following vertical timing registers are locked:

CR6
CR7 (bits 7,5,3,2,0)
CR9 (bit 5)
CR10
CR11 (bits 3-0)
CR15
CR16

CR6, CR7 registers are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers
0 = Horizontal timing registers are unlocked
1 = The following horizontal timing registers are locked:

CR0
CR1
CR2
CR3

CR4
CR5
CR17 (bit 2)

All these registers (except bit 2 of CR17) are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 7-6 Reserved

Configuration 1 Register (CONFG_REG1) (CR36)

Read/Write* Address: 3?5H, Indices 36H
Power-On Default: Depends on Strapping

* Bits 1-0 are read only. The other bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [7:0]. Other configuration strapping bits are found in CR37 and CR68.

PD Bits	CR 36 Bits	Value	Function
	System Bus Select		
1-0	1-0	00	Reserved
		01	VESA local bus
		10	PCI local bus
		11	Reserved
	Memory Page Mode Select		
3-2	3-2	00	Reserved
		01	Reserved
		10	Extended Data Out (EDO) Mode
		11	Fast Page Mode
	Enable Video BIOS Accesses (VL-Bus)		
4	4	0	Disable video BIOS accesses
		1	Enable video BIOS accesses
	Display Memory Size		
7-5	7-5	000	4 MBytes
		001	Reserved
		010	3 MBytes
		011	8 MBytes
		100	2 MBytes
		101	6 MBytes
		110	1 MByte
		111	Reserved

Configuration 2 Register (CONFG_REG2) (CR37)

Read/Write* Address: 3?5H, Indices 37H
Power-On Default: Depends on Strapping

* These bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [15:7]. Other configuration strapping bits are found in CR36 and CR68.

PD Bits	CR37 Bits	Value	Function
	Setup Select (VL-Bus)		
8	0	0	Disable Vision964 except for video BIOS accesses
		1	Enable Vision964
	Test Mode		
9	1	0	Test mode enabled (all outputs tri-stated)
		1	Test mode disabled (normal operation)
	Video BIOS ROM Size (VL-Bus)		
10	2	0	64-KByte BIOS ROM
		1	32-KByte BIOS ROM
	Dual $\overline{CAS}$ Select		
11	3	0	Dual $\overline{WE}$ byte select
		1	Dual $\overline{CAS}$ byte select
	RAMDAC Write Snooping (VL-Bus)		
12	4	0	Disable $\overline{LOCA}/\overline{SRDY}$ for RAMDAC writes
		1	Enable $\overline{LOCA}/\overline{SRDY}$ for RAMDAC writes
	Monitor Type Identification		
15-13	7-5		The S3 BIOS uses these three bits to determine monitor information.

Register Lock 1 Register (REG_LOCK1) (CR38)

Read/Write Address: 3?5H, Index 38
Power-On Default: 00H

Loading 01xx10xx (e.g., 48H) into this register unlocks the S3 VGA register set for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

Register Lock 2 Register (REG_LOCK2) (CR39)

Read/Write Address: 3?5H, Index 39
Power-On Default: 00H

Loading 101xxxxx (e.g., A0H) unlocks the system control and system extension registers for reading/writing (x = don't care). Loading 0A5H allows bits 7-2 of CR36, bits 7-0 of CR37 and bits 7-0 of CR68 to be written.

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

Miscellaneous 1 Register (MISC_1) (CR3A)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 3AH

7	6	5	4	3	2	1	0
PCIRB DISA	R	HST DFW	ENH 256	TOP MEM	ENB RFC	REF-CNT 1	0

Bits 1–0 REF-CNT - Alternate Refresh Count Control
00 = Refresh Count 0
01 = Refresh Count 1
10 = Refresh Count 2
11 = Refresh Count 3

If enabled by setting bit 2 of this register to 1, these bits override the refresh count in bit 6 of CR11 and specify the number of refresh cycles per horizontal line.

Bit 2 ENB RFC - Enable Alternate Refresh Count Control
0 = Alternate refresh count control (bits 1-0 of this register) is disabled
1 = Alternate refresh count control (bits 1-0 of this register) is enabled

Bit 3 TOP MEM - Enable Top of Memory Access
0 = Top of memory access disabled
1 = Simultaneous VGA text and Enhanced modes are enabled. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Bit 4 ENH 256 - Enable 8 Bits/Pixel or Greater Color for Enhanced Mode
0 = Attribute controller shift registers configured for 4-bit modes
1 = Attribute controller shift register configured for 8-, 16- and 24/32-bit color Enhanced modes

Bit 5 HST DFW - Enable High Speed Text Font Writing
0 = Disable high speed text font writing
1 = Enable high speed text font writing

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz.

Bit 6 Reserved

Bit 7 PCIRB DISA - PCI Read Bursts Disabled
0 = PCI read burst cycles enabled
1 = PCI read burst cycles disabled

Bit 7 of CR66 must be set to 1 before this bit is set to 1.

Data Transfer Execute Position Register (DT_EX_POS) (CR3B)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 3BH

The Data Transfer Execute Position is a 9-bit value that specifies horizontal position in character clocks of the start of the VRAM read data transfer cycle. The recommended value is halfway between the horizontal total (CR0) and the start horizontal sync position (CR4). Bit 6 of CR5D is bit 8 of this field. This register is enabled by bit 4 of CR34.

7	6	5	4	3	2	1	0
DATA TRANSFER EXECUTE POSITION							

Bits 7–0 DATA TRANSFER EXECUTE POSITION.
9-bit Value = the horizontal position in character clocks of the start of the VRAM read data transfer cycle. This register contains the least significant 8 bits of this value.

Interlace Retrace Start Register (IL_RTSTART) (CR3C)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 3CH

This value allows determination of the even/odd row active display starting positions when operating in an interlaced mode. This register is enabled by bit 5 of CR42.

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7–0 INTERLACE RETRACE START POSITION
Value = offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

Section 16: System Control Register Descriptions

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by changing a significant bit.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

System Configuration Register (SYS_CNFG) (CR40)

Read/Write Address: 3?5H, Index 40H
Power-On Default: 10H

7	6	5	4	3	2	1	0
BUS TNO 1	BUS TNO 0	WDL DLAY	RDY CTL	R	R	R	EN ENH

Bit 0 EN ENH - Enable Enhanced Register Access
0 = Enhanced register access disabled
1 = Enhanced register (x2E8H) access enabled

Bits 3–1 Reserved

Bits 4 RDY CTL- Ready Control (VL-Bus only)
0 = Minimum 0 wait state delay from $\overline{SADS}$ asserted to assertion of $\overline{SRDY}$ (for writes to the command FIFO). Bit 3 of CR58 must be set to 1 for this mode.
1 = Minimum 1 wait state delay from $\overline{SADS}$ asserted to assertion of $\overline{SRDY}$ (for writes to the command FIFO)(Default)

Bit 5 WDL DLAY - Write Latching Delay (VL-Bus only)
0 = Latch write data on the first rising edge of SCLK after the assertion of $\overline{RDYIN}$ (Default)
1 = Latch write data on the first rising edge of SCLK after the assertion of $\overline{SRDY}$

Bits 7–6 BUS TNO- Bus Turnaround Non-Overlap (VL-Bus only)
00 = $\overline{\text{ABEN}}$ - $\overline{\text{DBEN}}$ non-overlap delay = 1 unit
01 = $\overline{\text{ABEN}}$ - $\overline{\text{DBEN}}$ non-overlap delay = 2 units
10 = $\overline{\text{ABEN}}$ - $\overline{\text{DBEN}}$ non-overlap delay = 3 units
11 = $\overline{\text{ABEN}}$ - $\overline{\text{DBEN}}$ non-overlap delay = 4 units

These bits control the gap between the deassertion of $\overline{\text{ABEN}}$ and the assertion of $\overline{\text{DBEN}}$ and vice versa. This action switches the multiplexed AD[31:0] bus function from address to data.

BIOS Flag Register (BIOS_FLAG) (CR41)

Read/Write Address: 3?5H, Index 41H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BIOS-FLAG-REGISTER-1							

Bits 7–0 BIOS-FLAG-REGISTER-1
Used by the video BIOS. Users should not write to this register.

Mode Control Register (MODE_CTL) (CR42)

Read/Write Address: 3?5H, Index 42H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	INTL MODE	R	DOT-CLOCK-SELECT			

Bits 3–0 DOT-CLOCK-SELECT
These bits are effective when 11b is programmed in bits 3-2 of the Miscellaneous Output register (3C2H) and are strobed on GD[3:0] by the STWR signal. The bit coding is dependent on the clock generator capabilities.

Bit 4 Reserved

Bit 5 INTL MODE - Interlaced Mode
0 = Noninterlaced
1 = Interlaced

This bit enables CR3C.

Bits 7–6 Reserved

Extended Mode Register (EXT_MODE) (CR43)

Read/Write Address: 3?5H, Index 43H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HCTR X2	R	R	R	R	OLD LSW8	OLD RS2	VCLK EDG

Bit 0 VCLK EDG - Video Clock Edge Mode Select
0 = PA[7:0] values change every VCLK rising edge
1 = PA[7:0] values change every VCLK rising and falling edge (15/16 bits/pixel only)

Bit 1 OLD RS2 - DAC Register Select Bit 2
This is an extension bit of RS[1:0] for RAMDAC addressing. This is disabled if bits 1-0 of the Extended Video DAC Control register (CR55) are not 00b.

Bit 2 OLD LSW8 - Logical Screen Width Bit 8
This is an extension of the Offset (Screen Width) register (CR13). This is disabled if bits 5-4 of the Extended System Control 2 register (CR51) are not 00b.

Bits 6–3 Reserved

Bit 7 HCTR X2 - Horizontal Counter Double Mode
0 = Disable horizontal counter double mode
1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

Hardware Graphics Cursor Mode Register (HGC_MODE) (CR45)

Read/Write Address: 3?5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	BT485	HWGC 1280	HWC-CSEL 1	0	R	HWGC ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable
0 = Hardware graphics cursor disabled in any mode
1 = Hardware graphics cursor enabled in Enhanced mode

The hardware graphics cursor requires the use of the pixel address bus. However this bus is not used for Enhanced mode operation since pixel data is transferred via the VRAM SID lines. Therefore, the hardware graphics cursor will normally not be used with the Vision964.

Bit 1 Reserved

Bits 3-2 HWC-CSEL - Hardware Cursor Color Select
00 = Cursor colors are 4/8 bits/pixel (CRE and CRF define the colors)
01 = Cursor colors are 16 bits/pixel (CR4A and CR4B define the colors
10 = Cursor colors are 24 bits/pixel (CR4A and CR4B define the colors
11 = Cursor colors are 32 bits/pixel (CR4A and CR4B define the colors

These bits must match the pixel length settings in bits 5-4 of CR50

Bit 4 HWGC 1280 - Hardware Cursor Right Storage
0 = Function disabled
1 = For 4 bits/pixel, the last 256 bytes in each 1-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. For 8 bits/pixel, the last 512 bytes in each 2-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. In either case, bits 1-0 of CR4D must be 11b

Bit 5 BT485 - ODF Selection for Bt485A RAMDAC
0 = Pin 185 serves as the RS3 output
1 = Pin 185 serves as the ODF output to a Bt485A-compatible RAMDAC

The ODF (odd frame) function controls the timing of the cursor for interlaced modes when using Bt485A-compatible RAMDACs. This signal is low for an even field and high for an odd field. Pin 185 should be connected to the ODF pin of the RAMDAC through an external inverter.

Bits 7–6 Reserved

Hardware Graphics Cursor Origin-X Registers (HWGC_ ORGX(H)(L)) (CR46, CR47)

Read/Write Address: 3?5H, Index 46H, 47H
Power-On Default: 0000H

The high order three bits are written into CR46 and the low order byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10–0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15–11 Reserved

Hardware Graphics Cursor Origin-Y Registers (HWGC_ORGY(H)(L)) (CR48, CR49)

Read/Write Address: 3?5H, Index 48H, 49H
Power-On Default: Undefined

The high order three bits are written into CR48 and the low order byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10–0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line
The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15–11 Reserved

Hardware Graphics Cursor Foreground Color Stack Register (HWGC_FGSTK) (CR4A)

Read/Write Address: 3?5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-3)							

Bits 7–0 TRUE COLOR FOREGROUND STACK (0-3)

Four foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1, so four writes provide 32 bits of true color information. These registers are selectively enabled by bits 3-2 of CR45.

Hardware Graphics Cursor Background Color Stack Register (HWGC_BGSTK) (CR4B)

Read/Write Address: 3?5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-3)							

Bits 7–0 TRUE COLOR BACKGROUND STACK (0-3)

Four background color registers are stacked at this address. The stack pointer (common with CR4A) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1, so four writes provide 32 bits of true color information. These registers are selectively enabled by bits 3-2 of CR45.

Hardware Graphics Cursor Storage Start Address Registers (HWGC_STA(H)(L) (CR4C, CR4D)

Read/Write Address: 3?5H, Index 4CH, 4DH
Power-On Default: Undefined

The high order five bits are written into CR4C and the low order byte is written into CR4D.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	HWGC STA(H)					HWGC STA(L)							

Bits 11–0 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address

Bits 15–12 Reserved

Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (HWGC_DX) (CR4E)

Read/Write Address: 3?5H, Index 4EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5–0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position

This value is the offset (in pixels) from the left side of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the left screen border.

Bits 7–6 Reserved

Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (HGC_DY) (CR4F)

Read/Write Address: 3?5H, Index 4FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5–0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

This value is the offset (in pixels) from the top of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the top of the display.

Bits 7–6 Reserved

Section 17: System Extension Register Descriptions

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39).

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Extended System Cont 1 Register (EX_SCTL_1) (CR50)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 50H

7	6	5	4	3	2	1	0
GE-SCR-W 1	0	PXL-LNGH 1	0	R	ENB BREQ	R	GESW 2

Bit 0 Extension bit 2 of the screen width definition. See bits 7-6 below.

Bit 1 Reserved

Bit 2 ENB $\overline{\text{BREQ}}$ - Enable $\overline{\text{BREQ}}$ Function
0 = $\overline{\text{BREQ}}$, $\overline{\text{BGNT}}$ functions disabled
1 = $\overline{\text{BREQ}}$, $\overline{\text{BGNT}}$ functions enabled

Bit 3 Reserved

Bits 5–4 PXL-LNGH - Pixel Length Select
00 = 1 byte (Default). This corresponds to a pixel length of 4 or 8 bits/pixel in bit 7 of the Subsystem Status register (42E8H)
01 = 2 bytes. 16 bits/pixel
10 = Reserved
11 = 4 bytes. 32 bits/pixel

These bits select the pixel length for Enhanced mode command execution through the Graphics Engine.

Bits 7–6 GE-SCR-W - Graphics Engine Command Screen Pixel Width
Bit 0 of this register is the most significant bit of this definition.
000 = 1024 (or 2048 if bit 1 of CR31 =1) (Default)
001 = 640
010 = 800 (or 1600x1200x4 if bit 2 of 4AE8H = 1)
011 = 1280
100 = 1152
101 = Reserved
110 = 1600
111 = Reserved

Extended System Control 2 Register (EX_SCTL_2) (CR51)

Read/Write Address: 3?5H, Index 51H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	DIS SPXF	LOG-SCR-W 9	8	OLD-CBAD 19	18	OLD-DSAD 19	18

Bits 1–0 OLD-DSAD - Old Display Start Address Bits 19-18
These are extension bits of Memory Configuration register (CR31) bits 5-4 (Display Start Base Address). If the upper 5 display start address bits are programmed into bits 4-0 of CR69, these bits and bits 5-4 of CR31 are ignored.

Bits 3–2 OLD-CBAD - Old CPU Base Address Bits 19-18
These are extension bits of CRT Register Lock register (CR35) bits 3-0 (CPU Base Address). They becomes bits 19-18 of the CPU base address, enabling access to up to 4 MBytes of display memory. If the upper 7 CPU base address bits are programmed into bits 6-0 of CR6A, these bits and bits 3-0 of CR35 are ignored. Using CR6A enables access to up to 8 MBytes of display memory.

Bits 5–4 LOG-SCR-W - Logical Screen Width Bits 9-8
These are two extension bits of the Offset register (CR13). If the value of these bits is not 00b, bit 2 of the Extended Mode register (CR43) is disabled.

Bit 6 DIS SPXF - Disable Split Transfer
0 = Split VRAM transfers enabled
1 = Split VRAM transfers disabled

Split VRAM transfers (half the data in one SAM is transferred from the DRAM side to the serial out side while the other half is output to the RAMDAC) are required in all Vision964 Enhanced modes (bit 0 of 4AE8H set to 1). They are not required for VGA modes, but can be left enabled for these modes.

Bit 7 Reserved

Extended BIOS Flag 1 Register (EXT_BBFLG1) (CR52)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 52H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-1							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-1

See the S3 video BIOS documentation for the coding of this register. Note that this coding is different from that used with previous S3 accelerators.

Extended Memory Control 1 Register (EX_MCTL_1) (CR53)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 53H

7	6	5	4	3	2	1	0
ENB NBLW	SWP NBL	PAR VRAM	ENB MMIO	R	R	R	ENB WPB

Bit 0 ENB WPB - Enable Write Per Bit
0 = Disable Write Per Bit for all memory banks
1 = Enable Write Per Bit for all memory banks

Bits 3–1 Reserved

Bit 4 ENB MMIO - Enable MMIO Access
0 = Disable (Default)
1 = Enable Memory-Mapped I/O

The first 32-KByte MMIO area (A0000H-A7FFFH) is used for image transfers via E2E8H and E2EAH. The second 32-KByte MMIO area (A8000H-AFFFFH) is used for the Enhanced command registers (from 82E8H to BEE8H).

Bit 5 PAR VRAM - Parallel VRAM addressing
0 = Serial VRAM addressing mode
1 = Parallel VRAM addressing mode

This bit needs to be set to 1 to enable parallel addressing only when a 64-bit interleaved SID bus design is used (bits 5-4 of CR66 = 10b).

Bit 6 SWP NBL - Swap Nibbles
0 = No nibble swap
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7 Reserved

Extended Memory Control 2 Register (EX_MCTL_2) (CR54)

Read/Write Address: 3?5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
M PARAMETER					R	R	R

Bits 2–0 Reserved

Bits 7–3 M PARAMETER
5-bit Value = (number of 8-byte memory access cycles available for purposes other than filling the display FIFO) -1. This parameter should be maximized within the constraint that a display FIFO underrun is not allowed. See Section 9.4, Display Memory Access Control, for more information.

Extended RAMDAC Control Register (EX_DAC_CT) (CR55)

Read/Write Address: 3?5H, Index 55H
Power-On Default: 00H

7	6	5	4	3	2	1	0
TOFF VCLK	R	R	MS /X11	R	ENB GIR	DAC-R-SEL 3	2

Bits 1–0 DAC-R-SEL - DAC Register Select Bits 3-2
These are two extension bits of the RS[1:0] signals for RAMDAC addressing. If the value of these bits is not zero, bit 1 of the Extended Mode register (CR43) is disabled.

Bit 2 ENB GIR - Enable General Input Port Read
0 = RAMDAC reads enabled
1 = RAMDAC reads disabled. The $\overline{\text{RMSTRD}}$ and RS2 strobes for reading the General Input Port data are enabled

Bit 3 Reserved

Bit 4 MS/X11 - Hardware Cursor MS/X11 Mode
0 = MS-Windows mode (Default)
1 = X11-Windows mode

This bit select the type of decoding used for the 64x64x2 storage array of the hardware graphics cursor. See the Programming the Hardware Cursor section for a description of the decoding.

Bits 6–5 Reserved

Bit 7 TOFF VCLK - Tri-State Off VCLK Output
0 = Normal operation
1 = VCLK output is tri-stated off

External Sync Control 1 Register (EX_SYNC_1) (CR56)

Read/Write Address: 3?5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	TOFF SYNC	PRST ODDF	ESYN R/V	R	R	RMT ON

Bit 0 RMT ON - Remote Mode Operation
0 = Remote Mode operation off
1 = Remote Mode operation on. The VSYNC pin becomes the input for genlocking.

Bits 2-1 Reserved

Bit 3 ESYN R/V - External Sync Vertical Counter Reset Select
0 = Horizontal/Vertical counter reset sync (Default)
1 = Vertical counter-only reset sync with genlocking

If bit 0 (Remote Mode) is set to 1, the falling edge of the VSYNC input signal resets the vertical counter (every other frame in the interlaced mode) or both the horizontal and vertical counters.

Bit 4 PRST ODDF - Preset Frame Select (-EVEN/ODD)
0 = Start with the Even Frame after a V-counter reset (Default)
1 = Start with the Odd Frame after a V-counter reset

This bit is effective only when bit 3 = 1 with remote mode on (bit 0 = 1).

Bit 5 TOFF SYNC - Tri-State Off Sync Outputs
0 = Normal operation
1 = HSYNC, VSYNC, and $\overline{\text{BLANK}}$ become tri-state off outputs

Bits 7–6 Reserved.

External Sync Control 2 Register (EX_SYNC_2) (CR57)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 57H

7	6	5	4	3	2	1	0
HSYN-RESET-ADJUST				VSYN-RESET-ADJUST			
3	2	1	0	3	2	1	0

Bits 3–0 VSYN-RESET-ADJUST
This specifies the vertical delay line number of the V-counter reset from the falling edge of VSYNC. The set value must be not equal zero in Remote mode (bit 0 of CR56 = 1).

Bits 7–4 HSYN-RESET-ADJUST
This specifies the horizontal delay character number of the H-counter reset from the falling edge of VSYNC after VSYNC Reset Adjust.

Linear Address Window Control Register (LAW_CTL) (CR58)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 58H

7	6	5	4	3	2	1	0
R	SAM 256	R	ENB LA	LAT DEL	R	LAW-SIZE 1	0

Bits 1–0 LAW-SIZE - Linear Address Window Size
00 = 64 KBytes (Default)
01 = 1 MByte
10 = 2 MBytes
11 = 8 MBytes

Programmers should set these bits to 11b for a 4-MByte memory configuration and be aware that the second 4-MByte region of enabled address space is not backed with real memory.

Bit 2 Reserved

Bit 3 LAT DEL - Address Latch Delay Control (VL-Bus only)
0 = Address latching is delayed one clock (T2 cycle)
1 = Address latching occurs in the T1 cycle

This bit is effective only when one decode wait state is selected by setting bit 4 of CR40 to 1.

Bit 4 ENB LA - Enable Linear Addressing
0 = Disable linear addressing (Default)
1 = Enable linear addressing

Enabling linear addressing disables access to the A000H-AFFFH region unless banking is enabled via bit 0 of CR31, the window size is set to 64K via bits 1-0 of this register and A000H is specified as the base in CR59-5A.

Bit 5 Reserved

Bit 6 SAM 256 - Serial Access Mode 256 Words Control
0 = SAM control is 512 words
1 = SAM control is 256 words

This setting is VRAM-dependent. A setting of 1 always works. If the VRAM can support a setting of 0, this can enhance performance.

Bit 7 Reserved

Linear Address Window Position Registers (LAW_POS(X) (CR59-5A)

Read/Write Address: 3?5H, Index 59H-5AH
Power-On Default: 000AH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINEAR-ADDRESS-WINDOW-POSITION															

CR59 contains the upper byte (15-8) and CR5A contains the lower byte (7-0). These registers specify the Linear Address Window Position in 32-bit CPU address space. The Linear Address Window resides on a 64KB, 1MB, 2MB or 8MB memory boundary (size-aligned boundary). Some LSBs of this register (illustrated by "xx..xx" in the following table) are ignored because of the size-aligned boundary scheme.

LAW Size	Linear Address Window Position Register Bit(s)									
64KB	31-25	24	23	22	21	20	19	18	17	16
1MB	31-25	24	23	22	21	20	xx	xx	xx	xx
2MB	31-25	24	23	22	21	xx	xx	xx	xx	xx
8MB	31-25	24	23	xx	xx	xx	xx	xx	xx	xx

Bits 15–0 LINEAR-ADDRESS-WINDOW-POSITION - LA Window Position Bits 31-16
16-bit Value = the linear address window position in 32-bit CPU address space.

Bits 31-23 are common with bits 31-23 of the base address programmed into the PCI Base Address 0 register at address 10H-12H. Writes to these bits in either register will also be written to the other. In general, the bits should be programmed via the PCI configuration register. Writes to CR59 and CR5A should be read-modify- writes that do not change bits 31-23.

If a 64K window is specified and bit 0 of CR31 is set to 1, bits 5-0 of CR6A specify the 64K page of display memory to be accessed through a 64K window located at the address specified in these registers.

Extended BIOS Flag 2 Register (EXT_BFLG2) (CR5B)

Read/Write Address: 3?5H, Index 5BH
Power-On Default: 00H

15	14	13	12	11	10	9	8
EXT-BIOS-FLAG-REGISTER-2							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-2
Used by the BIOS.

General Output Port Register (GOUT_PORT) (CR5C)

Read/Write: See Bit Descriptions Address: 3?5H, Index 5CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
GENERAL-OUT-PORT				CLOCK-SELECT-OUT			

Bits 3–0 CLOCK-SELECT-OUT (Read Only)
The value stored in these bits is determined as shown in the following table. The bit values are driven on GD[3:0] when CR42 bits 3-0, 3C2H bits 3-2 or this register (bits 7-4) are written to and are strobed into the clock generator by STWR.

3C2H, Bits 3-2	CLOCK-SELECT-OUT
00	0000
01	0001
10	0010
11	Content of CR42 [3:0]

Bits 7–4 GENERAL-OUT-PORT (Read/Write)
These bits are user definable. They are driven on GD[7:4] when written and also when CR42 bits 3-0 or 3C2H bits 3-2 are written and are strobed into an external buffer by STWR.

Extended Horizontal Overflow Register (EXT_H_OVF) (CR5D)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 5DH

7	6	5	4	3	2	1	0
BGT 8	Vision964 8	EHS +32	SHS 8	EHB +64	SHB 8	HDE 8	HT 8

Bit 0 HT 8 - Horizontal Total (CR0) Bit 8

Bit 1 HDE 8 - Horizontal Display End (CR1) Bit 8

Bit 2 SHB 8 - Start Horizontal Blank (CR2) Bit 8

Bit 3 EHB+64 - End Horizontal Blank (CR3) + 64
0 = $\overline{\text{BLANK}}$ pulse unaffected
1 = $\overline{\text{BLANK}}$ pulse extended by 64 DCLKs

Bit 4 SHS 8 - Start Horizontal Sync Position (CR4) Bit 8

Bit 5 EHS+32 - End Horizontal Sync (CR5) + 32
0 = HSYNC pulse unaffected
1 = HSYNC pulse extended by 32 DCLKs

Bit 6 Vision964 8 - Data Transfer Position (CR3B) Bit 8

Bit 7 BGT 8 - Bus-Grant Terminate Position (CR5F) Bit 8

Extended Vertical Overflow Register (EXT_V_OVF) (CR5E)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 5EH

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

Bit 0 VT 10 - Vertical Total (CR6) Bit 10

Bit 1 VDE 10 - Vertical Display End (CR12) Bit 10

Bit 2 SVB 10 - Start Vertical Blank (CR15) Bit 10

Bit 3 Reserved

Bit 4 VRS 10 - Vertical Retrace Start (CR10) Bit 10

Bit 5 Reserved

Bit 6 LCM 10 - Line Compare Position (CR18) Bit 10

Bit 7 Reserved

Bus Grant Termination Position Register (BGNT_TPOS) (CR5F)

Read/Write Address: 3?5H, Index 5FH
Power-On Default: 00H

The Bus Grant Termination Position is a 9-bit value specifying the horizontal line position (in character clocks) at which an active $\overline{BGNT}$ signal is deasserted, requiring a secondary controller to give up control of the memory bus. A subsequent $\overline{BREQ}$ from the secondary memory controller will not be granted until after the start of the next scan line. This must be set to a value that ensures that enough time is available for RAM refresh and hardware cursor fetch. Bit 8 is bit 7 of CR5D. This value is effective only if bit 2 of CR50 is set to 1.

7	6	5	4	3	2	1	0
BGNT-TPOS							

Bits 7–0 BGNT_TPOS - Bus Grant Termination Position
9-bit Value = the horizontal line position (in character clocks) at and beyond which a bus grant ($\overline{BGNT}$) to an alternate memory controller is deasserted. This register contains the least significant 8 bits of this value.

Extended Memory Control 3 Register (EXT-MCTL-3) (CR60)

Read/Write Address: 3?5H, Index 60H
Power-On Default: 00H

7	6	5	4	3	2	1	0
N(DISP-FETCH-PAGE)							

Bits 7-0 N(DISP-FETCH-PAGE) - N Parameter
Value = (number of 4-byte (1 MByte of memory) or 8-byte (2 or 4 MBytes of memory) units written to the display FIFO before memory access is allowed to other requestors) -1. See Section 9.4, Display Memory Access Control, for more information.

Extended Memory Control 4 Register (EXT-MCTL-4) (CR61)

Read/Write Address: 3?5H, Index 61H
Power-On Default: 00H

7	6	5	4	3	2	1	0
ENB DFLC	R	R	R	R	L(DISP-FETCH-LENGTH) 10-8		

Bits 2-0 L(DISP-FETCH-LENGTH) 10-8 - L Parameter (Bits 10-8)
These are bits 10-8 of the L parameter. See the description of the L parameter in the description for CR62.

Bits 6-3 Reserved

Bit 7 ENB DFLC - Enable Display Fetch Length Control
0 = Display fetch length control (L parameter) disabled
1 = Display fetch length control (L parameter) enabled

Extended Memory Control 5 Register (EXT-MCTL-5) (CR62)

Read/Write Address: 3?5H, Index 62H
Power-On Default: 07H

These are the lower 8 bits of an 11-bit value used in conjunction with the M and N parameters to optimize performance. If the display FIFO is being filled when this value is reached, FIFO filling will be stopped and memory control will be switched to the M parameter. The upper three bits are bits 2-0 of CR61.

7	6	5	4	3	2	1	0
L(DISP-FETCH-LENGTH) 7-0							

Bits 7-0 L(DISP-FETCH-LENGTH) 7-0 - L Parameter (Bits 7-0)
11-bit Value = (number of bytes of displayed pixels per scan line) divided by 4 for 1-Byte memory configurations or divided by 8 for 2- or 4-MByte memory configurations. This register contains the least significant 8 bits of this value.

External Sync Delay Adjust High Register (EX-DL-ADJST-HI) (CR63)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 63H

This register provides the high order bits of values that specify delays for the vertical and horizontal sync resets. These delays are required for genlocking a second video source to a primary video source (both feeding the same RAMDAC). The purpose of the adjustment is to have the origin (0,0 coordinate) at the same screen position for both video sources.

7	6	5	4	3	2	1	0
HSYNC-RESET-ADJST				VSYNC-RESET-ADJST			

Bits 3-0 VSYNC-RESET-ADJST - VSYNC Reset Adjust (Bits 7-4)
This specifies the upper 4 bits of the VSYNC Reset Adjust. The lower 4 bits are bits 3-0 of CR57. This value specifies the number of scan lines the VSYNC reset in the slave is delayed from the falling edge of the VSYNC input from the master.

Bits 7-4 HSYNC-RESET-ADJST - HSYNC Reset Adjust (Bits 7-4)
This specifies the upper 4 bits of the HSYNC Reset Adjust. The lower 4 bits are bits 7-4 of CR57. This value specifies the number of character clocks the HSYNC reset in the slave is delayed from the falling edge of the VSYNC input from the master.

Genlocking Adjustment Register (CH-CRT-DOT-ADJST) (CR64)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 64H

This register allows finer-grain genlocking adjustments that those provided by CR57 and CR63.

7	6	5	4	3	2	1	0
CH ENB	CH-CLK-PH-ADJST			H-CTR ENB	H-CTR-DOT-ADD-ADJST		

Bits 2-0 H-CTR-DOT-ADD-ADJST - H-Counter Dot Addition Adjust
This value adjusts the timing of the H-Counter reset delay in terms of dot clocks. Bit 3 is the enable for this function.

Bit 3 H-CTR ENB - Enable for H-Counter Dot Addition Adjust
0 = Disable H-Counter Dot Addition Adjustment
1 = Enable H-Counter Dot Addition Adjustment

Bits 6-4 CH-CLK-PH-ADJST - Character Clock Phase Adjust
This specifies the delay (in dot clock units) of the character clock from the rising edge of VSYNC. Bit 7 is the enable for this function.

Bit 7 CH ENB - Enable for Character Clock Phase Adjust
0 = Disable character clock phase adjustment
1 = Enable character clock phase adjustment

Extended Miscellaneous Control Register (EXT-MISC-CTL) (CR65)

Read/Write Address: 3?5H, Index 65H
Power-On Default: 00H

7	6	5	4	3	2	1	0
ADR ADJ 1	ADR ADJ 0	R	R	R	ENB 3C3	DISA 1SC	SE DLAY

Bit 0 SE DLAY - Delay falling edge of SE
0 = Normal operation
1 = The falling edges of all $\overline{SE[3:0]}$ signals are delayed.

Setting this bit reduces the chance of data contention when alternate memory banks are outputting data to the same SID bus during parallel (interleaved) operation.

Bit 1 DISA 1SC - Disable 1st SC[1:0] Output
0 = Normal operation
1 = Disable generation of the early SC[1:0] output that occurs for every screen line during the blank period when split transfers are enabled.

Bit 2 ENB 3C3 - Enable 3C3H for Video Subsystem Setup
0 = 46E8H is the address for video subsystem setup
1 = 3C3H is the address for video subsystem setup

This bit allows the CPU to initialize a second video card.

Bits 5-3 Reserved

Bit 7-6 ADR ADJ - Address adjustment for split transfers
00 = No adjustment (32-bit SID bus or 64-bit serial SID bus operation)
01 = Reserved
10 = Split transfer address adjustment for 512 word SAMs used with a 128-bit SID bus (which includes 64-bit interleaved operation)
11 = Split transfer address adjustment for 256 word SAMs used with a 128-bit SID bus (which includes 64-bit interleaved operation)

These bits must be set in a manner consistent with bit 5 of CR53 and bits 5-4 of CR66.

Extended Miscellaneous Control 1 Register (EXT-MISC-1) (CR66)

Read/Write Address: 3?5H, Index 66H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI DE	TOFF PADT	SID-MODE 1	0	SC= VCLK	DIV-SC 2	1	0

Bits 2-0 DIV-SC - Divide SC, SE and VCLK
000 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK
001 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK/2
010 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK/4
011 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK/8
100 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK/16
101 = SC[1:0], $\overline{SE}$[3:0] and VCLK = DCLK/32
111 = Reserved

With a 64-bit memory data bus, 8 bytes are transferred to the RAMDAC each SC (serial or shift clock). For 32 bits/pixel serial operation, 2 pixels are transferred each SC. SC, $\overline{SE}$ and VCLK must then be divided by 2. Similarly, they must be divided by 4 for 15/16 bits/pixel serial operation, 8 for 8 bits/pixel serial operation and 16 or 4 bits/pixel serial operation. This assumes the DCLK input has not been previously divided down relative to the pixel clock rate used by the RAMDAC.

Bit 3 SC=VCLK - Set SC0 to VCLK Frequency
0 = Normal operation
1 = SC0 = VCLK frequency and SC1 = inverted VCLK frequency regardless of the setting of bits 5-4 of this register

Bits 5-4 SID-MODE - SID Operation Mode
00 = 64-bit serial (non-interleaved) SID bus operation
01 = 32-bit parallel (interleaved) SID bus operation
10 = 128-bit serial or 64-bit parallel (interleaved) SID bus operation
11 = 32-bit serial (non-interleaved) SID bus operation

If this field is set to 10b, bit 5 of CR53 must be set in a corresponding manner. See also bits 7-6 of CR65.

Bit 6 TOFF PADT - Tri-State Off Pixel Address Bus
0 = Normal operation
1 = PA[7:0] are set to tri-state off

Setting this bit turns off the PA[7:0] lines when using Enhanced (SID) modes with RAMDACs that multiplex the VGA and SID ports.

Bit 7 PCI DE - PCI Bus Disconnect Enable
0 = PCI bus disconnect disabled
1 = PCI bus disconnect enabled

Setting this bit to 1 allows PCI burst cycles to be interrupted if AD[1:0] ≠ 00b or if the address during the burst goes outside the address ranges supported by the Vision964.

Extended Miscellaneous Control 2 Register (EXT-MISC-2)(CR67)

Read/Write Address: 3?5H, Index 67H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	VCLK PHS

Bit 0 VCLK PHS - VCLK Phase With Respect to DCLK
0 = VCLK is 180° out of phase with DCLK (inverted)
1 = VCLK is in phase with DCLK

Bits 7–1 Reserved

Configuration 3 Register (CNFG-REG-3) (CR68)

Read/Write Address: 3?5H, Index 68H
Power-On Default: Depends on Strapping

This is the third byte (along with CR36 and CR37) of the power-on strapping bits. PD[23:16] are sampled on power-on reset and their states are written to bits 7-0 of this register. A5H must be written to CR39 to provide read/write access to this register.

7	6	5	4	3	2	1	0
RAS-PCG		RAS-LOW		MA-D-SEL		CAS-STR	
1	0	1	0	1	0	1	0

Bits 1-0 $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ Stretch Time
00 = 4 units delay
01 = 3 units delay
10 = 2 units delay
11 = 1 unit delay

Bits 3-2 MA-D-SEL - Memory Address Depth Select
00 = Reserved
01 = 128K (512 rows x 256 columns)
10 = Reserved
11 = 256K (512 rows x 512 columns)

Bits 5-4 $\overline{RAS}$-LOW - $\overline{RAS}$ Low Timing Select
00 = 6.5 MCLKs
01 = 5.5 MCLKs
10 = 4.5 MCLKs
11 = 3.5 MCLKs

Bits 7-6 $\overline{RAS}$-PCG - $\overline{RAS}$ Precharge Timing Select
00 = Reserved
01 = 4.5 MCLKs
10 = 3.5 MCLKs
11 = 2.5 MCLKs

Extended System Control 3 Register (EXT-SCTL-3)(CR69)

Read/Write Address: 3?5H, Index 69H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	DISPLAY-START-ADDRESS				

Bits 4–0 DISPLAY-START-ADDRESS
This field contains the upper 5 bits (20-16) of the display start address, allowing addressing of up to 8 MBytes of display memory. When a non-zero value is programmed in this field, bits 5-4 of CR31 and 1-0 of CR51 (the old display start address bits) are ignored.

Bits 7–5 Reserved

Extended System Control 4 Register (EXT-SCTL-4)(CR6A)

Read/Write Address: 3?5H, Index 6AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	CPU-BASE-ADDRESS						

Bits 6–0 CPU-BASE-ADDRESS
This field contains the upper 7 bits (20-14) of the CPU base address, allowing accessing of up to 8 MBytes of display memory via 64K pages. When a non-zero value is programmed in this field, bits 3-0 of CR35 and 3-2 of CR51 (the old CPU base address bits) are ignored. Bit 0 of CR31 must be set to 1 to enable this field. If linear addressing is enabled and a 64-KByte window is specified, these bits specify the 64K page to be accessed at the base address specified in CR59 and CR5A. Otherwise, the base address is normally at A000H.

Bit 7 Reserved

Extended BIOS Flag 3 Register (EBIOS-FLG3)(CR6B)

Read/Write Address: 3?5H, Index 6BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-3							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-3
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 4 Register (EBIOS-FLG4)(CR6C)

Read/Write Address: 3?5H, Index 6CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-4							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-4
This register is reserved for use by the S3 BIOS.

Extended Miscellaneous Control 3 Register (EXT-MISC-3)(CR6D)

Read/Write Address: 3?5H, Index 6DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	DELAY-SC-BY-VCLK			R	DELAY-BL-BY-DCLK		

Bits 2–0 DELAY-BL-BY-DCLK - Delay $\overline{\text{BLANK}}$ by DCLK
The $\overline{\text{BLANK}}$ active pulse is delayed by the number of DCLK units programmed into this field. The pulse width is not affected. This in conjunction with the setting in bits 6-4 of this register allow the coordination of the timing relationship between SC and $\overline{\text{BLANK}}$.

Bit 3 Reserved

Bits 6–4 DELAY-SC-BY-VCLK
SC[1:0] are delayed by the number of VCLK units programmed into this register. The pulse widths are not affected. This in conjunction with the setting in bits 2-0 of this register allow the coordination of the timing relationship between SC and $\overline{\text{BLANK}}$.

Bit 7 Reserved

Section 18: Enhanced Commands Register Descriptions

These registers support the Vision964 Enhanced drawing commands. Access to these registers is enabled via bit 0 of the System Configuration register (CR40).

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Subsystem Status Register (SUBSYS_STAT)

Read Only Address: 42E8H
Power-On Default: 0000H

This read-only register provides information on interrupt status, monitor I.D. and the number of bits per pixel. See the Subsystem Control (42E8H, Write Only) register for details on enabling and clearing interrupts.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								PXL	GIP DATA			FIFO	FIFO	GE	VSY
R	R	R	R	R	R	R	R	LNG	2	1	0	EMP	OVF	BSY	INT

Bit 0 VSY INT - Vertical Sync Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 1 GE BSY - Graphics Engine Busy Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 2 FIFO OVF - Command FIFO Overflow Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 3 FIFO EMP - Command FIFO Empty Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bits 6–4 GIP DATA - General Input Port Data
These bits reflect the states of GD[7:5] during power-on reset. These lines are strapped to provide design-specific information.

Bit 7 PXL LNG - Pixel Length (# of bit planes)
0 = 4-bit
1 = 8-bit

This defines the number of bit planes when bits 5-4 of the Extended System Control 1 register (CR50) are 00b.

Bits 15–8 Reserved

Subsystem Control Register (SUBSYS_CNTL)

Write Only Address: 42E8H
Power-On Default: 0000H

This register allows each of several interrupt sources to be enabled or disabled. Interrupt status (Subsystem Status (42E8H, Read Only) can be cleared. This register also controls the software reset of the graphics engine.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GE-RST				FIFO-ENB		GE	VSY					FIFO	FIFO	GEB	VSY
1	0	R	R	EMP	OVF	BSY	ENB	R	R	R	R	CLE	CLO	CLR	CLR

Bit 0 VSY CLR - Clear Vertical Sync Interrupt Status
0 = No change
1 = Clear

Bit 1 GEB CLR - Clear Graphics Engine Busy Interrupt Status
0 = No change
1 = Clear

Bit 2 FIFO CLO - Clear Command FIFO Overflow Interrupt Status
0 = No change
1 = Clear

Bit 3 FIFO CLE - Clear Command FIFO Empty Interrupt Status
0 = No change
1 = Clear

Bits 7–4 Reserved

Bit 8 VSY ENB - Vertical Sync Interrupt Enable
0 = Disable
1 = Enable

Bit 9 GE BSY- Graphics Engine Busy Interrupt Enable
0 = Disable
1 = Enable

Bit 10 FIFO-ENB OVF - Command FIFO Overflow Interrupt Enable
0 = Disable
1 = Enable

Bit 11 FIFO-ENB EMP - Command FIFO Empty Interrupt Enable
0 = Disable
1 = Enable

Bits 13–12 Reserved

Bits 15–14 GE-RST - Graphics Engine Software Reset
00 = No change
01 = Graphics Engine enabled
10 = Reset
11 = Reserved

Advanced Function Control Register (ADVFUNC_CNTL)

Read/Write Address: 4AE8H
Power-On Default: 0000H

This register enables or disables the enhanced display functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	MIO	LA	R	ENH PL	R	ENB EMO

Bit 0 ENB EMO - Enable Enhanced Functions
0 = Enable VGA and VESA planar (4 bits/pixel) modes (all modes using PA[7:0] for pixel data transfer)
1 = Enable all other modes (Enhanced and VESA non-planar- all modes transferring pixel data via the external SID bus)

Bit 1 Reserved

Bit 2 ENH PL - Enhanced modes pixel length
0 = 8 or more bits/pixel enhanced modes
1 = 4 bits/pixel enhanced modes

Bits 5-4 of CR50 are used to differentiate between 8-, 16- and 32-bit pixel lengths.

Bit 3 Reserved

Bit 4 LA - Enable Linear Addressing
0 = Disable linear addressing
1 = Enable linear addressing

This bit is ORed with bit 4 of CR58 and is equivalent to it.

Bit 5 MIO - Enable Memory Mapped I/O (MMIO)
0 = Disable MMIO
1 = Enable MMIO

This bit is ORed with bit 4 of CR53 and is equivalent to it.

Bits 15–6 Reserved

Current Y-Position Register(CUR_Y)

Read/Write Address: 82E8H
Power-On Default: Undefined

Writing to this register defines the vertical screen coordinate at which the next pixel will be drawn. Reading it produces the current vertical coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT Y-POSITION											

Bits 11–0 CURRENT Y-POSITION

Bits 15–12 Reserved

Current X-Position Register (CUR_X)

Read/Write Address: 86E8H
Power-On Default: Undefined

Writing to this register defines the horizontal screen coordinate at which the next pixel will be drawn. Reading it produces the current horizontal coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT X-POSITION											

Bits 11–0 CURRENT X-POSITION

Bits 15–12 Reserved

Destination Y-Position/Axial Step Constant Register (DESTY_AXSTP)

Read/Write Address: 8AE8H
Power-On Default: Undefined

This register defines the destination Y position for BitBLTs and pattern fills or the axial step constant for line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION Y-POSITION											

Bits 11–0 DESTINATION Y-POSITION
This setting applies only to BitBLTs and pattern fills.

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER AXIAL STEP CONSTANT													

Axial Step Constant = 2 * (min(|dx|,|dy|)) In other words, when drawing a line from point A to point B, determine the change in the X coordinate from A to B and the change in the Y coordinate from A to B. Take the smaller of the two changes and multiply its absolute value by 2.

Bits 13–0 LINE PARAMETER AXIAL STEP CONSTANT
This setting applies only to line draws.

Bits 15–14 Reserved

Destination X-Position/Diagonal Step Constant Register (DESTX_DIASTP)

Read/Write Address: 8EE8H
Power-On Default: Undefined

This register defines the destination X position for BitBLTs and pattern fills or the diagonal step constant for line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION X-POSITION											

Bits 11–0 DESTINATION X-POSITION
This setting applies only to BitBLTs and pattern fills.

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER DIAGONAL STEP CONSTANT													

Diagonal Step Constant = 2 * [min(|dx|,|dy|) - max(|dx|,|dy|)] See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in this equation.

Bits 13–0 LINE PARAMETER DIAGONAL STEP CONSTANT
This setting applies only to line draws.

Bits 15–14 Reserved

Line Error Term Read/Write Register (ERR_TERM)

Read/Write Address: 92E8H
Power-On Default: Undefined

This register specifies the initial error term for the line draw operation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER/ERROR TERM													

Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| - 1 if the starting X < the ending X
Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| if the starting X ≥ the ending X
See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in these equations.

Bits 13–0 LINE PARAMETER/ERROR TERM

Bits 15–14 Reserved

Major Axis Pixel Count Register (MAJ_AXIS_PCNT)

Read/Write Address: 96E8H
Power-On Default: Undefined

This register specifies the length (in pixels) of the major (longest) axis.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	RECTANGLE WIDTH/LINE PARAMETER MAX											

Bits 11–0 RECTANGLE WIDTH/LINE PARAMETER MAX
This parameter applies to BitBLTs, line draws and rectangle fills and pattern fills. Its value is the number of pixels along the major axis - 1.

Bits 15–12 Reserved

Graphics Processor Status Register (GP_STAT)

Read Only Address: 9AE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO-STATUS						HDW		FIFO-STATUS							
9	10	11	12	13	AE	BSY	R	1	2	3	4	5	6	7	8

Bits 7–0 FIFO-STATUS

In the following table, the leftmost column represents the value of FIFO status bit 1 (register bit 7). Each column to the right represents the value of the next higher FIFO status bit. A value of 0 read from any particular status bit position guarantees at least as many open FIFO slots as the number of that status bit. For example, if a 0 is read from status bit 9 (register bit 15), there are at least 9 open FIFO slots.

0000000000000 = 13 FIFO slots available
0000000000001 = 12 FIFO slots available
0000000000011 = 11 FIFO slots available
0000000000111 = 10 FIFO slots available
0000000001111 = 9 FIFO slots available
0000000011111 = 8 FIFO slots available
0000000111111 = 7 FIFO slots available
0000001111111 = 6 FIFO slots available
0000011111111 = 5 FIFO slots available
0000111111111 = 4 FIFO slots available
0001111111111 = 3 FIFO slots available
0011111111111 = 2 FIFO slots available
0111111111111 = 1 FIFO slots available
1111111111111 = 0 FIFO slots available

Bit 8 Reserved

Bit 9 HDW BSY - Hardware (Graphics Engine) Busy
0 = not busy
1 = busy - graphics command is executing

Bit 10 AE - All FIFO Slots Empty
0 = At least one FIFO slot is occupied
1 = All FIFO slots empty

Bits 15–11 FIFO-STATUS
These are the upper five bits of the FIFO status. See bits 7-0 for the interpretation.

Drawing Command Register (CMD)

Write Only Address: 9AE8H
Power-On Default: Undefined

This register specifies the drawing command and a number of associated control parameters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD-TYPE			BYTE		BUS SIZE		WAIT	DRWG-DIR.			DRAW	DIR	LAST	PX	
2	1	0	SWP	R	1	0	YES	2	1	0	YES	TYP	POF	MD	R

Bit 0 Reserved

Bit 1 PX MD - Select Across the Plane Pixel Mode
0 = Single pixel transferred at a time (through the plane mode)
1 = Multiple pixels transferred at a time (across the plane mode)

Bit 2 LAST POF - Last Pixel Off
0 = Last pixel of line or vector draw will be drawn
1 = Last pixel of line or vector draw will not be drawn

Bit 3 DIR TYP - Select Radial Direction Type
0 = x-y (axial)
1 = Radial

Bit 4 DRAW YES - Draw Pixel
0 = Move the current position only - don't draw
1 = Draw pixel(s)

Bits 7–5 DRWG-DIR - Select Drawing Direction
In the following table, radial drawing angle is measured counterclockwise from the X axis. For axial line draws, the line is drawn from left to right or a +X and from right to left for a -X, down for a +Y and up for a -Y. X or Y maj specifies the longest axis.

7–5	Radial (bit 3 = 1)	x-y (Axial - bit 3 = 0)
000	0°	–Y,X maj,–X
001	45°	–Y,X maj,+X
010	90°	–Y,Y maj,–X
011	135°	–Y,Y maj,+X
100	180°	+Y,X maj,–X
101	225°	+Y,X maj,+X
110	270°	+Y,Y maj,–X
111	315°	+Y,Y maj,+X

Bit 8 WAIT YES - Wait for CPU Data
0 = Use Graphics Engine-based data
1 = Wait for data to be transferred to or from the CPU through the E2E8H port

Bits 10–9 BUS SIZE - Select System Bus Size
00 = 8-bit
01 = 16-bit
10 = 32-bit
11 = Reserved

This parameter applies only to the Pixel Data Transfer (E2E8H, E2EAH) registers or when using memory-mapped I/O.

Bit 11 Reserved

Bit 12 BYTE SWP - Enable Byte Swap
0 = High byte first, low byte second
1 = Low byte first, high byte second

Bits 15–13 CMD-TYPE - Select Command Type

000 = NOP. This is used to set up short stroke vector drawing without writing a pixel.
001 = Draw Line. If bit 3 of this register is cleared to 0, the axial step constant, diagonal step constant and error term are used to draw the line. If bit 3 is set to 1, the line will be drawn at the angle specified by bits 7-5 and with a length in pixels as specified by the Major Axis Pixel Count (96E8H) register.
010 = Rectangle Fill. The Major Axis Pixel Count register specifies the number of pixels in each horizontal line and the Minor Axis Pixel Count (BEE8H, Index 00H) register specifies the number of horizontal lines.
011 = Reserved
100 = Reserved
101 = Reserved
110 = BitBLT. This operation copies a rectangle from one part of display memory to another. It uses the Destination X and Y, the Current X and Y and the Major and Minor Pixel Count registers.
111 = Pattern Fill. Same as a BitBlt except that an 8x8 patterned rectangle is transferred repeatedly to the destination rectangle. The starting X coordinate of the source rectangle should always be on an 8 pixel boundary.

Short Stroke Vector Transfer Register (SHORT_STROKE)

Write Only Address: 9EE8H
Power-On Default: Undefined

This register defines two short stroke vectors. These are drawn one at a time based on the setting of the BYTE SWAP bit (bit 12) in the Command (9AE8H) register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRWG-DIR			DRW	PIXEL-LENGTH				DRWG-DIR.			DRW	PIXEL-LENGTH			
2	1	0	-MV	3	2	1	0	2	1	0	-MV	3	2	1	0

Bits 3–0 PIXEL-LENGTH
Value = # pixels - 1

Bit 4 DRW -MV - Draw Pixel
0 = Move current position only - don't draw
1 = Draw pixel

Bits 7–5 DRWG-DIR.- Select Drawing Direction (measured counterclockwise from the X axis)
000 = 0°
001 = 45°
010 = 90°
011 = 135°
100 = 180°
101 = 225°
110 = 270°
110 = 315°

Bits 15–8 These bits duplicate bits 7-0 to define the second short stroke vector.

Background Color Register (BKGD_COLOR)

Read/Write Address: A2E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BACKGROUND COLOR															

Bits 31–0 BACKGROUND COLOR
If bit 9 of BEE8_EH is set to 1, this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Foreground Color Register (FRGD_COLOR)

Read/Write Address: A6E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOREGROUND COLOR															

Bits 31–0 FOREGROUND COLOR
If bit 9 of BEE8_EH is set to 1, this becomes a 32-bit register. If bit 9 of BEE8_EH is cleard to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Write Mask Register (WRT_MASK)

Read/Write Address: AAE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE WRITE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE WRITE MASK															

Bits 31–0 BIT-PLANE WRITE MASK
If bit i = 0, bitplane i is not updated.
If bit i = 1, bitplane i is updated.

Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1, this becomes a 32-bit register. If bit 9 of BEE8_EH is cleard to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Read Mask Register (RD_MASK)

Read/Write Address: AEE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE READ MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE READ MASK															

Bits 31–0 BIT-PLANE READ MASK
If bit i = 0, bitplane i is not used as a data source
If bit i = 1, bitplane i is used as a data source

Bit-plane read mask for BitBLT and image transfer functions. Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1, this becomes a 32-bit register. If bit 9 of BEE8_EH is cleard to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Color Compare Register (COLOR_CMP)

Read/Write Address: B2E8H
Power-On Default: Undefined

This register contains the color value that is compared against the current bitmap color if the color compare option is turned on by setting bit 8 of the Pixel Control (BEE8H, Index 0EH) to 1. Bit 7 of the Pixel Control register determines whether a match or a non-match results in a pixel update.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARISON COLOR WITH SOURCE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMPARISON COLOR WITH SOURCE															

Bits 31–0 COMPARISON COLOR WITH SOURCE
If bit 9 of BEE8_EH is set to 1, this becomes a 32-bit register. If bit 9 of BEE8_EH is cleard to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Background and Foreground Mix Registers (BKGD_MIX, FRGD_MIX)

Read/Write Address: B6E8H (Background), BAE8H (Foreground)
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when these registers are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CLR-SRC			MIX-TYPE			
R	R	R	R	R	R	R	R	R	1	0	R	3	2	1	0

Bits 3–0 MIX-TYPE - Select Mix Type
In the general case, a new color is defined. A logical operation such as AND or OR is then performed between it and the current bitmap color. If the bitplane to be written is enabled, the result of this logical "mix" is written to the bitmap as the new pixel color. The following table shows the mix types available (! = logical NOT).

0000	!current	1000	!current OR !new
0001	logical zero	1001	current OR !new
0010	logical one	1010	!current OR new
0011	leave current as is	1011	current OR new
0100	!new	1100	current AND new
0101	current XOR new	1101	!current AND new
0110	!current XOR new	1110	current AND !new
0111	new	1111	!current AND !new

Bit 4 Reserved

Bits 6–5 CLR-SRC - Select Color Source
00 = Background color (the register is the color source)
01 = Foreground color (the register is the color source)
10 = CPU data (the CPU is the color source)
11 = Display memory (the display memory is the color source)

Bits 15–7 Reserved

Read Register Data Register (RD_REG_DT)

Read Only Address: BEE8H
Power-On Default: Undefined

A read of this register produces a read of the register specified by bits 2-0 of the Read Register Select (BEE8H, Index 0FH) register. Each read of BEE8H causes the read index (bits 2-0 of BEE8H, Index 0FH) to increment by one. Registers BEE8H, Indices 0H to 0EH, 9AE8H, 42E8H and 46E8H can thus be rapidly read by successive reads from BEE8H.

Note: Writes to the BEE8H registers (except the read index register, Index 0FH) are pipelined. Therefore, to correctly read back a write to one of these registers, issue a NOP drawing command (a write to 9AE8H with bits 15-13 programmed to 000b) immediately after the BEE8H register write. Next, write the desired register index to BEE8H, Index 0FH and read the data from BEE8H.

The BEE8H registers are written directly by writing to BEE8H with the appropriate register index in bits 15-12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Minor Axis Pixel Count Register (MIN_AXIS_PCNT)

Write Only Address: BEE8H, Index 0H
Power-On Default: Undefined

This register specifies the length of the minor (smallest) axis in pixels.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RECTANGLE HEIGHT											

Bits 11–0 RECTANGLE HEIGHT
Value = (number of pixels in minor axis) - 1

Bits 15–12 INDEX = 0H

Top Scissors (SCISSORS_T)

Write Only Address: BEE8H, Index 1H
Power-On Default: Undefined

This register specifies the top of the clipping rectangle. It is the lowest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	CLIPPING TOP LIMIT											

Bits 11–0 CLIPPING TOP LIMIT

Bits 15–12 INDEX = 1H

Left Scissors (SCISSORS_L)

Write Only Address: BEE8H, Index 2H
Power-On Default: Undefined

This register specifies the left side of the clipping rectangle. It is the lowest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	CLIPPING LEFT LIMIT											

Bits 11–0 CLIPPING LEFT LIMIT

Bits 15–12 INDEX = 2H

Bottom Scissors (SCISSORS_B)

Write Only Address: BEE8H, Index 3H
Power-On Default: Undefined

This register specifies the bottom of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	CLIPPING BOTTOM LIMIT											

Bits 11–0 CLIPPING BOTTOM LIMIT

Bits 15–12 INDEX = 3H

Right Scissors (SCISSORS_R)

Write Only Address: BEE8H, Index 4H
Power-On Default: Undefined

This register specifies the right side of the clipping rectangle. It is the highest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	CLIPPING RIGHT LIMIT											

Bits 11–0 CLIPPING RIGHT LIMIT

Bits 15–12 INDEX = 4H

Pixel Control Register (PIX_CNTL)

Write Only Address: BEE8H, Index 0AH
Power-On Default: Undefined

See Bitmap Access Through the Graphics Engine in the Enhanced Mode Programming section for an explanation of how and when bits 7-6 of this register are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	R	R	R	R	DT-EX-SRC 1	0	R	R	R	R	R	R

Bits 5–0 Reserved

Bits 7–6 DT-EX-SRC - Select Mix Register
00 = Foreground Mix register is always selected
01 = Reserved
10 = CPU data determines Mix register selected
11 = Display memory current value determines Mix register selected

Bits 11–8 Reserved

Bits 15–12 INDEX = 0AH

Multifunction Control Miscellaneous 2 Register (MULT_MISC2)

Write Only
Power-On Default: D000H

Address: BEE8H, Index 0DH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
=1	=1	=0	=1	=0	=0	=0	=0	=0	SRC-BASE			=0	DST=BASE		

Bits 2–0 DST-BASE - Destination Base Address
000 = First destination memory address is in the 1st MByte of display memory
001 = First destination memory address is in the 2nd MByte of display memory
010 = First destination memory address is in the 3rd MByte of display memory
011 = First destination memory address is in the 4th MByte of display memory
100 = First destination memory address is in the 5th MByte of display memory
101 = First destination memory address is in the 6th MByte of display memory
110 = First destination memory address is in the 7th MByte of display memory
111 = First destination memory address is in the 8th MByte of display memory

This field supersedes bits 1-0 of BEE8H, Index E if any of these 3 bits are set to 1.

Bit 3 Reserved

Bits 6–4 SRC-BASE - Source Base Address
000 = First source memory address is in the 1st MByte of display memory
001 = First source memory address is in the 2nd MByte of display memory
010 = First source memory address is in the 3rd MByte of display memory
011 = First source memory address is in the 4th MByte of display memory
100 = First source memory address is in the 5th MByte of display memory
101 = First source memory address is in the 6th MByte of display memory
110 = First source memory address is in the 7th MByte of display memory
111 = First source memory address is in the 8th MByte of display memory

This field supersedes bits 3-2 of BEE8H, Index E if any of these three bits are set to 1.

Bits 11–7 Reserved

Bits 15–12 INDEX = 0DH

Multifunction Control Miscellaneous Register (MULT_MISC)

Write Only
Power-On Default: E000H

Address: BEE8H, Index 0EH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	R	R	CMR 32B	ENB CMP	SRC NE	SLW RM	EXT CLIP	RSF	SRC-BA 21	20	DEST-BA 21	20

Bits 1–0 DEST-BA 21 20 - Destination Base Address Bits 21-20
00 = First destination memory address is in the 1st MByte of display memory
01 = First destination memory address is in the 2nd MByte of display memory
10 = First destination memory address is in the 3rd MByte of display memory
11 = First destination memory address is in the 4th MByte of display memory

This field is superceded by bits 2-0 of BEE8H, Index D, if any of the BEE8H, Index D bits is set to 1.

Bits 3–2 SRC-BA 21 20 - Source Base Address Bits 21-20
00 = First source memory address is in the 1st MByte of display memory
01 = First source memory address is in the 2nd MByte of display memory
10 = First source memory address is in the 3rd MByte of display memory
11 = First source memory address is in the 4th MByte of display memory

This field is superceded by bits 6-4 of BEE8H, Index D, if any of the BEE8H, Index D bits is set to 1.

Bit 4 RSF - Select Upper Word in 32 Bits/Pixel Mode
0 = Selects lower 16 bits for accesses to 32-bit registers in 32 bpp mode
1 = Selects upper 16 bits for accesses to 32-bit registers in 32 bpp mode

Bit 5 EXT CLIP - Enable External Clipping
0 = Only pixels inside the clipping rectangle are drawn
1 = Only pixels outside the clipping rectangle are drawn

Bit 6 SLW RMW - Select Slow Read/Modify/Write Cycle
0 = Fast Read/Modify/Write Cycle
1 = Slow Read/Modify/Write Cycle

When the Graphics Engines does a raster operation involving current screen data, it must do a read/modify/write cycle. For a fast cycle, the read, modify and write each take one MCLK. For a slow cycle, a wait state is inserted so that the entire process requires 4 MCLKs.

Bit 7 SRC NE - Don't Update Bitmap if Source Not Equal to Color Compare Color
0 = Don't update current bitmap if the Color Compare (B2E8) register value is equal to the color value of the source bitmap
1 = Don't update current bitmap if the Color Compare (B2E8) register value is not equal to the color value of the source bitmap

This bit is only active if bit 8 of this register is set to 1.

Bit 8 ENB CMP - Enable Color Compare
0 = Disable color comparison
1 = Enable color comparison

Bit 9 CMR 32B - Select 32-Bit Command Registers
0 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 16-bit
1 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 32-bit. Byte and word accesses cannot be made.

Bits 11–10 Reserved = 0

Bits 15–12 INDEX = 0EH

Read Register Select Register (READ_SEL)

Write Only Address: BEE8H, Index 0FH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	R	R	R	R	R	R	R	R	READ-REG-SEL			

Bits 2–0 READ-REG-SEL - Read Register Select

When BEE8H is read, the value returned is determined by this read register index according to the following:
0000 = BEE8H, Index 0H
0001 = BEE8H, Index 1H
0010 = BEE8H, Index 2H
0011 = BEE8H, Index 3H
0100 = BEE8H, Index 4H
0101 = BEE8H, Index 0AH
0110 = BEE8H, Index 0EH
0111 = 9AE8H (Bits 15-13 of the read data are forced to 0.)
1000 = 42E8H (Bits 15-12 of the read data are forced to 0.)
1001 = 46E8H
1010 = BEE8H, Index 0DH

The read register index increments by one with each reading of BEE8H.

Bits 11–4 Reserved

Bits 15–12 INDEX = 0FH

Pixel Data Transfer Register (PIX_TRANS)

Write Only Address: E2E8H
Power-On Default: Undefined

All data to the Graphics Engine must pass through this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Pixel Data Transfer - Extension Register (PIX_TRANS_EXT)

Write Only Address: E2EAH
Power-On Default: Undefined

This register is an extension of E2E8H for 32-bit operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Section 19: PCI Register Descriptions

The PCI specification defines a configuration register space. These registers allow device relocation, device independent system address map construction and automatic configurations. The Vision964 provides a subset of these registers, which are described below.

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The Vision964 supports or returns 0 for the first 64 bytes of this space.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Vendor ID

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15–0 Vendor ID
This is hardwired to 5333H to identify S3 Incorporated.

Device ID

Read Only Address: 02H
Power-On Default: 88D0H

This read-only register identifies the device.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15–0 Device ID
88D0H

Command

Read/Write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles the Vision964 can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	DAC RSP	R	R	R	MEM	I/O

Bit 0 I/O - Enable Response to I/O Accesses
0 = Response to I/O space accesses is disabled
1 = Response to I/O space accesses enabled

Bit 1 MEM - Enable Response to Memory Accesses
0 = Response to memory space accesses is disabled
1 = Response to memory space accesses enabled

Bits 4–2 Reserved

Bit 5 DAC RSP - No Response to RAMDAC Register Accesses
0 = Vision964 responds to RAMDAC register accesses
1 = Vision964 does not respond to RAMDAC register accesses

Bits 15–6 Reserved

Status

Read/Write Address: 06H
Power-On Default: 0200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	DEVSEL		Reserved								

Bits 8–0 Reserved

Bits 10–9 DEVSEL - Device Select Timing
01 = Medium DEVSEL timing. (hardwired)

Bits 15–11 Reserved

Revision ID

Read/Write Address: 08H
Power-On Default: Stepping Dependent

This register contains the revision level of the Vision964.

7	6	5	4	3	2	1	0
REVISION ID							

Bits 7–0 REVISION ID

Programming Interface

Read/Write Address: 0AH
Power-On Default: 01H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	VGA

Bit 0 VGA
1 = The Vision964 supports the standard VGA programming interface. (hardwired)

Bits 7–1 Reserved

Base Address 0

Read/Write Address: 12H (high) 10H (low)
Power-On Default: 0000 0000H

This is a 32-bit register in PCI configuration space that provides for address relocation. The Vision964 maps the upper 9 bits of the register to the Linear Address Window Position registers CR59-CR5A. Bit 23 maps to bit 7 of CR5A and bits [31:24] map to bits 7-0 of CR59. Consequently, these bits map to system address bits [31:23].

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 0									R	R	R	R	R	R	R

Bit 0 MSI - Memory Space Indicator
0 = Base registers map into memory space (hardwired)

Bits 2–1 TYPE - Type of Address Relocation
00 = Locate anywhere in 32-bit address space (hardwired)

Bit 3 PREF - Prefetchable
0 = Does not meet the prefetchable requirements (hardwired)

Bits 22–4 Reserved

Bits 31–23 BASE ADDRESS 0
See the description for the Linear Address Window Position registers (CR59, CR5A). Writes to CR59 and CR5A will also update this field.

BIOS ROM Base Address

Read/Write Address: 32H (high) 30H (low)
Power-On Default: 000C 0000H

This is a 32-bit register in PCI configuration space that provides for video BIOS ROM address relocation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	ADE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIOS ROM BASE ADDRESS															

Bit 0 ADE - Address Decode Enable
0 = Accesses to the BIOS ROM address space defined in this register are disabled
1 = Accesses to the BIOS ROM address space defined in this register are enabled

Bits 15–1 Reserved

Bits 31–16 BIOS ROM BASE ADDRESS
These are the upper 16 bits of the BIOS ROM address.

Appendix A: Register Reference

This Appendix contains tables listing all the registers in each of categories corresponding to Sections 12-19 of this data book.

- CGA-Compatible
- MDA- and HGC- Compatible
- VGA
- S3 VGA
- System Control
- System Extension
- Enhanced Commands
- PCI Configuration Space

Within each table, registers are listed in order of increasing addresses/indices. Name, address, register bit descriptions with read/write status and the page number of the detailed register description are provided for each register. All addresses and indices are hexadecimal values.

A.1 CGA-COMPATIBLE REGISTERS

Table A-1. CGA-Compatible Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3D5	**10**		**Light Pen High**	**12-1**
	5-0	R	High 6 bits of light pen strobe address	
	7-6		Undefined	
3D5	**11**		**Light Pen Low**	**12-1**
		R	Low byte of light pen strobe address	
3D8			**CGA Mode Control**	**12-2**
	0	R/W	Select high resolution (80x25) text	
	1	R/W	Select graphics mode	
	2	R/W	Select black/white mode	
	3	R/W	Enable video output	
	4	R/W	Enable high resolution (640x200) graphics mode	
	5	R/W	Enable text blinking	
	7-6	R/W	Reserved	
3D9			**CGA Color Select**	**12-3**
	0	R/W	Select blue border	
	1	R/W	Select green border	
	2	R/W	Select red border	
	3	R/W	Select intensified border	
	4	R/W	Select background in alpha, high intensity in graphics	
	5	R/W	Select color set in 320x200 mode	
	7-6	R/W	Reserved	
3DA			**CGA Status**	**12-4**
	0	R	Border/blanking active (horizontal sync)	
	1	R	Light pen latch triggered	
	2	R	Reserved = 1 (light pen switch open)	
	3	R	Vertical sync active	
	7-4	R	Reserved	
3DB			**Reset Light Pen Flag**	**12-5**
	7-0	W	Reset light pen flag	
3DC			**Set Light Pen Flag**	**12-5**
	7-0	W	Set light pen flag	

A.2 MD- AND HGC-COMPATIBLE REGISTERS

Table A-2. MDA- and HGC-Compatible Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3B5	**10**		**Light Pen High**	**12-1**
	5-0	R	High 6 bits of the light pen strobe address	
	7-6	R	Undefined	
3B5	**11**		**Light Pen Low**	**12-1**
	7-0	R	Low byte of the light pen strobe address	
3B8			**MDA-Mode Control**	**13-1**
	2-0	R/W	Reserved	
	3	R/W	Enable video output	
	4	R/W	Reserved	
	5	R/W	Enable text blinking	
	7-6	R/W	Reserved	
3B8			**HGC-Mode Control**	**13-2**
	0	R/W	Reserved	
	1	R/W	Enable graphics mode (720x348)	
	2	R/W	Reserved	
	3	R/W	Enable video output	
	4	R/W	Reserved	
	5	R/W	Enable text blinking	
	6	R/W	Reserved	
	7	R/W	Select Hercules graphics video page 1(B8000H)	
3B9			**HGC-Set Light Pen Flag**	**13-3**
	7-0	W	Set light pen flag	
3BA			**HGC Status**	**13-3**
	0	R	Border/blanking active (horizontal sync)	
	1	R	Light pen flag on	
	2	R	Reserved = 1	
	3	R	Black/white video enabled	
	6-4	R	Reserved = 1	
	7	R	Vertical sync active	
3BA			**MDA Status**	**13-4**
	0	R	Border/blank active (horizontal sync)	
	2-1	R	Reserved = 1	
	3	R	Black/white video enabled	
	7-4	R	Reserved = 1	

Table A-2. MDA- and HGC-Compatible Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3BB			**Reset Light Pen Flag**	**13-4**
	7-0	W	Reset light pen flag	
3BF		**R/W**	**HGC Configuration**	**13-4**
	0	W	Graphics mode allowed	
	1	W	Unlock bit 7 of Hercules Mode register (upper memory page)	
	7-2	W	Undefined	

A.3 VGA REGISTERS

? = B for monochrome, D for color.

Table A-3. VGA Registers

Address	Index Bit(s)		Register Name Bit Description	Description Page
General or External Registers				
3C2			**Miscellaneous Output**	**14-1**
	0	W	Color emulation. Address based at 3Dx	
	1	W	Enable CPU access of video memory	
	3-2	W	Video (DCLK) select. See also bits 3-0 of CR42	
	4	W	Reserved	
	5	W	Select the high 64K page of memory	
	6	W	Make HSYNC an active low signal	
	7	W	Make VSYNC an active low signal	
3CC			**Miscellaneous Output**	**14-1**
	0	R	Color emulation. Address based at 3Dx	
	1	R	Enable CPU access of video memory	
	3-2	R	Video (DCLK) select. See also bits 3-0 of CR42	
	4	R	Reserved	
	5	R	Select the high 64K page of memory	
	6	R	Make HSYNC an active low signal	
	7	R	Make VSYNC an active low signal	
3?A			**Feature Control**	**14-2**
	2-0	W	Reserved	
	3	W	VSYNC is ORed with the internal display enable signal	
	7-4	W	Reserved	
3CA			**Feature Control**	**14-2**
	2-0	R	Reserved	
	3	R	VSYNC is ORed with the internal display enable signal	
	7-4	R	Reserved	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C2			**Input Status 0**	**14-3**
	3-0	R	Reserved	
	4	R	The SENSE/BREQ input is a logical 1	
	6-5	R	Reserved	
	7	R	Vertical retrace interrupt to the CPU is pending	
3?A			**Input Status 1**	**14-3**
	0	R	The display in not in active display mode	
	1	R	Light pen has been triggered	
	2	R	Reserved	
	3	R	Vertical retrace period is active	
	5-4	R	Feedback of two color outputs for test purposes	
	7-6	R	Reserved	
Sequencer Registers				
3C4			**Sequencer Index**	**14-4**
	7-0	R/W	Index to the sequencer register to be accessed	
3C5			**Sequencer Data**	**14-5**
	7-0	R/W	Data to or from the accessed sequencer register accessed	
3C5	**00**		**Reset (SR0)**	**14-5**
	0	R/W	Asynchronous reset (not functional for the Vision964)	
	1	R/W	Synchronous reset (not functional for the Vision964)	
	7-2	R/W	Reserved	
3C5	**01**		**Clocking Mode (SR1)**	**14-6**
	0	R/W	Character clocks are 8 dots wide	
	1	R/W	Reserved	
	2	R/W	Load the video serializers every second character clock	
	3	R/W	The internal dot clock is 1/2 the DCLK frequency	
	4	R/W	Load the video serializers every fourth character clock	
	5	R/W	Screen is turned off	
3C5	**02**		**Enable Write Plane (SR2)**	**14-6**
	3-0	R/W	Enables a CPU write to the corresponding color plane	
	7-4	R/W	Reserved	
3C5	**03**		**Character Font Select (SR3)**	**14-7**
	4, 1-0	R/W	Primary text mode character select	
	5,3-2	R/W	Secondary text mode character select	
	7-6	R/W	Reserved	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	04		**Memory Mode Control (SR4)**	14-8
	0	R/W	Reserved	
	1	R/W	Memory access to 256K allowed (required for VGA)	
	2	R/W	Sequential addressing for CPU video memory accesses	
	3	R/W	Module 4 addressing for CUP video memory accesses	
	7-4	R/W	Reserved	
3C5	08		**Unlock Extended Sequencer (SR8)**	14-9
	7-0	R/W	Load xxxx0110b to unlock SRD	
3C5	0D		**Extended Sequencer (SRD)**	14-9
	3-0	R/W	Reserved	
	5-4	R/W	HSYNC control for Green PC requirements	
	7-6	R/W	VSYNC control for Green PC requirements	
CRT Controller Registers				
3?4			**CRT Controller Index**	14-10
	7-0	R/W	Index to the CRTC register to be accessed	
3?5			**CRT Controller Data**	14-10
	7-0	R/W	Data to or from the CRTC register accessed	
3?5	00		**Horizontal Total (CR0)**	14-11
	7-0	R/W	Number of characters in a line -5	
3?5	01		**Horizontal Display End (CR1)**	14-11
	7-0	R/W	One less than the total number of displayed characters	
3?5	02		**Start Horizontal Blank (CR2)**	14-12
	7-0	R/W	Character count where horizontal blanking starts	
3?5	03		**End Horizontal Blank (CR3)**	14-12
	4-0	R/W	End position of horizontal blanking	
	6-5	R/W	Display enable skew in character clocks	
	7	R/W	Reserved	
3?5	04		**Start Horizontal Sync Position (CR4)**	14-13
	7-0	R/W	Character count where HSYNC goes active	
3?5	05		**End Horizontal Sync Position (CR5)**	14-13
	4-0	R/W	Position where HSYNC goes inactive	
	6-5	R/W	Horizontal retrace end delay in character clocks	
	7	R/W	End horizontal blanking bit 5	
3?5	06		**Vertical Total (CR6)**	14-14
	7-0	R/W	Number of lines - 2	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	07		**CRTC Overflow (CR7)**	14-14
	0	R/W	Vertical total bit 8	
	1	R/W	Vertical display end bit 8	
	2	R/W	Vertical retrace start bit 8	
	3	R/W	Start vertical blank bit 8	
	4	R/W	Line compare bit 8	
	5	R/W	Vertical total bit 9	
	6	R/W	Vertical display end bit 9	
	7	R/W	Vertical retrace start bit 9	
3?5	08		**Preset Row Scan (CR8)**	14-15
	4-0	R/W	Line where first character row begins	
	6-5	R/W	Number of bytes to pan horizontally	
	7	R/W	Reserved	
3?5	09		**Maximum Scan Line (CR9)**	14-15
	4-0	R/W	Character height in scan lines -1	
	5	R/W	Start vertical blank bit 9	
	6	R/W	Line compare bit 9	
	7	R/W	Double scanning (repeat each line) enabled	
3?5	0A		**Cursor Start Scan Line (CRA)**	14-16
	4-0	R/W	Cursor starting line within the character cell	
	5	R/W	Turns off the cursor	
	7-6	R/W	Reserved	
3?5	0B		**Cursor End Scan Line (CRB**	14-16
	4-0	R/W	Cursor ending line within the character cell	
	6-5	R/W	Cursor skew to right in characters	
	7	R/W	Reserved	
3?5	OC		**Start Address High (CRC)**	14-17
	7-0	R/W	Bits 15-8 of the display start address	
3?5	OD		**Start Address Low (CRD)**	14-17
	7-0	R/W	Bits 7-0 of the display start address	
3?5	OE		**Cursor Location Address High (& Hardware Cursor Foreground Color in Enhanced Mode) (CRE)**	14-17
	7-0	R/W	Bits 15-8 of the cursor location start address. For 4/8 bit Enhanced modes with an 8-bit DAC, this specifies the hardware cursor foreground color	
3?5	OF		**Cursor Location Address Low (& Hardware Cursor Background Color in Enhanced Mode) (CRF)**	14-18
	7-0	R/W	Bits 7-0 of the cursor location start address. For 4/8 bit Enhanced modes with an 8-bit DAC, this specifies the hardware cursor background color	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	10		**Vertical Retrace Start (CR10**	14-18
	7-0	R/W	Vertical retrace start in scan lines	
3?5	11		**Vertical Retrace End (CR11)**	14-18
	3-0	R/W	Vertical retrace end in scan lines	
	4	R/W	Clear the vertical retrace interrupt flip-flop	
	5	R/W	Disable vertical interrupts	
	6	R/W	Five RAM refresh cycles per horizontal line	
	7	R/W	Lock writes to CR0-CR7	
3?5	12		**Vertical Display End (CR12)**	14-19
	7-0	R/W	Number of scan lines of active video	
3?5	13		**Offset (CR13)**	14-20
	7-0	R/W	Memory start address jump from one scan line to the next	
3?5	14		**Underline Location (CR14)**	14-20
	4-0	R/W	Horizontal scan line where underline occurs	
	5	R/W	Memory address counter increment is 4 character clocks	
	6	R/W	Memory accessed as doublewords	
	7	R/W	Reserved	
3?5	15		**Start Vertical Blank (CR15)**	14-21
	7-0	R/W	Horizontal scan line where vertical blanking starts	
3?5	16		**End Vertical Blank (CR16**	14-21
	7-0	R/W	Horizontal scan line where vertical blanking ends	
3?5	17		**CRTC Mode Control (CR17)**	14-22
	0	R/W	Enable bank 2 mode for CGA emulation	
	1	R/W	Enable bank 4 mode for CGA emulation	
	2	R/W	Use horizontal retrace clock divided by 2	
	3	R/W	Enable count by 2 mode	
	4	R/W	Reserved	
	5	R/W	Enable CGA mode address wrap	
	6	R/W	Use byte address mode	
	7	R/W	Horizontal and vertical retrace signals enabled	
3?5	18		**Line Compare (CR18)**	14-23
	7-0	R/W	Line at which memory address counter cleared to 0	
3?5	22		**CPU Latch Data (CR22)**	14-24
	7-0	R	Value in the CPU latch in the graphics controller	
3?5	24,26		**Attribute Controller Flag/Index**	14-24
	5-0	R	Value of the attribute controller index data at 3C0H	
	6	R	Reserved	
	7	R	State of inverted internal address flip-flop	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
Graphics Controller Registers				
3CE			**Graphics Controller Index**	**14-25**
	3-0	R/W	Index to the graphics controller register to be accessed	
	7-4	R/W	Reserved	
3CF			**Graphics Controller Data**	**14-25**
	7-0	R/W	Data to or from the graphics controller register accessed	
3CF	**00**		**Set/Reset (GR0)**	**14-26**
	3-0	R/W	Color value for CPU memory writes	
	7-4	R/W	Reserved	
3CF	**01**		**Enable Set/Reset (GR1)**	**14-26**
	3-0	R/W	Enable planes for writing GR0 data	
	7-4	R/W	Reserved	
3CF	**02**		**Color Compare (GR2)**	**14-27**
	3-0	R/W	Reference color for color compare operations	
	7-4	R/W	Reserved	
3CF	**03**		**Raster Operation/Rotate Counter (GR3)**	**14-27**
	2-0	R/W	Number of right rotate positions for a CPU memory write	
	4-3	R/W	Select raster operation (logical function)	
	7-5	R/W	Reserved	
3CF	**04**		**Read Plane Select (GR4)**	**14-28**
	1-0	R/W	Select planes for reading	
	7-2	R/W	Reserved	
3CF	**05**		**Graphics Controller Mode (GR5)**	**14-29**
	1-0	R/W	Select write mode	
	2	R/W	Reserved	
	3	R/W	Enable read compare operation	
	4	R/W	Select odd/even addressing	
	5	R/W	Select odd/even shift mode	
	6	R/W	Select 256 color shift mode	
	7	R/W	Reserved	
3CF	**06**		**Memory Map Mode Control (GR6)**	**14-30**
	0	R/W	Select graphics mode memory addressing	
	1	R/W	Chain odd/even planes	
	3-2	R/W	Select memory mapping	
	7-4	R/W	Reserved	
3CF	**07**		**Color Don't Care (GR7)**	**14-31**
	3-0	R/W	Select color plane used for color comparison	
	7-4	R/W	Reserved	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3CF	**08**		**Bit Mask (GR8)**	**14-31**
	7-0	R/W	Each bit is a mask for the corresponding memory plane bit	
Attribute Registers				
3C0			**Attribute Controller Index**	**14-32**
	4-0	R/W	Index to the attribute controller register to be accessed	
	5	R/W	Enable video display	
	7-6	R/W	Reserved	
3C1/0			**Attribute Controller Data**	**14-33**
	7-0	R/W	Data to or from the attribute controller register accessed	
3C1/0	**00–0F**		**Palette Register (AR0–ARF)**	**14-33**
	5-0	R/W	Color value	
	7-6	R/W	Reserved	
3C1/0	**10**		**Attribute Mode Control (AR10**	**14-34**
	0	R/W	Select graphics mode	
	1	R/W	Select monochrome display	
	2	R/W	Enable line graphics characters	
	3	R/W	Enable blinking	
	4	R/W	Reserved	
	5	R/W	Enable top panning	
	6	R/W	Select 256 color mode	
	7	R/W	Bits 5-4 of video output come from AR14_1-0	
3C1/0	**11**		**Border Color (AR11)**	**14-35**
	7-0	R/W	Border color value	
3C1/0	**12**		**Color Plane Enable (AR12)**	**14-35**
	3-0	R/W	Display plane enable	
	5-4	R/W	Select inputs to bits 5-4 of 3?AH	
	7-6	R/W	Reserved	
3C1/0	**13**		**Horizontal Pixel Panning (AR13)**	**14-36**
	3-0	R/W	Number of pixels to shift the display to the left	
	7-4	R/W	Reserved	
3C1/0	**14**		**Pixel Padding (AR14)**	**14-37**
	1-0	R/W	Bits 5-4 of the video output if AR10_7 = 1	
	3-2	R/W	Bits 7-6 of the video output	
	7-4	R/W	Reserved	
Setup Registers				
102			**Setup Option Select**	**14-38**
	0	R/W	Chip responds to commands, addresses and data	
	7-1	R/W	Reserved	

Table A-3. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
46E8			**Video Subsystem Enable**	**14-39**
	2-0	W	Reserved	
	3	W	Enable video I/O and memory address decoding	
	4	W	Put chip in setup mode	
	7-5	W	Reserved	
RAMDAC Registers				
3C6			**DAC Mask**	**14-40**
	7-0	R/W	Pixel read mask	
3C7			**DAC Read Index**	**14-40**
	7-0	W	Index to palette register to be read	
3C7			**DAC Status**	**14-41**
	1-0	R	Shows whether previous DAC cycle was a read or write	
	7-2	R	Reserved	
3C8	–		**DAC Write Index**	**14-41**
	7-0	R/W	Index to palette register to be written or General Input Port read data	
3C9			**DAC Data**	**14-42**
	7-0	R/W	Data from register pointed to by DAC Read or Write Index	

A.4 S3 VGA REGISTERS

The Vision964 has additional registers to extend the functions of basic VGA. These registers are located in CRT Controller address space at locations not used by IBM. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

The additional VGA registers are described in the following table:

Table A-4. S3 VGA Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	30		**Chip ID/Rev (CR30)**	15-1
	3-0	R	Chip revision status (stepping)	
	7-4	R	Chip Identification	
3?5	31		**Memory Configuration (CR31)**	15-1
	0	R/W	Enable base address offset (CR6A_6-0)	
	1	R/W	Enable two-page screen image	
	2	R/W	Enable VGA 16-Bit Memory Bus Width	
	3	R/W	Use Enhanced mode memory mapping	
	5-4	R/W	Old display start address bits 17-16 (see CR69_4-0)	
	6	R/W	Enable high speed text display font fetch mode	
	7	R/W	Reserved	
3?5	32		**Backward Compatibility 1 (CR32)**	15-2
	1-0	R/W	Force 7 or 9 dot clocks/character clock	
	2	R/W	Force character clock to high rate (not 1/2 dot clock)	
	3	R/W	Enable backward compatibility modes (CGA, MDA, HGC)	
	5-4	R/W	Reserved	
	6	R/W	Use standard VGA memory wrapping at 256K boundary	
	7	R/W	Tri-state SC[1:0] and SE[3:0]	
3?5	33		**Backward Compatibility 2 (CR33)**	15-3
	0	R/W	Reserved	
	1	R/W	Disable write protection provided by CR11_7 on CR7_1,6	
	2	R/W	Reserved	
	3	R/W	VCLK is inverted DCLK	
	4	R/W	Disable writes to RAMDAC registers (3C6H-3C9H)	
	5	R/W	BLANK signal active during entire non-active video period	
	6	R/W	Disable writes to Palette/Overscan registers (AR0-ARF)	
	7	R/W	Override 3D8H_3 video enable to eliminate flicker	

Table A-4. S3 VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	34		**Backward Compatibility 3 (CR34)**	15-4
	3-0	R/W	Reserved	
	4	R/W	Enable Data Transfer Execute Position register (CR3B)	
	5	R/W	Lock SR1_0 to fix selection of 8/9 dots/character	
	6	R/W	Reserved	
	7	R/W	Lock 3C2H_3-2 to fix DCLK frequency	
3?5	35		**CRT Register Lock (CR35)**	15-5
	3-0	R/W	Old CPU base address (see CR6A_6-0)	
	4	R/W	Lock Vertical Timing registers	
	5	R/W	Lock Horizontal Timing registers	
	7-6	R/W	Reserved	
3?5	36		**Configuration 1 (CR36)**	15-6
	1-0	R	Select System bus (PCI or VL-Bus)	
	3-2	R/W	Select Memory page mode (fast page or EDO)	
	4	R/W	Enable BIOS ROM accesses (VL-Bus)	
	7-5	R/W	Define display memory size	
3?5	37		**Configuration 2 (CR37)**	15-6
	0	R/W	Enable Vision964 operation (VL-Bus)	
	1	R/W	Enable test mode (outputs tri-stated)	
	2	R/W	Select 32K or 64K BIOS ROM size	
	3	R/W	Select dual CAS or dual WE VRAMs	
	4	R/W	Define RAMDAC write snooping (VL-Bus)	
	7-5	R/W	Specify monitor information	
3?5	38		**Register Lock 1 (CR38)**	15-8
	7-0	R/W	Unlock S3 VGA registers (CR30-CR3C)	
3?5	39		**Register Lock 2 (CR39)**	15-8
	7-0	R/W	Unlock System Control, System Extension and Strapping registers (CR40-CR4F, CR50-CR6D)	
3?5	3A		**Miscellaneous 1 (CR3A)**	15-9
	1-0	R/W	Select alternate refresh count per horizontal line	
	2	R/W	Enable alternate refresh count (CR3A_1-0)	
	3	R/W	Enable simultaneous VGA text and Enhanced modes	
	4	R/W	Enable 8-, 16- or 24/32-bit color Enhanced modes	
	5	R/W	Enable high speed text font writing	
	6	R/W	Reserved	
	7	R/W	Disable PCI bus read burst cycles	

Table A-4. S3 VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	3B		**Data Transfer Execute Position (CR3B)**	15-10
	7-0	R/W	Specify VRAM data transfer start position	
3?5	3C		**Interlace Retrace Start (CR3C)**	15-10
	7-0	R/W	Specify interlaced mode retrace start position	

A.5 SYSTEM CONTROL REGISTERS

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

The following table summarizes the System Control registers.

Table A-5. System Control Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	40		**System Configuration (CR40)**	16-1
	0	R/W	Enable Enhanced mode register access	
	3-1	R/W	Reserved	
	4	R/W	Ready Control (VL-Bus)	
	5	R/W	Select write data latch timing (VL-Bus)	
	7-6	R/W	Select A/D bus turnaround non-overlap timing (VL-Bus)	
3?5	41		**BIOS Flag (CR41)**	16-2
	7-0	R/W	Used by the video BIOS	
3?5	42		**Mode Control (CR42)**	16-2
	3-0	R/W	DCLK select when 3C2H_3-2 are 11b	
	4	R/W	Reserved	
	5	R/W	Select Interlaced mode	
	6	R/W	Reserved	

Table A-5. System Control Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	43		**Extended Mode (CR43)**	16-3
	0	R/W	Select 16 bits/pixel double-edge clocking	
	1	R/W	Old DAC register select bit 2	
	2	R/W	Old logical screen width bit 8	
	3	R/W	Reserved	
	4	R/W	Enable I/O port accesses at x148H	
	6-5	R/W	Reserved	
	7	R/W	Enable horizontal counter double mode	
3?5	45		**Hardware Graphics Cursor Mode (CR45)**	16-3
	0	R/W	Enable hardware graphics cursor	
	1	R/W	Reserved	
	3-2	R/W	Select hardware cursor color depth	
	4	R/W	Set up space at right of bit map for hardware cursor	
	5	R/W	The RS3/ODF pin functions as ODF	
	7-6	R/W	Reserved	
3?5	46–47		**Hardware Graphics Cursor Origin-X (CR46-CR47)**	16-4
	10-0	R/W	X-coordinate of the hardware cursor left side	
	15-11	R/W	Reserved	
3?5	48–49		**Hardware Graphics Cursor Origin-Y (CR48-CR49)**	16-5
	10-0	R/W	Y-coordinate of the hardware cursor upper line	
	15-11	R/W	Reserved	
3?5	4A		**Hardware Graphics Cursor Foreground Stack (CR4A)**	16-5
	7-0	R/W	Hardware cursor foreground color (4 registers)	
3?5	4B		**Hardware Graphics Cursor Background Stack (CR4B)**	16-6
	7-0	R/W	Hardware cursor background color (4 registers)	
3?5	4C–4D		**Hardware Graphics Cursor Start Address (CR4C-CR4D)**	16-6
	12-0	R/W	Hardware cursor start address	
	15-13	R/W	Reserved	
3?5	4E		**Hardware Graphics Cursor Pattern Display Start X-Pixel Position (CR4E)**	16-6
	5-0	R/W	Hardware cursor display start x-coordinate	
	7-6	R/W	Reserved	
3?5	4F		**Hardware Graphics Cursor Pattern Display Start Y-Pixel Position (CR4F)**	16-7
	5-0	R/W	Hardware cursor display start y-coordinate	
	7-6	R/W	Reserved	

A.6 SYSTEM EXTENSION REGISTERS

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39). ? = B for monochrome, D for color.

Table A-6. System Extension Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**50**		**Extended System Cont 1 (CR50)**	**17-1**
	0	R/W	Most significant bit of screen width definition (see bits 7-6)	
	1	R/W	Reserved	
	2	R/W	Enable shared frame buffer memory bus arbitration	
	3	R/W	Reserved	
	5-4	R/W	Pixel length select	
	7-6	R/W	With bit 0, screen width definition	
3?5	**51**		**Extended System Cont 2 (CR51)**	**17-2**
	1-0	R/W	Old display start address bits 19-18	
	3-2	R/W	Old CPU base address bits 19-18	
	5-4	R/W	Logical screen width bits 9-8	
	6	R/W	Disable split transfers	
	7	R/W	Reserved	
3?5	**52**		**Extended BIOS Flag 1 (CR52)**	**17-3**
	7-0	R/W	Used by the video BIOS	
3?5	**53**		**Extended Memory Cont 1 (CR53)**	**17-3**
	0	R/W	Enable write per bit	
	3-1	R/W	Reserved	
	4	R/W	Enable memory-mapped I/O access	
	5	R/W	Enable parallel VRAM addressing	
	6	R/W	Enable nibble swap	
	7	R/W	Reserved	
3?5	**54**		**Extended Memory Cont 2 (CR54)**	**17-4**
	7-0	R/W	Reserved	
3?5	**55**		**Extended DAC Control (CR55)**	**17-4**
	1-0	R/W	DAC register select bits 3-2	
	2	R/W	Enable General Input Port read	
	3	R/W	Reserved	
	4	R/W	Enable X-11 windows hardware cursor mode	
	6-5	R/W	Reserved	
	7	R/W	VCLK output pin is tri-stated	

Table A-6. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	56		**External Sync Cont 1 (CR56)**	17-5
	0	R/W	Enable remote mode operation (genlocking)	
	2-1	R/W	Reserved	
	3	R/W	Select vertical counter-only reset sync with genlocking	
	4	R/W	Select odd frame after a vertical counter reset	
	5	R/W	HSYNC, VSYNC and BLANK become tri-state off	
	7-6	R/W	Reserved	
3?5	57		**External Sync Cont 2 (CR57)**	17-6
	3-0	R/W	Vertical reset adjustment from falling edge of VSYNC	
	7-4	R/W	Horizontal reset adjustment from falling edge of VSYNC	
3?5	58		**Linear Address Window Control (CR58)**	17-6
	1-0	R/W	Linear addressing window size	
	2	R/W	Reserved	
	3	R/W	Address latch timing control (VL-Bus)	
	4	R/W	Enable linear addressing	
	5	R/W	Reserved	
	6	R/W	Serial access mode control is 256 words	
	7	R/W	Reserved	
3?5	59-5A		**Linear Address Window Position (CR59-5A)**	17-7
	15-0	R/W	Linear addressing window position bits 31-16	
3?5	5B		**Extended BIOS Flag 2 (CR5B)**	17-8
	7-0	R/W	Used by the video BIOS	
3?5	5C		**General Out Port (CR5C)**	17-8
	3-0	R	Reflection of content of CR42_3-0 (DCLK select bits)	
	7-4	R/W	General Output Port	
3?5	5D		**Extended Horizontal Overflow (CR5D)**	17-9
	0	R/W	Horizontal total bit 8 (CR0)	
	1	R/W	Horizontal display end bit 8 (CR1)	
	2	R/W	Start horizontal blank bit 8 (CR2)	
	3	R/W	BLANK pulse extended by 64 DCLKs	
	4	R/W	Start horizontal sync position bit 8 (CR4)	
	5	R/W	HSYNC pulse extended by 32 DCLKs	
	6	R/W	Data transfer execute position bit 8 (CR3B)	
	7	R/W	Bus grant terminate position bit 8 (CR5F)	

Table A-6. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	5E		**Extended Vertical Overflow (CR5E)**	17-9
	0	R/W	Vertical total bit 10 (CR6)	
	1	R/W	Vertical display end bit 10 (CR12)	
	2	R/W	Start vertical blank bit 10 (CR15)	
	3	R/W	Reserved	
	4	R/W	Vertical retrace start bit 10 (CR10)	
	5	R/W	Reserved	
	6	R/W	Line compare position bit 10 (CR18)	
	7	R/W	Reserved	
3?5	5F		**Bus Grant Termination Position (CR5F)**	17-10
	7-0	R/W	Termination position in character clocks for BGNT signal	
3?5	60		**Extended Memory Control 3 (CR60)**	17-10
	7-0	R/W	Reserved	
3?5	61		**Extended Memory Control 4 (CR61)**	17-11
	7-0	R/W	Reserved	
3?5	62		**Extended Memory Control 5 (CR62)**	17-11
	7-0	R/W	Reserved	
3?5	63		**External Sync Delay Adjust High (CR63)**	17-12
	3-0	R/W	VSYNC reset adjustment - upper 4 bits	
		R/W	HSYNC reset adjustment - upper 4 bits	
3?5	64		**Genlocking Adjustment (CR64)**	17-12
	2-0	R/W	Horizontal counter dot addition adjustment	
	3	R/W	Enable for bits 2-0	
	6-4	R/W	Character clock phase adjustment	
	7	R/W	Enable for bits 6-4	
3?5	65		**Extended Miscellaneous Control (CR65)**	17-13
	0	R/W	Delay falling edge of SE	
	1	R/W	Disable early SC[1:0] output when split transfers enabled	
	2	R/W	Enable 3C3H port for video subsystem setup	
	5-3	R/W	Reserved	
	7-6	R/W	Serial/parallel addressing specification	
3?5	66		**Extended Miscellaneous Control 1 (CR66)**	17-14
	2-0	R/W	SC, SE and VCLK = fractions of DCLK	
	3	R/W	SC0 = VCLK and SC1 = inverted VCLK	
	5-4	R/W	Select SID operation mode	
	6	R/W	PA[7:0] are tri-stated off	
	7	R/W	Enable PCI bus disconnect	

Table A-6. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	67		**Extended Miscellaneous Control 2 (CR67)**	17-15
	0	R/W	VCLK is in phase with DCLK	
		R/W	Reserved	
3?5	68		**Configuration 3 (CR68)**	17-15
		R/W	CAS, WE and OE stretch time selection	
		R/W	Memory address depth select	
		R/W	RAS low timing select	
		R/W	RAS precharge timing select	
3?5	69		**Extended System Control 3 (CR69)**	17-16
	4-0	R/W	Display start address bits 20-16	
	7-5	R/W	Reserved	
3?5	6A		**Extended System Control 4 (CR6A)**	17-16
	6-0	R/W	CPU base address bits 20-14	
	7	R/W	Reserved	
3?5	6B		**Extended BIOS Flag 3 (CR6B)**	17-17
	7-0	R/W	Used by the video BIOS	
3?5	6C		**Extended BIOS Flag 4 (CR6C)**	17-17
	7-0	R/W	Used by the video BIOS	
3?5	6D		**Extended Miscellaneous Control (CR6D**	17-17
	2-0	R/W	Number of DCLK periods to delay BLANK	
	3	R/W	Reserved	
	6-4	R/W	Number of VCLK units to delay SC[1:0]	
	7	R/W	Reserved	

A.7 ENHANCED COMMANDS REGISTERS

This section lists the registers which support the Vision964 enhanced drawing functions. All of these registers are byte or word-addressed and are enabled only if bit 0 of the System Configuration register (CR40) is set to 1.

Table A-7. Enhanced Commands Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
42E8			**Subsystem Status**	**18-1**
	0	R	Vertical sync interrupt status	
	1	R	Graphics Engine busy interrupt status	
	2	R	FIFO overflow interrupt status	
	3	R	FIFO empty interrupt status	
	6-4	R	General Input Port data from power-on strapping	
	7	R	4 or 8 bit planes	
	15-8	R	Reserved	
42E8			**Subsystem Control**	**18-2**
	0	W	Clear vertical sync interrupt status	
	1	W	Clear Graphics Engine busy interrupt status	
	2	W	Clear FIFO overflow interrupt status	
	3	W	Clear FIFO empty interrupt status	
	7-4	W	Reserved	
	8	W	Vertical sync interrupt enabled	
	9	W	Graphics Engine busy interrupt enabled	
	10	W	FIFO overflow interrupt enabled	
	11	W	FIFO empty interrupt enabled	
	13-12	W	Reserved	
	15-14	W	Graphics Engine software reset selection	
4AE8			**Advanced Function Control**	**18-3**
	0	R/W	Enable Enhanced mode functions	
	1	R/W	Reserved	
	2	R/W	Specify 4 bits/pixel Enhanced mode	
	3	R/W	Reserved	
	4	R/W	Enable linear addressing	
	5	R/W	Enable memory-mapped I/O	
	15-6	R/W	Reserved	
82E8			**Current Y Position**	**18-4**
	11-0	R/W	Pixel vertical screen coordinate	
	15-12	R/W	Reserved	
86E8			**Current X Position**	**18-4**
	11-0	R/W	Pixel horizontal screen coordinate	
	15-12	R/W	Reserved	

Table A-7. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8AE8			**Destination Y Position/ Axial Step Constant**	**18-5**
	11-0/ 13-0	R/W	Destination Y position for BitBlts and pattern fills/Axial step constant for line draws	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
8EE8			**Destination X Position/ Diagonal Step Constant**	**18-5**
	11-0/ 13-0	R/W	Destination X position for BitBlts and pattern fills/Axial step constant for line draws	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
92E8			**Error Term**	**18-6**
	13-0	R/W	Error term for line draws	
	15-14	R/W	Reserved	
96E8			**Major Axis Pixel Count**	**18-6**
	11-0	R/W	Length of the longest axis (pixels - 1)	
	15-12	R/W	Reserved	
9AE8			**Graphics Processor Status**	**18-7**
	7-0	R	Low 8 bits of field showing FIFO slots available (see bits 15-11)	
	8	R	Reserved	
	9	R	Graphics Engine busy	
	10	R	All FIFO slots empty	
	5-11	R	High 5 bits of FIFO status (see bits 7-0)	
9AE8			**Drawing Command**	**18-8**
	0	W	Reserved	
	1	W	Select across the plane pixel mode	
	2	W	Last pixel will not be drawn	
	3	W	Select radial drawing direction	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	8	W	Wait for CPU data	
	10-9	W	Select system bus size	
	11	W	Reserved	
	12	W	Enable byte swap	
	15-13	W	Select command type	
9EE8			**Short Stroke Vector Transfer**	**18-10**
	3-0	W	Length of vector 1 (pixels - 1)	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	15-8	W	Duplicate of bits 7-0 to define second short stroke vector	
A2E8			**Background Color**	**18-11**
	31-0	R/W	Background color value	

Table A-7. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
A6E8			**Foreground Color**	**18-11**
	31-0	R/W	Foreground Color value	
AAE8			**Bitplane Write Mask**	**18-12**
	31-0	R/W	Each bit enables updating of corresponding bit plane	
AEE8			**Bitplane Read Mask**	**18-12**
	31-0	R/W	Each bit enables reading of corresponding bit plane	
B2E8			**Color Compare**	**18-13**
	31-0	R/W	Color value to be compared with current bitmap color	
B6E8			**Background Mix**	**18-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BAE8			**Foreground Mix**	**18-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BEE8			**Read Register Data**	**18-14**
	15-0	R	Data from register selected by bits 2-0 of BEE8H_E	
BEE8	**0**		**Minor Axis Pixel Count**	**18-15**
	11-0	W	Rectangle height (pixels - 1)	
	15-12	W	Reserved	
BEE8	**1**		**Top Scissors**	**18-15**
	11-0	W	Top side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**2**		**Left Scissors**	**18-15**
	11-0	W	Left side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**3**		**Bottom Scissors**	**18-16**
	11-0	W	Bottom side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**4**		**Right Scissors**	**18-16**
	11-0	W	Right side of the clipping rectangle	
	15-12	W	Reserved	

Table A-7. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
BEE8	**A**		**Pixel Control**	**18-16**
	5-0	W	Reserved	
	7-6	W	Select mix register	
	11-8	W	Reserved	
	15-12	W	0AH (index)	
BEE8	**D**		**Multifunction Control Miscellaneous 2**	**18-17**
	2-0	W	Destination base address location in memory	
	3	W	Reserved	
	6-4	W	Source base address location in memory	
	11-7	W	Reserved	
	15-12	W	0DH (index)	
BEE8	**E**		**Multifunction Control Miscellaneous**	**18-18**
	1-0	W	Destination base address bits 21-20	
	3-2	W	Source base address bits 21-20	
	4	W	Select upper word for 32-bit register accesses	
	5	W	Only pixels outside the clipping rectangle are drawn	
	6	W	Select slow read/modify/write cycle	
	7	W	Don't update bitmap if source is not equal to color compare color	
	8	W	Enable color comparison	
	9	W	Select 32-bit command registers	
	11-10	W	Reserved	
	15-12	W	0EH (index)	
BEE8	**F**		**Read Register Select**	**18-19**
	2-0	W	Select register to be read	
	11-4	W	Reserved	
	15-12	W	0FH (index)	
E2E8			**Pixel Data Transfer**	**18-15**
	15-0	W	Data transfer register (CPU to Graphic Engine) - low word	
E2EA			**Pixel Data Transfer-Extension**	**18-20**
	15-0	W	Data transfer register (CPU to Graphic Engine) - high word	

A.8 PCI CONFIGURATION SPACE REGISTERS

When a PCI configuration read or write command is issued, AD[7:0] contain the address of the register in the configuration space to be accessed.

Table A-8. PCI Configuration Space Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
00			**Vendor ID**	**19-1**
	15-0	R	Hardwired to 5333H	
02			**Device ID**	**19-2**
	15-0	R	Hardwired to 88D0H	
04			**Command**	**19-2**
	0	R/W	Response to I/O space accesses enabled	
	1	R/W	Response to memory space accesses enabled	
	4-2	R/W	Reserved	
	5	R/W	No response to RAMDAC register accesses	
	15-6	R/W	Reserved	
06			**Status**	**19-3**
	8-0	R/W	Reserved	
	10-9	R/W	Hardwired to select medium device select timing	
	15-11	R/W	Reserved	
08			**Revision ID**	
	7-0	R/W	Revision level of the chip (stepping)	
0A			**Programming Interface**	**19-3**
	0	R/W	Hardwired to indicate support for standard VGA programming	
	7-1	R/W	Reserved	
10			**Base Address 0**	**19-4**
	0	R/W	Hardwired to indicate base registers map into memory space	
	2-1	R/W	Hardwired to allow mapping anywhere in 32-bit address space	
	3	R/W	Hardwired to indicate does not meet prefetchable requirements	
	22-4	R/W	Reserved	
	31-23	R/W	Base address 0	
30			**BIOS Base Address**	**19-5**
	0	R/W	Enable access to BIOS ROM address space	
	15-1	R/W	Reserved	
	31-16	R/W	Upper 16 bits of BIOS ROM address	

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		8		°C/W
Thermal Resistance Θ_{JA} (Still Air)		37		°C/W
Power Dissipation			1.75	W
Junction Temperature			125	°C

2.2 MECHANICAL DIMENSIONS

The Vision964 comes in a 208-pin PQFP package. The mechanical dimensions are given in Figure 2-1.

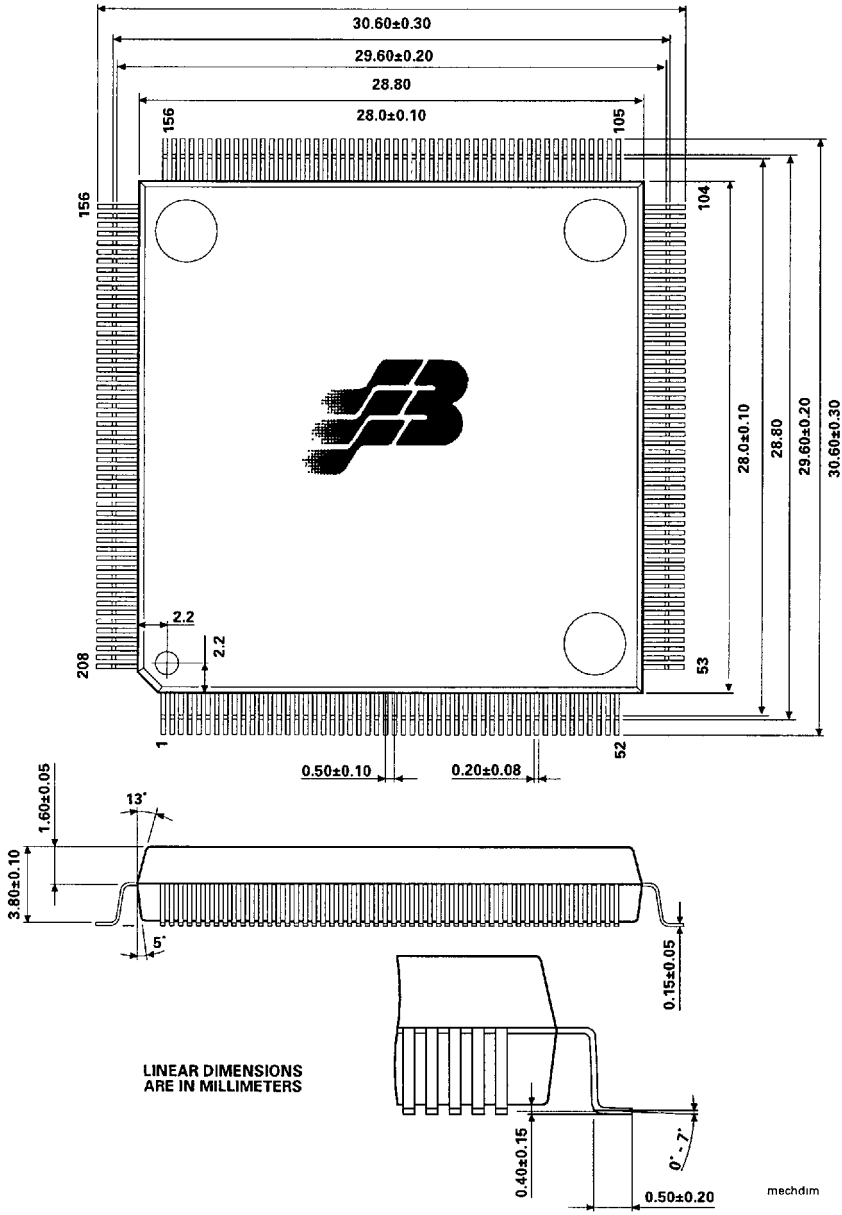


Figure 2-1. 208-pin PQFP Mechanical Dimensions