CMOS 8-Bit Microcontroller

TMP87C444N, TMP87C844N

The 87C444/844 is the high speed and high performance 8-bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input/output ports, two multi-function timer/counters, serial bus interface, 8-bit D/A conversion outputs and 8-bit A/D conversion inputs on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87C444N	4 Kbytes	256 bytes	P-SDIP42-600-1.78	TMP87P844N
TMP87C844N	8 Kbytes			

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Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time: 0.5 μs (at 8 MHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
- Bit manipulations(Set/Clear/Complement/Move/Test/Exclusive Or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump / Vector call)

◆10 interrupt sources (External: 3, Internal: 7)
- All sources have independent latches each, and nested interrupt control is available.
- 3 edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

◆5 Input/Output ports (34 pins)
◆Two 16-bit Timer/Counters
Timer, Event counter, Programmable Pulse Generator output
Pulse width measurement, External trigger timer, Window modes
◆Time Base Timer (Interrupt frequency: 1 Hz to 15625 Hz)
◆Divider output function (frequency: 1 kHz to 8 kHz)
◆Watchdog Timer
- Interrupt source/reset output (programmable)

◆Serial bus Interface
- I2C-bus, 8-bit SIO modes: 1 channel
- 8-bit SIO: 1 channel

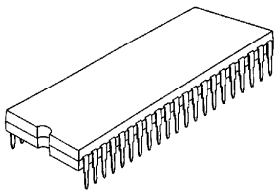
◆8-bit D/A converter
- 8 analog outputs
- Builtin OP-Amp.

◆8-bit successive approximate type A/D converter with sample and hold
- 4 analog inputs
- Conversion time: 23 μs at 8 MHz

◆Power saving operating modes
- IDLE mode: CPU stops, and Peripherals operate. Release by interrupts.

◆Operating voltage: 4.5 to 5.5 V at 8 MHz
◆Emulation Pod: BM87C844N0A

P-SDIP42-600-1.78



TMP87C844N
TMP87C444N
TMP87P844N

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Pin Assignments (Top View)

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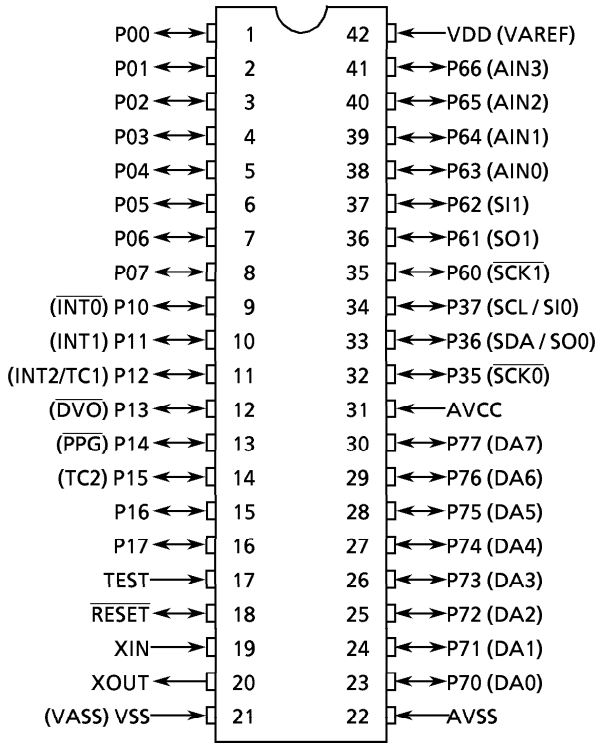

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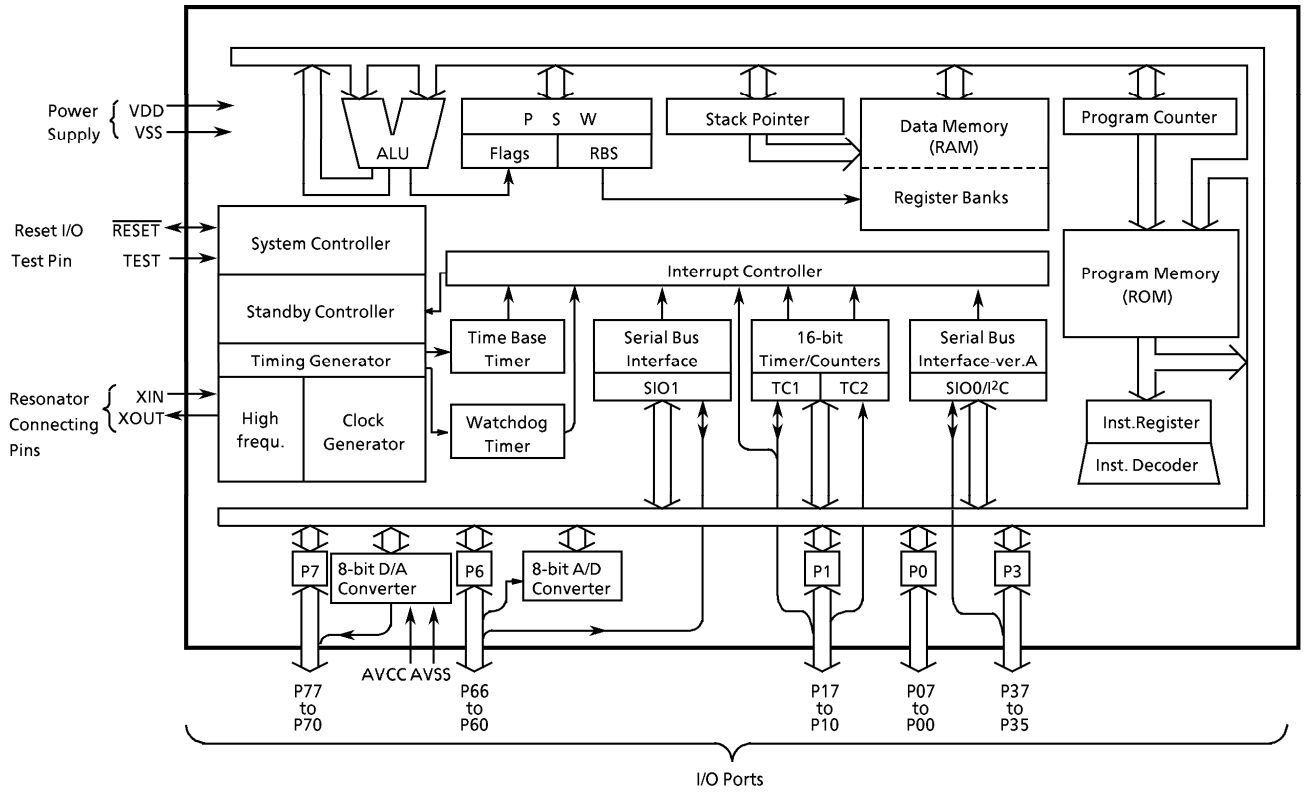
Block Diagram



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Pin Function

Pin Name	Input/Output	Function	
P07~P00	I/O	Two 8-bit programmable input/output ports (tri-state) Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output or a PPG output, the latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer / Counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2/TC1)	I/O (Input)		External interrupt input 2 or Timer / Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P37 (SCL/SI0)	I/O (I/O/Input)	3-bit input/output port with latch. When used as an input port or a SBI input/output, the latch must be set to "1".	I^2C bus serial clock input/output or SIO0 serial data input
P36 (SDA/SO0)	I/O (I/O/Output)		I^2C bus serial data input/output or SIO0 serial data output
P35 ($\overline{SCK0}$)	I/O (I/O)		SIO0 serial clock input/output
P66 (AIN3) ~P63 (AIN0)	I/O (Input)	7-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as a SIO1 input/output the latch must be set to "1". When used as an analog input, select analog input enable in the ADCCR.	A/D converter analog inputs
P62 (SI1)	I/O (Input)		SIO1 serial data input
P61 (SO1)	I/O (Output)		SIO1 serial data output
P60 ($\overline{SCK1}$)	I/O (I/O)		SIO1 serial clock input/output
P77 (DA7) ~P70 (DA0)	I/O (Output)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. (Only the case of the DACCR1 = "1", I/O contorol can be available). When used as an analog output, the DACCR1 must be set to "0".	D/A converter analog outputs
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD (VAREF)	Power Supply	+ 5 V	Analog reference voltage input for the A/D converter (High)
VSS (VASS)		0 V (GND)	Analog reference voltage input for the A/D converter (Low)
AVCC		Analog reference voltage input for the D/A converter (High)	
AVSS		Analog reference voltage input for the D/A converter (0V)	

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OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87C444/844. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR / DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

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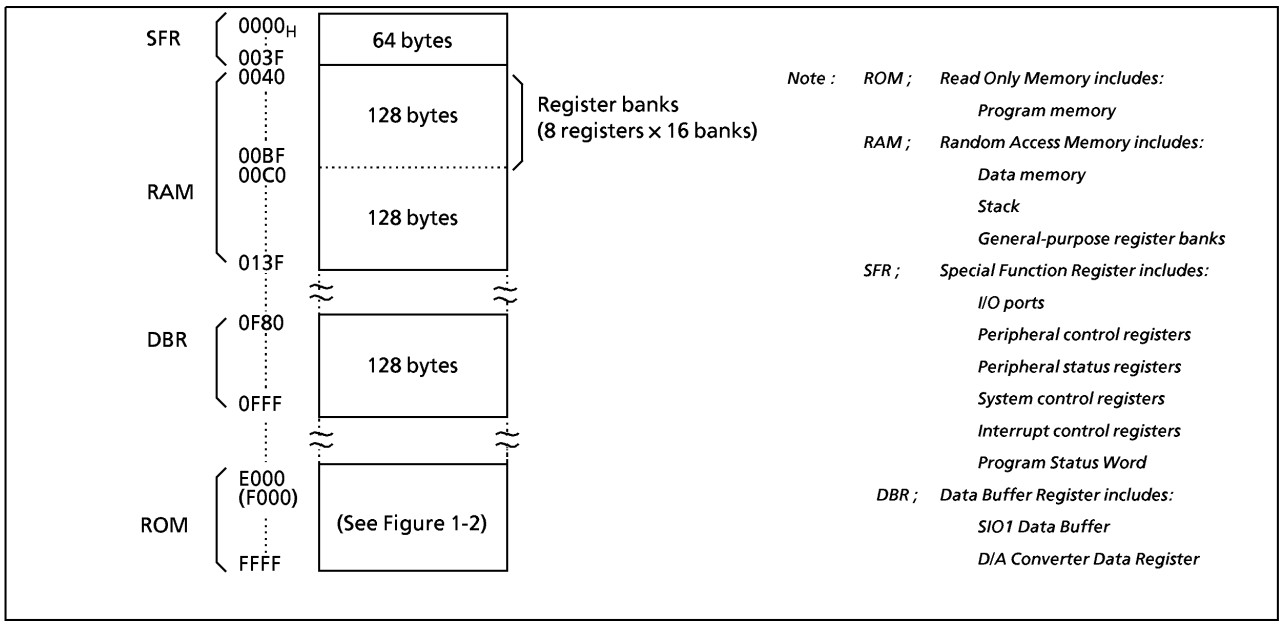

Figure 1-1. Memory Address Map

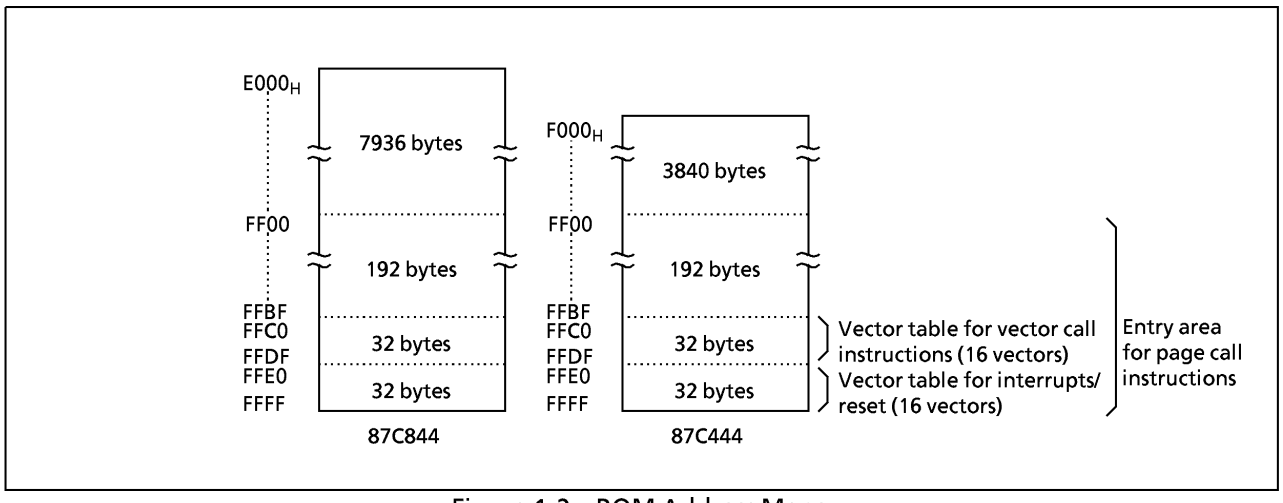

Figure 1-2. ROM Address Maps

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Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except $\overline{RESET}$	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P3, P6, P7	3.2	mA
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P3, P6, P7	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

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Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	8.0	MHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

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D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5V, V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports and Tri-state ports					
	I_{IN3}	$\overline{RESET}$					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
	R_{IN3}	Port P7		4	6	10	
Output Leakage Current	I_{LO1}	Open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	± 2	
Output High Voltage	V_{OH1}	Tri- state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
	V_{OH2}	Port P7	V_{DD} = 4.5 V, I_{OH} = – 0.2 mA				
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Supply Current in NORMAL mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 8 MHz	–	8	14	mA
Supply Current in IDLE mode				–	4	6	mA

Note 1: Typical values show those at T_{opr} = 25°C, V_{DD} = 5V.
Note 2: Input Current: I_{IN1}, I_{IN3} ; The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{AREF} / I_{DREF}.

A/D Conversion Characteristics

(Topr = – 30 to 70°C: V_{SS} = V_{ASS} = 0V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	V_{DD} = V_{AREF}	4.5	—	5.5	V
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{AREF}		—	0.5	1.0	mA
Nonlinearity Error		V_{AREF} = V_{DD} = 5.000 V V_{ASS} = V_{SS} = 0.000 V	—	—	± 2	LSB
Zero point Error			—	—	± 2	
Full Scale Error			—	—	± 2	
Total Error			—	—	± 3	

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D/A Conversion Characteristics

($V_{SS} = A_{VSS} = 0$, $V_{DD} = 4.5$ to 5.5 V, Topr = – 30 to 70°C)

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage		A_{VCC}		4.5	–	V_{DD}	V
Current Dissipation		I_{DREF}	No Loading, All channel operating	–	–	25	mA
Resolution				–	–	8	bits
Accuracy	Nonlinearity Error		A_{VCC} = 5.000 V: A_{VSS} = 0.000 V	–	–	± 2.0	LSB
	Differential Nonlinearity Error		Monotonicity Guarantee (Note)	–	–	± 3/4	
Settling time		T_{SU}	Loading condition: c = 15 pF	–	–	20	ms
OP-Amp output Voltage Range		V_{AO}	No Loading	0.03	–	A_{VCC} – 0.25	V
			I_{AO} = 1.2 mA / I_{AO} = – 200 μA	0.3	–	A_{VCC} – 0.3	
OP-Amp output Drive Range		I_{AO}	A_{VCC} – 0.5 to 0.5V	–	+ 2/ – 1	–	mA
Maximum Capacitors connected to D/A output		C_{OL}		–	–	15	pF

Note: Differential nonlinearity error does not include quantizing error.

A.C. Characteristics

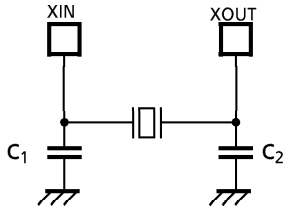
(V_{SS} = 0V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.5	–	4	μs
		In NORMAL mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) , fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					

Recommended Oscillating Condition

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Conditions	
					C_1	C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
	Crystal Oscillator	8 MHz	TOYOKOM	210B 8.0000	20 pF	20 pF



High-frequency

Note: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube).

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