FlashFlex51 MCU
SST89C54 / SST89C58

Data Sheet

FEATURES:

- **8-bit 8051-Compatible Microcontroller (MCU) with Embedded SuperFlash Memory**
  - Fully Software Compatible
  - Development Toolset Compatible
  - Pin-For-Pin Package Compatible
- **SST89C54/58 Operation**
  - 0 to 33MHz at 5V
- **256 Bytes Internal RAM**
- **Dual Block SuperFlash EEPROM**
  - SST89C58:
    32 KByte primary block (128-Byte sector size) +
    4 KByte secondary block (64-Byte sector size)
  - SST89C54:
    16 KByte primary block (128-Byte sector size) +
    4 KByte secondary block (64-Byte sector size)
  - Individual Block Security Lock with SoftLock
  - Concurrent operation during
    In-Application Programming (IAP)
  - Memory Re-mapping for Interrupt Support during IAP
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **Three High Current Drive Ports (16 mA each)**
- **Three 16-bit Timers/Counters**
- **Full-Duplex Serial Port (UART)**
- **Six Interrupt Sources at 2 Priority Levels**
- **Programmable Watchdog Timer (WDT)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **TTL- and CMOS-Compatible Logic Levels**
- **Low Power Modes**
  - Power-down Mode with External Interrupt Wake-up
  - Standby (Stop Clock)
- **Low Voltage at 2.7V (0 to 12MHz)**
- **PDIP-40, PLCC-44 and TQFP-44 Packages**
- **Temperature Ranges:**
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)

PRODUCT DESCRIPTION

The SST89C54 and SST89C58 are members of the FlashFlex51 family of 8-bit microcontroller products designed and manufactured with the state-of-the-art SuperFlash CMOS semiconductor process technology. The device uses the same 8051 instruction set and is pin-for-pin compatible with standard 8051 microcontroller devices.

The device comes with 20/36 KByte of on-chip flash EEPROM program memory using SST's patented and proprietary CMOS SuperFlash EEPROM technology with SST's field-enhancing, tunneling injector, split-gate memory cells. The SuperFlash memory is partitioned into 2 independent program memory blocks. The primary SuperFlash Block 0 occupies 16/32 KByte of internal program memory space and the secondary SuperFlash Block 1 occupies 4 KByte of internal program memory space. The 4 KByte secondary SuperFlash block can be mapped to the highest or lowest location of the 64 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory. The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and firmware for SST's devices. During the power-on reset, the device can be configured as a slave to an external host for source code storage or as a master to an external host for an in-application programming (IAP) operation. The device is designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The device is pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. An example of bootstrap loader is available for the user's reference and convenience only. SST does not guarantee the functionality nor the usefulness of the sample bootstrap loader. Chip-Erase operations will erase the pre-programmed sample code.

In addition to 20/36 KByte of SuperFlash EEPROM program memory on-chip, the device can address up to 64 KByte of external program memory. In addition to 256 x8 bits of on-chip RAM, up to 64 KByte of external RAM can be addressed.

SST's highly reliable, patented SuperFlash technology and memory cell architecture have a number of important advantages for designing and manufacturing flash EEPROMs. These advantages translate into significant cost and reliability benefits for our customers.

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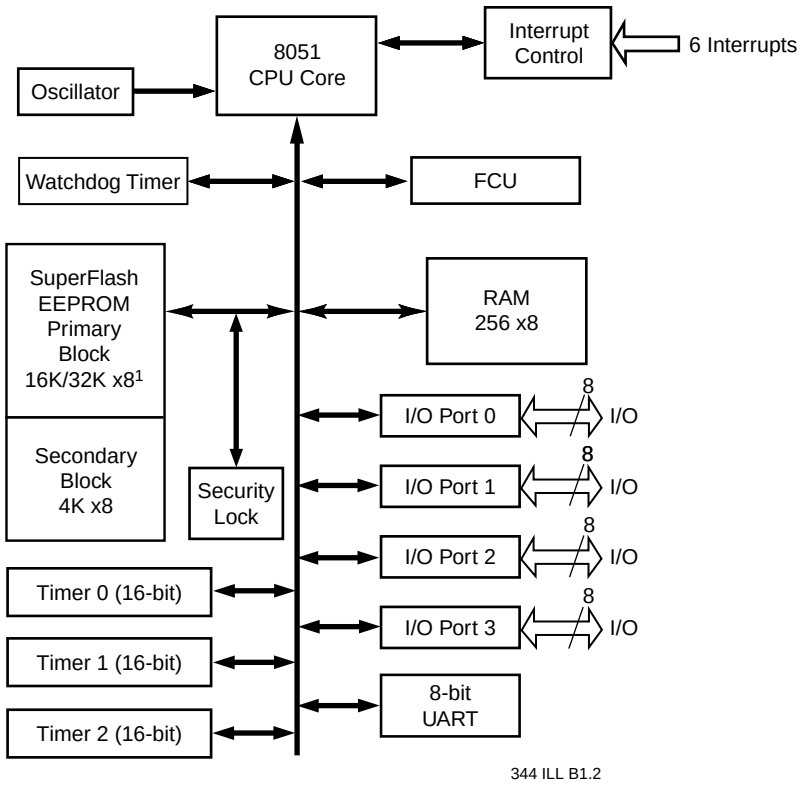
1.0 FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



1. 16K x 8 for SST89C54
   32K x 8 for SST89C58

FCU = Flash Control Unit
8051 CPU Core = ALU, ACC, B-Reg., Instruction Reg., PC, Timing and Control, etc.

2.0 PIN ASSIGNMENTS

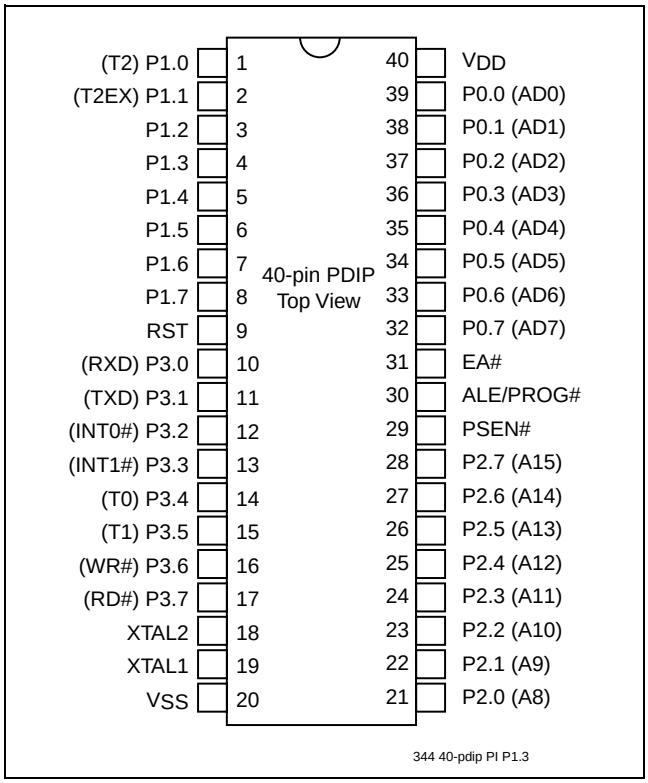


FIGURE 2-1: PIN ASSIGNMENTS FOR 40-PIN PDIP

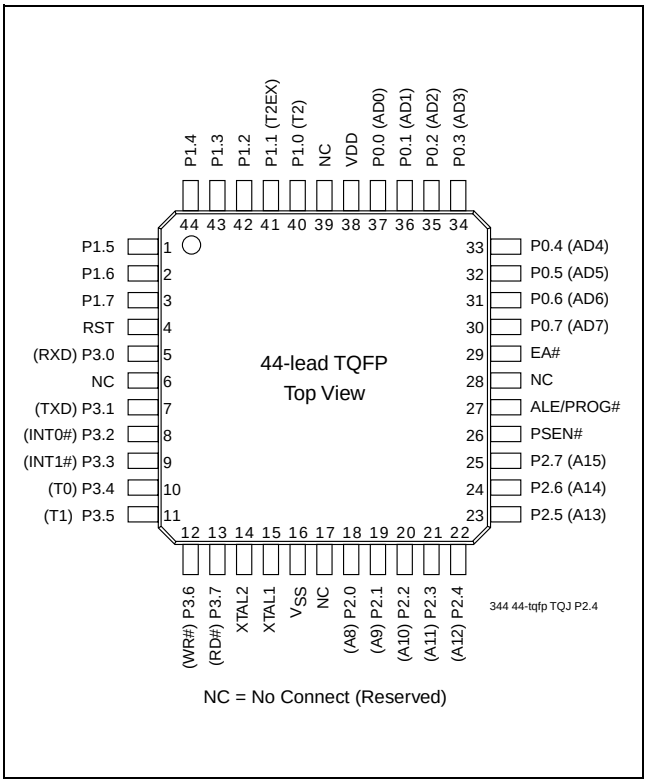


FIGURE 2-2: PIN ASSIGNMENTS FOR 44-LEAD TQFP

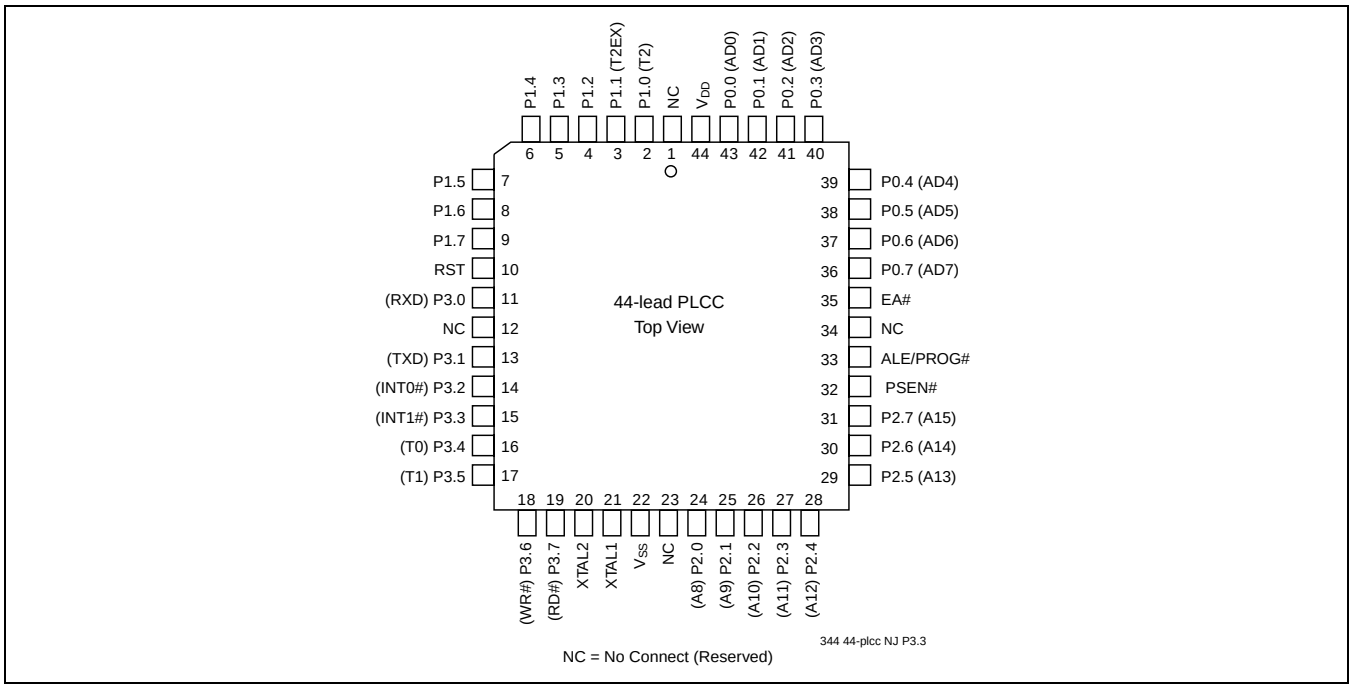


FIGURE 2-3: PIN ASSIGNMENTS FOR 44-LEAD PLCC

2.1 Pin Descriptions

TABLE 2-1: PIN DESCRIPTIONS (1 OF 2)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P1[7:0]	I/O with internal pull-ups	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have '1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. P1[5, 6, 7] have high current drive of 16mA. Port 1 also receives the low-order address bytes during external host mode programming and verification.
P1[0]	I	**T2:** External count input to Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger
P2[7:0]	I/O with internal pull-ups	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have '1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application it uses strong internal pull-ups when outputting '1's. Port 2 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3[7:0]	I/O with internal pull-ups	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have '1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. Port 3 serves the functions of various special features of the device. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3[0]	I	**RXD:** UART - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 input
P3[3]	I	**INT1#:** External Interrupt 1 input
P3[4]	I	**T0:** External Count input to Timer/Counter 0
P3[5]	I	**T1:** External Count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to External Program Memory. When the device is executing code from Internal Program Memory, PSEN# is inactive ("H"). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to External Data Memory. While the RST input is continually held high (for more than ten machine cycles), a forced high-to-low input transition on the PSEN# pin will bring the device into the external host mode programming.

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TABLE 2-1: PIN DESCRIPTIONS (2 OF 2)

Symbol	Type[1]	Name and Functions
RST	I	**Reset:** A high logic state on this pin for two machine cycles, while the oscillator is running, will reset the device. If the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held high, the device will enter the external host mode. Otherwise, the device will enter the normal operation mode.
EA#	I	**External Access Enable:** EA#[2] must be connected to V_{IL} in order to enable the device to fetch code from External Program Memory. EA# must be strapped to V_{IH} for internal program execution. However, security lock level 4 will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[3] of 12V (see Electrical Specification, Section 12.0).
ALE/ PROG#[4]	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[5] is emitted at a constant rate of 1/6 the crystal frequency and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory.
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generation circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. EA# is not sampled and latched on reset after level 2 or level 3 locked. MCU will jump to run internal code if EA# changes from V_{IL} to V_{IH}. This is a security compromise. Use level 4 lock to fix.
3. It is not necessary to receive a 12V programming supply voltage during flash programming.
4. Applying 10-50 KΩ pull-up resistor to this pin may improve the device's performance.
5. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.

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3.0 MEMORY ORGANIZATION

The SST89C54/58 has separate address spaces for program and data memory.

3.1 Program Flash Memory

There are two internal flash memory blocks in the SST89C54/58. The primary flash memory Block 0 has 16/32 KByte and occupies the address space 0000H to 3FFFH/7FFFH. The secondary flash memory Block 1 has 4 KByte and occupies the address space F000H to FFFFH.

The 16/32K x8 primary SuperFlash block is organized into 128/256 sectors. Each sector contains 2 rows and each row has 64 Bytes.

The 4K x8 secondary SuperFlash block is organized into 64 sectors. Each sector contains 2 rows. Each row contains 32 Bytes. Figure 3-1 shows the sector organization for SST89C54/58.

When internal code operation is enabled (EA# = 1), the primary 16/32 KByte flash memory block is always visible to the program counter for code fetching. Figures 3-2 and 3-3 show the program memory organizations for the SST89C54/58.

When internal code operation is enabled (EA# = 1), the secondary 4 KByte flash memory block is selectively visible for code fetching. When bit 7 of the SuperFlash Configuration mailbox register (SFCF[7]), is set, the secondary 4 KByte block will be visible for code fetching.

3.1.1 Code Corruption Due to Brown-out

The MCU will still run a user's application code even if the V_{DD} drops down to 2V, far below the minimum working voltage of 2.7V. This can cause the program counter (PC) to get lost and sometimes lead to code corruption. The solution is to use an off-chip voltage supervisory chip to keep the MCU in reset state whenever the V_{DD} drops below 2.7V.

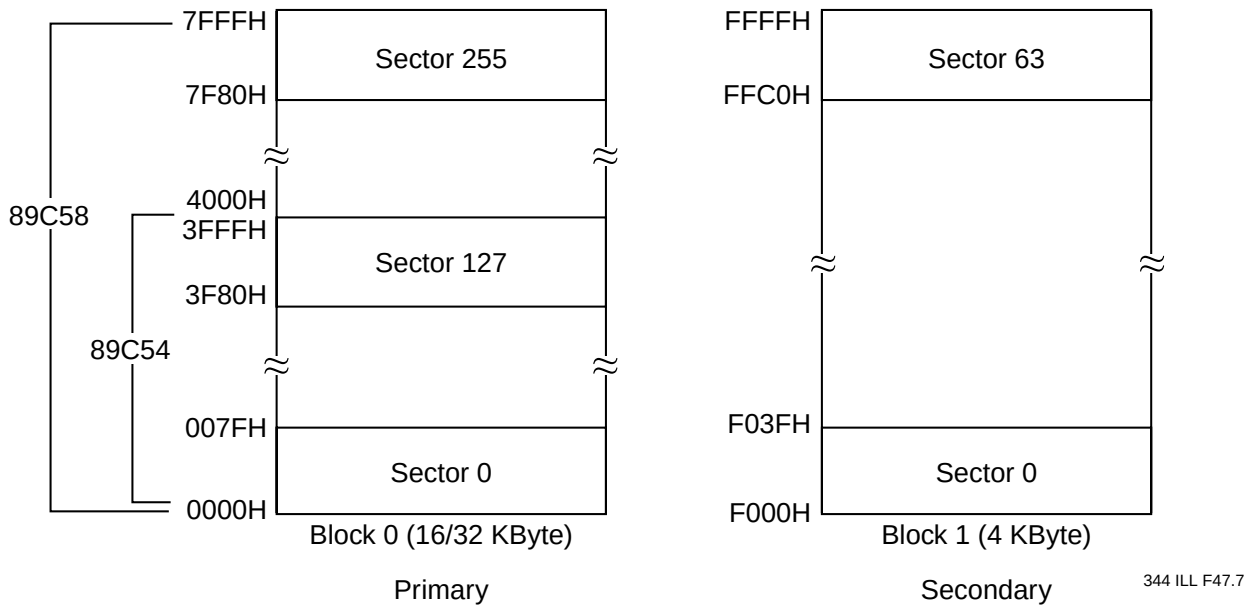

FIGURE 3-1: SECTOR ORGANIZATION

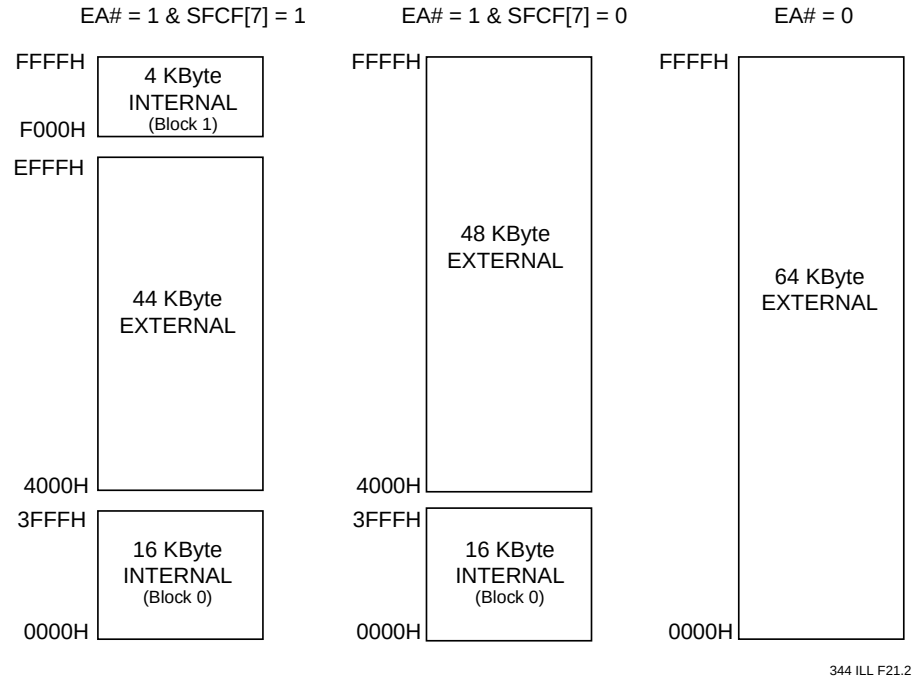

FIGURE 3-2: SST89C54 PROGRAM MEMORY ORGANIZATION

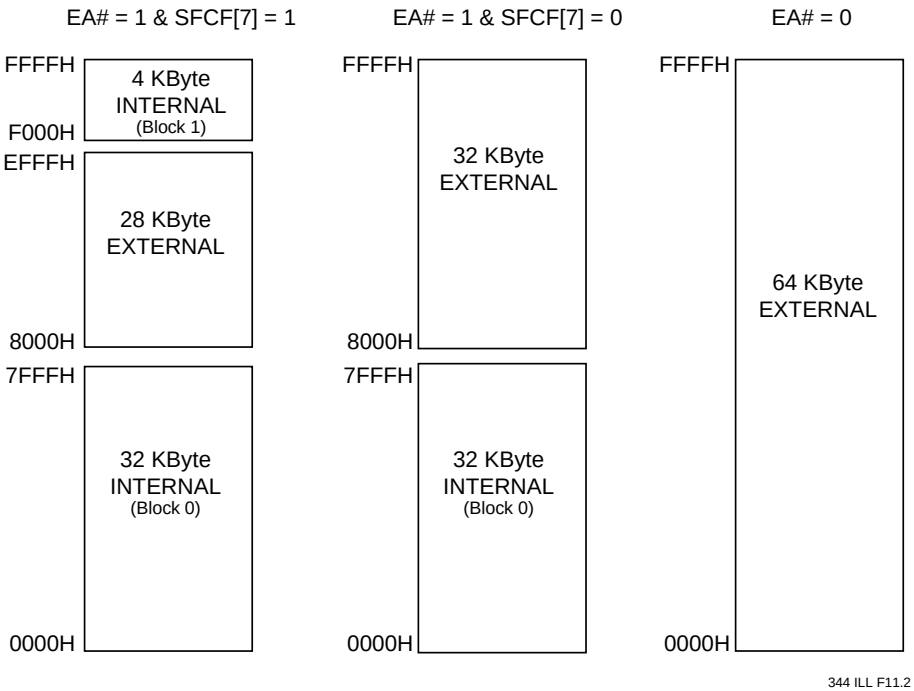

FIGURE 3-3: SST89C58 PROGRAM MEMORY ORGANIZATION

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3.2 Memory Re-mapping

The SST89C54/58 memory re-mapping feature allows users to re-map the secondary flash memory block physical address to overlay the lower order logical address so that interrupts can be serviced when the primary flash memory block (Block 0) is busy under Program/Erase operation.

Since Block 0 occupies the low order program address space of the 8051 architecture where the interrupt vectors reside, those interrupt vectors will normally not be available when Block 0 is being programmed.

SST89C54/58 provides four options of memory re-mapping (Refer to Table 3-1). When the lowest 4 KByte are re-mapped, any program access within logical address range 0000H-0FFFH will have the 4 most significant address bits forced to "1", redirecting the access to F000H-FFFFH. Note that the physical contents of the overlaid portion of Block 0 (i.e. physical locations 0000H-0FFFH in the current example) will not be addressable by the program counter, but only accessible through IAP registers. Block 1 is still accessible through F000H-FFFFH. Block 1 is addressable by the program counter in both logical address ranges 0000H-0FFFH and F000H-FFFFH.

3.2.1 Activation and Deactivation of Memory Re-mapping

The actual amount of memory that is re-mapped is controlled by Map-En[1:0] bits as shown in Table 3-1. The Map-En[1:0] bits are the same bits as SFCF[1:0]. The Map-En[1:0] bits are under software control and can be changed during program execution. Since changing re-mapping will cause program re-location, it is advisable that the instruction that changes the Map-En[1:0] be in the portion of memory that is not affected by the re-mapping change. (See Figures 3-4 and 3-5 and the application note, *Memory Re-Mapping of the SST89C54/58 Microcontroller*).

The Map-En[1:0] bits are initialized at Reset according to the contents of two non-volatile register bits, Re-Map[1:0]. The Re-Map[1:0] bits are programmed via PROG_RB1 and PROG_RB0 external host mode and IAP commands. Refer to "External Host Programming Mode" in Section 4.1 or IAP section for description.

The contents of Map-En[1:0] are only updated according to Re-Map[1:0] on a successful reset. Any subsequent alteration to the Re-Map[1:0] bits will not automatically change the Map-En[1:0] bits without a reset. Similarly, changes to Map-En[1:0] during program execution will not change Re-Map[1:0] bits.

To deactivate memory re-mapping, a Chip-Erase operation will revert Re-Map[1:0] to the default status of "11", disabling re-map. Programming 00b to Map-En register also deactivates memory re-mapping, during the run time.

TABLE 3-1: RE-MAPPING TABLE

RE-MAP[1:0][1]	Map-En[2,3]	Comments
11	00	Re-mapping is turned off. Program memory is in normal configuration.
10	01	1 KByte of flash memory location is re-mapped. Program access to location 0000H-03FFH is redirected to F000H-F3FFH.
01	10	2 KByte of flash memory location are re-mapped. Program access to location 0000H-07FFH is redirected to F000H-F7FFH.
00	11	4 KByte of flash memory location is re-mapped. Program access to location 0000H-0FFFH is redirected to F000H-FFFFH.

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1. Map-En[1:0] are nonvolatile registers which are examined only during Reset.
2. Map-En[1:0] are initialized according to RE-MAP[1:0] during Reset.
3. Map-En[1:0] are located in SFCF[1:0], they determine the re-mapping configuration. They may be changed by the program at run time.

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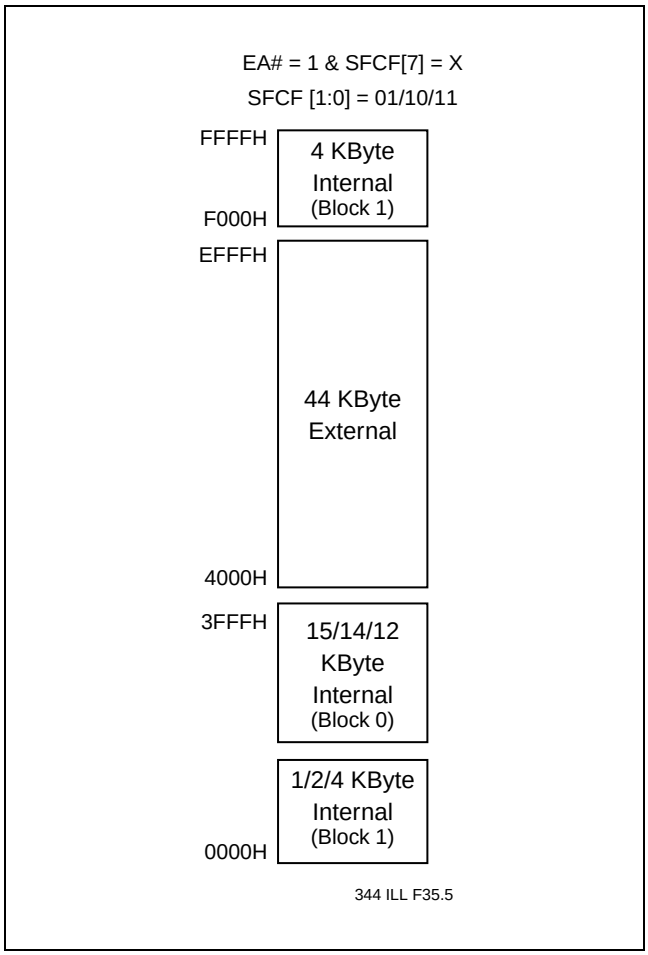

FIGURE 3-4: SST89C54 RE-MAPPED PROGRAM MEMORY ORGANIZATION

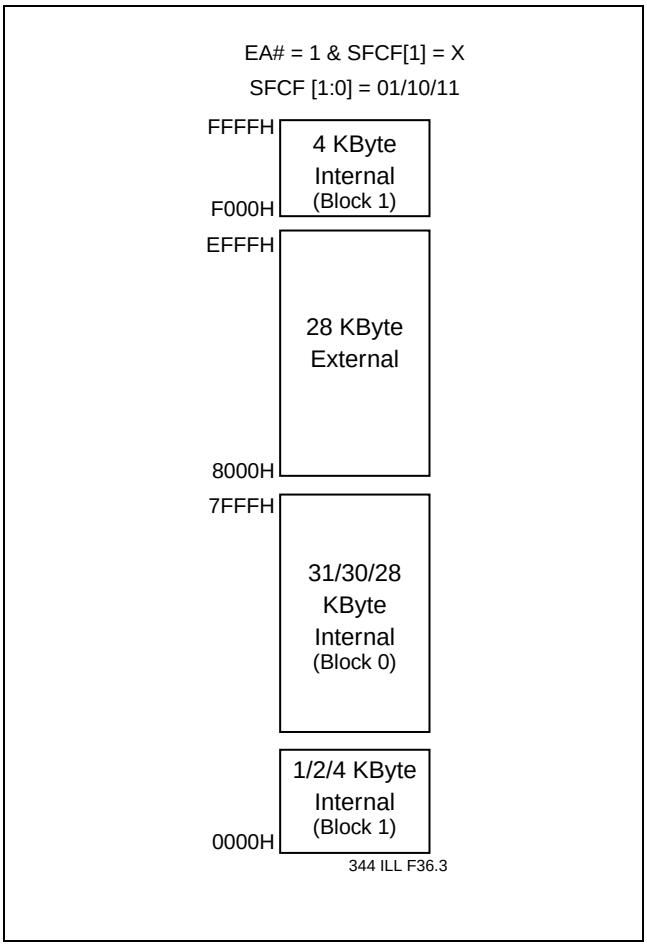

FIGURE 3-5: SST89C58 RE-MAPPED PROGRAM MEMORY ORGANIZATION

3.3 Data RAM Memory

SST89C54/58 have 256 Bytes x8 bits internal RAM and can address up to 64 KByte of external data memory.

3.4 Special Function Registers

Most of the unique features of the FlashFlex51 microcontroller family are controlled by bits in special function registers (SFRs) located in the FlashFlex51 SFR memory map shown below. Individual descriptions of each SFR are provided and Reset values indicated in Tables 3-3 to 3-7.

TABLE 3-2: FLASHFLEX51 SFR MEMORY MAP

	8 BYTES								
F8H									FFH
F0H	B[1]								F7H
E8H									EFH
E0H	ACC[1]								E7H
D8H									DFH
D0H	PSW[1]								D7H
C8H	T2CON[1]		RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	WDTC[1]								C7H
B8H	IP[1]								BFH
B0H	P3[1]	SFCF	SFCM	SFAL	SFAH	SFDT	SFST		B7H
A8H	IE[1]								AFH
A0H	P2[1]								A7H
98H	SCON[1]	SBUF							9FH
90H	P1[1]								97H
88H	TCON[1]	TMOD	TL0	TL1	TH0	TH1			8FH
80H	P0[1]	SP	DPL	DPH			WDTD	PCON	87H

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1. SFRs are bit addressable.

3.4.1 SST89C54/58 Special Function Registers

TABLE 3-3: CPU RELATED SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B*	B Register	F0H	B[7:0]								00H
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE*	Interrupt Enable	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00H
IP*	Interrupt Priority	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx000000b
PCON	Power Control	87H	SMOD	-	-	-	GF1	GF0	PD	-	0xxx0000b

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1. Bit Addressable SFRs

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TABLE 3-4: FLASH MEMORY PROGRAMMING SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB						LSB	RESET Value
SFCF	SuperFlash Configuration	B1H	VIS	IAPEN	-	-	-	-	Map-En	00xxxxxxb
SFCM	SuperFlash Command	B2H	FIE	FCM						00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A7 to A0 (SFAL)							00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A15 to A8 (SFAH)							00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register							00H
SFST	SuperFlash Status	B6H	SB[2:0]		-	BUSY	Flash_busy	-	-	xxxx00xxb

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SuperFlash Configuration Register (SFCF)

Location	7	6	5	4	3	2	1	0	Reset Value
B1H	VIS	IAPEN	-	-	-	-	Map-En1	Map-En0	00xxxxxxb

Symbol	Function
VIS	Upper flash block visibility. 1: 4 KByte flash block visible from F000H-FFFFH. 0: 4 KByte flash block not visible. The VIS bit is ignored when re-map is in effect: The VIS bit is “don’t care” after re-mapped 1KB, 2KB or 4KB. VIS controls the visibility of Block 1 to program counter (PC) only when re-map is 0 KByte.
IAPEN	Enable IAP operation. 1: IAP commands are enabled. 0: IAP commands are disabled.
Map-En1	Map enable bit 1.
Map-En0	Map enable bit 0. Map-En[1:0] are initialized to default value according to RE-MAP[1:0] during Reset. Refer to Table 3-1.

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SuperFlash Command Register (SFCM)

Location	7	6	5	4	3	2	1	0	Reset Value
B2H	FIE	FCM6	FCM5	FCM4	FCM3	FCM2	FCM1	FCM0	00000000b

Symbol	Function
FIE	Flash Interrupt Enable. 1: INT1# is re-assigned to signal IAP operation completion. External INT1# interrupts are ignored. 0: INT1# is not reassigned.
FCM[6:0]	Flash operation command. 000_0001b Chip-Erase 000_0110b Burst-Program 000_1011b Sector-Erase 000_1100b Byte-Verify[1] 000_1101b Block-Erase 000_1110b Byte-Program 000_1111b Prog-SB1[2] 000_0011b Prog-SB2[2] 000_0101b Prog-SB3[2] 000_1000b Prog-RB0[2] 000_1001b Prog-RB1[2] All other combinations are not implemented, and reserved for future use.

1. Byte-Verify has a single machine cycle latency and will not generate any INT1# interrupt regardless of FIE.
2. These commands must reside in Block 0 (32 KByte Block) only or external code memory.

SuperFlash Address Register (SFAL)

Location	7	6	5	4	3	2	1	0	Reset Value
B3H	SuperFlash Low Order Byte Address Register								00000000b

Symbol	Function
SFAL	Mailbox register for interfacing with flash memory block. (Low order address register).

SuperFlash Address Register (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00000000b

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00000000b

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

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SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1	SB2	SB3	-	Busy	Flash_busy	-	-	xxxx00xxb

Symbol	Function
SB1	Security bit 1.
SB2	Security bit 2.
SB3	Security bit 3. Please refer to Table 8-1 for security lock options.
BUSY	Burst-Program completion polling bit. 1: Device is busy with flash operation. 0: Device is available for next Burst-Program operation.
Flash_busy	Flash operation completion polling bit. 1: Device is busy with flash operation. 0: Device has fully completed the last command, including Burst-Program.

TABLE 3-5: WATCHDOG TIMER SFRS

WDTC[1]	Watchdog Timer Control	C0H	-	-	-	-	WDRE	WDTS	WDT	SWDT	X0H
WDTD	Watchdog Timer Data/Reload	86H									00H

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1. Bit Addressable SFRs

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	-	-	-	WDRE	WDTS	WDT	SWDT	xxxx0000b

Symbol	Function
WDRE	Watchdog timer reset enable. 1: Enable watchdog timer reset. 0: Disable watchdog timer reset.
WDTS	Watchdog timer reset flag. 1: Hardware sets the flag on watchdog overflow. 0: External hardware reset clears the flag. Flag can also be cleared by writing a 1. Flag survives if chip reset happened because of watchdog timer overflow.
WDT	Watchdog timer refresh. 1: Software sets the bit to force a watchdog timer refresh. 0: Hardware resets the bit when refresh is done.
SWDT	Start watchdog timer. 1: Start WDT. 0: Stop WDT.

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
86H	Watchdog Timer Data/Reload								00000000b

Symbol	Function
WDTD	Initial/Reload value in Watchdog Timer, new value won't be effective until WDT is set.

TABLE 3-6: TIMER/COUNTERS SFRS

TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer / Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

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1. Bit Addressable SFRs

Note: T2MOD register is not implemented.

TABLE 3-7: INTERFACE SFRS

SBUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
SCON[1]	Serial Port Control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2 EX	T2	FFH
P2[1]	Port 2	A0H	P2[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH

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1. Bit Addressable SFRs

4.0 FLASH MEMORY PROGRAMMING

The SST89C54/58 internal flash memory can be programmed or erased using the following two methods:

- External host mode
- In-Application Programming (IAP) mode

4.1 External Host Programming Mode

External Host Programming mode allows the user to program the Flash memory directly without using the CPU. External host mode is entered by forcing PSEN# from a logic high to a logic low while RST input is being held continuously high. The device will stay in external host mode as long as RST = "1" and PSEN# = "0".

A Read-ID operation is necessary to "arm" the device, no other external host mode command can be enabled until a Read-ID is performed. In external host mode, the internal Flash memory blocks are accessed through the reassigned I/O port pins (see Figure 4-1 for details) by an external host, such as an MCU programmer, PCB tester or a PC controlled development board.

When the chip is in the external host mode, Port 0 pins are assigned to be the parallel data input and output pins. Port 1 pins are assigned to be the non-multiplexed low order address bus signals for the internal flash memory (A_7-A_0). The first six bits of Port 2 pins (P2[5:0]) are assigned to be the non-multiplexed upper order address bus signals for the internal flash memory (A_{13}-A_8) along with two of the Port 3 pins (P3[5] as A_{15} and P3[4] as A_{14}). Two upper order Port 2 pins (P2[7] and P2[6]) and two upper order Port 3 pins (P3[7] and P3[6]) along with RST, PSEN#, ALE/PROG#, EA# pins are assigned as the control signal pins. The Port 3 pin (P3[3]) is assigned to be the ready/busy status signal, which can be used for handshaking with the external host during a flash memory programming operation. The flash memory programming operation (Erase, Program, Verify, etc.) is internally self-timed.

The insertion of an "arming" command prior to entering the external host mode by utilizing the Read-ID operation provides additional protection for inadvertent writes to the internal flash memory caused by a noisy or unstable system environment during power-up or brown-out conditions.

The external host mode uses twelve (12) hardware commands, which are decoded from the control signal pins, to facilitate the internal flash memory erase, program and verify processes. The external host mode is enabled on the falling edge of PSEN#. The external host mode commands are enabled on the falling edge of ALE/PROG#. The list in Table 4-1 outlines all the commands and the respective control signal assignment.

TABLE 4-1: EXTERNAL HOST MODE COMMANDS

Operation	RST	PSEN#	ALE/PROG#	EA#	P3[7]	P3[6]	P2[7]	P2[6]	P0[7:0]	P1[7:0]	P3[5:4] P2[5:0]
Read-ID	V_{IH1}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	DO	AL	AH
Chip-Erase	V_{IH1}	V_{IL}	⇓[1]	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X
Block-Erase	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	X	A[15:12]
Sector-Erase	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	AL	AH
Byte-Program	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	DI	AL	AH
Burst-Program	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	DI	AL	AH
Byte-Verify (Read)	V_{IH1}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	DO	AL	AH
Prog-SB1	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	X
Prog-SB2	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X
Prog-SB3	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	X
Prog-RB0	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	X	X	X
Prog-RB1	V_{IH1}	V_{IL}	⇓	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X

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1. Symbol ⇓ signifies a negative pulse and the command is asserted during the low state of ALE/PROG# input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: V_{IL} = Input Low Voltage; V_{IH} = Input High Voltage; V_{IH1} = Locig High Level (RST); X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output; A[15:12] = 0xxxb for Block 0 (SST89C58), A[15:12] = 00xxb for Block 0 (SST89C54), and A[15:12] = "1111b" for Block 1.

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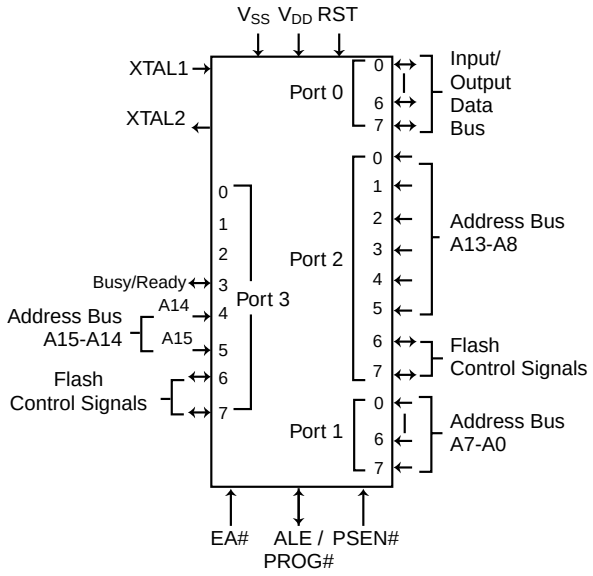

FIGURE 4-1: I/O PIN ASSIGNMENTS FOR EXTERNAL HOST MODE

4.1.1 Product Identification

The Read-ID command accesses the signature bytes that identify the device as an SST89C54/58 and the manufacturer as SST (See Table 4-2). External programmers primarily use these signature bytes in the selection of programming algorithms. The Read-ID command is selected by the byte code of 00H on P2[7:6] and P3[7:6]. See Figure 12-12 for timing waveforms.

TABLE 4-2: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	30H	BFH
Device ID		
SST89C54	31H	E4H
SST89C58	31H	E2H

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4.1.2 Arming Command

An arming command sequence must take place before any external host mode sequence command is recognized by the SST89C54/58. This prevents accidental triggering of external host mode commands due to noise or programmer error. The arming command is as follows:

1. PSEN# goes low while RST is high. This will set the device in external host mode, re-configuring the pins.
2. A Read-ID command is issued and held for 1 ms.

After the above sequence, all other external host mode commands are enabled. Before the Read-ID command is received, all other External Host commands received are ignored.

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4.1.3 External Host Mode Commands

The twelve SST89C54/58 external host mode commands are Read-ID, Chip-Erase, Block-Erase Sector-Erase, Byte-Program, Burst-Program, Byte-Verify, Prog-SB1, Prog-SB2, Prog-SB3, Prog-RB0 and Prog-RB1. See Table 4-1 for all signal logic assignments and Table 12-11 for the timing parameter for the external host mode commands. The critical timing for all Erase and Program commands is self-generated by the on-chip flash memory controller. The high-to-low transition of the PROG# signal initiates the Erase and Program commands, which are synchronized internally. The Read commands are asynchronous reads, independent of the PROG# signal level.

The following three commands are used for erasing all or part of the memory array. Memory locations that are to be programmed must be in the erased state (0FFH) prior to programming.

The Chip-Erase command erases all bytes in both memory blocks. This command ignores the Security Lock status and will erase the Security bits and the RE-MAP bits. See Figure 12-13 for timing waveforms.

The Block-Erase command erases all bytes in one of the memory blocks (16/32KB or 4KB). This command will not be enabled if the security lock is enabled on the selected memory block. The selection of the memory block to be erased is determined by A[15:12]. If A15 is a “0”, then the primary flash memory Block 0 (16/32KB), is selected. If A[15:12] = “1111b”, then the secondary flash memory Block 1 (4KB) is selected. See Figure 12-14 for the timing waveforms.

The Sector-Erase command erases all of the bytes in a sector. The sector size for the primary flash memory (Addresses 0000H-3FFFH/7FFFH) is 128 Bytes. The sector size for the secondary flash memory (Addresses F000H-FFFFH) is 64 bytes. This command will not be executed if the Security lock is enabled on the selected memory block. The selection of the memory sector to be erased is determined by A[15:6] for Block 0 A[15:5] for Block 1. See Figure 12-15 for timing waveforms.

The Byte-Program and Burst-Program commands are used for programming new data into the memory array. Selection of which Program command to use will be dependent upon the desired programming field size. Programming will not take place if any security locks are enabled on the selected memory block.

The Byte-Program command programs data into a single byte. See Figure 12-16 for timing waveforms.

The Burst-Program command programs data to an entire row, sequentially byte-by-byte. See Figure 12-17 for timing waveforms.

The Byte-Verify command allows the user to verify that the SST89C54/58 correctly performed an Erase or Program command. This command will be disabled if any security locks are enabled on the selected memory block. See Figure 12-18 for timing waveforms.

The Prog-SB1, Prog-SB2, Prog-SB3 commands program the security bits. The functions of these bits are described in a Security Lock section and also in Table 8-1. Once programmed, these bits can only be erased through a Chip-Erase command.

The Prog-RB1, and Prog-RB0 commands program the RE-MAP[1:0] bits. The functions of these bits are described in the Memory Re-mapping section and also in Table 3-1. Once programmed, these bits can only be erased through Chip-Erase command.

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4.1.4 External Host Mode Clock Source

In external host mode, an internal oscillator will provide clocking for the SST89C54/58. The on-chip oscillator will be turned on as the SST89C54/58 enters external host mode; i.e. when PSEN# goes low while RST is high. The oscillator provides both clocking for the flash control unit as well as timing references for Program and Erase operations. During external host mode, the CPU core is held in reset. Upon exit from external host mode, the internal oscillator is turned off.

The same oscillator also provides the time base for the watchdog timer and timing references for IAP mode Program and Erase operations. See more detailed description in later sections.

4.1.5 Flash Operation Status Detection Via External Host Handshake

The SST89C54/58 provide two methods for an external host to detect the completion of a flash memory operation to optimize the Program or Erase time. The end of a flash memory operation cycle can be detected by: 1) monitoring the READY/BUSY# bit at P3[3]; 2) monitoring the Data# Polling bit at P0[7] and P0[3].

4.1.5.1 Ready/Busy# (P3[3])

The progress of the flash memory programming can be monitored by the READY/BUSY# output signal. P3[3] is driven low, some time after ALE/PROG# goes low during a flash memory operation to indicate the Busy# status of the flash control unit (FCU). P3[3] is driven high when the Flash programming operation is completed to indicate the Ready status.

During a Burst-Program operation, P3[3] is driven high (Ready) in between each byte programmed among the burst to indicate the ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it should then put the data/address (within the same row) of the next byte on the bus and drive ALE/PROG# low (pulse), before the time-out limit expires. See Table 12-11 for details. Burst-Program command presented after time-out will wait until the next cycle. Therefore, it will have longer programming time.

4.1.5.2 Data# Polling (P0[7] and P0[3])

During a Program operation, any attempts to read (Byte-Verify), while the device is busy, will receive the complement of the data for the last byte loaded (logic low, i.e. “0” for an erase) on P0[3] and P0[7] with the rest of the bits “0”. During a Program operation, the Byte-Verify command will read the data from the last byte loaded, not the data at the address specified.

During a Burst-Program operation, the true data will be read from P0[7], when the device completes each byte programmed among the burst to indicate the Ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it should then put the data/address (in the same row) of the next byte on the bus and drive ALE/PROG# low immediately, before the time-out limit expires (See Table 12-11 for details.). The true data will be read from P0[3], when the Burst-Program command is terminated and the device is ready for the next operation.

After security lock-bits are set:

- If read on universal programmer, e.g. external host mode, the programmer will read 00H instead of 0FFH.
- If read by MOVC instruction, the programmer will return 0FFH regardless of true data if MOVC is executed in a block with lower level lock.
- If read by the IAP Byte-Verify command, then SFDT won’t update its data, i.e. SFDT will keep its OLD data unchanged, so the user’s application code will get random data based on the old SFDT value. This IAP Byte-Verify command is executed in a block with lower level lock.

The termination of the Burst-Program can be accomplished by: 1) Change to a new row address (Note: the Address range is different for the 4Kx8 flash Block 1 and for the 16/32K x 8 flash Block 0.); 2) Change to a new command that requires a high to low transition of the ALE/PROG# (for example, any Erase or Program command, 3) Wait for time out limit to expire (20 µs) before programming the next byte.

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4.1.6 Instructions to Perform External Host Mode Commands

To program data into the memory array, apply power supply voltage (V_{DD}) to V_{DD} and RST pins, and perform the following steps:

1. Maintain RST high and toggle PSEN# from logic high to low, in sequence per the appropriate timing diagram.
2. Raise EA# High (either V_{IH} or V_H).
3. Issue Read-ID command to enable the external host mode.
4. Verify that the memory blocks or sectors for programming is in the erased state, FFH. If they are not erased, then erase them using the appropriate Erase command.
5. Select the memory location using the address lines (P1[7:0], P2[5:0], P3[5:4]).
6. Present the data in on P0[7:0].
7. Pulse ALE/PROG#, observing minimum pulse width.
8. Wait for low to high transition on READY/BUSY# (P3[3]).
9. Repeat steps 5 - 8 until programming is finished.
10. Verify the flash memory contents.

4.2 In-Application Programming Mode

The SST89C54/58 offers 20/36 KByte of in-application programmable flash memory. During in-application programming, the CPU of the microcontroller enters IAP mode. The two blocks of flash memory allows the CPU to concurrently execute user code from one block, while the other is being reprogrammed. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The mailbox registers (SFST, SFCM, SFAL, SFAH, SFDT and SFCF) located in the Special Function Register (SFR), control and monitor the device's erase and program process.

Table 4-3 outlines the commands and their associated settings of the mailbox registers.

4.2.1 In-Application Programming Mode Clock Source

During IAP mode, both the CPU core and the flash controller unit (FCU) are driven off the external clock. However, an internal oscillator will provide timing references for Program and Erase operations. The duration of Program and Erase operations will be identical between external host mode and In-Application mode. The internal oscillator is only turned on when required, and is turned off as soon as the Flash operation is complete.

4.2.2 IAP Enable Bit

The IAP enable bit, SFCF[6], initializes in-application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

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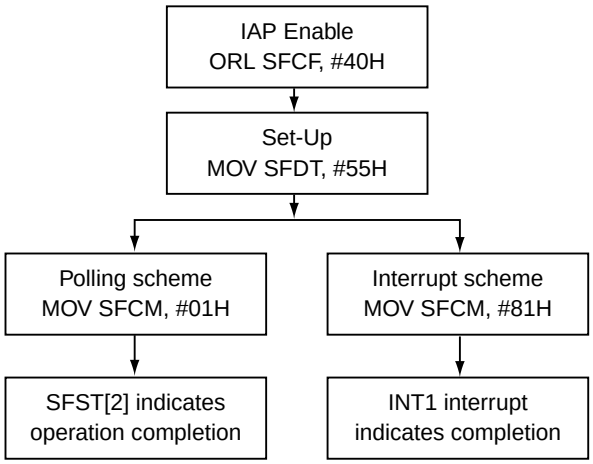
4.2.3 In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the (SFCM) register will initiate all of the operations. All commands (except Chip-Erase) will not be enabled if the security features are enabled on the selected memory block.

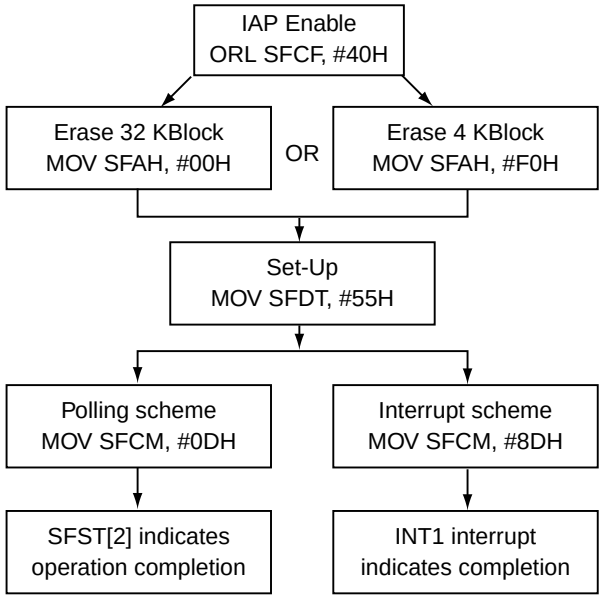
The two Program commands are for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFH. If the memory is not erased, then erase it with an appropriate Erase command. **Do not write (Program or Erase) to a block that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

The Chip-Erase command erases all bytes in both memory blocks (16/32KB and 4KB). This command ignores the Security Lock status and will erase the security lock bits and RE-MAP bits. The Chip-Erase command sequence is as follows:



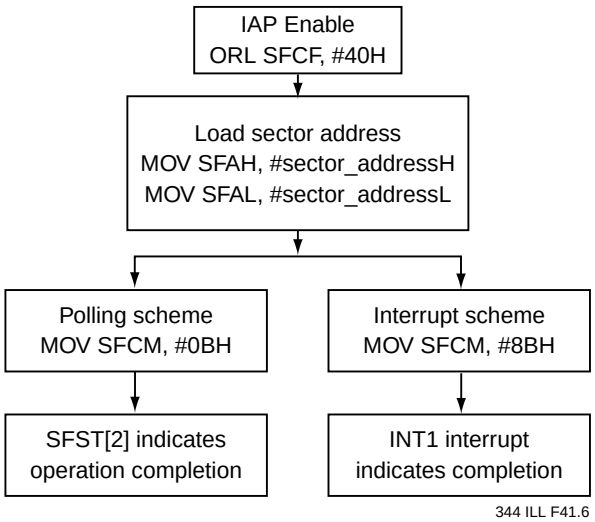
344 ILL F39.4

The Block-Erase command erases all bytes in one of the two memory blocks (16/32KB or 4KB). The selection of the memory block to be erased is determined by the (SFAH[7]) of the SuperFlash Address Register. The primary flash memory Block 0 is selected (16/32KB) as follows: for SST89C58, SFAH[7] = 0 selects Block 0; for SST89C54, SFAH[7:6] = 00 selects Block 0. For both, SFAH[7:4] = 1111b selects the secondary flash memory Block 1 (4KB). The Block-Erase command sequence is as follows:



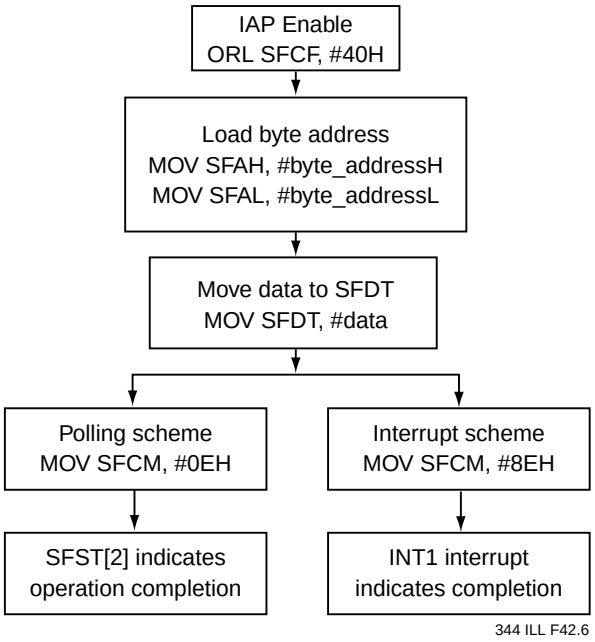
344 ILL F40.8

The Sector-Erase command erases all of the bytes in a sector. The sector size for the primary flash memory Block 0 is 128 Bytes. The sector size for the secondary flash memory Block 1 is 64 Bytes. The selection of the sector to be erased is determined by the contents of SFAH, SFAL. Please refer to Figure 3-1 for an illustration of memory sector organization. The Sector-Erase command sequence is as follows:

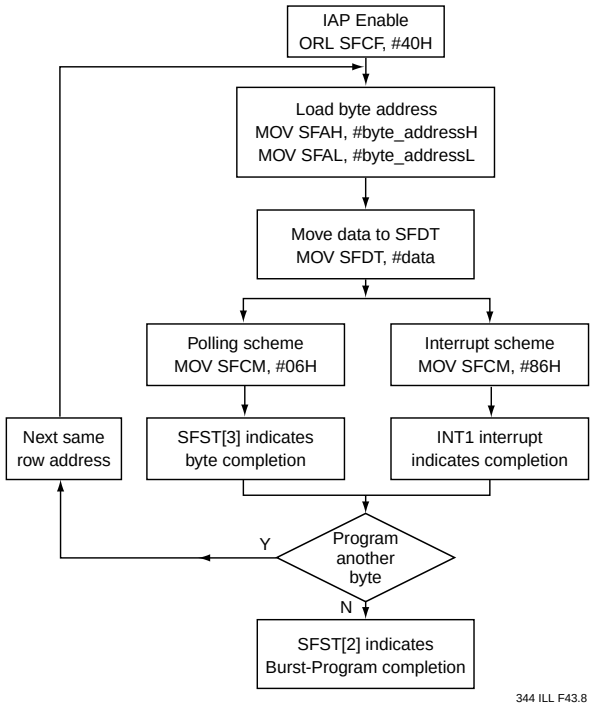


344 ILL F41.6

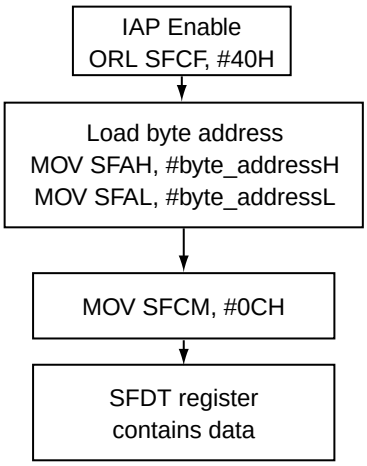
The Byte-Program command programs data into a single byte location. The Byte-Program command sequence is as follows:



The Burst-Program command programs data into half of a sector (row) which has the same row address, sequentially byte-by-byte. Refer to the Memory Organization section in Figure 3-1 for details. The MOVC instruction and all IAP commands except Burst-Program are invalid during the Burst-Program cycle. The Burst-Program command sequence is as follows:

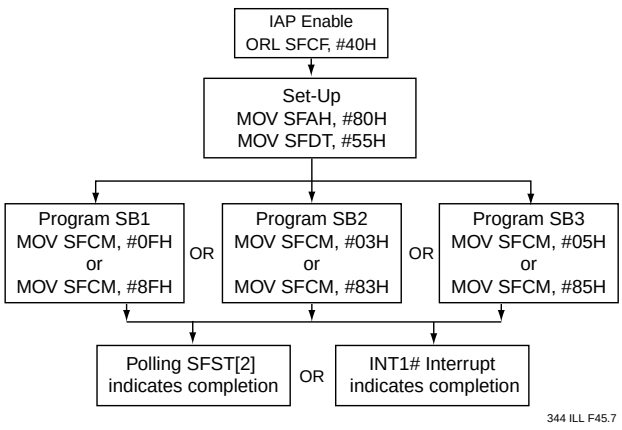


The Byte-Verify command allows the user to verify that the SST89C54/58 has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT. The user is required to check that the previous Flash operation has fully completed before issuing a Byte-Verify. Byte-Verify command execution time is short enough that there is no need to poll for command completion and no interrupt is generated. The Byte-Verify command sequence is as follows:



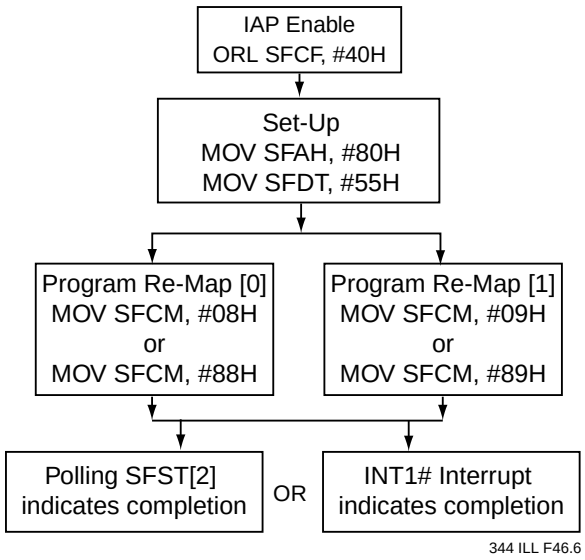
Prog-SB3, Prog-SB2, Prog-SB1 commands are used to program the Security bits (see Table 8-1). Upon completion of any of those commands, the security options will be updated immediately.

Security bits previously in un-programmed state can be programmed by these commands. The Prog-SB3, Prog-SB2, Prog-SB1 sequences are as follows:



Prog-RB1, Prog-RB0 commands are used to program the RE-MAP[1:0] bits (see Table 3-1). These commands only change the RE-MAP[1:0] bits and have no effect on Map-En[1:0] until after a reset cycle. Therefore, the effect of these commands is not immediate.

Re-Map bits previously in un-programmed state can be programmed by these commands. The Prog-RB1, Prog-RB0 sequences are as follows:



Prog-SB3, Prog-SB2, Prog-SB1, Prog-RB1, and Prog-RB0 commands must reside only in Block 0 (32 KByte block) or external code memory.

Any such instructions issued from Block 1 may cause unpredictable program behavior.

4.2.4 Polling

A command that uses the polling method to detect flash operation completion should poll on the Flash_busy bit (SFST[2]). When Flash_busy de-asserts (logic 0), the device is ready for the next operation.

The BUSY bit (SFST[3]) is provided for Burst-Program. In between bytes within a burst sequence, the Busy bit will become logic 0 to indicate that the next Burst-Program byte should be presented. Completion of the full burst cycle is indicated also by Flash_busy bit (SFST[2]).

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory. MOVC instruction will fail if it is directed at a flash block that is still busy.

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4.2.5 Interrupt Termination

If interrupt termination is selected, (SFCM[7] is set), then an interrupt (INT1) will be generated to indicate flash operation completion. Under this condition, the INT1 becomes an internal interrupt source. The INT1# pin can now be used as a general purpose port pin and it cannot be a source of External Interrupt 1.

For an interrupt to occur, EX1 and EA bits of IE register must be set. The IT1 bit of TCON register must also be set for edge trigger detection.

Important: The user cannot program Security/Re-Map bits while code is running in Block 1. The user can only program security SBx/Re-Map bits when code is running in external code memory or when code is running in Block 0. The solution is to use MOV SFAH, #80H; before issuing any IAP commands to program security bits or Re-Map bits.

TABLE 4-3: IN-APPLICATION PROGRAMMING MODE COMMANDS

Operation	SFAH [7:0]	SFAL [7:0]	SFDT [7:0]	SFCM [6:0][1]
Chip-Erase	X	X	55H	01H
Block-Erase	AH[2]	X	55H	0DH
Sector-Erase	AH	AL	X	0BH
Byte-Program	AH	AL	DI	0EH
Burst-Program	AH	AL	DI	06H
Byte-Verify (Read)	AH	AL	DO	0CH
Prog-SB3	80H	X	55H	05H
Prog-SB2	80H	X	55H	03H
Prog-SB1	80H	X	55H	0FH
Prog-RB1	80H	X	55H	09H
Prog-RB0	80H	X	55H	08H

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1. Interrupt/Polling enable for flash operation completion
   SFCM[7] = 1: Interrupt enable for flash operation completion
   0: polling enable for flash operation completion
2. SFAH[7] = 0 selects Block 0 for SST89C58; SFAH[7:6] = 00 selects Block 0 for SST89C54; SFAH[7:4] = FH selects Block 1

Note: X = Don't Care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output
All other values are in hex.
SFCF[6] = 1 enables IAP command. SFCF[6] = 0 disables IAP command.

5.0 TIMERS/COUNTERS

The SST89C54/58 have three 16-bit registers that can be used as either timers or event counters. The three Timers/Counters are the Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated with a pair of 8-bit registers in the SFRS. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

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6.0 SERIAL I/O

The SST89C54/58 serial I/O port is a full-duplex UART (Universal Asynchronous Receiver/Transmitter) that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively. The serial I/O port performs the function of an UART. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The serial I/O port has four modes of operation which are selected by the Serial Port mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in Mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) special function register is cleared and the Reception Enable/Disable (REN) bit of the SCON register is set. Reception is initiated in other modes by the incoming start bit if the REN bit of the SCON register is set.

7.0 WATCHDOG TIMER

The SST89C54/58 offer a hardware programmable Watchdog Timer (WDT) for fail safe operation against software hangup and automatic reset recovery.

To protect the system against software hangup, the software has to refresh the WDT within a user defined time period. If the software fails to do this periodic refresh, an internal hardware reset will be initiated if enabled (WDRE=1). The software can be designed such that the WDT times out if the program does not work properly. It also times out if a software error is based on hardware related problems.

The WDT in the SST89C54/58 share the same time base with the flash controller unit. When the flash controller unit is operating, the time base will be re-started by the hardware periodically, therefore delaying the time-out period of the watchdog timer. The upper 8-bits of the time base register are used as the reload register of the WDT.

The internal oscillator that drives the WDT operates within a frequency range as shown in Table 12-1. Minimum clock cycle for the WDT is 7.7ms, typical 10ms.

Figure 7-1 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control watchdog timer operation.

Note:

- WDTD won't be effective until bit WDT is set.
- A WDTD register can not be set to 0FFH.
- WDT timeout period = (255-WDTD) x 7.7ms (min.)

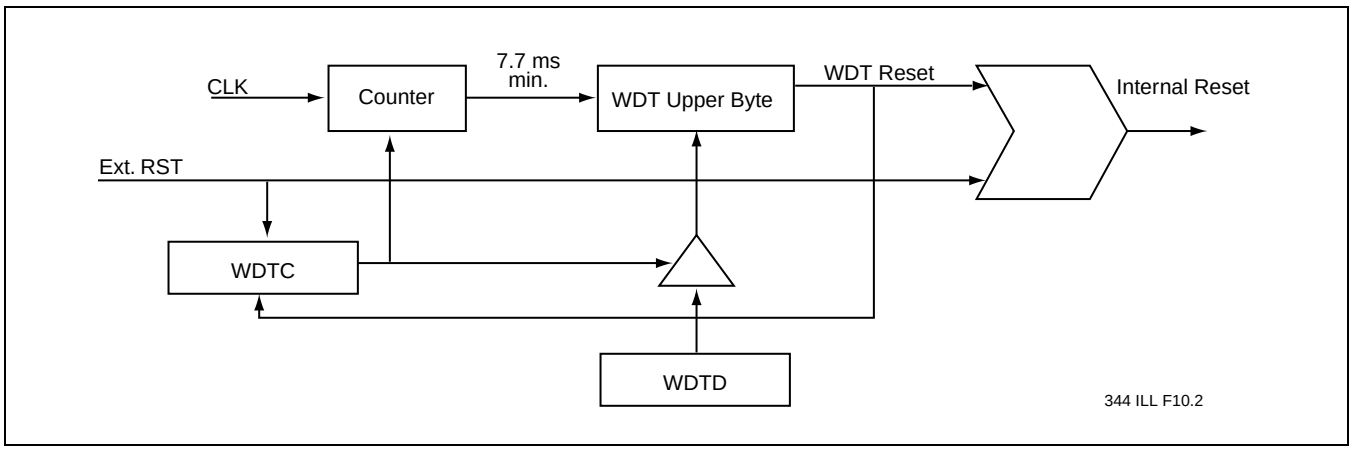

FIGURE 7-1: BLOCK DIAGRAM OF PROGRAMMABLE WATCHDOG TIMER

8.0 SECURITY LOCK

The Security feature protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory locations. There are two different types of security locks in the SST89C54/58 security lock system, hard lock and SoftLock. (See Figure 8-1 and Table 8-1.)

8.1 Hard Lock

When the hard lock is activated, the MOVC instructions executed from unlocked or SoftLocked program address space, are disabled from reading code bytes in hard locked memory blocks (See Table 8-2). The hard lock can either lock both flash memory blocks or just lock the upper flash memory block (Block 1). All External Host and IAP commands except for Chip-Erase are ignored by the hard locked memory blocks.

8.2 SoftLock

SoftLock allows flash contents to be altered under a secure environment. This lock option allows the user to update program code in the SoftLocked memory block through in-application programming mode under a predetermined secure environment. For example, if the Block 1 (4KB) memory is hard locked, and the Block 0 (16KB/32KB) memory is SoftLocked, code residing in Block 1 can program Block 0. The following IAP mode commands issued through the command mailbox register, SFCM, executed from a hard locked block can be operated on a SoftLocked block: Block-Erase, Sector-Erase, Byte-Program, Burst-Program and Byte-Verify.

In external host mode, SoftLock behaves the same as a hard lock.

8.3 Security Lock Status

The three bits that indicate the SST89C54/58 security lock status, SB1, SB2 and SB3, are located in SFST[7:5]. As shown in Figure 8-1 and Table 8-1, the three security lock bits control the lock status of the primary and secondary blocks of memory. There are four distinct levels of security lock status. In the first level, none of the security lock bits are programmed and both blocks are unlocked. In the second level, although, both blocks are now locked and cannot be written, they are available for Read operation via Byte-Verify. In the third level, three different options are available: Block 1 hard lock / Block 0 SoftLock, SoftLock on both blocks, and hard lock on both blocks. Locking both blocks is the same as Level 2 except Read operation isn't available. The fourth level of security is the most secure level. It doesn't allow read/write of internal memory or boot from external memory. Please note that for unused combinations of the security lock bit the chip will default to Level 4 status.

For details on how to program the security lock bits, refer to the External Host Programming Mode (Section 4.1) and in-application programming mode (Section 4.2).

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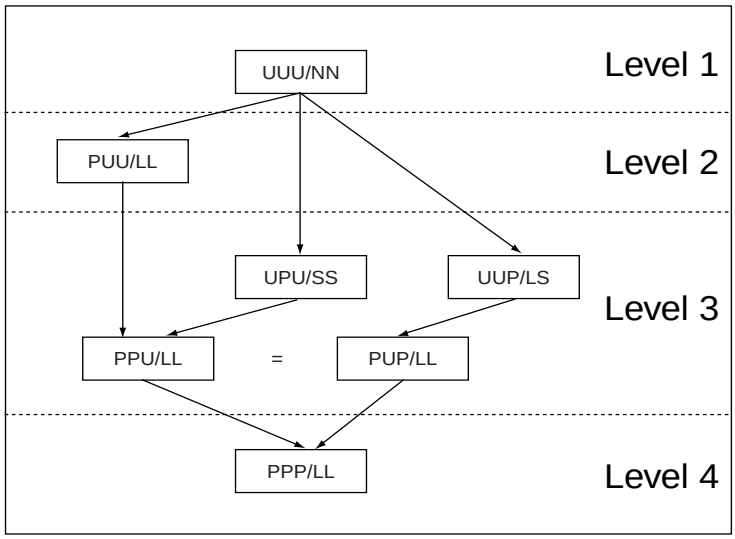

Note: P = Programmed (Cell logic state = 0),
U = Unprogrammed (Cell logic state = 1)
N = Not Locked, L = Hard Locked, S = SoftLocked

FIGURE 8-1: SECURITY LOCK LEVELS

TABLE 8-1: SECURITY LOCK OPTIONS

Level	Security Lock Bits[1,2]				Security Status of:		Security Type
	SFST[7:5]	SB1	SB2	SB3	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	Hard Lock	Hard Lock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	110 101	P P	P U	U P	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	010	U	P	U	SoftLock	SoftLock	Level 2 plus Verify disabled, code in Block 1 can program Block 0 and vice versa.
	001	U	U	P	Hard Lock	SoftLock	Level 2 plus Verify disabled, code in Block 1 can program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3, Hard Lock/Hard Lock but MCU will start code execution from the internal memory regardless of EA#.

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1. SFST[7:5] = Security Lock Decoding Bits (SB1, SB2, SB3)
2. P = Programmed (Cell logic state = 0);
   U = Unprogrammed (Cell logic state = 1)
   All unused combinations default to level 4, “PPP”

TABLE 8-2: SECURITY LOCK ACCESS TABLE

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed on C58/54
				External Host[3]	IAP	
4	111b/011b[4] (Hard Lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
3	101b/110b (Hard Lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	001b (Block 0 = SoftLock, Block 1 = Hard Lock)	Block 0	Block 0	N	N	Y
			Block 1	N	N	N[5]
			External	N/A	N	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	010b (SoftLock on both blocks)	Block 0	Block 0	N	N	Y
			Block 1	N	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
2	100b (Hard Lock on both blocks)	Block 0	Block 0	Y	N	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	N	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	N	N
			External	N/A	N/A	Y
1	000b (Unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	Y
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	Y
		External	Block 0/1	Y	Y	Y
			External	N/A	N/A	Y

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1. Location of MOVC or IAP instruction.
2. Target Address is the location of the instruction being read.
3. External Host Byte-Verify access does not depend on a source address.
4. 011b is an unused combination and defaults to security level 4
5. MOVC is normally not allowed when accessing data in Block 1 at addresses F000H-FFFFH.
   MOVC is allowed when Block 1 is re-mapped and target address is within 0000H-03FFH/07FFH/0FFFH (1K/2K/4K re-map).

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9.0 RESET

A system reset initializes the MCU and begins program execution at program memory location 0000H. The reset input for the SST89C54/58 is the RST pin. In order to reset the device, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE and PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform correct reset. This level must not be affected by external element. A system reset will not affect the 256 Bytes of on-chip RAM while the SST89C54/58 is running, however, the contents of the on-chip RAM during power up are indeterminate. All Special Function Registers (SFR) return to their reset values, which are outlined in Tables 3-3 to 3-7.

9.1 Power-On Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high. **Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash.**

When power is applied to the SST89C54/58, the RST pin must be high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid Power-On Reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10µF capacitor and to V_{SS} through an 8.2 Kohm resistor as shown in Figure 10-1. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 10 ms. The oscillator start-up time depends on the crystal frequency.

Crystal	Typical Start-up Time
10MHz	1ms
1MHz	10ms

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause corruption in the flash memory.

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10.0 POWER-SAVING MODES

The SST89C54/58 provides power saving modes of operation for applications where power consumption is critical. The two power saving modes are: Power Down and Standby (Stop Clock).

10.1 Power Down Mode

The Power Down mode is entered by setting the PD bit in the PCON register. In Power Down mode, the clock is stopped and external interrupts are active for level sensitive interrupt only.

The SST89C54/58 exits Power Down mode through either an enabled external level sensitive interrupt INTx or a hardware reset. The interrupt clears the PD bit, the oscillator restarts and stablizes, then the program resumes execution beginning at the instruction immediately following the one which invoked the Power Down mode. The hardware reset redefines all the SFRs but does not change the on-chip RAM.

10.2 Standby Mode (Stop Clock)

Standby mode is similar to Power Down mode, except that Power Down mode is initiated by a software command and Standby mode is initiated by external hardware gating off the external clock to the SST89C54/58. The on-chip RAM and SFR data are maintained in the Standby mode. The device resumes operation at the next instruction when the clock is reapplied to the part.

Table 10-1 outlines the two power-saving modes, including entry and exit procedures and MCU functionality.

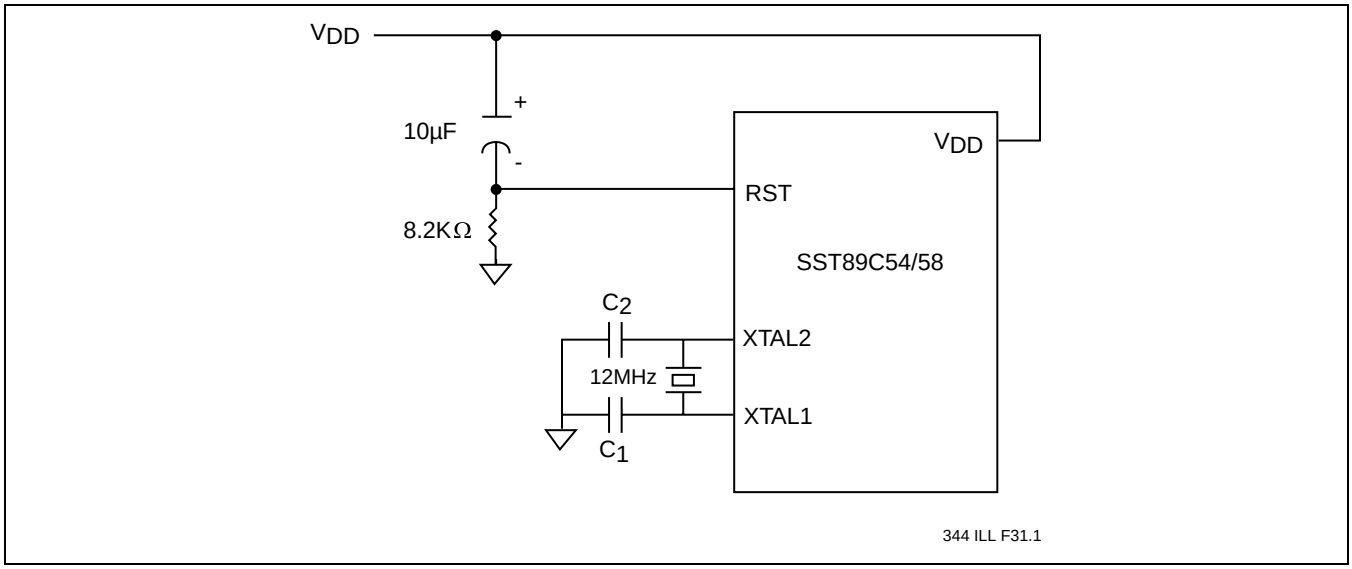

FIGURE 10-1: POWER-ON RESET CIRCUIT

TABLE 10-1: SST89C54/58 POWER SAVING MODES

Mode	Initiated by	Current Drain	State of MCU	Exited by
Power Down Mode	Software (Set PD bit in PCON) MOV PCON, #02H	Typically 15-20 µA. Minimum V_{DD} for Power Down mode is 2.7V.	CLK is stopped. On-chip SRAM and SFR data will be maintained. ALE and PSEN# signals at a LOW level during Power Down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt INTx or hardware reset. Start of interrupt clears PD bit and exits Power Down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power Down mode. A user could consider placing two or three NOP instructions after the instruction that invokes Power Down mode to eliminate any problems, or by hardware reset.
Standby (Stop Clock) Mode	External hardware gates turn off the external clock input to the MCU. This gating should be synchronized with an input clock transition (low-to-high or high-to-low).	Typically 15-20 µA. Minimum V_{DD} for Standby mode is 2.7V.	CLK is frozen. On-chip RAM and SFR data is maintained. ALE and PSEN# are maintained at the levels prior to the clock being frozen.	Gate ON external clock. Program execution resumes at the instruction following the one during which the clock was gated off.

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11.0 CLOCK INPUT OPTIONS

Shown in Figure 11-1 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external crystal oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15pF once the external signal meets the V_{IL} and V_{IH} specifications.

11.1 Recommended Capacitor Values for Crystal Oscillator

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 capacitors should be adjusted appropriately for each design. Table 11-1 below, shows the typical values for C1 and C2 by crystal type.

TABLE 11-1: RECOMMENDED VALUES FOR C1 AND C2 BY CRYSTAL TYPE

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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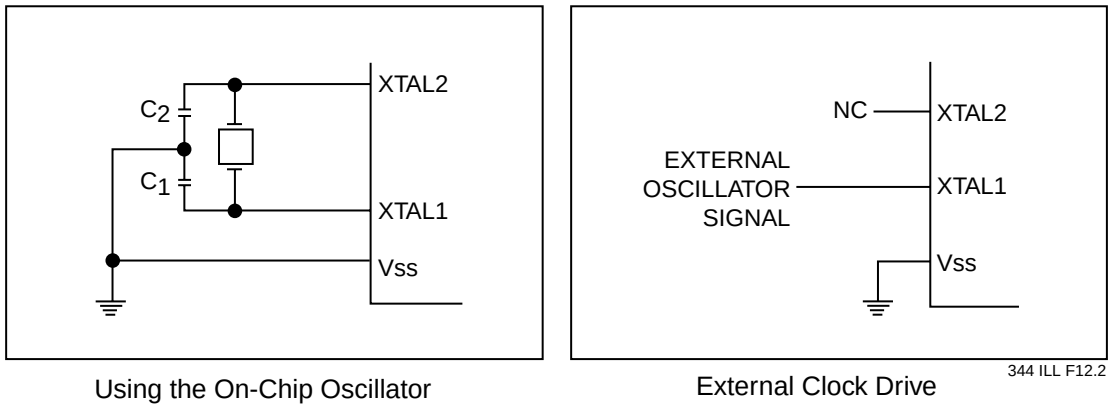

FIGURE 11-1: OSCILLATOR CHARACTERISTICS

12.0 ELECTRICAL SPECIFICATION

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to + 150°C
Voltage on EA# Pin to V_{SS} . . . . . -0.5V to +14.0V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to +6.5V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time. (Based on package heat transfer limitations, not device power consumption.)

Note: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

TABLE 12-1: OPERATING RANGE

Symbol	Description	Min.	Max	Unit
T_a	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage	2.7	5.5	V
f_{OSC}	Oscillator Frequency	0	33	MHz
	For in-application programming	0.25	33	MHz

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TABLE 12-2: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12-3: AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . C_L = 100 pF
See Figures 12-6 and 12-8

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TABLE 12-4: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 12-5: PIN IMPEDANCE (V_{DD}=3.3V, Ta=25 °C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance[2]	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}	Pin Inductance		20 nH

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Pin capacitance is characterized but not tested. EA# pin is 25 pF max.

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12.1 DC Electrical Characteristics

TABLE 12-6: DC ELECTRICAL CHARACTERISTICS
T_a = -40°C TO +85°C, 33MHZ DEVICES; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	$4.5 < V_{DD} < 5.5$	-0.5	$0.2\ V_{DD}$ - 0.1	V
V_{IH}	Input High Voltage (Ports 0,1,2,3)	$4.5 < V_{DD} < 5.5$	$0.2V_{DD}$ + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	$4.5 < V_{DD} < 5.5$	$0.7V_{DD}$	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16 mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100 µA[2]		0.3	V
		I_{OL} = 1.6 mA[2]		0.45	V
		I_{OL} = 3.5 mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200 µA[2]		0.3	V
		I_{OL} = 3.2 mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10 µA	V_{DD} - 0.3		V
		I_{OH} = -30 µA	V_{DD} - 0.7		V
		I_{OH} = -60 µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200 µA	V_{DD} - 0.3		V
		I_{OH} = -3.2 mA	V_{DD} - 0.7		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V	-1	-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	$0.45 < V_{IN} < V_{DD}$-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
I_{DD}	Power Supply Current[6]				
	In-Application Programming mode				
	@ 12 MHz			70	mA
	@ 33 MHz			88	mA
	Active Mode				
	@ 12 MHz			22	mA
	@ 33 MHz			45	mA
	Standby (Stop Clock) Mode	T_a = 0°C to +70°C		100	µA
		T_a = -40°C to +85°C		125	µA
	Power Down Mode	Minimum V_{DD} = 2.7V			
		T_a = 0°C to +70°C		40	µA
		T_a = -40°C to +85°C		50	µA

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TABLE 12-7: DC ELECTRICAL CHARACTERISTICS
T_a = -40°C TO +85°C, 12MHZ DEVICES; V_{DD} = 3.0-3.6V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.3	-0.5	0.7	V
V_{IH}	Input High Voltage (ports 0, 1, 2, 3)	2.7 < V_{DD} < 3.3	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V_{DD} < 3.3	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7V			
		I_{OL} = 16 mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 2.7V			
		I_{OL} = 100 µA[2]		0.3	V
		I_{OL} = 1.6 mA[2]		0.45	V
		I_{OL} = 3.5 mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 2.7V			
		I_{OL} = 200 µA[2]		0.3	V
		I_{OL} = 3.2 mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 2.7V			
		I_{OH} = -10 µA	V_{DD} - 0.3		V
		I_{OH} = -30 µA	V_{DD} - 0.7		V
		I_{OH} = -60 µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 2.7V			
		I_{OH} = -200 µA	V_{DD} - 0.3		V
		I_{OH} = -3.2 mA	V_{DD} - 0.7		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V	-1	-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
I_{DD}	Power Supply Current[6]				
	In-Application Programming mode			70	mA
	Active Mode			22	mA
	Standby (Stop Clock) Mode	T_a = 0°C to +70°C		70	µA
		T_a = -40°C to +85°C		88	µA
	Power Down Mode	Minimum V_{DD} = 2.7V			
		T_a = 0°C to +70°C		40	µA
		T_a = -40°C to +85°C		50	µA

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1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 & 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE & PSEN# = 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 & 2 may cause the V_{OH}, ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.

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5. Pins for Ports 1, 2 & 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. See Figures 12-9, 12-10 and 12-11 and for test conditions. Minimum V_{DD} for Power Down is 2.7V.

12.2 AC Electrical Characteristics

AC Characteristics: (Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

TABLE 12-8: AC ELECTRICAL CHARACTERISTICS (1 OF 2)
T_a = -40°C TO +85°C, V_{DD} = 3.0-3.6V @12MHz,4.5-5. 5V @ 33MHz, V_{SS} = 0

		Oscillator						
		12MHz		33MHz		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency					0	33	MHz
T_{LHLL}	ALE Pulse Width	127		20		$2T_{CLCL}$ - 40		ns
T_{AVLL}	Address Valid to ALE Low	43				T_{CLCL} - 40 (3V)		ns
				5		T_{CLCL} - 25 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	53				T_{CLCL} - 30 (3V)		ns
				5		T_{CLCL} - 25 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		234				$4T_{CLCL}$ - 65 (3V)	ns
					55		$4T_{CLCL}$ - 65 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	53				T_{CLCL} - 30 (3V)		ns
				5		T_{CLCL} - 25 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	205		45		$3T_{CLCL}$ - 45		ns
T_{PLIV}	PSEN# Low to Valid Instr In		145				$3T_{CLCL}$ - 55 (3V)	ns
					35		$3T_{CLCL}$ - 55 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#	0		0		0		ns
T_{PXIZ}	Input Instr Float After PSEN#		59				T_{CLCL} - 25 (3V)	ns
					5		T_{CLCL} - 25 (5V)	ns
T_{PXAV}	PSEN# to Address Valid	75		22		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		312				$5T_{CLCL}$ - 80 (3V)	ns
					70		$5T_{CLCL}$ - 80 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	400		80		$6T_{CLCL}$ - 100		ns
T_{WLWH}	Write Pulse Width (WE#)	400		80		$6T_{CLCL}$ - 100		ns
T_{RLDV}	RD# Low to Valid Data In		252				$5T_{CLCL}$ - 90 (3V)	ns
					60		$5T_{CLCL}$ - 90 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		0		ns
T_{RHDZ}	Data Float After RD#		106				$2T_{CLCL}$ - 60 (3V)	ns
					35		$2T_{CLCL}$ - 25 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		517				$8T_{CLCL}$ - 90 (3V)	ns
					150		$8T_{CLCL}$ - 90 (5V)	ns
T_{AVDV}	Address to Valid Data In		585				$9T_{CLCL}$ - 90 (3V)	ns
					180		$9T_{CLCL}$ - 90 (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	200	300	40	140	$3T_{CLCL}$ - 50	$3T_{CLCL}$ + 50	ns
T_{AVWL}	Address to RD# or WR# Low	203				$4T_{CLCL}$ - 130 (3V)		ns
				45		$4T_{CLCL}$ - 75 (5V)		ns
T_{QVWX}	Data Valid to WR# Transition	33				T_{CLCL} - 50 (3V)		ns
				0		T_{CLCL} - 30 (5V)		ns

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TABLE 12-8: AC ELECTRICAL CHARACTERISTICS (CONTINUED) (2 OF 2)
T_a = -40°C TO +85°C, V_{DD} = 3.0-3.6V @12MHZ,4.5-5. 5V @ 33MHZ, V_{SS} = 0

		Oscillator						
		12MHz		33MHz		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
T_{WHQX}	Data Hold After WR#	33				T_{CLCL} - 50 (3V)		ns
				3		T_{CLCL} - 27 (5V)		ns
T_{QVWH}	Data Valid to WR# High	433				$7T_{CLCL}$ - 150 (3V)		ns
				140		$7T_{CLCL}$ - 70 (5V)		ns
T_{RLAZ}	RD# Low to Address Float		0		0		0	ns
T_{WHLH}	RD# to WR# High to ALE High	43	123			T_{CLCL} - 40 (3V)	T_{CLCL} + 25 (3V)	ns
				5	55	T_{CLCL} - 25 (5V)	T_{CLCL} + 25 (5V)	ns

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Explanation of Symbols Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

T_{AVLL} = Time from Address Valid to ALE Low
T_{LLPL} = Time from ALE Low to PSEN# Low

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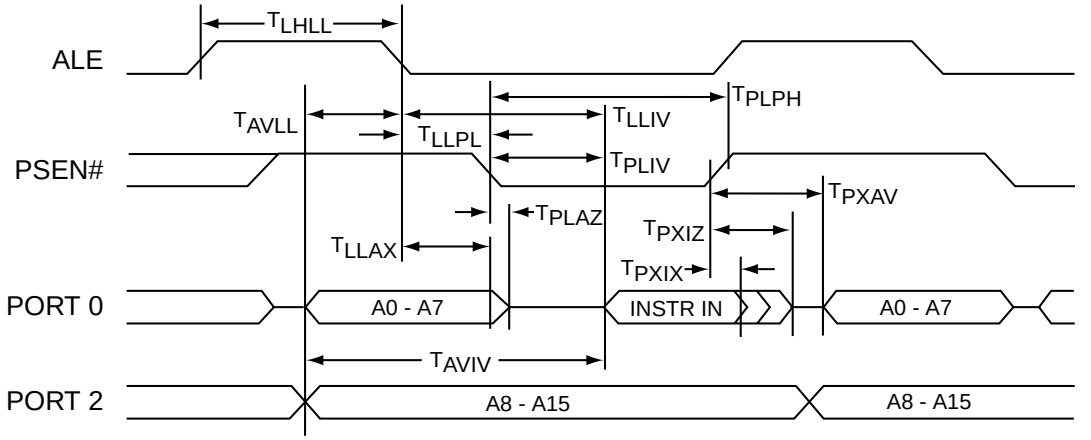

FIGURE 12-1: EXTERNAL PROGRAM MEMORY READ CYCLE

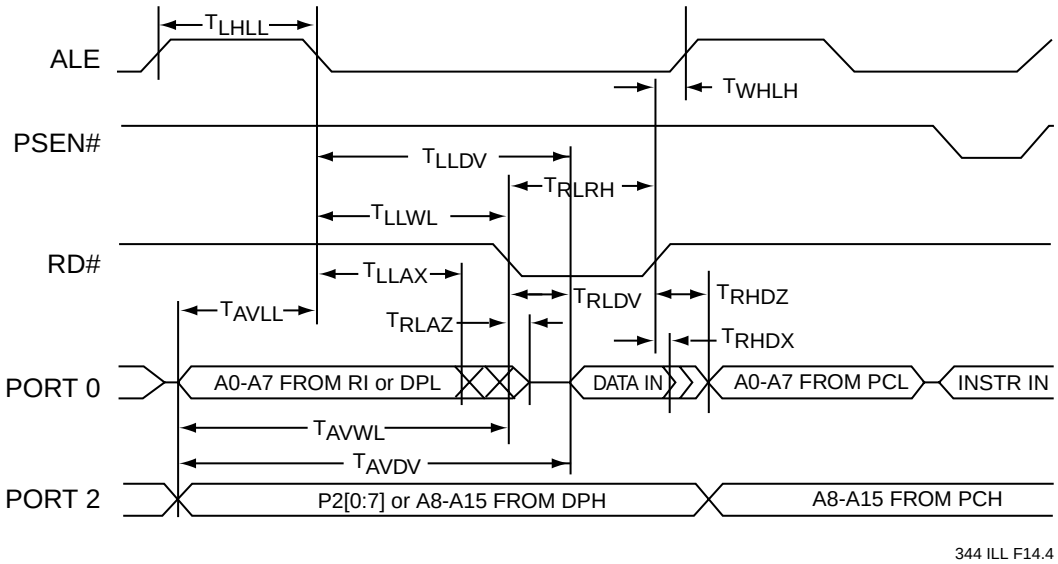

FIGURE 12-2: EXTERNAL DATA MEMORY READ CYCLE

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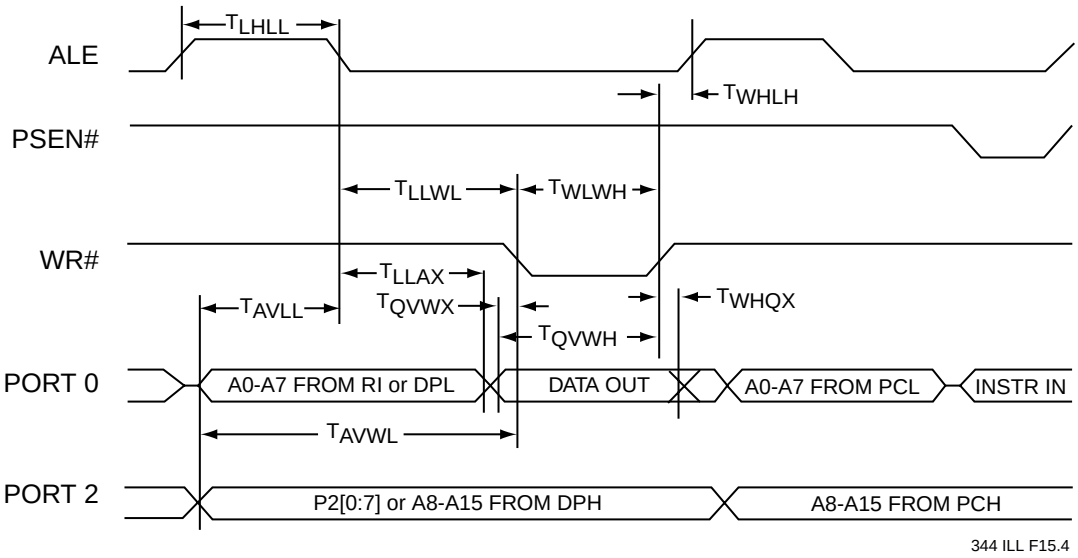

FIGURE 12-3: EXTERNAL DATA MEMORY WRITE CYCLE

TABLE 12-9: EXTERNAL CLOCK DRIVE

		Oscillator						
		12MHz		33MHz		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency					0	33	MHz
T_{CLCL}	Clock Period	83		30				ns
T_{CHCX}	High Time			10.5		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time			10.5		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		5			ns
T_{CHCL}	Fall Time		20		5			ns

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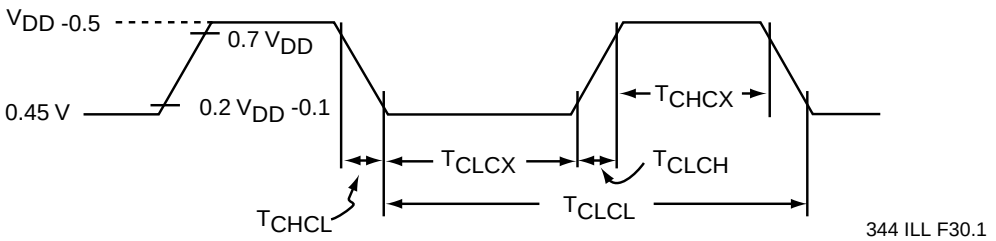

FIGURE 12-4: EXTERNAL CLOCK DRIVE WAVEFORM

TABLE 12-10: SERIAL PORT TIMING

Symbol	Parameter	Oscillator						Units
		12MHz		33MHz		Variable		
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1		0.36		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		167		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50				$2T_{CLCL}$ - 117		ns
				10		$2T_{CLCL}$ - 50		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		167		$10T_{CLCL}$ - 133	ns

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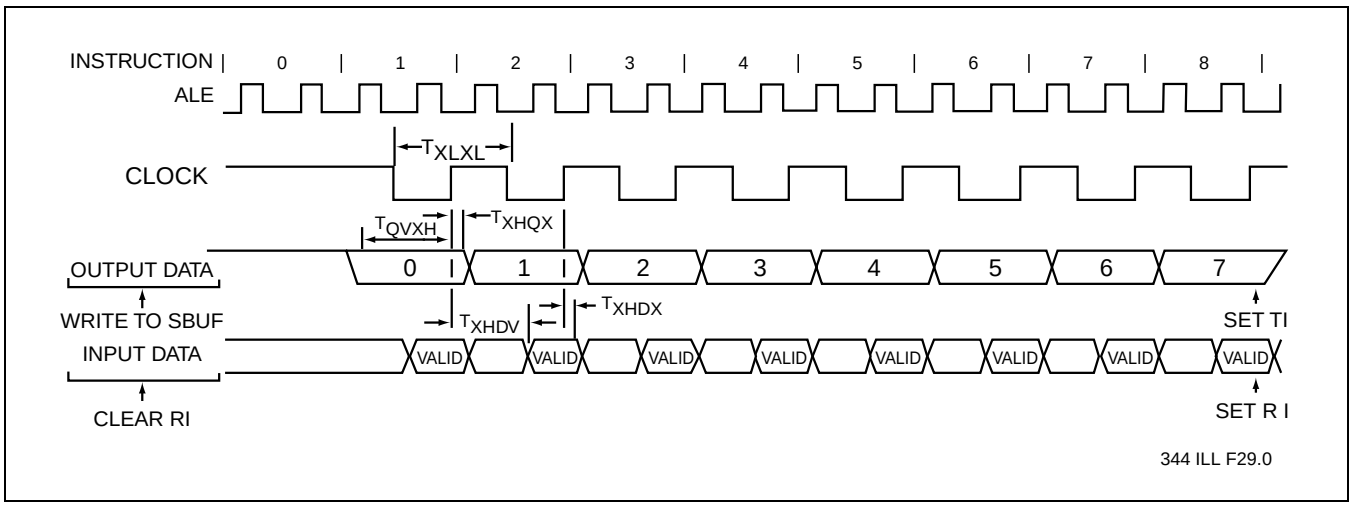
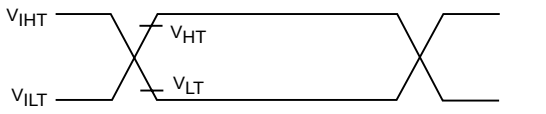


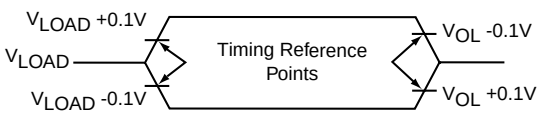
FIGURE 12-5: SHIFT REGISTER MODE TIMING WAVEFORMS



AC Inputs during testing are driven at V_{IHT} (V_{DD} -0.5V) for Logic "1" and V_{ILT} (0.45V) for a Logic "0". Measurement reference points for inputs and outputs are at V_{HT} ($0.2V_{DD}$ + 0.9) and V_{LT} ($0.2V_{DD}$ - 0.1)

Note: V_{HT}- V_{HIGH} Test
V_{LT}- V_{LOW} Test
V_{IHT}-V_{INPUT} HIGH Test
V_{ILT}- V_{INPUT} LOW Test

FIGURE 12-6: AC INPUT/OUTPUT TEST WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

FIGURE 12-7: FLOAT WAVEFORM

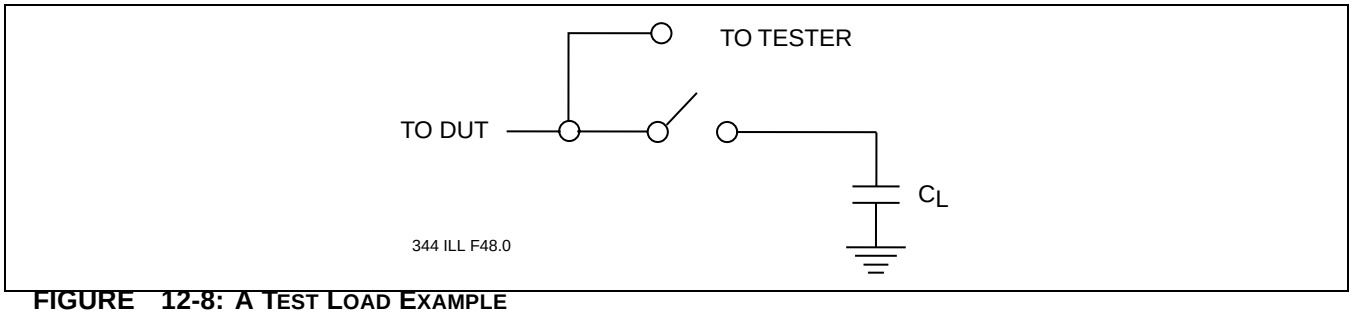


FIGURE 12-8: A TEST LOAD EXAMPLE

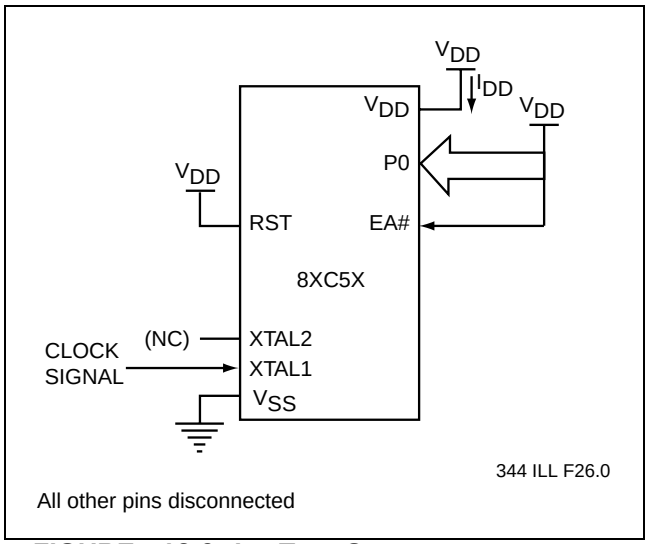


FIGURE 12-9: I_{DD} TEST CONDITION, ACTIVE MODE

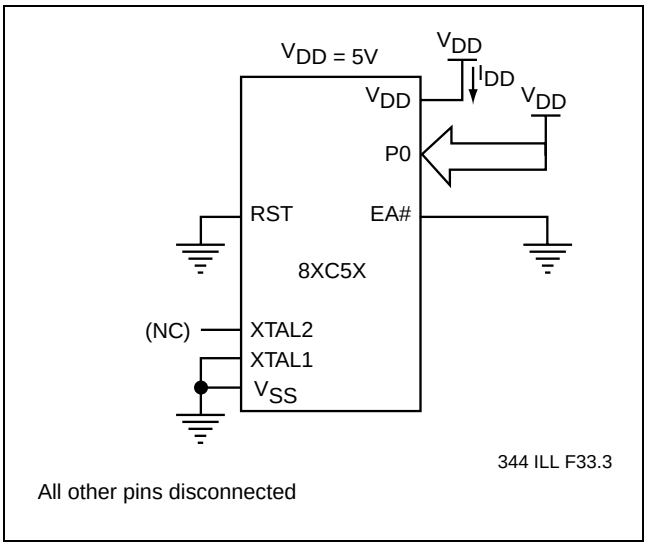


FIGURE 12-11: I_{DD} TEST CONDITION, STANDBY (STOP CLOCK) MODE

Note: Idle mode is not supported.

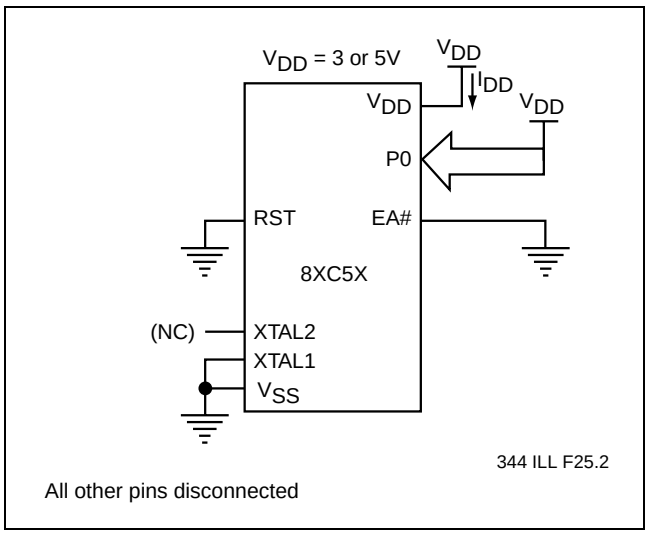


FIGURE 12-10: I_{DD} TEST CONDITION, POWER DOWN MODE

TABLE 12-11: FLASH MEMORY PROGRAMMING/VERIFICATION PARAMETERS

Parameter[1,2]	Symbol	Min	Max	Units
Reset Setup Time	T_{SU}	3		µs
Read-ID Command Width	T_{RD}	1		µs
PSEN# Setup Time	T_{ES}	1.125		µs
Address, Command, Data Setup Time	T_{ADS}	0		ns
Chip-Erase Time	T_{CE}		11.7	ms
Block-Erase Time	T_{BE}		9.4	ms
Sector-Erase Time	T_{SE}	1.1	2.3	ms
Program Setup Time	T_{PROG}	1.2		µs
Address, Command, Data Hold	T_{DH}	0		ns
Byte-Program Time[3]	T_{PB}		110	µs
Verify Command Delay Time	T_{OA}		50	ns
Verify High Order Address Delay Time	T_{AHA}		50	ns
Verify Low Order Address Delay Time	T_{ALA}		50	ns
First Burst-Program Byte Time[4]	T_{BUP1}		85	µs
Burst-Program Time[3,4]	T_{BUP}	31	45	µs
Burst-Program Recovery[4]	T_{BUPRCV}		110	µs
Burst-Program Time-Out Limit	T_{BUPTO}	20		µs

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1. Program and Erase times will scale inversely relative to programming clock frequency.
2. All timing measurements are from the 50% of the input to 50% of the output.
3. Each byte must be erased before program.
4. External host mode only.

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12.3 Flash Memory Programming Timing Diagrams with External Host Mode

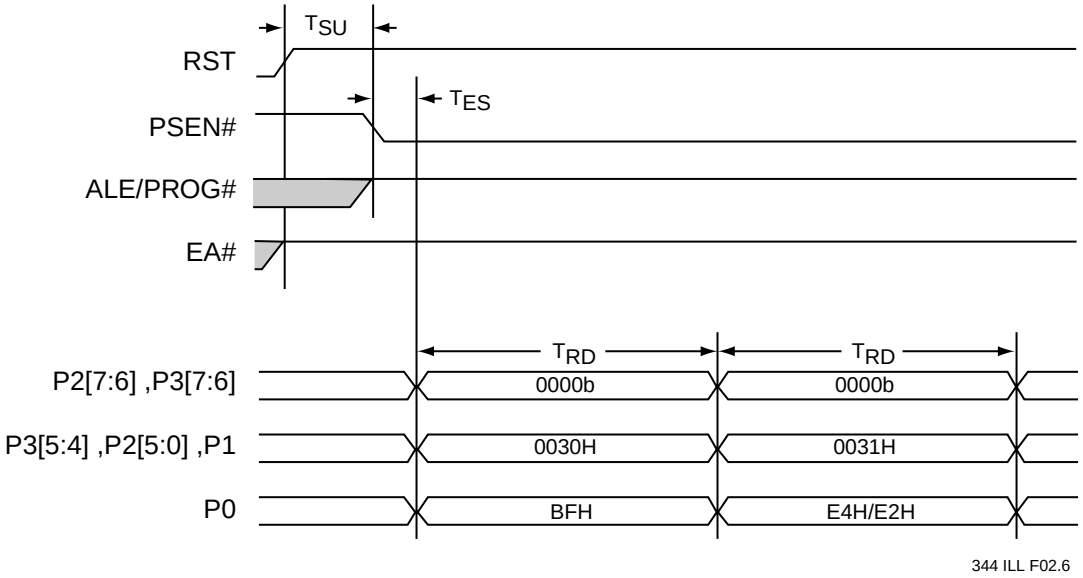


FIGURE 12-12: READ-ID
Read chip signature and identification registers at the addressed location.

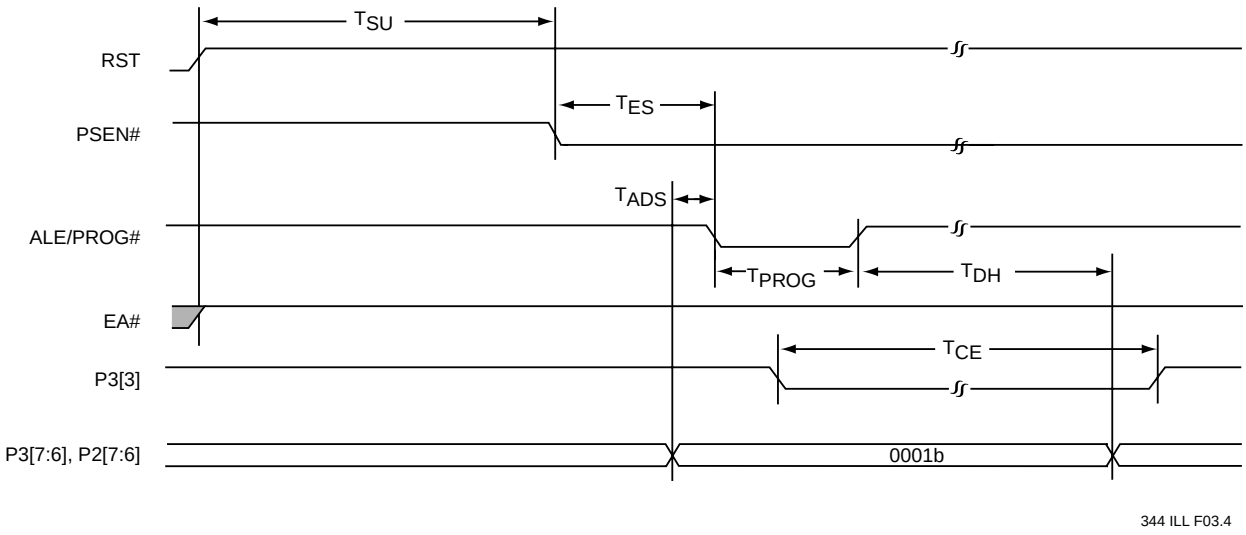


FIGURE 12-13: CHIP-ERASE
Erase both flash memory blocks. Security lock is ignored and the security bits are erased too.

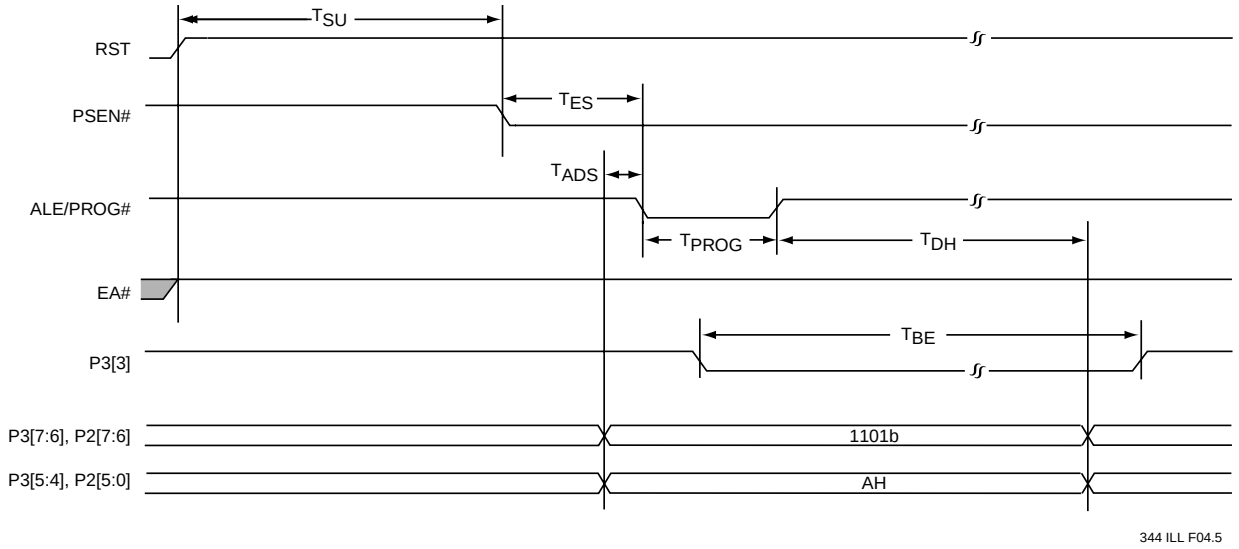


FIGURE 12-14: BLOCK-ERASE
Erase one of the flash memory blocks, if the security lock is not activated on that flash memory block. The highest address bits A[15:12] determines which block is erased. For example, if A15 is “0”, primary flash memory block is erased. If A[15:12] = “1111b”, the secondary block is erased.

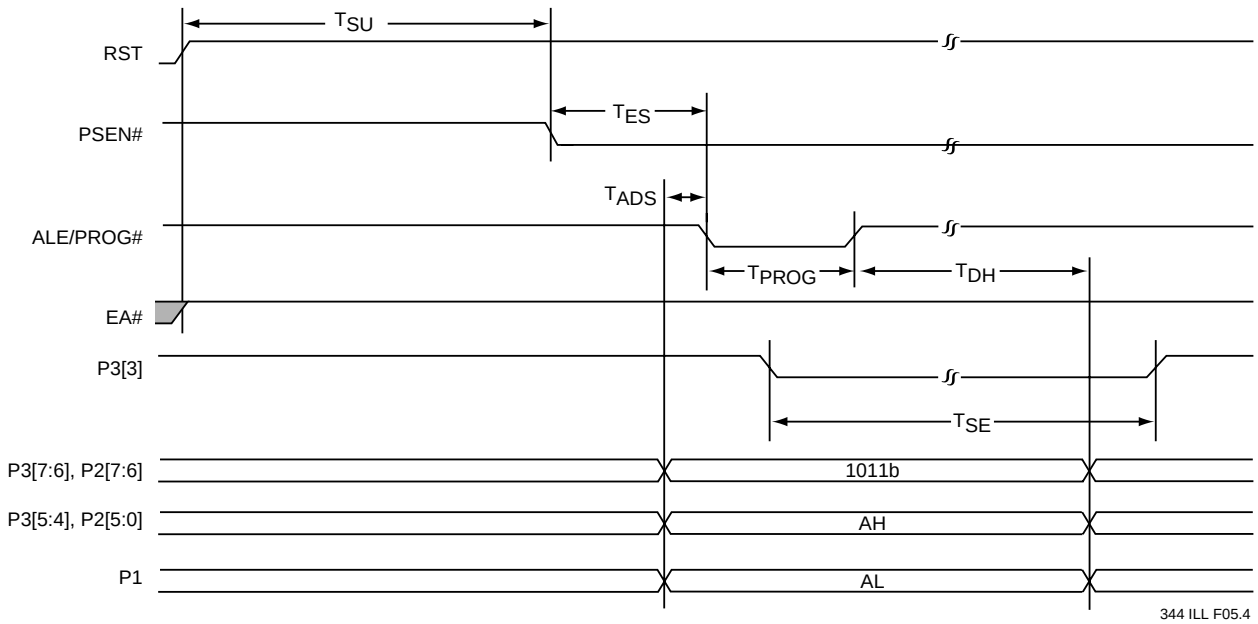


FIGURE 12-15: SECTOR-ERASE
Erase the addressed sector if the security lock is not activated on that flash memory block.

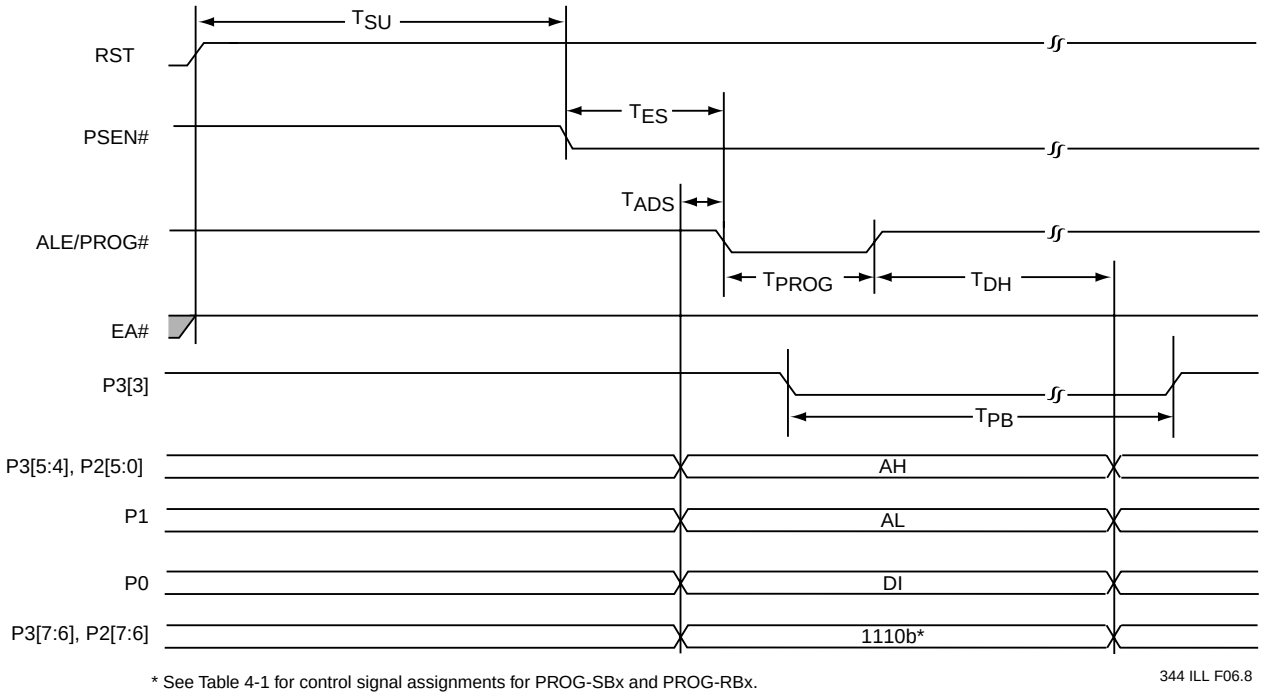


FIGURE 12-16: BYTE-PROGRAM; PROG-SB3, PROG-SB2, PROG-SB1, PROG-RB1, AND PROG-RB0

Program the addressed code byte if the byte location has been successfully erased and not yet programmed. Byte-Program operation is only allowed when the security lock is not activated on that flash memory block.

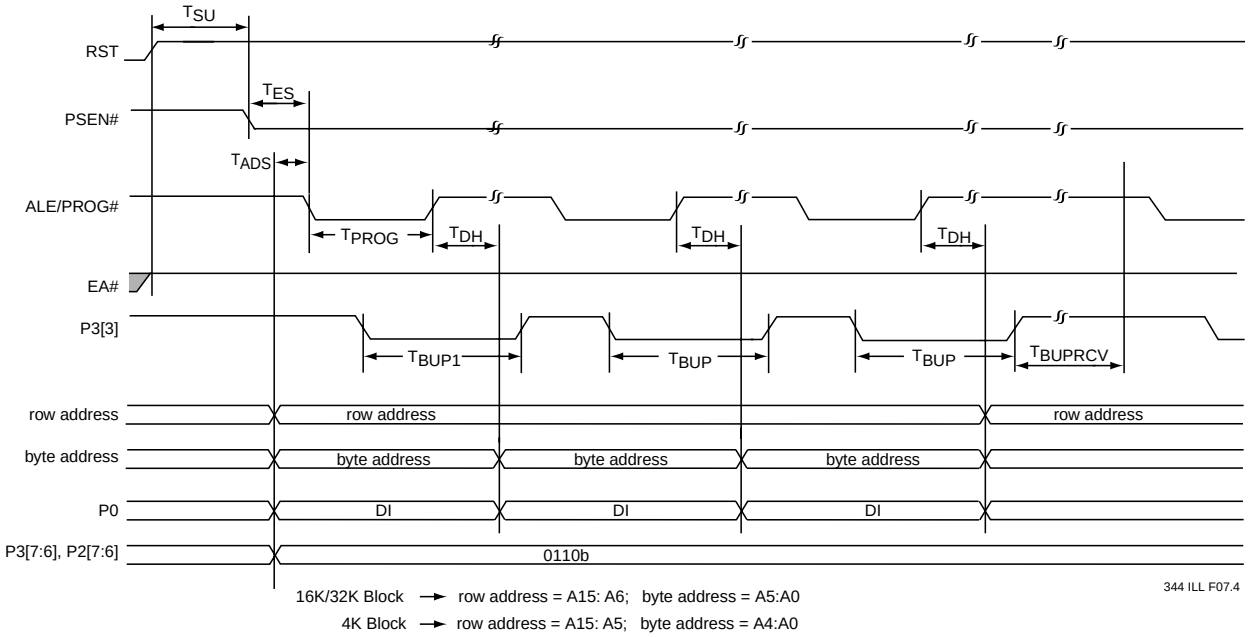


FIGURE 12-17: BURST-PROGRAM
Program the entire addressed row by burst programming each byte sequentially within the row if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

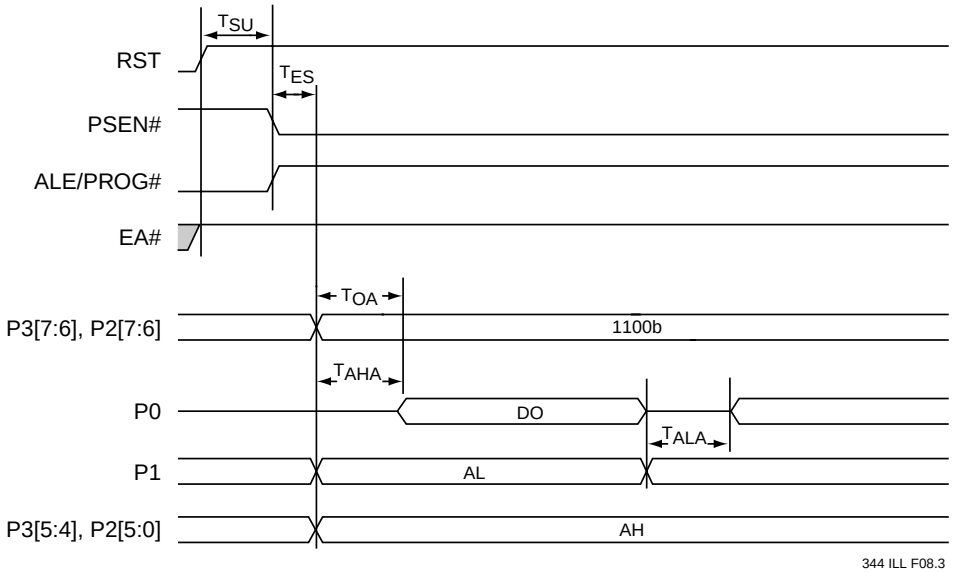
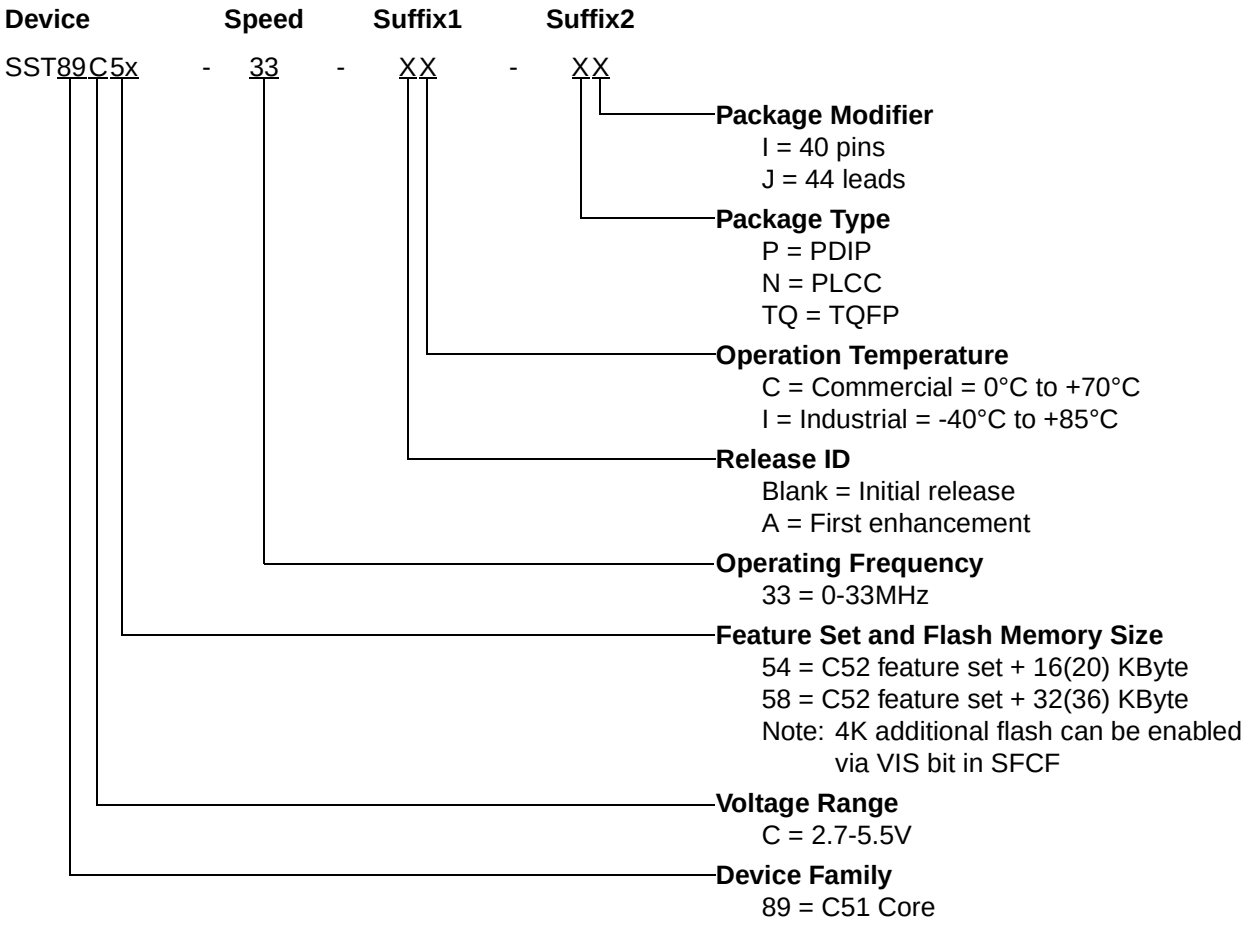


FIGURE 12-18: BYTE-VERIFY
Read the code byte from the addressed flash memory location if the security lock is not activated on that flash memory block.

13.0 PRODUCT ORDERING INFORMATION



13.1 Valid Combinations

Valid combinations for SST89C54

SST89C54-33-C-PI	SST89C54-33-C-NJ	SST89C54-33-C-TQJ
SST89C54-33-I-PI	SST89C54-33-I-NJ	SST89C54-33-I-TQJ

Valid combinations for SST89C58

SST89C58-33-C-PI	SST89C58-33-C-NJ	SST89C58-33-C-TQJ
SST89C58-33-I-PI	SST89C58-33-I-NJ	SST89C58-33-I-TQJ

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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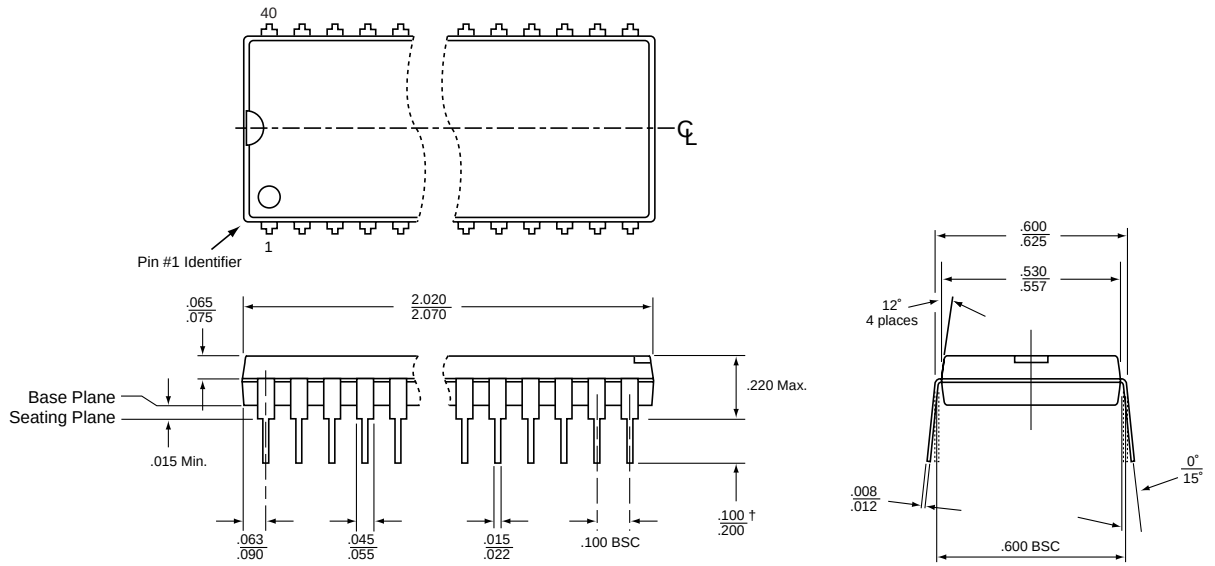
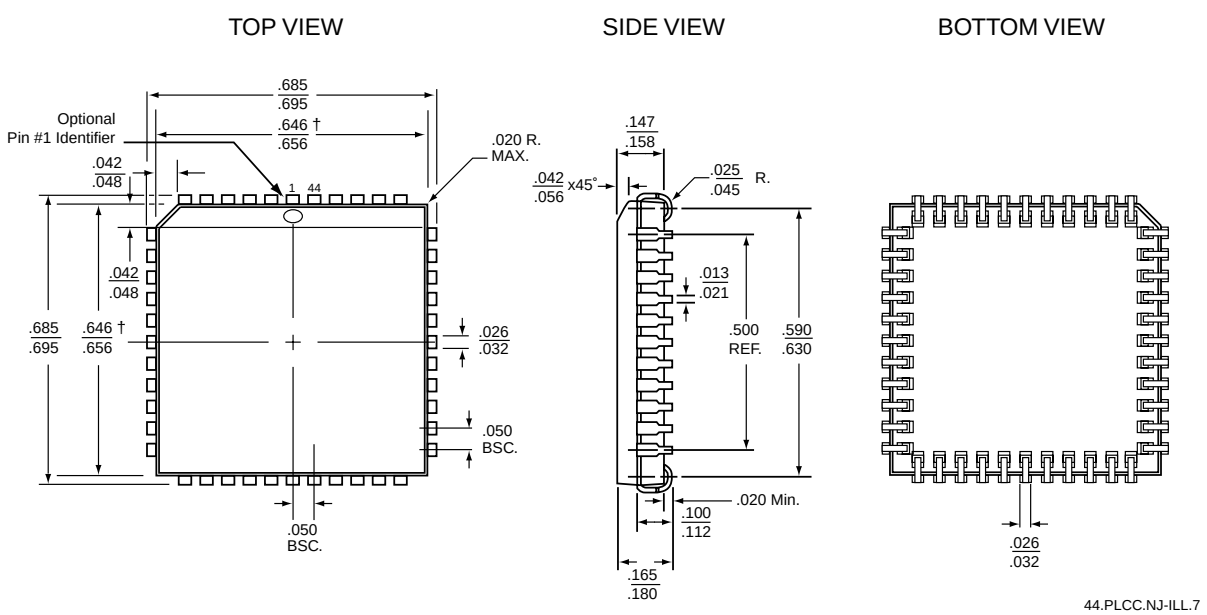
14.0 PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .115; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

40.pdipPI-ILL.7

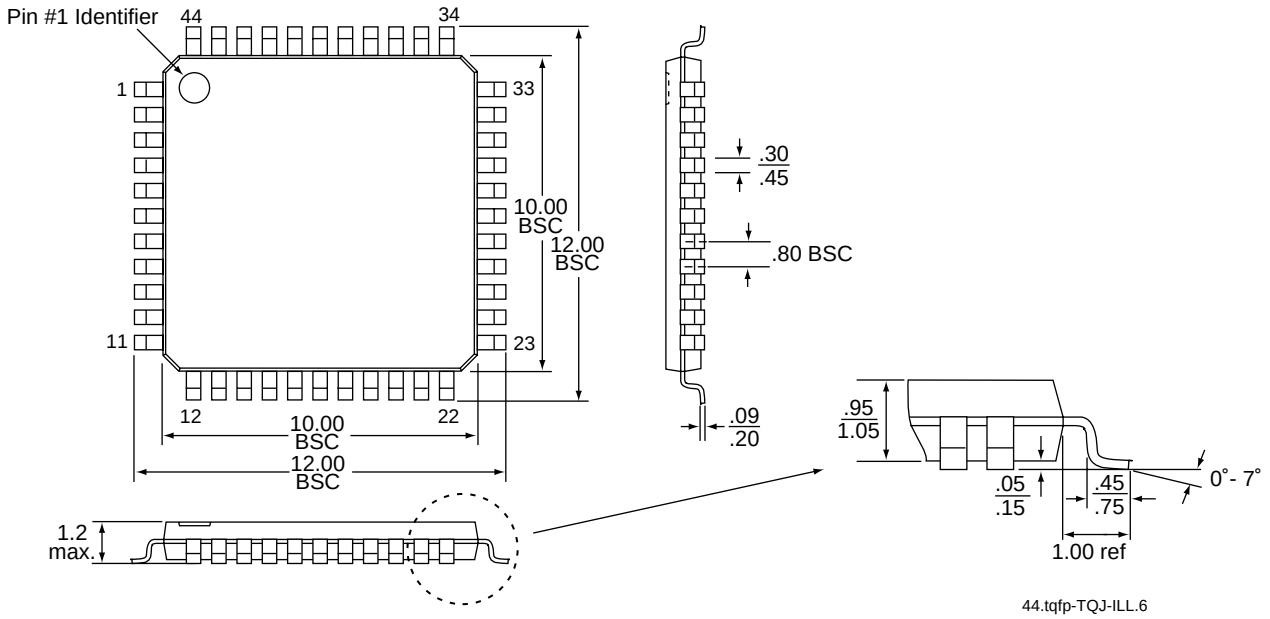
40-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PI



44.PLCC.NJ-ILL.7

Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .650; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

44-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NJ



Note:
1. Complies with JEDEC publication 95 MS-026 ACB dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±0.05) mm.
4. Package body dimensions do not include mold flash. Maximum allowable mold flash is .25mm.

44-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQJ

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