



IDT<sup>®</sup> 89HPEB383  
PCI Express<sup>®</sup> Bridge

User Manual

July 2011

6024 Silver Creek Valley Road, San Jose, California 95138  
Telephone: (800) 345-7015 • (408) 284-8200 • FAX: (408) 284-2775  
Printed in U.S.A.  
©2011 Integrated Device Technology, Inc.

---

---

#### GENERAL DISCLAIMER

Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

#### CODE DISCLAIMER

Code examples provided by IDT are for illustrative purposes only and should not be relied upon for developing applications. Any use of the code examples below is completely at your own risk. IDT MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND CONCERNING THE NONINFRINGEMENT, QUALITY, SAFETY OR SUITABILITY OF THE CODE, EITHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. FURTHER, IDT MAKES NO REPRESENTATIONS OR WARRANTIES AS TO THE TRUTH, ACCURACY OR COMPLETENESS OF ANY STATEMENTS, INFORMATION OR MATERIALS CONCERNING CODE EXAMPLES CONTAINED IN ANY IDT PUBLICATION OR PUBLIC DISCLOSURE OR THAT IS CONTAINED ON ANY IDT INTERNET SITE. IN NO EVENT WILL IDT BE LIABLE FOR ANY DIRECT, CONSEQUENTIAL, INCIDENTAL, INDIRECT, PUNITIVE OR SPECIAL DAMAGES, HOWEVER THEY MAY ARISE, AND EVEN IF IDT HAS BEEN PREVIOUSLY ADVISED ABOUT THE POSSIBILITY OF SUCH DAMAGES. The code examples also may be subject to United States export control laws and may be subject to the export or import laws of other countries and it is your responsibility to comply with any applicable laws or regulations.

#### LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

# Contents

<b>About this Document</b> .....	<b>1</b>
Scope .....	1
Document Conventions .....	1
Revision History .....	3
<b>1. Functional Overview</b> .....	<b>5</b>
1.1 Overview .....	5
1.2 Features .....	6
1.2.1 General Features .....	6
1.2.2 PCIe Features .....	7
1.2.3 PCI Features .....	7
1.3 Device Architecture .....	8
1.4 Typical Applications .....	10
<b>2. Signal Descriptions</b> .....	<b>13</b>
2.1 Overview .....	13
2.2 PCIe Interface Signals .....	14
2.3 PCI Interface Signals .....	15
2.4 EEPROM Interface Signals .....	18
2.5 JTAG Interface Signals .....	19
2.6 Power-up Signals .....	19
2.7 Power Supply Signals .....	20
<b>3. Data Path</b> .....	<b>21</b>
3.1 Overview .....	21
3.1.1 Upstream Data Path .....	21
3.1.2 Downstream Data Path .....	22
3.2 Transaction Management .....	23
3.2.1 Upstream Transaction Management .....	23
3.2.2 Downstream Transaction Management .....	24
3.3 Buffer Structure .....	24
3.3.1 Upstream Non-posted Buffer .....	24
3.3.2 Upstream Posted Buffer .....	25
3.3.3 Downstream Non-posted Buffer .....	26
3.3.4 Downstream Posted Buffer .....	26
3.4 Flow Control .....	26
3.5 Prefetching Algorithm .....	27
3.6 Short Term Caching .....	28
3.7 Polarity Inversion .....	28
<b>4. Addressing</b> .....	<b>29</b>
4.1 Overview .....	29
4.2 Memory-mapped I/O Space .....	29

4.3	Prefetchable Space .....	31
4.4	I/O Space .....	32
4.5	VGA Addressing .....	34
4.6	ISA Addressing .....	35
4.7	Non-transparent Addressing .....	37
4.7.1	PCIe to PCI Non-prefetchable Address Remapping .....	37
4.7.2	PCIe to PCI Prefetchable Address Remapping .....	37
4.7.3	PCI to PCIe Address Remapping .....	38
4.8	Legacy Mode .....	41
<b>5.</b>	<b>Configuration Transactions .....</b>	<b>43</b>
5.1	Overview .....	43
5.2	Configuration Transactions .....	43
5.2.1	Type 0 Configuration Transactions .....	44
5.2.2	Type 1 Configuration Transactions .....	44
5.2.3	Type 1 to Type 0 Conversion .....	45
5.2.4	Type 1 to Type 1 Forwarding .....	45
5.2.5	Type 1 to Special Cycle Forwarding .....	46
5.3	PCIe Enhanced Configuration Mechanism .....	46
5.4	Configuration Retry Mechanisms .....	47
<b>6.</b>	<b>Bridging .....</b>	<b>49</b>
6.1	Overview .....	49
6.2	Flow Control Advertisements .....	49
6.3	Buffer Size and Management .....	50
6.4	Assignment of Requestor ID and Tag .....	50
6.5	Forwarding of PCIe to PCI .....	50
6.5.1	PCIe Memory Write Request .....	50
6.5.2	PCIe Non-posted Requests .....	50
6.6	Forwarding of PCI to PCIe .....	51
6.6.1	PCI Memory Write Request .....	51
6.6.2	PCI Non-posted Requests .....	52
6.7	PCI Transaction Support .....	53
6.8	PCIe Transaction Support .....	54
6.9	Message Transactions .....	55
6.9.1	INTx Interrupt Signaling .....	55
6.9.2	Power Management .....	55
6.9.3	Locked Transaction .....	55
6.9.4	Slot Power Limit .....	55
6.9.5	Vendor-defined and Device ID .....	55
6.10	Transaction Ordering .....	56
6.11	Exclusive Access .....	57
<b>7.</b>	<b>PCI Arbitration .....</b>	<b>59</b>
7.1	Overview .....	59
7.2	Block Diagram .....	59

7.3	PCI Arbitration Scheme .....	60
<b>8.</b>	<b>Interrupt Handling .....</b>	<b>63</b>
8.1	Overview .....	63
8.2	Interrupt Sources .....	64
8.3	Interrupt Routing .....	64
<b>9.</b>	<b>Error Handling .....</b>	<b>65</b>
9.1	Overview .....	65
9.2	PCIe as Originating Interface .....	68
9.2.1	Received Poisoned TLPs .....	69
9.2.2	Received ECRC Errors .....	70
9.2.3	PCI Uncorrectable Data Errors .....	71
9.2.4	PCI Uncorrectable Address/Attribute Errors .....	72
9.2.5	Received Master-Abort on PCI Interface .....	73
9.2.6	Received Target-Abort On PCI Interface .....	74
9.3	PCI as Originating Interface .....	75
9.3.1	Received PCI Errors .....	76
9.3.2	Unsupported Request Completion Status .....	79
9.3.3	Completer Abort Completion Status .....	79
9.4	Timeout Errors .....	79
9.4.1	PCIe Completion Timeout Errors .....	80
9.4.2	PCI Delayed Transaction Timeout Errors .....	80
9.5	Other Errors .....	80
9.6	Error Handling Tables .....	81
<b>10.</b>	<b>Reset and Clocking .....</b>	<b>87</b>
10.1	Reset .....	87
10.1.1	PCIe Link Reset .....	88
10.1.2	PCI Bus Reset .....	89
10.2	Clocking .....	90
10.2.1	PCIe Clocking .....	90
10.2.2	PCI Clocking .....	91
<b>11.</b>	<b>Power Management .....</b>	<b>93</b>
11.1	Overview .....	93
11.1.1	Features .....	93
11.1.2	Unsupported Features .....	94
11.2	Power Management Capabilities .....	94
11.3	Power States .....	94
11.3.1	ASPM .....	94
11.3.2	L0 State .....	95
11.3.3	L0s State .....	95
11.3.4	L1 State .....	95
11.3.5	L2/L3 Ready .....	95
11.3.6	L3 State .....	95

11.3.7	LDn State . . . . .	95
11.3.8	Link State Summary . . . . .	96
11.3.9	Device Power States . . . . .	97
11.3.10	D0 State . . . . .	97
11.3.11	D3 <sub>Hot</sub> State . . . . .	97
11.3.12	D3 <sub>Cold</sub> State . . . . .	97
11.3.13	D State Transitions . . . . .	98
11.3.14	Power Management Event . . . . .	98
11.3.15	Power State Summary . . . . .	99
11.4	Power Saving Modes . . . . .	100
<b>12.</b>	<b>Serial EEPROM . . . . .</b>	<b>101</b>
12.1	Overview . . . . .	101
12.2	System Diagram . . . . .	102
12.3	EEPROM Image . . . . .	104
12.4	Functional Timing . . . . .	105
<b>13.</b>	<b>JTAG . . . . .</b>	<b>109</b>
13.1	Overview . . . . .	109
13.2	TAP Controller Initialization . . . . .	110
13.3	Instruction Register . . . . .	110
13.4	Bypass Register . . . . .	110
13.5	JTAG Device ID Register . . . . .	110
13.6	JTAG Register Access . . . . .	111
13.6.1	Register Access from JTAG . . . . .	111
13.6.2	Write Access to Registers from the JTAG Interface . . . . .	111
13.6.3	Read Access to Registers from JTAG Interface . . . . .	112
13.7	Dedicated Test Pins . . . . .	113
13.8	Accessing SerDes TAP Controller . . . . .	113
<b>14.</b>	<b>Register Descriptions . . . . .</b>	<b>115</b>
14.1	Overview . . . . .	115
14.2	PCI Configuration Space . . . . .	117
14.3	Register Map . . . . .	120
14.3.1	PCI Identification Register . . . . .	123
14.3.2	PCI Control and Status Register . . . . .	124
14.3.3	PCI Class Register . . . . .	128
14.3.4	PCI Miscellaneous 0 Register . . . . .	129
14.3.5	PCI Bus Number Register . . . . .	130
14.3.6	PCI Secondary Status and I/O Limit and Base Register . . . . .	131
14.3.7	PCI Memory Base and Limit Register . . . . .	134
14.3.8	PCI PFM Base and Limit Register . . . . .	135
14.3.9	PCI PFM Base Upper 32 Address Register . . . . .	136
14.3.10	PCI PFM Limit Upper 32 Address Register . . . . .	136
14.3.11	PCI I/O Address Upper 16 Register . . . . .	137
14.3.12	PCI Capability Pointer Register . . . . .	138

---

14.3.13	PCI Bridge Control and Interrupt Register	139
14.3.14	Secondary Retry Count Register	145
14.3.15	PCI Miscellaneous Control and Status Register	147
14.3.16	PCI Miscellaneous Clock Straps Register	150
14.3.17	Upstream Posted Write Threshold Register	152
14.3.18	Completion Timeout Register	153
14.3.19	Clock Out Enable Function and Debug Register	154
14.3.20	SERRDIS_OPQEN_DTC Register	155
14.4	Upstream Non-transparent Address Remapping Registers	156
14.4.1	NTMA Control Register	156
14.4.2	NTMA Primary Upper Base Register	157
14.4.3	NTMA Secondary Lower Base Register	157
14.4.4	NTMA Secondary Upper Base Register	158
14.4.5	NTMA Secondary Lower Limit Register	158
14.4.6	NTMA Secondary Upper Limit Register	159
14.5	PCI Capability Registers	159
14.5.1	SSID/SSVID Capability	159
14.5.2	SSID Capability Register	160
14.5.3	SSID ID Register	161
14.5.4	PCI Power Management Capability Register	162
14.5.5	PCI Power Management Control and Status Register	164
14.5.6	EEPROM Control Register	166
14.5.7	Secondary Bus Device Mask Register	167
14.5.8	Short-term Caching Period Register	169
14.5.9	Retry Timer Status Register	170
14.5.10	Prefetch Control Register	171
14.6	PCIe Capability Registers	173
14.6.1	PCIe Capabilities Register	173
14.6.2	PCIe Device Capabilities Register	175
14.6.3	PCIe Device Control and Status Register	177
14.6.4	PCIe Link Capabilities Register	180
14.6.5	PCIe Link Control Register	182
14.7	Downstream Non-transparent Address Remapping Registers	184
14.7.1	Secondary Bus Non-prefetchable Address Remap Control Register	184
14.7.2	Secondary Bus Non-prefetchable Upper Base Address Remap Register	185
14.7.3	Secondary Bus Prefetchable Address Remap Control Register	185
14.7.4	Secondary Bus Prefetchable Upper Base Address Remap Register	186
14.7.5	Primary Bus Non-prefetchable Upper Base Address Remap Register	186
14.7.6	Primary Bus Non-prefetchable Upper Limit Remap Register	187
14.8	Advanced Error Reporting Capability Registers	188
14.8.1	PCIe Advanced Error Reporting Capability Register	188
14.8.2	PCIe Uncorrectable Error Status Register	189
14.8.3	PCIe Uncorrectable Error Mask Register	190
14.8.4	PCIe Uncorrectable Error Severity Register	191
14.8.5	PCIe Correctable Error Status Register	192

14.8.6	PCIe Correctable Error Mask Register	193
14.8.7	PCIe Advanced Error Capabilities and Control Register	194
14.8.8	PCIe Header Log 1 Register	195
14.8.9	PCIe Header Log 2 Register	195
14.8.10	PCIe Header Log 3 Register	196
14.8.11	PCIe Header Log 4 Register	196
14.8.12	PCIe Secondary Uncorrectable Error Status Register	197
14.8.13	PCIe Secondary Uncorrectable Error Mask Register	198
14.8.14	PCIe Secondary Uncorrectable Error Severity Register	199
14.8.15	PCIe Secondary Error Capabilities and Control Register	200
14.8.16	PCIe Secondary Header Log 1 Register	200
14.8.17	PCIe Secondary Header Log 2 Register	201
14.8.18	PCIe Secondary Header Log 3 Register	202
14.8.19	PCIe Secondary Header Log 4 Register	202
14.8.20	Replay Latency Register	203
14.8.21	ACK/NACK Update Latency Register	204
14.8.22	N_FTS Register	205
14.9	PCIe and SerDes Control and Status Registers	207
14.9.1	Base Offset Address Calculation	207
14.9.2	PCIe Per-Lane Transmit and Receive Registers	208
14.9.3	PCIe Transmit and Receive Status Register	208
14.9.4	PCIe Output Status and Transmit Override Register	209
14.9.5	PCIe Receive and Output Override Register	210
14.9.6	PCIe Debug and Pattern Generator Control Register	211
14.9.7	PCIe Pattern Matcher Control and Error Register	212
14.9.8	PCIe SS Phase and Error Counter Control Register	213
14.9.9	PCIe Scope Control and Frequency Integrator Register	214
14.9.10	PCIe Clock Module Control and Status Registers	215
14.9.11	PCIe Control and Level Status Register	215
14.9.12	PCIe Control and Level Override Register	216

## 15. Electrical Characteristics .....219

15.1	Absolute Maximum Ratings	219
15.2	Recommended Operating Conditions	220
15.3	Power Characteristics	220
15.4	Power Supply Sequencing	221
15.5	DC Operating Characteristics	221
15.6	AC Timing Specifications	222
15.6.1	PCI Interface AC Signal Timing	222
15.6.2	PCIe Differential Transmitter Output Specification	223
15.6.3	PCIe Differential Receiver Input Specifications	227
15.6.4	Reference Clock	230
15.6.5	Boundary Scan Test Signal Timing	231
15.6.6	Reset Timing	231
15.7	AC Timing Waveforms	232



**16. Packaging . . . . . 235**

- 16.1 Pinouts and Mechanical Diagrams . . . . . 236
  - 16.1.1 QFP Package Pinout . . . . . 236
  - 16.1.2 QFP Package Drawing . . . . . 237
  - 16.1.3 QFN Package Pinout . . . . . 239
  - 16.1.4 QFN Package Drawing . . . . . 240
- 16.2 Thermal Characteristics . . . . . 242
- 16.3 Moisture Sensitivity . . . . . 244

**17. Ordering Information . . . . . 245**

**Glossary . . . . . i**

**Index . . . . . iii**



# Figures

Figure 1:	PEB383 Block Diagram	6
Figure 2:	PEB383 Device Architecture	8
Figure 3:	Network Interface Card Application	10
Figure 4:	DVR Card Application	11
Figure 5:	Motherboard Application	11
Figure 6:	ExpressCard Application	12
Figure 7:	Upstream Data Path[update for PEB383]	22
Figure 8:	Downstream Data Path	23
Figure 9:	Memory-mapped I/O Address Space	30
Figure 10:	64-bit Prefetchable Memory Address Range	32
Figure 11:	I/O Address Space	34
Figure 12:	ISA Mode I/O Addressing	36
Figure 13:	Memory Window Remapping Example	40
Figure 14:	PCIe Configuration Address Format	43
Figure 15:	PCI Type 0 Configuration Address Format	44
Figure 16:	PCI Type 1 Configuration Address Format	44
Figure 17:	PCI Arbiter Block Diagram	59
Figure 18:	PCI Arbitration Priority	60
Figure 19:	Arbitration Pointers – Example 1	61
Figure 20:	Arbitration Pointers – Example 2	61
Figure 21:	Interrupt Handling Diagram	63
Figure 22:	PCIe Flowchart of Device Error Signaling and Logging Operations	67
Figure 23:	Transaction Error Forwarding with PCIe as Originating Interface	68
Figure 24:	Transaction Error Forwarding with PCI as Originating Interface	75
Figure 25:	Reset Timing	88
Figure 26:	PCIe Clocking	90
Figure 27:	PCI Clocking	91
Figure 28:	PCIe Link Power Management States	96
Figure 29:	D State Transitions	98
Figure 30:	EEPROM Interface	102
Figure 31:	9-bit EEPROM Read Timing	105
Figure 32:	16-bit EEPROM Read Timing	106
Figure 33:	9-bit EEPROM Write Timing	106
Figure 34:	16-bit EEPROM Write Timing	107
Figure 35:	EEPROM WREN Instruction Timing	107
Figure 36:	EEPROM RDSR Instruction Timing	107
Figure 37:	Read/Write Access from JTAG — Serial Data In	111
Figure 38:	Observe from JTAG — Serial Data Out	111
Figure 39:	PCIe SerDes Connections	113
Figure 40:	Transmitter Eye Voltage and Timing Diagram	226
Figure 41:	Minimum Receiver Eye Timing and Voltage Compliance Specification	229
Figure 42:	Weighing Function for RMS Phase Jitter Calculation	230

---

Figure 43: Input Timing Measurement Waveforms . . . . .	232
Figure 44: Output Timing Measurement Waveforms . . . . .	233
Figure 45: PCI TOV (max) Rising Edge AC Test Load . . . . .	233
Figure 46: PCI TOV (max) Falling Edge AC Test Load . . . . .	233
Figure 47: PCI TOV (min) AC Test Load . . . . .	234

## Tables

Table 1:	Pin Types	13
Table 2:	PCIe Interface Signals	14
Table 3:	PCI Interface Signals	15
Table 4:	EEPROM Interface Signals	18
Table 5:	JTAG Interface Signals	19
Table 6:	Power-up Signals	19
Table 7:	Power Supply Signals	20
Table 8:	Completion Buffer Allocation	25
Table 9:	Initial Credit Advertisement	27
Table 10:	PCI Transaction Support	53
Table 11:	PCIe Transaction Support	54
Table 12:	Transaction Ordering	56
Table 13:	Error Forwarding Requirements (Step A to Step B) for Received PCIe Errors	68
Table 14:	Bridge Requirements for Transactions Requiring a Completion (Immediate Response)	68
Table 15:	Error Forwarding Requirements for Received PCI Errors	75
Table 16:	Error Forwarding Requirements for PCI Delayed Transaction	76
Table 17:	ECRC Errors	81
Table 18:	Poisoned TLP Errors	81
Table 19:	Malformed TLP Errors	82
Table 20:	Link and Flow Control Errors	83
Table 21:	Uncorrectable Data/Address Errors	84
Table 22:	Received Master/Target Abort Error	85
Table 24:	Request Errors	86
Table 23:	Completion Errors	86
Table 25:	Reset Summary	87
Table 26:	Reset Timing	88
Table 27:	PCI Clocking	91
Table 28:	PCIe Link States	96
Table 29:	Power Management State Summary	99
Table 30:	Power saving modes	100
Table 31:	EEPROM Image	104
Table 32:	PCI Type 1 Configuration Header	117
Table 33:	SSID Capability Registers	117
Table 34:	Power Management Capability Registers	118
Table 35:	PCIe Capability Registers	118
Table 36:	Advanced Error Reporting Capability Registers	118
Table 37:	Register Map	120
Table 38:	SerDes Per-lane and Clock Control and Status Register Map	207
Table 39:	TX_LVL Values	216
Table 40:	Absolute Maximum Ratings – PCI	219
Table 41:	Absolute Maximum Ratings – PCIe	219
Table 42:	Recommended Operating Conditions	220

---

Table 43:	PEB383 Power Dissipation . . . . .	220
Table 44:	PEB383 Power Dissipation per Supply . . . . .	221
Table 45:	DC Operating Characteristics . . . . .	221
Table 46:	PCI Clock (PCI_CLK) Specification . . . . .	222
Table 47:	PCIe Differential Transmitter Output Specification . . . . .	223
Table 48:	PCIe Differential Receiver Input Specifications . . . . .	227
Table 49:	Reference Clock (PCIE_REFCLK_n/p) Electrical Characteristics . . . . .	230
Table 50:	Boundary Scan Test Signal Timings . . . . .	231
Table 51:	Reset Timing . . . . .	231
Table 52:	Thermal Specifications — 66MHz . . . . .	242
Table 53:	Thermal Specifications — 33MHz . . . . .	243

---

## About this Document

This section discusses the following topics:

- “Scope” on page 1
  - “Document Conventions” on page 1
- 

## Scope

The PEB383 User Manual discusses the features, configuration requirements, and design architecture of the PEB383.

## Document Conventions

This document uses the following conventions.

### Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase “n”. An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME <sub>n</sub>	NAME <sub>n</sub> [3]
Active high	NAME	NAME[3]

### Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal’s active or inactive state (they are denoted by “\_p” and “\_n”, respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME <sub>p</sub> = 0 NAME <sub>n</sub> = 1	NAME <sub>p</sub> [3] = 0 NAME <sub>n</sub> [3] = 1
Active	NAME <sub>p</sub> = 1 NAME <sub>n</sub> = 0	NAME <sub>p</sub> [3] is 1 NAME <sub>n</sub> [3] is 0

## Object Size Notation

- A *byte* is an 8-bit object.
- A *word* is a 16-bit object.
- A *doubleword* (Dword) is a 32-bit object.

## Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).
- Registers that have multiple iterations are denoted by {*x..y*} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

## Symbols



This symbol indicates a basic design concept or information considered helpful.



This symbol indicates important configuration information or suggestions.



This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

## Specification Status

- Version 0.25 – This specification describes early design and functional information about a device. It is available at the G2 gate, which precedes the definition and planning phase.
- Version 0.5 – This specification describes early design and functional information about a device. It is available after the G2 gate, but during the definition and planning phase.
- Version 0.75 – This specification describes the majority of functional information about a device. It is available at the G3 gate, which precedes the development phase.
- Version 1.0 – This specification describes all the functional information about a device. It is available at the G4 gate, which precedes the qualification (tape-out) phase.



---

## Revision History

**October 22, 2009:** Initial publication of PEB383 User Manual.

**November 18, 2009:** Updated pinouts for QFN and QFP packages.

**December 8, 2009:** Updated pinouts and package drawings for QFN and QFP packages.

**December 18, 2009:** Added simulated power numbers to Table 43. Updated Tables 51 and 52 with simulated Thermal Characteristics values. Updated pinouts and package drawings for QFN and QFP packages.

**January 20, 2010:** In Table 7, changed power numbers for Core, PCIe, and PLL from 1.0V to 1.05V in the Description column and from 1.2V to 1.05V in the Design Rec. column. In Table 42, changed power numbers for Core, PCIe, and PLL from 1.2V to 1.05V and also changed minimum and maximum values for these 3 parameters. In Table 43, changed power numbers for Core, PCIe, and PLL from 1.0V to 1.05V.

**March 29, 2010:** In Table 3, changed pull-up resistor values from 2.4K to 8.2K for Interrupts A, B, C, and D.

**May 5, 2010:** In Table 42, changed TA min and max temperatures to 0 and 70 respectively. In Section 15.3, updated old Table 43 and added new Table 44 for Power Dissipation values.

**May 28, 2010:** In Chapter 16, Packaging, updated QFP package drawing. Added new Chapter 17, Ordering Information.

**August 3, 2010:** In Chapter 17, added Tape and Reel to ordering codes.

**November 23, 2010:** In Chapter 16, replaced existing QFN package drawing with revised PSC-4327.

**January 5, 2011:** In Chapter 13, section 13.7, deleted last bullet containing reference to TEST\_BIDIR\_CTRL.

**March 7, 2011:** In Chapter 14, changes bit types labeled RE to RWL, added description for RWL in section 14.1, revised description for bits 0 and 1 in register CLKOUT\_ENB\_FUNC\_DBG, and changed Reset Value in RID field to 0x01 in register PCI\_CLSS. In Chapter 16, section 16.1.2, added revised 128-pin QFP package drawing.

**May 17, 2011:** In Chapter 14, section 14.5.1, added text to the third paragraph that starts with “Note that...”. Added ZB silicon to Order page in Chapter 17.

**May 26, 2011:** In Chapter 15, Table 42, changed maximum ambient temperature from 70 to 85°C.

**June 21, 2011:** In Chapter 2, Table 3, changed pull-up for PCI\_INTA-D pins from 8.2K to 2.4K.

**July 25, 2011:** In Chapter 2, Table 3, revised text in Design Recommendation for PCIE\_REFCLK pins.



---

# 1. Functional Overview

Topics discussed include the following:

- “Overview”
- “Features”
- “Device Architecture”
- “Typical Applications”

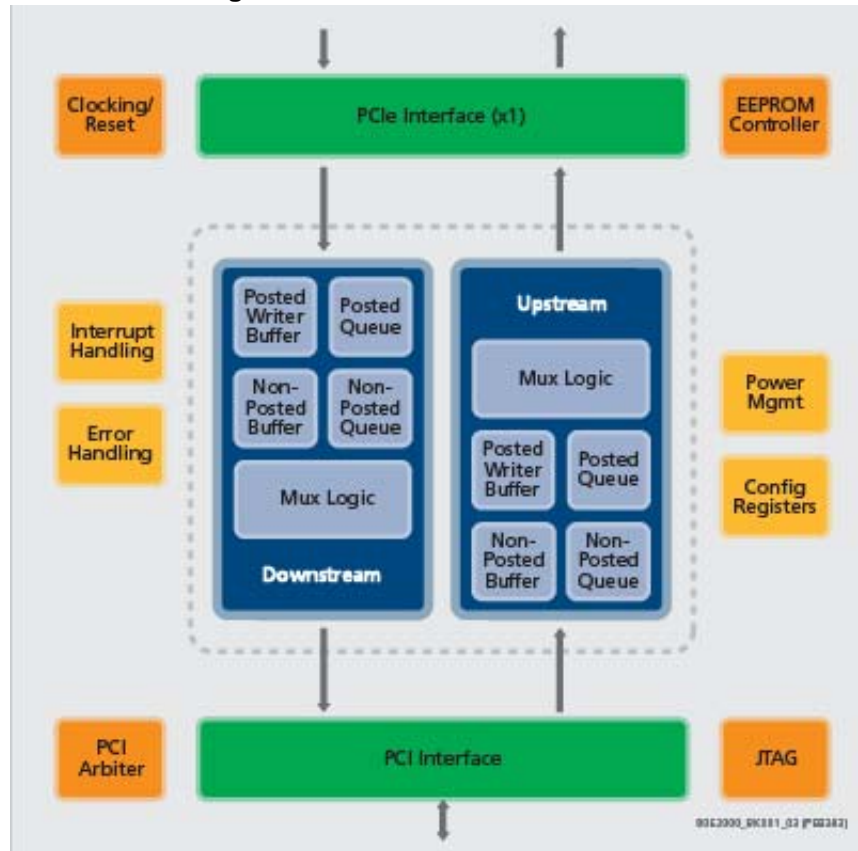
---

## 1.1 Overview

The IDT PEB383 is a high-performance bus bridge that connects the PCI Express (PCIe) protocol to the PCI bus standard (see [Figure 1](#)).

The PEB383’s PCIe Interface supports a x1 lane PCIe configuration. This enables the bridge to offer exceptional throughput performance of up to 2.5 Gbps per transmit and receive direction. The device’s PCI Interface can operate up to 66 MHz. This interface offers designers extensive flexibility by supporting the following addressing modes: transparent, and non-transparent.

Figure 1: PEB383 Block Diagram



## 1.2 Features

The PEB383's key features are listed in the following sub-sections.

### 1.2.1 General Features

- Forward bridge, PCIe to PCI
- Single store and forward for optimal latency performance
- Supports two modes of addressing:
  - Transparent: For efficient, flow-through configurations
  - Non-transparent: For address remapping of the PCIe and the PCI domains
- Compliant to the following specifications:
  - *PCI Express Base Specification (Revision 1.1)*
  - *PCI Express-to-PCI/PCI-X Bridge Specification (Revision 1.0)*
  - *PCI-to-PCI Bridge Specification (Revision 1.2)*
  - *PCI Local Bus Specification (Revision 3.0)*
  - *PCI Bus Power Management Interface Specification (Revision 1.2)*

- 3.3V PCI I/Os with 5V tolerant I/Os
- Support for four external PCI bus masters through an integrated arbiter
- Support for external PCI bus arbiter
- Support for Masquerade mode (can overwrite vendor and device ID from EEPROM)
- JTAG IEEE 1149.1, 1149.6
- Support for D0, D3 hot, D3 cold power management states
- Support for Subsystem ID (SSID) and Subsystem Vendor ID (SSVID)
- Legacy mode support for subtractive decode
- Exclusive access using PCI\_LOCKn
- Packaged in a 14x14mm 128 pin TQFP and a 10x10mm 132 pin QFN.

### 1.2.2 PCIe Features

- 1 lane
- 128-byte maximum payload
- Advanced error reporting capability
- End-to-end CRC (ECRC) check and generation
- Up to four outstanding memory reads
- 512-byte read completion buffer
- ASPM L0s link state power management
- ASPM L1
- Legacy interrupt signaling

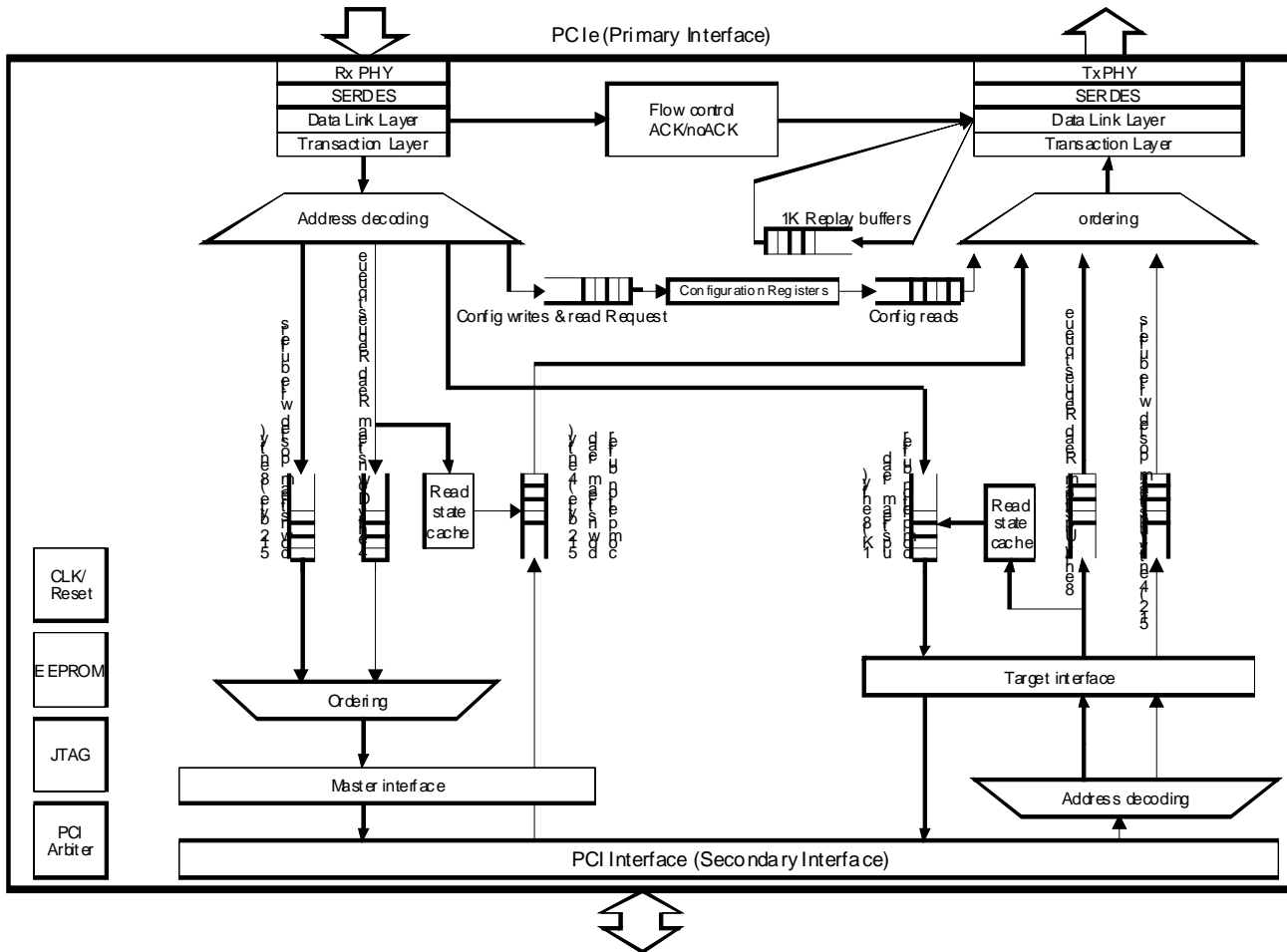
### 1.2.3 PCI Features

- 32/64-bit addressing
- 32-bit data bus
- 5V tolerant
- Exclusive access using PCI\_LOCKn
- 25-, 33-, 50-, and 66-MHz operation
- Up to four outstanding read requests
- 1-KB read completion buffer
- Clock outputs for four PCI devices
- Short-term caching support

## 1.3 Device Architecture

A high-level, architectural diagram of the PEB383 is displayed in Figure 2. For more information about data flow through the device, see “Upstream Data Path” and “Downstream Data Path”.

Figure 2: PEB383 Device Architecture



Packets received on the PCIe Interface are processed by the data link layer and transaction layer, if applicable. If a packet is destined for the transaction layer, its address is decoded and forwarded to the appropriate destination:

- Configuration register
- Downstream posted write buffer
- Downstream read request queue
- Downstream read completion buffer

PCI data that is destined for the PCIe fabric are subject to PCIe ordering rules. Data is pulled from the appropriate queue:

- Configuration register
- Upstream posted write buffer
- Upstream read request queue
- Upstream read completion buffer

PCI transactions that are decoded for the PCIe address space are forwarded to the appropriate queue:

- Upstream read request queue
- Upstream posted write buffer

Transactions destined for downstream devices on the PCI bus, are subject to PCI ordering rules. Data is pulled from the appropriate queue:

- Downstream posted write buffer
- Downstream read request queue

PCIe is a serialized protocol at the physical layer, and a packetized protocol at the data link layer. The PCIe lane operates at 2.5 Gb symbol rate, or at 2.0 Gb data rate; the difference is a result of the 8/10b coding process. The PEB383 uses the following processes to ensure the accurate and timely delivery of data through the data link layer:

- Credit-based flow control – Prevents data loss and congestion
- ACK/noACK protocol and End-to-End CRC (ECRC) – Ensures reliable data delivery if bit errors occur
- Replay buffer – Replays packets that are not acknowledged by the receiver (NAK)

In contrast, PCI is a parallel data interface at the physical layer. PCI is a non-packetized protocol. When a bus master starts a read or a write transaction, it indicates only the starting transaction address to the target, and not the size of the read or write. In the case of a PCI write, which is initiated on the PCI Interface and is destined for the root complex, the data is written into an upstream posted write buffer in the PEB383. The end of the write transaction is signaled by the master on the PCI bus. Once the write is completed the data can be forwarded to the PCIe Interface. If the posted write buffer is about to overflow, the PEB383 indicates a retry/disconnect on the PCI bus. Once the posted write buffer empties, the PEB383 can accept additional write transactions. The PEB383 will split write transactions as required to meet PCIe constraints: to prevent a write crossing a 4-KB boundary; if byte enables are used throughout the transaction; or if the quantity of data exceeds the maximum payload size (see MAX\_SIZE in “[PCIe Device Capabilities Register](#)”). The upstream posted write buffer is managed as a simple FIFO.

A read initiated on the PCI bus that is decoded for an upstream target is handled as a delayed transaction by the PEB383. The bridge latches the read transaction and attempts to reserve buffer space in its upstream read completion buffer. If space is successfully reserved in the buffer, the PEB383 initiates a read on the PCIe Interface. When the read data is returned from the root complex, it is stored in the upstream read completion buffer. PCI-initiated reads, however, do not define the amount of data to read. Once the master on the PCI bus retries the read transaction, the transaction is checked to determine if the read data is returned. If it has the read data, the PEB383 responds as the target and transfers the read data to the PCI bus. Note the upstream read completion buffer is not a simple FIFO, as the order that masters on the PCI bus retry is not deterministic. If the completion buffer becomes empty prior to the transaction completing, the PEB383 disconnects from the PCI bus. When the read transaction is completed, the PEB383 discards any prefetched data that is not used and frees up the buffer. The maximum number of outstanding read requests per master is controlled by DTL[7:0] bits in “Secondary Retry Count Register”.

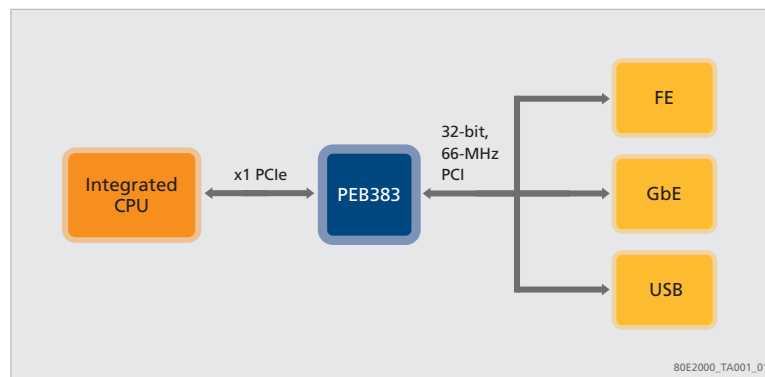
A write initiated on the PCIe Interface with the target on the downstream PCI bus is written into the downstream posted write buffer. The PEB383 acts as the master for the transaction and arbitrates for the PCI bus and initiates the write transaction. The downstream posted write buffer is managed as a FIFO. There will always be space available in the buffer to accept packet data because of the flow control method used by the PCIe data link layer. If the downstream posted write buffer is about to overflow, the upstream device will be informed of this by its lack of credits and will not send any more write data to the PEB383.

A read initiated on the PCIe Interface with the target on the downstream PCI bus is written into the downstream read request queue. The downstream read request queue is managed with flow control credits to prevent overflowing. The PEB383 latches the read transaction and attempts to reserve space in the downstream read completion buffer. If space is successfully reserved in the buffer, the PEB383 acts as the master for the transaction and initiates a read transaction on the PCI bus. Programmable address decoders instruct the PEB383 which transactions on the PCI bus to forward upstream, and which transactions on the PCIe link to forward downstream.

## 1.4 Typical Applications

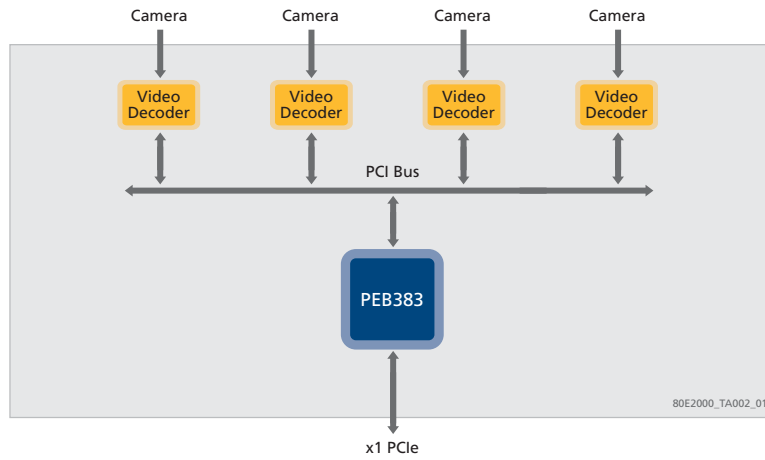
This section illustrates some typical applications for the PEB383.

**Figure 3: Network Interface Card Application**

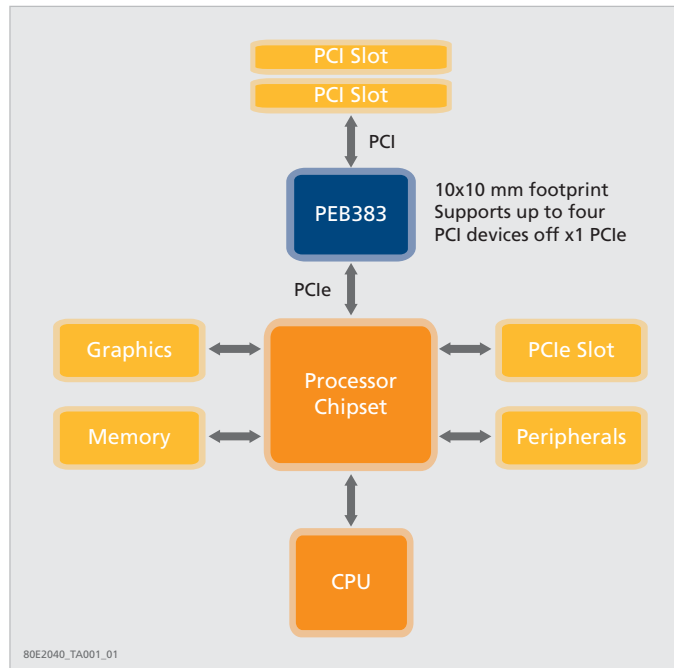




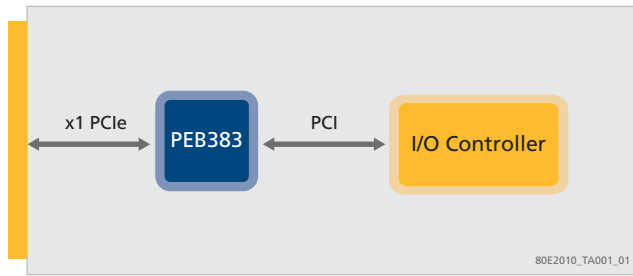
**Figure 4: DVR Card Application**



**Figure 5: Motherboard Application**



**Figure 6: ExpressCard Application**



## 2. Signal Descriptions

Topics discussed include the following:

- “Overview”
- “PCIe Interface Signals”
- “PCI Interface Signals”
- “EEPROM Interface Signals”
- “JTAG Interface Signals”
- “Power-up Signals”
- “Power Supply Signals”

### 2.1 Overview

Signals are classified according to the types defined in the following table.

**Table 1: Pin Types**

Pin Type	Definition
3.3 OD	3.3V CMOS open-drain output
3.3 3-state	3.3V CMOS tri-state output
3.3 Bidir	3.3V CMOS bi-directional
3.3 Bidir PU	3.3V CMOS bi-directional with 265K (+/- 45K) pull-up resistor
3.3 Bidir OD	3.3V CMOS bi-directional open-drain
3.3 In	3.3V CMOS input
3.3 In PU	3.3V CMOS input with 265K (+/- 45K) pull-up resistor
3.3 Out	3.3V CMOS output
PCI Bidir	PCI bi-directional
PCI Bidir OD	PCI bi-directional open-drain
PCI In	PCI input
PCI Out	PCI output
PCI OD	PCI output open-drain

**Table 1: Pin Types (Continued)**

Pin Type	Definition
PCIe Diff Out	PCIe differential output
PCIe Diff In	PCIe differential input

## 2.2 PCIe Interface Signals

**Table 2: PCIe Interface Signals**

Name	Pin Type	Description	Design Recommendation
PCIe_PERSTn	3.3 In	Master reset in: 0 = PEB383 in reset 1 = PEB383 in normal mode	Direct connect to the PERST# signal.
PCIe_TXD_n PCIe_TXD_p	PCIe Diff Out	Transmit Data. These differential pair signals send PCIe 8b/10b encoded symbols and an embedded clock to the link partner.	DC blocking capacitors must be placed in the link between the transmitter and the receiver. Place a 0603 or 0402 0.075uF to 0.1uF ceramic capacitor on each TXD_n, TXD_p signal.
PCIe_RXD_n PCIe_RXD_p	PCIe Diff In	Receive Data. These differential pair signals receive PCIe 8b/10b encoded symbols and an embedded clock from the link partner.	DC blocking capacitors must be placed in the link between the transmitter and the receiver; however, the DC blocking capacitors are normally placed near the transmitter. When designing an add-in card, capacitors are not required on this link. When designing a system board, the DC blocking capacitors should be placed near the transmitter.
PCIe_REFCLK_n PCIe_REFCLK_p	PCIe Diff In	Reference Clock. 100-MHz differential reference clock.	Refer to Board Design Guidelines.
PCIe_REXT	Analog	-	This signal must be connected to VSS with a 191-ohm (1%) resistor.

## 2.3 PCI Interface Signals

**Table 3: PCI Interface Signals**

Name	Pin Type	Description	Design Recommendation
PCI_AD[31:0]	PCI Bidir	Address/Data Bus. These multiplexed signals provide a 32/64-bit address and 32-bit data bus.	None.
PCI_CBEn[3:0]	PCI Bidir	Command/Byte Enables. These multiplexed signals indicate the current transaction type.	None.
PCI_CLK	PCI In	PCI Input Clock. This signal provides timing for the PEB383, either from an external clock or from one of the PCI_CLKO[4:0] signals (see " <b>Clocking</b> ").	None.
PCI_CLKO[4:0]	PCI Out	PCI Output Clocks (see " <b>Clocking</b> ").	Point-to-point connection to PCI device. IDT recommends a 33 Ohm series termination resistor. In Master clocking mode, PCI_CLKO[4] should be connected to PCI_CLK.
PCI_DEVSELn	PCI Bidir	Device Select. A target device asserts this signal when it decodes its address on the bus. The master samples the signal at the beginning of a transaction, and the target rescinds it at the end of the transaction.	Pull up (8.2K) to VIO_PCI.
PCI_FRAMEn	PCI Bidir	Frame. The current initiator drives this signal to indicate the start and duration of a transaction, and the bus target samples it. The bus master rescinds the signal at the end of the transaction.	Pull up (8.2K) to VIO_PCI.

**Table 3: PCI Interface Signals (Continued)**

Name	Pin Type	Description	Design Recommendation
PCI_GNTn[3:0]	PCI Bidir / PCI Out	<p>Bus Grant. The PEB383 uses these multifunction signals to grant access to the PCI bus; however, they are used differently depending on whether or not the PEB383 PCI arbiter is used. If the arbiter is used, then PCI_GNTn[3:0] are outputs used by the PEB383 to grant access to the bus (see “<a href="#">PCI Arbitration</a>”).</p> <p>If an external arbiter is used, PCI_GNTn[0] is an input that is driven by the arbiter to grant the PEB383 access to the bus. The remaining pins, PCI_GNTn[3:1], remain as outputs.</p> <p>The input/output mode is controlled by bit[9] of “<a href="#">PCI Miscellaneous 0 Register</a>” on page 129.</p> <p>Note: The PCI bus arbiter can be placed on the last bus master by bit[8] of “<a href="#">PCI Miscellaneous 0 Register</a>” on page 129.</p>	PCI_GNTn[3:0] outputs connect directly to the PCI device’s PCI_GNTn inputs. Pull ups are not required on unused outputs.
PCI_INTDn	PCI In	Interrupt D.	Pull-up (2.4K) to VIO_PCI.
PCI_INTCn	PCI In	Interrupt C.	Pull-up (2.4K) to VIO_PCI.
PCI_INTBn	PCI In	Interrupt B.	Pull-up (2.4K) to VIO_PCI.
PCI_INTAn	PCI In	Interrupt A.	Pull-up (2.4K) to VIO_PCI.
PCI_IRDYn	PCI Bidir	Initiator Ready. The bus master asserts this signal to indicate it is ready to complete the current transaction.	Pull-up (8.2K) to VIO_PCI.
PCI_LOCKn	PCI OD	Lock. This signal is used by the bus master to lock the currently addressed memory target during a series of exclusive access transactions (see “ <a href="#">Exclusive Access</a> ”).	Pull up (8.2K) to VIO_PCI.

**Table 3: PCI Interface Signals (Continued)**

Name	Pin Type	Description	Design Recommendation
PCI_M66EN	PCI In	66-MHz Enable. This signal enables the PCI Interface for 66-MHz operation. 0 = 33-MHz operation 1 = 66-MHz operation	PCI_M66EN is used only in master clocking mode. <u>Embedded designs</u> Tied to ground for 33-MHz operation; otherwise, pull up to VIO_PCI. <u>Bused designs using PCI slots for add-in cards</u> Place a 10K pull-up resistor (to VIO_PCI) on PCI_M66EN and route the signal from slot to slot. In slave clocking mode, PCI_M66EN can be tied to ground.
PCI_PAR	PCI Bidir	Parity. This signal carries even parity across PCI_AD[31:0] and PCI_CBE[3:0]. The bus master asserts this signal for the address and write data phases. The bus target asserts it for read data phases.	No pull-up or pull-down resistor is required.
PCI_PERRn	PCI Bidir	Parity Error. This signal indicates a parity error occurred during the current data phase. The bus target that receives the data asserts this signal.	Pull up (8.2K) to VIO_PCI.
PCI_PMEn	PCI In	Power Management Event. This signal indicates a power management event occurred (see "Power Management").	Pull up (8.2K) to VIO_PCI.
PCI_REQn[3:0]	PCI In PCI Bidir	Bus Request. These signals are used to request access to the PCI bus. They are used differently, however, depending on whether or not the PEB383 PCI arbiter is used. If the PCI arbiter is used, then PCI_REQn[3:0] are inputs used by external masters to request access to the bus.  If an external arbiter is used, PCI_REQn[0] is an output used by the PEB383 to request access to the bus, while PCI_REQn[3:1] should be pulled high, as they are still inputs.  The input/output mode is controlled by bit[9] of "PCI Miscellaneous 0 Register" on page 129.  Note: The PCI bus arbiter can be placed on the last bus master by bit[8] of "PCI Miscellaneous 0 Register" on page 129.	Pull up (8.2K) to VIO_PCI.

**Table 3: PCI Interface Signals (Continued)**

Name	Pin Type	Description	Design Recommendation
PCI_RSTn	PCI Out	PCI reset: This signal resets all devices on the PC bus.	No pull-up or pull-down resistor is required.
PCI_SERRn	PCI Bidir OD	System Error. This signal indicates an address or attribute phase parity error occurred.	Pull-up (8.2K) to VIO_PCI.
PCI_STOPn	PCI Bidir	Stop. A bus target asserts this signal to indicate it wants to stop the current transaction on the current data phase.	Pull-up (8.2K) to VIO_PCI.
PCI_TRDYn	PCI Bidir	Target Ready. The bus target asserts this signal to indicate it is ready to complete the current data phase.	Pull-up (8.2K) to VIO_PCI.

## 2.4 EEPROM Interface Signals

**Table 4: EEPROM Interface Signals**

Name	Pin Type	Description	Design Recommendation
SR_CLK	3.3 Out	Serial ROM clock: This signal is derived from REFCLKn/p (see "System Diagram").	No pull-up or pull-down resistor is required.
SR_CS <sub>n</sub>	3.3 Out	Serial ROM chip select: This active-low signal activates the chip-select (CS) on the external EEPROM.	
SR_DIN	3.3 Out	Serial ROM data in: This signal transfers output data from the PEB383 to the EEPROM.	
SR_DOUT	3.3 In PU	Serial ROM data out: This signal transfers input data from the EEPROM to the PEB383.	



## 2.5 JTAG Interface Signals

Table 5: JTAG Interface Signals

Name	Pin Type	Description	Design Recommendation
JTAG_TCK	3.3 In	Test Clock. This signal clocks state information and data into and out of the PEB383 during boundary scan.	Connect to 3.3V using a 2K pull-up resistor.
JTAG_TDI	3.3 In PU	Test Data Input. This signal, in conjunction with JTAG_TCK, shifts data and instructions into the TAP controller in a serial bit stream.	Connect to 3.3V using a 2K pull-up resistor.
JTAG_TDO	3.3 Out	Test Data Output. This signal, in conjunction with JTAG_TCK, shifts data and instructions from the TAP controller in a serial bit stream.	If JTAG is not used, leave unconnected.
JTAG_TMS	3.3 In PU	Test Mode Set. This signal controls the state of the TAP controller.	Connect to 3.3V using a 2K pull-up resistor.
JTAG_TRSTn	3.3 In PU	Test Reset. This signal forces the TAP controller into an initialized state. This signal must be pulsed or pulled low externally to reset the TAP controller.	If JTAG is not used, connect this pin to a 2K pull-down resistor. If JTAG is used, connect to output of AND gate where inputs are TRST# and PERST#. For more information, see the <i>PEB383 Evaluation Board User Manual</i> .
TEST_BCE	3.3 In	Test Boundary Scan Compatibility Enabled. This input aids 1149.6 testing and Scope function of PHYs.	For 1149.1 Boundary Scan testing, this pin must be low. For 1149.6 Boundary Scan testing, this pin must be high.
TEST_ON	3.3 In	This signal controls scan shift enable.	Pull down for normal operation.

## 2.6 Power-up Signals

Table 6: Power-up Signals

Name	Pin Type	Description	Design Recommendation
PWRUP_PLL_BYPASS	3.3 In	PLL bypass. This signal bypasses the PLL in the PCI clock generation (see <b>“PCI Clocking”</b> ). 0 = Normal operation 1 = PLL bypass	This signal should always be tied low.

## 2.7 Power Supply Signals

**Table 7: Power Supply Signals**

Name	Pin Type	Description	Design Recommendation <sup>a</sup>
VDD	Core power	1.05V core power	None.
VDD_PCI	I/O power	3.3 volt I/O power for PCI and 3.3V I/O power for CMOS	None.
VDD_PCIE	Core power	1.05V power for SerDes	Connect these signals to the 1.05V source through a ferrite bead. <sup>b</sup>
VDDA_PCIE	Analog power	3.3V analog power for SerDes	Connect these signals to the 3.3V source through a ferrite bead. <sup>b</sup>
VDDA_PLL	Analog power	1.05V analog power for PLL	Connect these signals to the 1.05V source through a ferrite bead. <sup>b</sup>
VIO_PCI	I/O power	5.0 I/O power, for 5.0V I/O compliance. This signal can also be tied to 3.3V if 5.0V compliance is not required.	Connect these signals to a 3.3V or 5V source depending on the PCI devices attached to the PEB383 PCI bus.
VSS	GND	GND, core power	None.
VSS_IO	GND	GND, I/O power	None.
VSSA_PLL	GND	GND, analog PLL power	None.

a. For filtering and decoupling information for these signals, see “Power Supply Filtering and Decoupling” in the *PEB383 Board Design Guidelines*.

b. For more information, see “Analog Power Supply Filtering” in the *PEB383 Board Design Guidelines*.

---

## 3. Data Path

Topics discussed include the following:

- “Overview”
- “Transaction Management”
- “Buffer Structure”
- “Flow Control”
- “Prefetching Algorithm”
- “Short Term Caching”
- “Polarity Inversion”

---

### 3.1 Overview

The PEB383 uses two buffering methods for transferring data between its PCIe and PCI ports:

- Two-stage buffering for its upstream data path
- One-stage buffering in its downstream data path

These buffering methods are summarized in the following sub-sections.

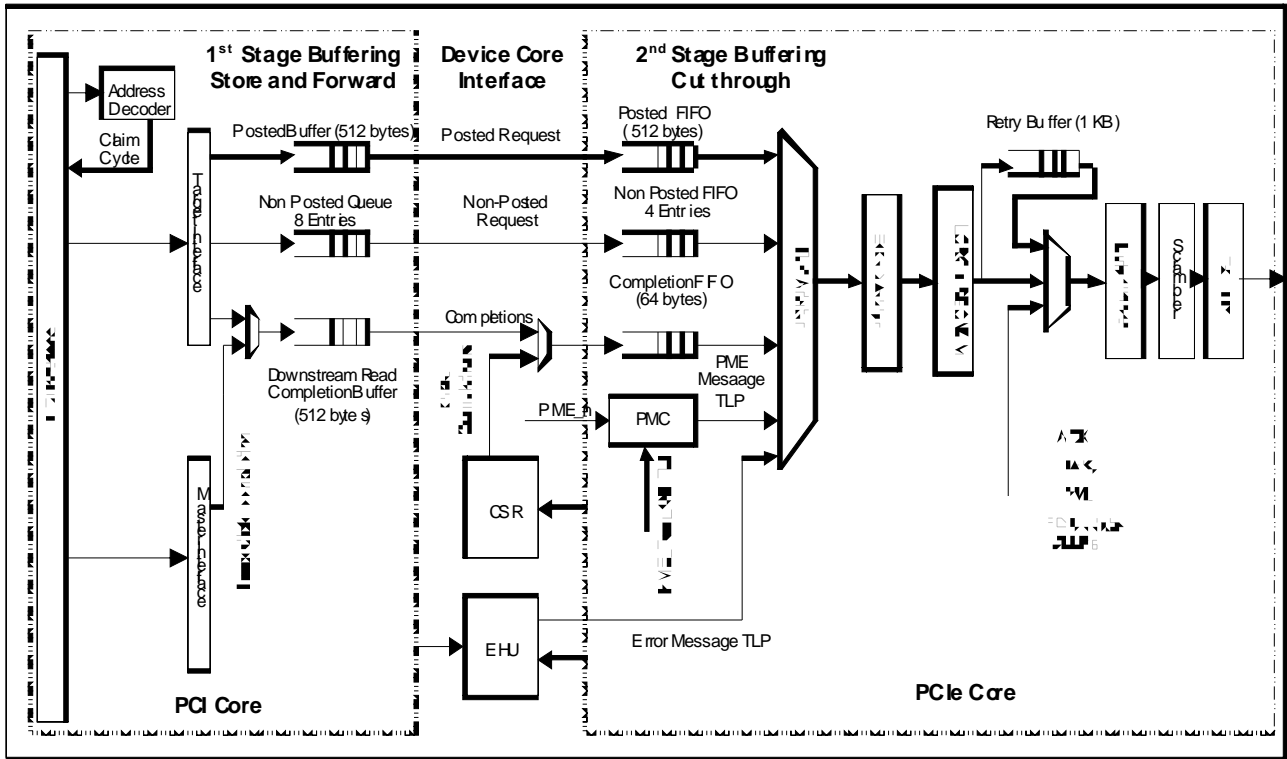
#### 3.1.1 Upstream Data Path

Two-stage buffering in the upstream path consists of two different sized buffers for each transaction type: posted, non-posted, and completion (see [Figure 7](#)).

The first-stage buffering in the PCI Core, which supports the store and forward method, meets the synchronization requirements of PCI and PCIe. This buffer design also provides optimized throughput and improved latencies.

The second-stage buffering in the PCIe Core, which supports the cut-through method, handles the possible backpressure due to scaled down link, lack of flow control credits, and replay. Posted and completion buffers allow the PEB383 to accept a few more cycles of data transfer even after the assertion of stall which indicates to the initiator in the PCI Core to stop the data transfer. This buffer design ensures idle cycles are not inserted in data cycles while forwarding TLPs to its egress block.

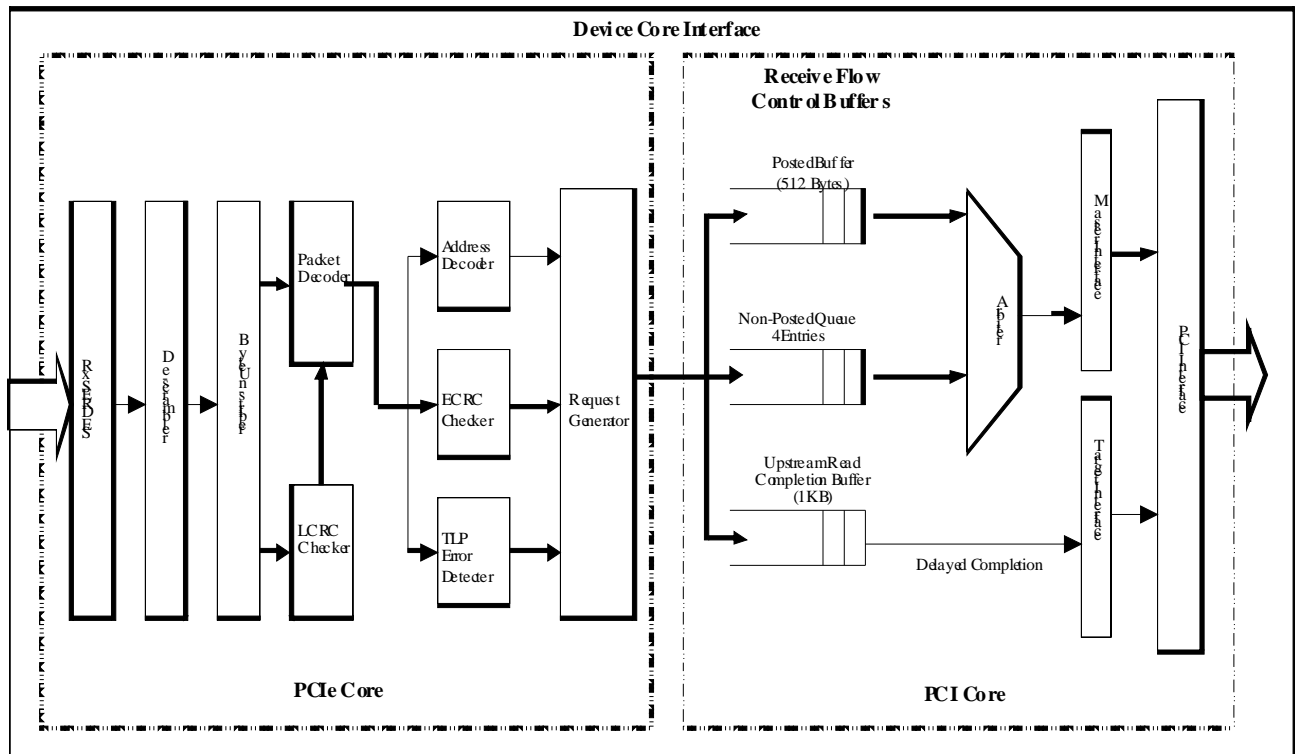
Figure 7: Upstream Data Path[update for PEB383]



### 3.1.2 Downstream Data Path

In the downstream path, the PEB383 uses one-stage buffering for each type of transaction (see Figure 8). These buffers support the store and forward method, receive flow control, protocol differences, synchronization, and error handling requirements.

Figure 8: Downstream Data Path



## 3.2 Transaction Management

The following sub-sections describe how the PEB383 handles upstream and downstream transactions.

### 3.2.1 Upstream Transaction Management

Transactions that originate on the PCI Interface that are destined for the PCIe Interface are stored in the respective queues or buffers in the PCI clock domain, and are then forwarded to the PCIe Core (see [Figure 7](#)). PCI buffer logic decomposes the received transactions as per the PCIe constraints (for example, MAX\_RD\_SIZE, MAX\_PAY\_SIZE, RCB, and 4-KB address boundary). Three sets of data and control signals for the three types of transactions (posted, non-posted, and completions) are used between the PCI and PCIe Cores.

Transactions are stored temporarily in the PCIe Core buffers before they are used to construct TLPs, and are then made visible to TLP arbiter. The TLPs are processed by the TLP arbiter only after ordering rules are satisfied. The TLP arbiter selects one of the five input TLPs (error message, PME message, posted, completion, and non-posted TLPs) in a round-robin mode if sufficient credits and retry buffer space is available for the specific TLPs. The TLP arbiter continues to check the available credit and retry buffer space against each of the active inputs, and selects the one that meets the constraint. The ECRC adder calculates and appends a 32-bit ECRC value to the end of the TLP selected by the arbiter if ECRC generation is enabled by software, and then forwards the TLP to the Data link layer.

The Data link layer applies a sequence number to the TLP received from transaction layer block, and then calculates and appends a 32-bit LCRC value to ensure integrity during the transmission across the physical lanes. A copy of the TLP sent to the physical layer is stored in the retry buffer for future replay if there is negative acknowledgement from the other end component. The Retry buffer replays the stored unacknowledged TLPs if it receives a NAK or replay timer expiration.

The Byte striper block of the physical layer unit appends start and end characters to the TLP received from Data link layer, and then multiplexes the bytes of the packet onto the lanes. These bytes on the lanes are scrambled using LFSR to eliminate repetitive bit patterns in the bit stream. The scrambled 8-bit characters are sent to the SerDes to convert to a 10-bit character in order to transmit it in a serial bit stream on the physical lanes.

### 3.2.2 Downstream Transaction Management

In the downstream path, the physical layer unit converts the incoming serial bit stream into a parallel symbol stream, de-scrambles the bytes in the transmit path, assembles packets, and then sends them to the Data link layer unit (see [Figure 8](#)).

The Data link layer unit checks for LCRC and sequence number errors for packets received from the physical layer unit. If there are no errors, LCRC and sequence number fields are stripped and resultant TLP is sent to Transaction layer unit.

The Transaction layer unit checks for ECRC errors and framing violations based on header fields and ECRC fields in the TLP received from the Data link layer unit. It extracts routing information based on the header fields and determines whether to forward or reject the TLP. The ECRC field is stripped and the resulting information in the TLP header, payload, and any detected error information, is sent to the PCI Core.

The PEB383 uses receive flow control buffers in the PCI Core instead of in the PCIe Core to store downstream requests or completions to be forwarded on the PCI Interface.

## 3.3 Buffer Structure

The following sub-sections describe the three PEB383 buffer structures:

- Upstream non-posted buffer
- Upstream posted buffer
- Downstream non-posted buffer
- Downstream posted buffer

### 3.3.1 Upstream Non-posted Buffer

There are four entries in the upstream read request queue. The 1-KB completion buffer is split up into 4 x 256-byte segments. When a read occurs on the PCI bus a read request is FIFO queued in one of the 4 entry non-posted request queue, if there is space. The PCI transaction is retried so that the master will return when the bridge has fetched the data. If there are unallocated completion buffers (equal or greater than the programed allocation size) a PCIe read request is sent upstream, requesting the programed allocation amount of data.

By default the programmed allocation amount of buffers that are allocated is equal to the prefetch size. In order to prevent one device from consuming all the buffers, the allocation size can be programmed to be less than the prefetch size. For example, if the prefetch size was set to 1 KB, then only one outstanding request would result, as once all the buffers are allocated no more requests can be sent. The allocation size can be programmed to be 512 bytes (or 256, 128) so that 1, 2, or 4 outstanding requests are possible (see MAX\_BUF\_ALOC bits in the “Upstream Posted Write Threshold Register”).

**Table 8: Completion Buffer Allocation**

Bit setting ---->	MAX_BUF_ALOC							
	0b11		0b10		0b01		0b11	
Prefetch	ALOC <sup>a</sup>	ORR <sup>b</sup>	ALOC	ORR	ALOC	ORR	ALOC	ORR
1024 bytes	1024	1	512	2	256	4	256	4
512 bytes	512	2	512	2	256	4	256	4
256 bytes	256	4	256	4	256	4	256	4
128 bytes	128	4	128	4	128	4	128	4

a. Completion buffer allocation in bytes.

b. Number of Outstanding Read Requests.

The requests are sent in order — small requests do not pass large requests — as completion buffers are unallocated. Otherwise, this would cause unfairness since smaller requests could block larger requests. The completions can occur out of order; that is, the bridge always responds with completion data if it is in the buffers. This is done to improve throughput when there are multiple outstanding read requests.

### 3.3.1.1 Non-posted Write Buffer

The PEB383 supports one non-posted write transaction. Similar to read requests, its request information is stored in one of the eight request queue entries, and its data is stored in a 32-bit register. Non-posted write requests are forwarded onto the PCIe Core in two PCIe clock cycles. Request information is forwarded in the first cycle, while 32-bit data is forwarded in the second cycle.

### 3.3.2 Upstream Posted Buffer

The upstream posted buffer is a FIFO of size 512 bytes that stores memory write transactions that originate on the PCI Interface and are destined to devices on PCIe Interface. The PEB383 completes the posted transactions on the originating bus before forwarding them to the PCIe Interface. Unlike the read buffers, the amount of space assigned to each transaction is dynamic. A single transaction can use 512 bytes of buffer space. The PEB383 translates all types of memory write transactions from the PCI Interface to memory write requests on the PCIe Interface. The PEB383 terminates a new transaction with retry and an active transaction with disconnect if sufficient buffer space is not available.

The PEB383 uses an 8-deep request FIFO to store the request information, including first and last Dwords byte enables of the received transactions.

Memory write transactions can contain any or all invalid payload bytes, where as memory write and invalidate (MWI) transactions carry all the valid payload bytes. The PEB383 decomposes the received transactions with non-contiguous byte enables on 32-byte boundaries while writing into the request FIFO.

The PCI Core makes a request to the PCIe Core if one of the following conditions is met:

- All data bytes of the transaction are received and are stored in the data buffer
- Received data bytes count exceeds the programmed threshold value (see UPST\_PWR\_THRES in “Upstream Posted Write Threshold Register”)
- Received data bytes count exceeds the PCIe maximum payload size (see MAX\_PAY\_SIZE in “PCIe Device Control and Status Register”)
- Address plus received data bytes count exceeds 4 KB
- Data with non-contiguous byte enables

### 3.3.3 Downstream Non-posted Buffer

The 512-byte, downstream non-posted buffer stores the data returned for the non-posted requests that originate on the PCIe Interface and are destined for PCI devices.

A single completion of up to 512-bytes can be stored here. A single outstanding read is issued to the PCI side.

### 3.3.4 Downstream Posted Buffer

The 512-byte downstream posted write buffer stores the payload of memory write transactions that originate on the PCIe Interface and are destined for PCI devices. The amount of space assigned to each transaction is dynamic.

The PEB383 uses an 8-deep request FIFO to store the request information, including the first and last Dwords byte enables. The PEB383 initiates a transaction on the PCI Interface only after a complete packet is stored in the buffer. The PEB383 attempts another outstanding transaction only if the current transaction is either successfully completed or terminated with either master or target abort.

## 3.4 Flow Control

The PEB383 handles packet-based protocol on its PCIe Interface, and transaction-based protocol on its PCI Interface. PCI requesters initiate transactions without prior knowledge on receiver buffer status. As a result, flow control is managed through retries and disconnects that can waste bus bandwidth. In comparison, PCIe requesters initiate requests while having prior knowledge on receiver buffer availability status, and therefore, eliminate the wasteful effects of unnecessary retries and disconnects.

The PEB383 does not issue retries or disconnects on the PCI Interface for completions returned for a downstream read request, but may issue retries or disconnects for a posted or non-posted transaction on the PCI Interface based on the buffer space availability.



The PEB383 uses flow control buffers in the PCI Core for three categories of downstream traffic. The amount of flow control buffer space availability is conveyed to the other end of the component using flow control credits. The PEB383 advertises infinite credits for completions as it ensures enough buffer space is available to store the returned completion data before initiating a read request. The PEB383 advertises initial flow control credits as follows. Each credit of data is 16 bytes.

**Table 9: Initial Credit Advertisement**

Credit Type	Initial Advertisement
Posted Header (PH)	0x08
Posted Data (PD)	0x020
Non-Posted Header (NPH)	0x04
Non-Posted Data (NPD)	0x01
Completion Header (CPLH)	0x00 (Infinite)
Completion Data (CPLD)	0x000 (Infinite)

## 3.5 Prefetching Algorithm

The PEB383 prefetches the data by default for the transaction that uses Memory Read Line or Memory Read Multiple command. The PEB383 does not prefetch the data by default for the transaction that uses the memory read command since the bridge does not know whether or not the transaction address falls in prefetchable region.

The prefetch algorithm is configured for various commands as follows:

- Memory read – Controlled by P\_MR, MRL\_66 and MRL\_33 of the “**Prefetch Control Register**”. The default value of these bits indicates that either one Dword in 32-bit bus mode or two Dwords in 64-bit bus mode is prefetched.
- Memory read line – Controlled by P\_MRL, MRL\_66 and MRL\_33 of the “**Prefetch Control Register**”. The default value of these bits indicates that either 128 bytes in 32-bit bus mode or 256 bytes in 64-bit bus mode is prefetched. The PEB383 prefetches one cacheline if P\_MRL is set to 0.
- Prefetch algorithm for memory read multiple command is controlled by P\_MRM, MRM\_66 and MRM\_33 of the “**Prefetch Control Register**”. The default value of these bits indicates that either 256 bytes in 32-bit bus mode or 384 bytes in 64-bit bus mode is prefetched. The PEB383 prefetches two cachelines if P\_MRM is set to 0.

## 3.6 Short Term Caching

This feature provides performance improvements in situations where upstream devices are not able to stream data continuously to meet the prefetching needs of the PEB383. As defined in the *PCI-to-PCI Bridge Specification (Revision 1.2)*, when the bus master completes a transaction, the bridge is required to discard the balance of any data that was prefetched for the master. To prevent performance impacts when dealing with devices between requester and completer that can only stream data of 128 to 512 bytes due to buffering constraints, the PEB383 uses “Short Term Caching.” This feature provides a time-limited read data cache in which the PEB383 will not discard prefetched read data after the request completes on the initiating bus.

To enable Short Term Caching, set the STC\_EN bit in the “**PCI Miscellaneous Control and Status Register**”. When enabled, the PEB383 does not discard the additional prefetched data when the read transaction completes on the initiating bus. The PEB383 then continues to prefetch data up to the amount specified in the “**Prefetch Control Register**”. If the initiator generates a new transaction that requests the previously prefetched data, the PEB383 returns that data.

The PEB383 discards data after some of the data for a request is returned to the initiator and one of the following conditions is met:

- Short-term discard timer is expired before the initiator has requested additional data (see “**Short-term Caching Period Register**”).
- An upstream posted transaction is received on the PCI Interface



Short-term caching should only be used in systems that can ensure the data provided to the master has not been modified since the initial transaction.

## 3.7 Polarity Inversion

The PEB383 supports polarity inversion. For information on how to use this feature, see the *PEB383 Board Design Guidelines*.

---

## 4. Addressing

Topics discussed include the following:

- “Overview”
- “Memory-mapped I/O Space”
- “Prefetchable Space”
- “I/O Space”
- “VGA Addressing”
- “ISA Addressing”
- “Non-transparent Addressing”
- “Legacy Mode”

---

### 4.1 Overview

This chapter discusses the various types of address decoding performed by the PEB383 when it forwards transactions upstream and downstream. The memory and I/O address ranges are defined using a set of base and limit registers in the bridge’s configuration header. The base and limit address registers define the address ranges that a bridge forwards downstream transactions. These registers are effectively inversely decoded to determine the address ranges on the PCI Interface for transactions that are forwarded upstream to the PCIe Interface.

### 4.2 Memory-mapped I/O Space

Memory transactions are forwarded across the PEB383 when their address falls within a window defined by one of the following registers:

- “PCI Memory Base and Limit Register”
- “PCI PFM Base and Limit Register”

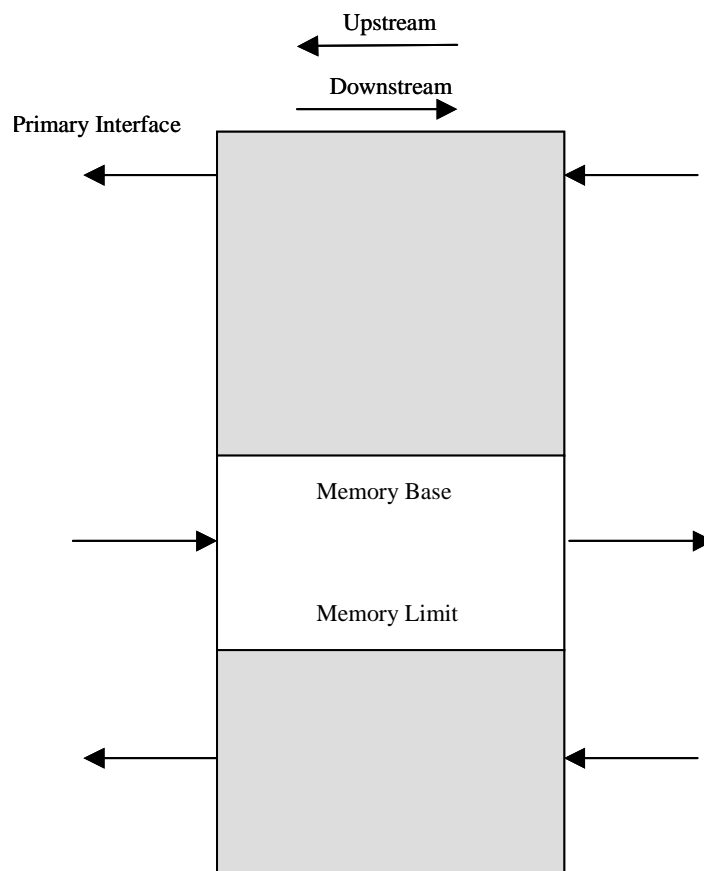
The memory-mapped I/O address spacing maps memory address ranges of devices that are not prefetchable. For PCI to PCIe reads, prefetching occurs in this space only if the Memory Read Line or Memory Read Multiple commands are issued on the PCI bus. When either of these commands is used, the quantity of data prefetched is determined by the prefetching algorithm defined in “[Prefetching Algorithm](#)”. For PCIe-to-PCI, the number of bytes to read is determined by the Memory Read Request TLP.

The response of the bridge to memory-mapped I/O transactions is controlled by the following:

- MS bit in “**PCI Control and Status Register**” – This bit must be set to allow memory transactions to be forwarded downstream. If not set, all memory transactions on the PCI bus are forwarded to the PCIe link. In addition, if not set, all memory requests on the PCIe Interface are completed with an Unsupported Request status.
- BM bit in “**PCI Control and Status Register**” – This bit must be set to allow memory transactions to be forwarded upstream. If this bit is not set, all memory transactions on the PCI bus are ignored.
- VGA\_EN bit in “**PCI Bridge Control and Interrupt Register**”

The PEB383 forwards memory transactions downstream from its PCIe Interface to its PCI Interface if a memory address is in the range defined by the Memory Base and Memory Limit registers (when the base is less than or equal to the limit), as shown in **Figure 9**. A memory transaction on the PCI Interface that is within this address range, however, is not be forwarded upstream to the PCIe Interface. Any memory transactions on the PCI Interface that are outside this address range are forwarded upstream to the PCIe Interface (provided they are not in the address range defined by the set of prefetchable memory address registers).

**Figure 9: Memory-mapped I/O Address Space**



The memory-mapped I/O address range that is defined by the Base and Limit registers are always aligned to a 1-MB boundary and has a size granularity of 1 MB.

## 4.3 Prefetchable Space

The prefetchable address space maps memory address ranges of devices that are prefetchable; that is, devices that do not have side-effects during reads. For PCI-to-PCIe reads, prefetching occurs in this space for all memory read commands (MemRd, MemRdLine, MemRdMult) issued on the PCI bus. For these Read commands, the PEB383 prefetches data according to prefetching algorithm defined in “[Prefetching Algorithm](#)”. For PCIe-to-PCI reads, the number of bytes to be read is determined by the Memory Read Request.

The Prefetchable Memory Base, Prefetchable Memory Limit, Prefetchable Base Upper 32 Bits, and Prefetchable Limit Upper 32 Bits registers in the bridge configuration header specify an address range that is used by the bridge to determine whether to forward PCIe and PCI memory read and memory write transactions across the bridge. The prefetchable memory address range defined by these registers is always aligned to a 1-MB boundary and has a size granularity of 1 MB. If the address specified by the Prefetchable Memory Base and Prefetchable Base Upper 32 Bits registers is set to a value higher than the address specified by the Prefetchable Memory Limit and Prefetchable Limit Upper 32 Bits registers, the address range is disabled.

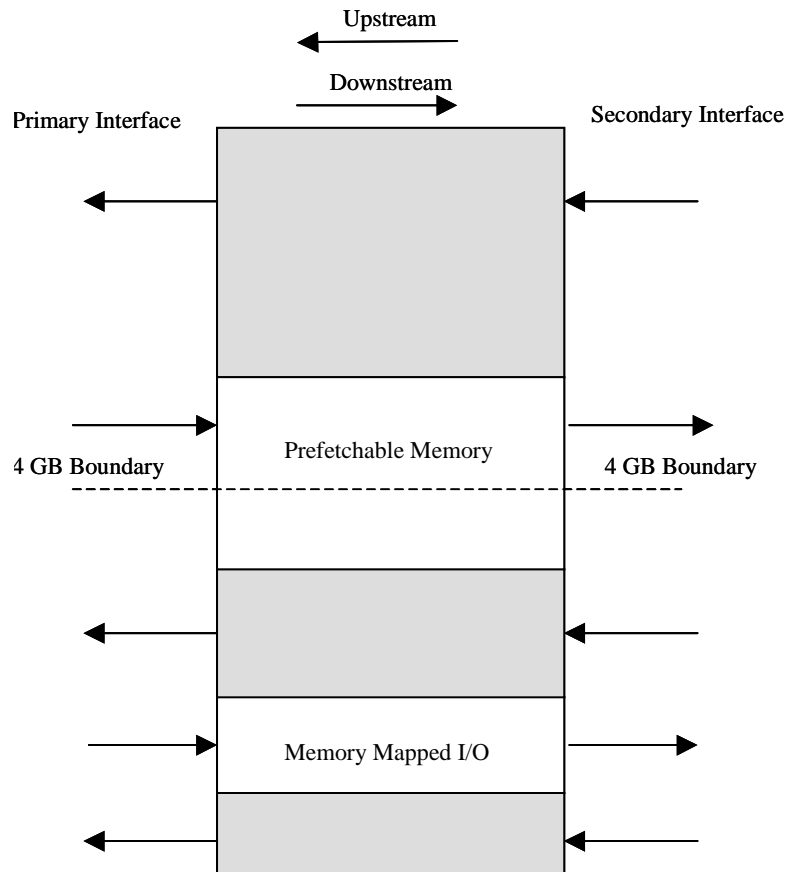
Following register bits effect the response by the bridge to memory transactions:

- Memory Enable bit in “[PCI Control and Status Register](#)”
- Bus Master Enable bit in “[PCI Control and Status Register](#)”
- VGA Enable bit in “[PCI Bridge Control and Interrupt Register](#)”

The PEB383 forwards memory transactions downstream from its PCIe Interface to its PCI Interface if a memory address is in the range defined by the Prefetchable Memory Base and Prefetchable Memory Limit registers. Conversely, a memory transaction on the PCI Interface that is within this address range is not be forwarded upstream to the PCIe Interface. Any memory transactions on the PCI Interface that are outside this address range are forwarded upstream to the PCIe Interface (provided they are not in the address range defined by the memory-mapped I/O address range registers).

If the Prefetchable Memory Base is programmed to have a value greater than the Prefetchable Memory Limit, then the prefetchable memory range is disabled. In this case, all memory transaction forwarding is determined by the memory-mapped I/O base and limit registers. Note that all four prefetchable base and limit registers must be considered when disabling the prefetchable range.

Unlike non-prefetchable memory-mapped I/O memory, Prefetchable memory can be located below, above, or span across the first 4-GB address boundary. [Figure 10](#) illustrates a prefetchable memory window that spans across the 4-GB address boundary. Memory locations above 4 GB are accessed using 64-bit addressing. PCIe memory transactions that use the Short Address (32-bit) format can target a non-prefetchable memory window or the portion of a prefetchable memory window that is below the first 4-GB address boundary. Memory transactions that use the Long Address (64-bit) format can target the portion of a prefetchable memory window that is at or above the first 4-GB address boundary.

**Figure 10: 64-bit Prefetchable Memory Address Range**

## 4.4 I/O Space

I/O Base, I/O Limit, I/O Base Upper 16 Bits, and I/O Limit Upper 16 Bits registers in the PEB383 configuration header specify an address range that is used by the bridge to determine whether to forward I/O read and I/O write transactions across the bridge. If the address specified by the I/O Base and I/O Base Upper 16 Bits registers is set to a value greater than the address specified by the I/O Limit and I/O Limit Upper 16 Bits registers, the address range is disabled.

The response of the bridge to I/O transactions is controlled by the following configuration register bits:

- I/O Space Enable bit in “PCI Control and Status Register”
- Bus Master Enable bit in “PCI Control and Status Register”
- ISA Enable bit in “PCI Bridge Control and Interrupt Register”
- VGA Enable bit in “PCI Bridge Control and Interrupt Register”

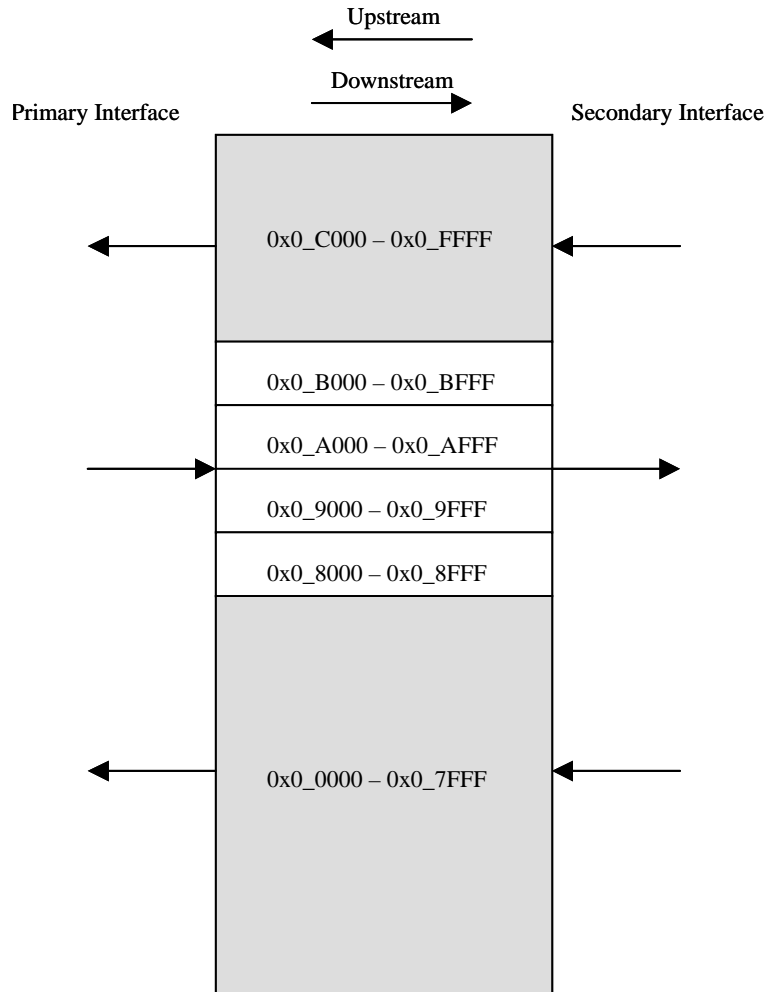
The I/O Enable bit must be set for any I/O transaction to be forwarded downstream. If this bit is not set, all I/O transactions on the PCI bus are forwarded to the PCIe link. If this bit is not set, all PCIe Interface I/O requests are completed with Unsupported Request status.

---

The Bus Master Enable bit must be set for any I/O transaction to be forwarded upstream. If this bit is not set, all I/O transactions on the PCI bus are ignored.

If ISA Enable bit is set, the bridge does not forward any I/O transactions downstream that are in the top 768 bytes of each 1-KB block within the first 64 KB of address space. Only transactions in the bottom 256 bytes of each 1-KB block are forwarded downstream. If the ISA Enable bit is clear, then all addresses within the range defined by the I/O base and limit registers are forwarded downstream. I/O transactions with addresses above 64 KB are forwarded according to the range defined by the I/O base and limit registers. If the ISA Enable bit is set, the bridge forwards upstream any I/O transactions on the PCI bus that are in the top 768 bytes of each 1-KB block within the first 64 KB of address space, even if the address is within the I/O base and limit. All other transactions on the PCI bus are forwarded upstream if they fall outside the range defined by the I/O base and limit registers. If the ISA Enable bit is clear, then all PCI bus I/O addresses outside the range defined by the I/O base and limit registers are forwarded upstream.

A bridge uses the I/O Base and I/O Limit registers to determine whether to forward I/O transactions across the bridge, as shown in [Figure 11](#). The I/O address range defined by these registers is always aligned to a 4-KB boundary and has a size granularity of 4 KB. A bridge forwards I/O read and I/O write transactions from its PCIe Interface to its PCI Interface if the address is in the range defined by the I/O base and I/O limit registers (when the base is less than or equal to the limit). Conversely, I/O transactions on the PCI bus in the address range defined by these registers are not forwarded upstream by the bridge. I/O transactions on the PCI bus that are outside the defined address range are forwarded upstream.

**Figure 11: I/O Address Space**

## 4.5 VGA Addressing

The PEB383 supports VGA addressing. The VGA\_EN bit in the “**PCI Bridge Control and Interrupt Register**” controls the response by the bridge to both VGA frame buffer addresses and to VGA register addresses. If the VGA Enable bit is set, the bridge decodes and forwards memory accesses to VGA frame buffer addresses and I/O accesses to VGA registers from the PCIe Interface to the PCI Interface (and block forwarding from PCI to PCIe of these same accesses).

The VGA\_16BIT\_EN bit in the “**PCI Bridge Control and Interrupt Register**” selects between 10-bit and 16-bit VGA I/O address decoding, and is applicable when the VGA Enable bit is 1.

VGA memory addresses are 0x0A\_0000 through 0x0B\_FFFF



VGA I/O Addresses (Address bits 15:10 are not decoded when the VGA 16-Bit Decode bit is 0b) are:

- Address bits 9:0 = 0x3B0 through 0x3BB and 0x3C0 through 0x3DF (VGA 16-Bit Decode bit is 0b)
- Address bits 15:0 = 0x03B0 through 0x03BB and 0x03C0 through 0x03DF (VGA 16-bit Decode bit is 1b)

The VGA Palette Snoop Enable bit is implemented as read-only with a value of zero.

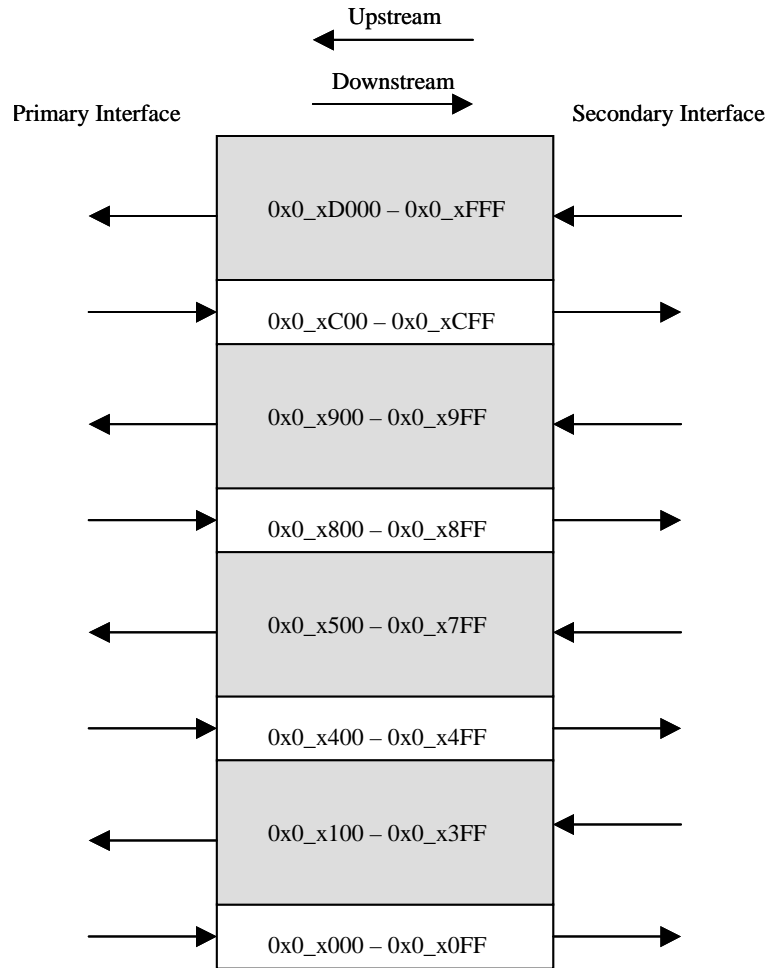
## 4.6 ISA Addressing

The PEB383 supports ISA addressing through ISA Enable bit in the “**PCI Bridge Control and Interrupt Register**”. The ISA Enable affects only I/O addresses that are in the bridge’s I/O range (as defined by the I/O Base, I/O Base Upper 16 Bits, I/O Limit, and I/O Limit Upper 16 Bits) and in the first 64 KB of PCI I/O Space (0000 0000h to 0000 FFFFh). If this bit is set and the I/O address meets the stated constraints, the PEB383 blocks the forwarding of I/O transactions downstream if the I/O address is in the top 768 bytes of each naturally aligned 1-KB block. If the ISA Enable bit is clear, the PEB383 forwards downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers.

If the ISA Enable bit is set, I/O transactions on the PCI bus in the top 768 bytes of any 1-KB address block within the first 64 KB of PCI I/O space is forwarded upstream, even if the address is between the I/O base and I/O limit addresses. **Figure 12** illustrates this mapping for a 4-KB range.

The ISA Enable bit only affects the I/O address decoding behavior of the bridge. It does not affect the bridge's prefetching, posting, ordering, or error handling behavior.

**Figure 12: ISA Mode I/O Addressing**



## 4.7 Non-transparent Addressing

At power-up, the host processor discovers the need for non-transparent bridging and enables the address remapping of prefetchable, non-prefetchable, and I/O ranges through configuration. Before enabling address remapping of the base and limit values, the remapped address ranges need to be programmed. The “**Downstream Non-transparent Address Remapping Registers**” allow downstream accesses to be mapped to arbitrary positions in PCI memory space. While the Memory Base and Limit registers always define the range of addresses to be claimed on the PCIe link and forwarded to the PCI bus, cycles that are claimed have their addresses modified because of the difference in the base addresses of the windows on the two buses.

### 4.7.1 PCIe to PCI Non-prefetchable Address Remapping

Downstream transactions that fall within the address window defined by the “**PCI Memory Base and Limit Register**” are remapped according to the address window defined by the “**Secondary Bus Non-prefetchable Address Remap Control Register**” and “**Secondary Bus Non-prefetchable Upper Base Address Remap Register**”. The following equations describe the address remapping process:

- $PriSecNPDiff = PriNPBase - SecNPBase$ , where
  - **PriSecNPDiff**: Defines the difference between the Primary Non-prefetchable Base and the Secondary Non-prefetchable Base.
  - **PriNPBase**: Defined in the previous paragraph.
  - **SecNPBase**: Defined by “**Secondary Bus Non-prefetchable Address Remap Control Register**” and “**Secondary Bus Non-prefetchable Upper Base Address Remap Register**”.
- $SecNPAddr = PriNPAddr - PriSecNPDiff$ , where
  - **SecNPAddr**: Defines the remapped address that the PEB383 presents on the PCI bus.
  - **PriNPAddr**: Defines the address presented to the PEB383 that falls within the registers described in the previous paragraph.
  - **PriSecNPDiff**: See previous bullet.

### 4.7.2 PCIe to PCI Prefetchable Address Remapping

Downstream transactions that fall within the address window defined by the “**PCI PFM Base and Limit Register**”, “**PCI PFM Base Upper 32 Address Register**”, and “**PCI PFM Limit Upper 32 Address Register**” are remapped according to the address window defined by the “**Secondary Bus Prefetchable Address Remap Control Register**” and “**Secondary Bus Prefetchable Upper Base Address Remap Register**”. The following equations describe the address remapping process:

- $PriSecPFDiff = PriPFBase - SecPFBase$ , where
  - **PriSecPFDiff**: Defines the difference between the Primary Prefetchable Base and the Secondary Prefetchable Base.
  - **PriPFBase**: Defined by the registers listed above.
  - **SecPFBase**: Defined by “**Secondary Bus Prefetchable Address Remap Control Register**” and “**Secondary Bus Prefetchable Upper Base Address Remap Register**”.

- $\text{SecPFAddr} = \text{PriPFAddr} - \text{PriSecPFDiff}$ , where
  - **SecPFAddr**: Defines the remapped address the PEB383 presents on PCI bus.
  - **PriPFAddr**: Defines the address presented to the PEB383 that falls within the registers described in the previous paragraph.
  - **PriSecPFDiff**: See previous bullet.

### 4.7.3 PCI to PCIe Address Remapping

Because the addresses of the downstream memory windows on the PCI bus have been shifted from their locations on the PCIe link, the address range of cycles that a bridge will not claim on the PCI bus must also be shifted. Therefore, memory cycles with addresses from SecNPBase (see “**Secondary Bus Non-prefetchable Address Remap Control Register**” and “**Secondary Bus Non-prefetchable Upper Base Address Remap Register**”) to SecNPLimit or from SecFPBase (see “**Secondary Bus Prefetchable Address Remap Control Register**” and “**Secondary Bus Prefetchable Upper Base Address Remap Register**”) to SecFPLimit will not be claimed by the bridge on the PCI bus.

The Secondary Bus Non-prefetchable Limit is described in the following equation:

- $\text{SecNPLimit} = \text{PriNPLimit} - \text{PriSecNPDiff}$ , where
  - **PriNPLimit**: Defined by “**PCI Memory Base and Limit Register**” and the additional “**Primary Bus Non-prefetchable Upper Limit Remap Register**”.
  - **PriSecNPDiff**: Defines the difference between the Primary Non-prefetchable Base and the Secondary Non-prefetchable Base.

The Secondary Prefetchable Limit is described in the following equation:

- $\text{SecPFLimit} = \text{PriPFLimit} - \text{PriSecPFDiff}$ , where
  - **PriPFLimit**: Defined by “**PCI PFM Base and Limit Register**” and “**PCI PFM Base Upper 32 Address Register**”.
  - **PriSecPFDiff**: Defines the difference between the Primary Prefetchable Base and the Secondary Prefetchable Base.

Once the address is claimed as defined above, a memory cycle is forwarded from the PCI bus to the PCIe link with its address modified according to the Non-transparent Address (NTMA) remapping windows (see offsets 0x68 to 0x7C):

- NTMA window remapping

The NTMA Secondary Base (see “[NTMA Secondary Lower Base Register](#)” and “[NTMA Secondary Upper Base Register](#)”) and NTMA Secondary Limit (see “[NTMA Secondary Lower Limit Register](#)” and “[NTMA Secondary Upper Limit Register](#)”) define memory windows in the PCI bus memory space that are mapped to arbitrary positions on the PCIe link. The resulting location of the NTMA window on the PCIe link is defined by the following equations:

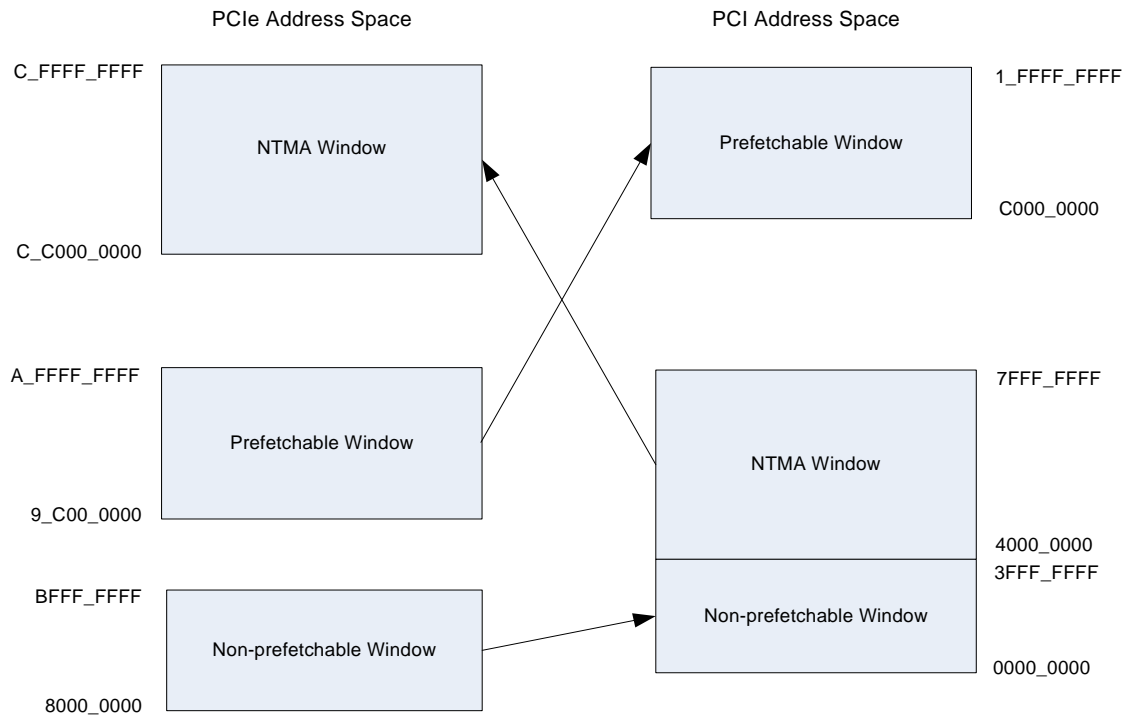
- $\text{PriSecNTMADiff} = \text{PriNTMABase} - \text{SecNTMABase}$ , where
  - **PriNTMABase**: Defined by “[NTMA Control Register](#)” and “[NTMA Primary Upper Base Register](#)”.
  - **SecNTMABase**: Defined by “[NTMA Secondary Lower Base Register](#)” and “[NTMA Secondary Upper Base Register](#)”.
- $\text{PriNTMALimit} = \text{SecNTMALimit} + \text{PriSecNTMADiff}$ , where
  - **SecNTMALimit**: Defined by “[NTMA Secondary Lower Limit Register](#)” and “[NTMA Secondary Upper Limit Register](#)”.
  - **PriSecNTMADiff**: See previous bullet.

A memory cycle whose address falls within a NTMA window on the PCI bus will have its address on the PCIe link modified by the following equation:

- $\text{PriNTMAAddr} = \text{SecNTMAAddr} + \text{PriSecNTMADiff}$ , where
  - **SecNTMAAddr**: Secondary NTMA Address, which must fall within the window defined by the NTMA Secondary Base and Limit registers.
  - **PriSecNTMADiff**: See previous bullet.

Transactions that are claimed on PCI Interface, and which are outside the NTMA window, are forwarded upstream without address remapping. Software should ensure that the location of the NTMA window on the PCI bus is outside of the PCI bus memory windows, and that the NTMA window on the PCIe link is outside of the PCIe link memory windows, or undefined operation may result. [Figure 13](#) displays an example of memory window remapping.

**Figure 13: Memory Window Remapping Example**



***I/O Address Remapping***

The “**PCI I/O Address Upper 16 Register**” in the PEB383 configuration space indicates the number of upper bits of the I/O address that are not used when forwarding downstream I/O space cycles to the PCI bus. This allows I/O addresses to be translated down into the address range that is available on the PCI bus. There is no enable bit for I/O address remapping; any non-zero value in this register remaps the I/O transactions to a different address location, as described in this section.

## 4.8 Legacy Mode

When the PEB383 is in Legacy mode it supports subtractive decode. This is a non-standard feature that is enabled through the LEGACY bit in the “**PCI Miscellaneous Clock Straps Register**”.

When the PEB383 is in legacy mode, all MWr, MRd, IOWr, and IORd transactions received on the upstream port (PCIe) that do not decode to an internal address are forwarded to the PCI Interface. When the device is not in legacy mode, TLPs that do not fall between the base and limit registers are handled as Unsupported Requests (UR).

When the LEGACY bit is set, the PROG field of “**PCI Class Register**” is changed to 0x1, indicating to software that a subtractive bridge is present.

When the LEGACY bit is set all PCIe capabilities are hidden from software, and the following occurs:

1. Next pointer in “**PCI Power Management Capability Register**” is set to 0, indicating it is the last capability
2. “**PCIe Capability Registers**” are treated as reserved
3. “**Advanced Error Reporting Capability Registers**” are treated as reserved
4. Extended configuration registers are treated as reserved



When the PEB383 is configured in Legacy mode, the PCIe root port must also be configured to support subtractive decode.





## 5. Configuration Transactions

Topics discussed include the following:

- “Overview”
- “Configuration Transactions”
- “PCIe Enhanced Configuration Mechanism”
- “Configuration Retry Mechanisms”

### 5.1 Overview

Each device in a PCIe or PCI system has a configuration space that is accessed using configuration transactions in order to define its operational characteristics. This chapter describes how the PEB383 handles PCIe configuration requests.

### 5.2 Configuration Transactions

There are two types of configuration transactions: Type 0 and Type 1. Type 0 configuration transactions access the PEB383’s internal configuration registers, while Type 1 configuration transactions access devices that reside downstream of the PEB383. Type 1 transactions are converted to Type 0 transactions if they target devices that reside on the downstream PEB383 bus. If the transaction is intended for a device that is downstream of the bus directly below the PEB383, the transaction is passed through the PEB383 as a Type 1 configuration transaction. If the transaction is not targeted for the PEB383 or any device below the PEB383, the transaction is rejected. Configuration transactions are only initiated by the Root Complex in PCIe-based systems.

Configuration address formats are as follows.

**Figure 14: PCIe Configuration Address Format**

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	Reserved	Extended Register Address	Register Address	Reserved

**Figure 15: PCI Type 0 Configuration Address Format**

31	16	15	11	10	8	7	2	1	0
Unique Address (AD[31:16]) corresponding to a particular Device Number)		Reserved		Function Number		Register Number		00	

**Figure 16: PCI Type 1 Configuration Address Format**

31	24	23	16	15	11	10	8	7	2	1	0
Reserved		Bus Number		Device Number		Function Number		Register Number		01	

### 5.2.1 Type 0 Configuration Transactions

The PEB383 responds to PCIe Type 0 configuration transactions that address its configuration space. This type of transaction configures the PEB383 and is not forwarded downstream. The PEB383 ignores Type 0 configuration transactions that originate on the PCI Interface. If a Type 0 configuration cannot be processed, the PEB383 handles it as an Unsupported Request.

### 5.2.2 Type 1 Configuration Transactions

PCIe Type 1 configuration transactions are used for device configuration in a hierarchical bus system. The Bus Number field contained in the header of a Type 1 configuration transaction specifies a unique PCI bus in the PCI bus hierarchy. The PEB383 compares the specified Bus Number with two register fields — Secondary Bus Number and Subordinate Bus Number in “**PCI Bus Number Register**” — that are programmed by system software or firmware to determine whether or not to forward a Type 1 configuration transactions across the bridge.

If a Type 1 configuration transaction is received on the PCIe Interface, the following sequence of tests is completed on the Bus Number field to determine how the PEB383 should handle the transaction:

1. If the Bus Number field is equal to the Secondary Bus Number value and the conditions for converting the transaction into a Special Cycle transaction are met, the PEB383 forwards the configuration request to its PCI Interface as a Special Cycle transaction. If the conditions are not met, the PEB383 forwards the configuration request to the PCI Interface as a Type 0 configuration transaction.
2. If the Bus Number field is not equal to the Secondary Bus Number value but is in the range of the Secondary Bus Number and the Subordinate Bus Number (inclusive) values, the Type 1 configuration request is specifying a Bus Number that is located behind the bridge. In this case, the PEB383 forwards the configuration request to the PCI Interface as a Type 1 configuration transaction.
3. If the Bus Number field does not satisfy the tests 1 and 2, the Type 1 configuration request indicates a Bus Number that is not located behind the bridge. In this case, the configuration request is invalid and PEB383 handles this as an Unsupported Request.

### 5.2.3 Type 1 to Type 0 Conversion

If a PCIe Type 1 configuration transaction's Bus Number field is equal to the Secondary Bus Number value, and the conditions for conversion to a Special Cycle transaction are not met, the PEB383 forwards the transaction to the PCI bus as a Type 0 configuration transaction. In this case, a device connected to the PCI Interface of the bridge is the target of the Type 0 configuration transaction.

To translate and convert a PCIe Type 1 configuration transaction to a PCI Type 0 configuration transaction, the PEB383 does the following:

- Sets address bits PCI\_AD[1:0] as 0b00
- Sets address bits PCI\_AD[7:2] the same as the PCIe transaction's Register Address field
- Sets address bits PCI\_AD[10:8] the same as PCIe transaction's Function Number field
- For a Secondary bus operating in PCI mode, it drives value 0b0000 on address PCI\_AD[15:11]
- For a Secondary bus operating in PCI, the PEB383 checks if the received Extended Register Address field is zero. If this field is non-zero, the PEB383 does not forward the transaction and treats it as an Unsupported Request on PCIe and a received Master-Abort on the destination bus. If the field is zero, the PEB383 decodes the PCIe Device Number field and asserts a single address bit in the range PCI\_AD[31:16] during the address phase (for device numbers in the range 0b0\_0000 to 0b0\_1111b).

### 5.2.4 Type 1 to Type 1 Forwarding

If a PCIe Type 1 configuration transaction is received and the value specified by the Bus Number field is within the range of bus numbers between the Secondary Bus Number (exclusive) and the Subordinate Bus Number (inclusive), the PEB383 forwards the transaction to its PCI Interface as a Type 1 configuration transaction. In this case, the target of the transaction does not reside on the PCI Interface but is located on a bus segment further downstream.

To translate the forwarded transaction from a PCIe Type 1 configuration request to a PCI Type 1 configuration transaction, the PEB383 does the following:

- Sets address bits PCL\_AD[1:0] as 0b01
- PCI Register Number, Function Number, Device Number, and Bus Number (address bits PCL\_AD[23:2]) are generated directly – that is, unmodified – from the PCIe configuration transaction’s Register Address, Function Number, Device Number, and Bus Number fields, respectively.
- Checks if the received Extended Register Address field is zero. If this field is non-zero, the PEB383 does not forward the transaction and treats it as an Unsupported Request on PCIe and a received Master-Abort on the destination bus. If the field is zero, the PEB383 generates PCL\_AD[27:24] as 0b0000.

### 5.2.5 Type 1 to Special Cycle Forwarding

When the PEB383 receives a PCIe Type 1 configuration write request transaction, it converts it to a Special Cycle on its PCI Interface when the following conditions are met by the transaction:

- The Bus Number field matches the Secondary Bus Number register value
- The Device Number field is all ones (equals 0b1\_1111)
- The Function Number field is all ones (equals 0b111)
- The Register Address and Extended Register Address are both all zeros (equal 0b00\_0000 and 0b0000, respectively).

## 5.3 PCIe Enhanced Configuration Mechanism

The PCIe Enhanced Configuration Mechanism adds four additional bits to the Register Address field, thereby expanding the space to 4096 bytes. The PEB383 forwards configuration transactions only when the Extended Register Address bits are all zero. This prevents address aliasing on the PCI bus that does not support Extended Register Addressing. If a configuration transaction targets the PCI bus and has a non-zero value in the Extended Register Address field, the PEB383 handles the transaction as if it received a Master-Abort on the PCI bus and then does the following:

- Sets the appropriate status bits for the destination bus, as if the transaction had executed and resulted in a Master-Abort
- Generates a PCIe completion with Unsupported Request status

## 5.4 Configuration Retry Mechanisms

A PCIe-to-PCI bridge is required to return a completion for all configuration requests that cross the bridge from PCIe to PCI prior to expiration of the Completion Timeout timer in the Root Complex. This requires that bridges take ownership of all configuration requests forwarded across the bridge. If the configuration request to PCI completes successfully prior to the bridge's timer expiration, the bridge returns a completion with Normal Status on PCIe for that request. If the configuration request to PCI encounters an error condition prior to the bridge's timer expiration, the bridge returns an appropriate error completion on PCIe. If the configuration request to PCI does not complete either successfully or with an error, prior to timer expiration, the bridge is required to return a completion with Configuration Retry Status (CRS) on PCIe for that request.

After the PEB383 returns a completion with CRS on PCIe, it continues to keep the configuration transaction active on the PCI bus. For PCI, the PEB383 keeps retrying the transaction until it completes on the PCI bus. When the configuration transaction completes on the PCI bus after the return of a completion with CRS on PCIe, the PEB383 discards the completion information. Bridges that use this option are also required to implement Bridge Configuration Retry Enable in the "PCIe Device Control and Status Register". If this bit is cleared, the bridge does not return a completion with CRS on behalf of configuration requests forwarded across the bridge. The lack of a completion results in eventual Completion Timeout at the Root Complex.



---

## 6. Bridging

Topics discussed include the following:

- “Overview”
- “Flow Control Advertisements”
- “Buffer Size and Management”
- “Assignment of Requestor ID and Tag”
- “Forwarding of PCIe to PCI”
- “Forwarding of PCI to PCIe”
- “PCI Transaction Support”
- “PCIe Transaction Support”
- “Message Transactions”
- “Transaction Ordering”
- “Exclusive Access”

---

### 6.1 Overview

The PEB383 provides a connection path between a PCI bus and a PCIe link. The main function of the PEB383 is to allow transactions between a master or a transmitter on one bus/link, and a target or a receiver on the other bus/link. The PCI Interface can operate in 32-bit PCI mode up to 66 MHz. Transactions flow through the PEB383 can be classified as follows:

- PCIe-to-PCI
- PCI-to-PCIe

### 6.2 Flow Control Advertisements

The flow control method on the PCI Interface is managed through retries or disconnects, where as on the PCIe link it is managed using flow control credits.

On the PCI Interface, the PEB383 issues retries to new request transactions and issues a disconnect for the active transaction if the internal request queues or data storage buffers are full or approaching full.

On PCIe Interface, the PEB383 periodically conveys its available buffer space to the other end component in terms of flow control credits using flow control packets. The PEB383 advertises flow control credits as per PCIe protocol requirements.

## 6.3 Buffer Size and Management

The PEB383 provides sufficient buffering to satisfy PCIe bridging requirements. The PEB383 does not overcommit its buffers: it forwards requests onto the other side only when enough buffer space is reserved to handle the returned completions.

The PEB383 uses 1-KB retry buffering, which is large enough to ensure that under normal operating conditions upstream traffic is never throttled. Ack latency value, internal processing delays, and receiver L0s exit latency values, are considered for determining the Retry buffer size.

## 6.4 Assignment of Requestor ID and Tag

The PEB383 assigns a unique transaction ID for all the non-posted requests forwarded to upstream devices. The PEB383 takes ownership of the upstream transactions on behalf of original requestors, and stores the transaction-related state information needed to return the completions to the original requestors. The action of replacing the original transaction's requester ID and/or Tag fields with the bridge's own assigned values is referred to as taking ownership of the transaction.

For upstream non-posted requests, the PEB383 assigns the PCIe requester ID using its secondary bus number and sets both the device number and function number fields to zero. For the upstream transactions, the PEB383 sets the Tag field to a request enqueued entry number.

## 6.5 Forwarding of PCIe to PCI

The PEB383 forwards posted, non-posted, and upstream read completions to the PCI devices, and stores the non-posted TLPs' state information to return the completion TLPs to the PCIe Interface.

### 6.5.1 PCIe Memory Write Request

The PEB383 forwards the received PCIe Memory Write Requests to the PCI Interface with either Memory Write (MW) or Memory Write and Invalidate (MWI) command. The PEB383 translates the request into a PCI transaction using the MWI command if it meets the MWI command rules specified in the *PCI Local Bus Specification (Revision 3.0)*, and the MWI bit is set in the **“PCI Control and Status Register”**. An MW command is used for the remaining part of the MWI transaction if the transaction is disconnected such that the remaining request does not meet the MWI command rules. The PEB383 does not support relaxed ordering among the received requests. It forwards all requests in the order they are received even if the relaxed ordering bit is set for some of the requests.

### 6.5.2 PCIe Non-posted Requests

The PEB383 translates the PCIe Memory Read Requests into PCI transactions that use a PCI memory read command (that is, Memory Read, Memory Read Line, or Memory Read Multiple) based on its cacheline size value, requested byte enables, and prefetchable and non-prefetchable memory windows. PCIe Read Request command translation is completed as follows:

- Memory Read if the PCIe Request falls into the non-prefetchable address range defined by the **“PCI Memory Base and Limit Register”**.



- Memory Read Line if the PCIe Request falls into the prefetchable range defined by the “**PCI PFM Base and Limit Register**”, and the requested data size is less than or equal to the value specified in Cacheline Size of the “**PCI Miscellaneous 0 Register**”.
- Memory Read Multiple if the PCIe Request falls into the prefetchable range defined by the “**PCI PFM Base and Limit Register**”, and the requested the data size is greater than or equal to the value specified in Cacheline Size of the “**PCI Miscellaneous 0 Register**”.

The PEB383 supports a single outstanding request. It does not attempt to read beyond the requested length. The PEB383 decomposes the requests if the requested data length is greater than 128 bytes, and returns the completions in 128-byte boundary fragments.

The PEB383 uses PCI byte enable fields such that the byte enable information is preserved and no additional bytes are requested for the transactions that fall into the non-prefetchable address range (for example, Configuration, I/O, and Memory read commands).

## 6.6 Forwarding of PCI to PCIe

The PEB383 forwards posted and non-posted requests and downstream read completions to PCIe devices, and stores the non-posted requests’ state information to return the delayed completions to the requester.

### 6.6.1 PCI Memory Write Request

The PEB383 translates the received Memory Write (MW) and Memory Write and Invalidate (MWI) transactions into PCIe Memory Write Requests. The PEB383 uses a 512-byte posted buffer to post the received transactions. Write requests are fragmented if one of the following PCIe constraints is met:

- Address plus length crosses the 4-KB boundary
- Burst writes with discontinuous byte enables
- Payload size exceeds MAX\_PAY\_SIZE in “**PCIe Device Control and Status Register**”

The PEB383 terminates a posted transaction with retry only if the buffers are filled with previously received memory requests, or if the bridge is locked from the PCIe side (see “**Locked Transaction**”). For more information on locked accesses, see “**Exclusive Access**”.

## 6.6.2 PCI Non-posted Requests

The PEB383 processes all non-posted transactions as delayed transactions. The PEB383 first terminates the received non-posted transaction with retry and then forwards it onto the PCIe Interface. The PEB383 stores the request-related state information while forwarding the request onto the PCIe Interface. This information tracks the requests repeated by the master and returned completions for the request. Since PCI read requests do not specify the amount of data to be read, the PEB383 uses a programmable prefetch algorithm to determine the amount of data to be read on behalf of the original requester. The PEB383 does not attempt to prefetch past the 4-KB address boundary on behalf of the original requester. The PEB383 stores the returned completion until the PCI requester repeats the initial request and terminates the delayed transaction. If short-term caching is enabled (see STC\_EN in “**PCI Miscellaneous Control and Status Register**”), the PEB383 responds to subsequent requests with the incremental addresses issued by the master until the programmed number of data bytes are transferred to the master or the short-term discard timer is expired (see ST\_DIST\_EN in “**SERRDIS\_OPQEN\_DTC Register**”).

The PEB383 enqueues up to four requests and issues the initial requests on the PCIe Interface in the order they were received; however, the ordering is not guaranteed for the subsequent requests of decomposed transactions.

The PEB383 discards the enqueued delayed request if the requested data is not returned before the completion timeout is expired (see “**Completion Timeout Register**”), and returns a delayed completion with target abort to the requester (see DISCARD2 in “**PCI Bridge Control and Interrupt Register**”). A delayed completion is discarded if the requester does not repeat the initial request or if the requester disconnects the delayed completion after few data bytes are transferred.

## 6.7 PCI Transaction Support

The following table lists the transactions supported by the PCI Interface.

**Table 10: PCI Transaction Support**

Cmd	Transaction <sup>a</sup>	PCI Interface	
		As a Master	As a Target
0000b	Interrupt Acknowledge	NA	NA
0001b	Special Cycle	Yes	NA
0010b	I/O Read	Yes	Yes
0011b	I/O Write	Yes	Yes
0100b	Rsvd	NA	NA
0101b	Rsvd	NA	NA
0110b	Memory Read	Yes	Yes
0111b	Memory Write	Yes	Yes
1000b	Rsvd	NA	NA
1001b	Rsvd	NA	NA
1010b	Configuration Read	Yes	NA
1011b	Configuration Write	Yes	NA
1100b	Memory Read Multiple	Yes	Yes
1101b	Dual Address Cycle	Yes	Yes
1110b	Memory Read Line	Yes	Yes
1111b	Memory Write and Invalidate	Yes	Yes

a. For unsupported transactions, see [“PCIe as Originating Interface”](#).

## 6.8 PCIe Transaction Support

The following table lists the transactions supported by the PCIe Interface.

**Table 11: PCIe Transaction Support**

TLP Type	Transaction <sup>a</sup>	PCIe Interface	
		As a Transmitter	As a Receiver
MRd	Memory Read Request	Yes	Yes
MRdLk	Memory Read Request Locked	NA	Yes
MWr	Memory Write Request	Yes	Yes
IORd	I/O Read Request	Yes	Yes
IOWr	I/O Write Request	Yes	Yes
CfgRd0	Configuration Read Type 0	NA	Yes
CfgWr0	Configuration Write Type 0	NA	Yes
CfgRd1	Configuration Read Type 1	NA	Yes
CfgWr1	Configuration Write Type 1	NA	Yes
Msg	Message Request	Yes	Yes
MsgD	Message Request with Data Payload	NA	Yes
MsgD (Vendor Defined)	Vendor-Defined Message Request With Data Payload	No	No
Cpl	Completion without Data	Yes	Yes
CplD	Completion with Data	Yes	Yes
CplLk	Completion without Data for MRR- Locked	Yes	NA
CplDLk	Completion with Data for MRR - Locked	Yes	NA

a. For unsupported transactions, see [“PCIe as Originating Interface”](#).

## 6.9 Message Transactions

Message transactions are used for in-band communication of events, and therefore, eliminate the need for sideband signals. PCIe messages are routed depending on specific bit field encodings in the message request header.

### 6.9.1 INTx Interrupt Signaling

The PEB383 forwards the INTx interrupts – PCI\_INT[A:D]n – generated by PCI devices onto the PCIe Interface, as PCIe Assert\_INTx and Deassert\_INTx messages (for more information, see “[Interrupt Handling](#)”).

### 6.9.2 Power Management

Power management messages support Power Management Events (PME) signaled by sources integrated into the bridge and for devices downstream of the bridge. The PEB383 forwards the power management events (PCI\_PME<sub>n</sub>) from PCI devices onto the PCIe Interface using PCIe PME messages (for more information, see “[Power Management Event](#)”).

### 6.9.3 Locked Transaction

Unlock messages support locked transaction sequences in the downstream direction. This type of message indicates the end of a locked sequence. The PEB383 supports locked transactions in the downstream direction and uses unlocked messages to unlock itself from the PCIe Interface (see “[Exclusive Access](#)”).

### 6.9.4 Slot Power Limit

These messages are transmitted to downstream devices by the root complex or a switch. The PEB383 copies the set slot power limit payload into the Set Slot Power Limit Scale and Set Slot Power Value fields of the “[PCIe Device Capabilities Register](#)”.

### 6.9.5 Vendor-defined and Device ID

These messages are used for vendor-specific purposes. The PEB383 does not support forwarding of these messages. It terminates Device ID message transactions on the PCI Interface with Master-Abort. It silently discards the Vendor-defined Type 1 message TLPs and handles the Vendor-defined Type 0 message TLPs as Unsupported Requests.

The PEB383 ignores the receipt of Ignored messages. It handles the receipt of Error signaling messages as Unsupported Requests. The PEB383 handles the receipt of INTx messages as malformed TLPs.

## 6.10 Transaction Ordering

**Table 12** defines the transaction ordering rules that are followed by the PEB383. These rules apply uniformly to all types of transactions, including Memory, I/O, Configurations, and Messages.

In the table, the columns represent a first received transaction while the rows represent a subsequently received transaction. Each table entry indicates the ordering relationship between the two transactions. The table entries are defined as follows:

- Yes – The second transaction is allowed to pass the first transaction.
- No – The second transaction is not allowed to pass the first transaction.

The PEB383 does not allow a posted transaction to pass another posted transaction even if the relaxed ordering attribute bit is set. However, the device allows a Read completion with the relaxed ordering attribute bit set to pass a posted transaction.

Table entries with 1) and 2) are defined as follows:

1. Indicates the ordering relationship when the relaxed ordering attribute bit is clear in the second transaction header information.
2. Indicates the ordering relationship when the relaxed ordering attribute bit is set in the second transaction header information.

**Table 12: Transaction Ordering**

		Posted Request	Non-Posted Request		Completion	
Can Row Pass Column?		Memory Write or Message Request	Read Request	I/O or Configuration Write Request	Read Completion	I/O or Configuration Write Completion
Posted Request	Memory Write or Message Request	1) No	Yes	Yes	1) Yes	1) Yes
		2) No			2) Yes	2) Yes
Non-Posted Request	Read Request	No	Yes	Yes	Yes	Yes
	I/O or Configuration	No	Yes	Yes	Yes	Yes
Completion	Read Completion	1) No	Yes	Yes	1) Yes	Yes
		2) Yes			2) Yes	
	I/O or Configuration Write Completion	No	Yes	Yes	Yes	Yes

## 6.11 Exclusive Access

The PEB383 provides an exclusive access method, which allows non-exclusive accesses to proceed while exclusive accesses take place. This allows a master to hold a hardware lock across several accesses without interfering with non-exclusive data transfer. Locked transaction sequences are generated by the host processor(s) as one or more reads followed by a number of writes to the same location(s). The PEB383 supports locked transactions only in the downstream direction. Upstream Lock transactions are handled with the LOCKn signal ignored.

A Lock is established when all the following conditions are met:

- A PCIe device initiates a Memory Read Lock (MRdLk) request to read from a target PCI device
- LOCKn is asserted on the PCI bus
- The target PCI device responds with a TRDYn

The bus is unlocked when the Unlock Message TLP is received on the PCIe link.

The PEB383 enters into target-lock state when it receives a MRdLk TLP, and enters into full-lock state when it receives successful completion from the target device. The PEB383 attempts locked read request on the PCI bus only after all the requests received prior to the locked request are completed on the bus. While in target-lock state, the PEB383 handles all the received TLPs with UR but continues to accept the transactions on the PCI Interface.

When the PEB383 enters into full-lock state, all upstream transactions on the PCI Interface are retried and all the downstream requests on the PCIe Interface, except Memory transactions, are handled as UR. Requests pending in upstream queues or buffers and internally generated messages are not allowed to be forwarded to the PCIe Interface until the PEB383 is unlocked from the PCIe Interface. However, the PEB383 accepts read completions for upstream read requests that were issued before the lock was established on the PCI bus when they return on the PCIe link.

As soon as the PCI bus is locked, any PCIe cycle to PCI is driven with the PCI\_LOCKn pin asserted, even if that specific cycle is not locked. This is not expected to occur because under the lock, the upstream component must not send any non-locked transactions downstream.

During the LOCK sequence, when the initial locked read command results in a master or target abort on the PCI bus, the PEB383 does not establish lock, and it sends a completion packet on the PCIe link with an error status. In case of a subsequent memory read or memory write receiving a target or master abort during a LOCK sequence, the PEB383 unlocks only after the unlock message is received on the PCIe Interface.





## 7. PCI Arbitration

Topics discussed include the following:

- “Overview”
- “Block Diagram”
- “PCI Arbitration Scheme”

### 7.1 Overview

The PCI internal bus arbiter manages access to the PCI bus for up to five requesters, including the PEB383. The bus arbiter has the following features:

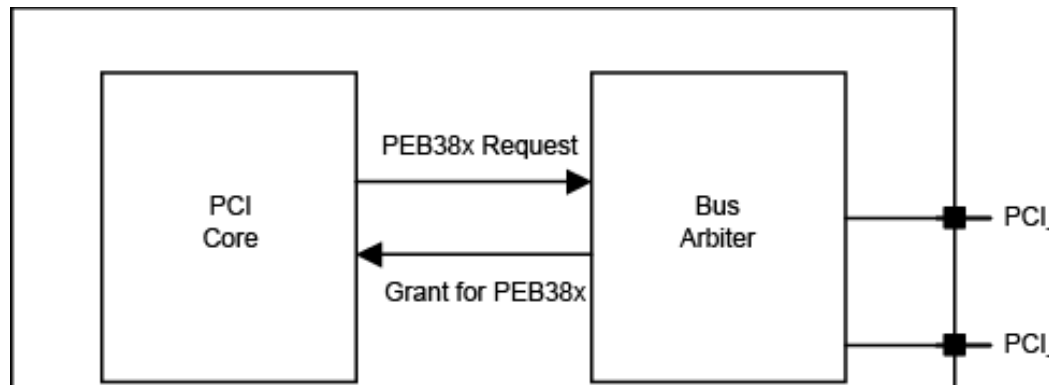
- Supports five requests (four external and one internal, the PEB383)
- Can be programmed to give high and low priorities for requesters
- Bus is parked on latest master given grant

### 7.2 Block Diagram

The bus arbiter handles internal requests from the PCI Core and external requests from devices on the PCI bus (see [Figure 17](#)). When the arbiter is enabled, the PEB383 asserts the grant for PCI devices and for the PCI Core. When the arbiter is disabled, there must be an external arbiter on the PCI bus that handles PEB383 requests through the PCI\_REQ[0]n signal, and grants bus access using the PCI\_GNT[0] signal.

Grants and Requests are bi-directional pins. PCI\_REQ[0]n is output enabled when the internal arbiter is disabled. Enable of PCI\_REQ[3:1]n are always hardcoded to 1'h0. PCI\_GNT[0] is an input pin when the internal arbiter is disabled.

**Figure 17: PCI Arbiter Block Diagram**



## 7.3 PCI Arbitration Scheme

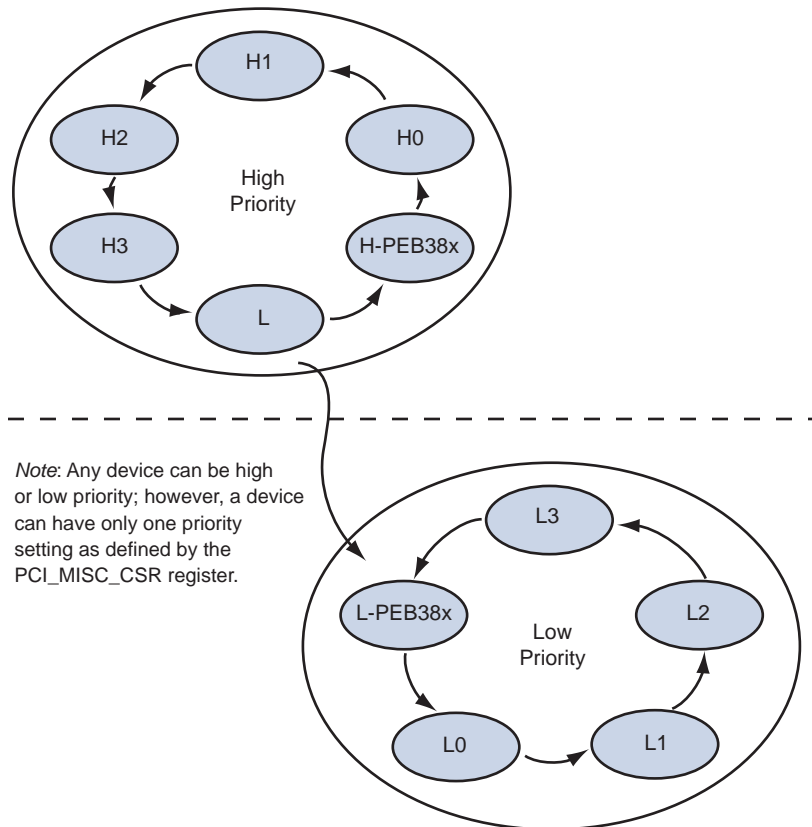
The arbiter can be programmed to enable or disable, and prioritize, each requester using the “**PCI Miscellaneous Control and Status Register**”.

The PEB383, by default, is assigned a high priority and the other requesters are assigned a low priority. Based on the priority setting, requesters are divided into two groups of high and low priority. Within a group, priority is determined using a round-robin method (see **Figure 18**). The low-priority group is handled as one member of the high-priority group.

By default, the PCI arbiter initially parks the bus on the PEB383. After servicing the requesters when the bus is in idle state, the arbiter is parked on the last served requester.

The priority method is shown in **Figure 18**. Note that any one request input can only be mapped to high or low priority. If, for example, PCI\_REQ2n is mapped to low priority, then the H2 state is skipped over.

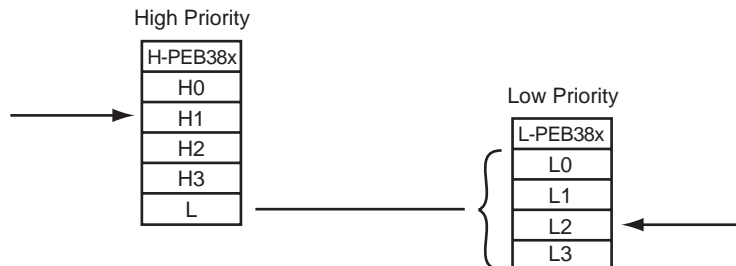
**Figure 18: PCI Arbitration Priority**



The PEB383 also keeps track of which requester, in each priority group, was last served. This is achieved with two arbitration pointers, one for each priority. When a new requester is granted the bus, the pointer(s) advance. This gives each requester a fair chance of being selected first when multiple requesters request the bus.

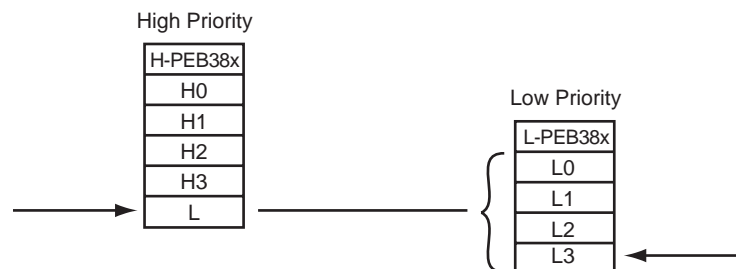
This is shown conceptually in [Figure 19](#). Here the last served high priority device is H1, and the last served low priority device is L2. When the high priority pointer is at H1, the order of priority is H2, H3, Low, H-PEB383, H0, and H1.

**Figure 19: Arbitration Pointers – Example 1**



When the transaction for device 1 is complete, all input requests are sampled to determine which device should be granted next. If there are no requests the pointer stays at H1, and no grants are given. If two requests occur at the same time — in this example, L3 and H1 — then L3 is granted and the pointers advance as shown in [Figure 20](#).

**Figure 20: Arbitration Pointers – Example 2**



Once L3 is completed, the input requests are sampled again. H0 and H1 are now requesting the bus. H0 would then obtain access to the bus because the new priority ordering is H-PEB383, H0, H1, H2, H3, L. The initial ordering of the requests is not considered; that is, H1 requested before H0, but H0 wins as it is first in the priority list. This ensures that all requestors obtain equal access within a priority group.

After asserting the grant, if the bus is in an idle state for  $M$  clock cycles grant is de-asserted.



## 8. Interrupt Handling

Topics discussed include the following:

- “Overview”
- “Interrupt Sources”
- “Interrupt Routing”

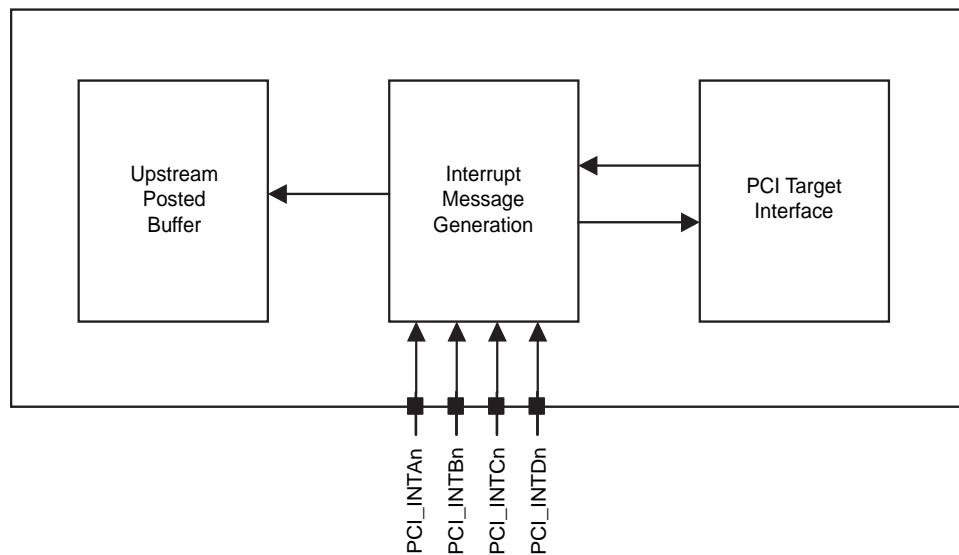
### 8.1 Overview

The PEB383 supports the two types of interrupts that originate on a PCI bus:

- Legacy PCI interrupts, PCI\_INT[D:A]n
- Message-based interrupts
  - Message Signaled Interrupts (MSI)
  - Enhanced Message Signaled Interrupts (MSI-X)

The PEB383’s PCI Interface forwards legacy INTx assertion/de-assertions in the form of Assert\_INTx and Deassert\_INTx messages on its PCIe link. The PEB383 handles MSI and MSI-X transactions as PCI memory write transactions. When the bridge receives an MSI/MSI-X transaction on its PCI Interface, it forwards it as a memory write TLP on its PCIe link. Both INTx messages and MSI/MSI-X transactions flow through the PEB383’s upstream posted buffer, as displayed in [Figure 21](#).

**Figure 21: Interrupt Handling Diagram**



The Interrupt Message Generation module connects to the PCI Target Interface, external PCI\_INT[D:A]n interrupts, and the upstream posted buffer (see [Figure 21](#)). Assertion and de-assertion of interrupts are stored in the form of Assert\_INTx and Deassert\_INTx flags. These flags are kept asserted until the posted buffer can handle corresponding assert and de-assert messages. If an interrupt pin is toggled when the PCI Interface is engaged with a PCI-initiated posted transaction, assert or de-assert message loading into the upstream posted request buffer is stalled until the upstream posted transaction terminates. Posted transactions are retried on the AD bus while an interrupt message is loaded into the posted buffer. A De-assert message always follows an Assert message. More than one interrupt pin can toggle at any point of time; however, a round-robin arbitration schedules the interrupt message transmission.

There is no buffering for interrupt messages before loading them into the upstream posted buffer. Therefore, only one pair of Assert\_INTx and Deassert\_INTx messages is loaded into the buffer when allowed. In the worst case, the bridge may send duplicate messages; however, this is permitted according to the *PCI Express Base Specification (Revision 1.1)*.

## 8.2 Interrupt Sources

The PEB383 does not have an internal source of interrupts: it forwards legacy PCI\_INT[D:A]n interrupts from the PCI Interface to the PCIe Interface in the form of Assert[D:A] and De-assert[D:A] messages with PEB383 PCIe transaction IDs.

## 8.3 Interrupt Routing

Interrupt remapping is not performed by the PEB383. Legacy interrupts, PCI\_INT[A:D]n, are routed to the upstream PCIe port in the form of Assert\_INTx and Deassert\_INTx [A,B,C,D] messages.

---

## 9. Error Handling

Topics discussed include the following:

- “Overview”
- “PCIe as Originating Interface”
- “PCI as Originating Interface”
- “Timeout Errors”
- “Other Errors”
- “Error Handling Tables”

---

### 9.1 Overview

This chapter discusses how the PEB383 handles errors that occur during the processing of upstream and downstream transactions. For all errors that are detected by the bridge, it sets the appropriate Error Status bits – PCI Error bit(s) and PCIe Error status bit(s) – and generates an error message on PCIe, if enabled.

Each error condition has an error severity level programmable by software, and a corresponding error message generated on PCIe. Each detected error condition has a default error severity level (fatal or non-fatal) and, when enabled, has a corresponding error message generated on PCIe. The error severity level is software programmable.

PCIe link error message generation is controlled by the following bits:

- SERR\_EN in the “PCI Bridge Control and Interrupt Register”
- FTL\_ERR\_EN in the “PCIe Device Control and Status Register”
- NFTL\_ERR\_EN in the “PCIe Device Control and Status Register”
- COR\_ERR\_EN in the “PCIe Device Control and Status Register”

ERR\_FATAL PCIe messages are enabled for transmission if either of the following bits is set:

SERR\_EN in “PCI Control and Status Register”, or FTL\_ERR\_EN in “PCIe Device Control and Status Register”.

ERR\_NONFATAL messages are enabled for transmission if either of the following bits is set: SERR\_EN in “**PCI Control and Status Register**”, or NFTL\_ERR\_EN in “**PCIe Device Control and Status Register**”.

ERR\_COR messages are enabled for transmission if COR\_ERR\_EN is set in “**PCIe Device Control and Status Register**”.

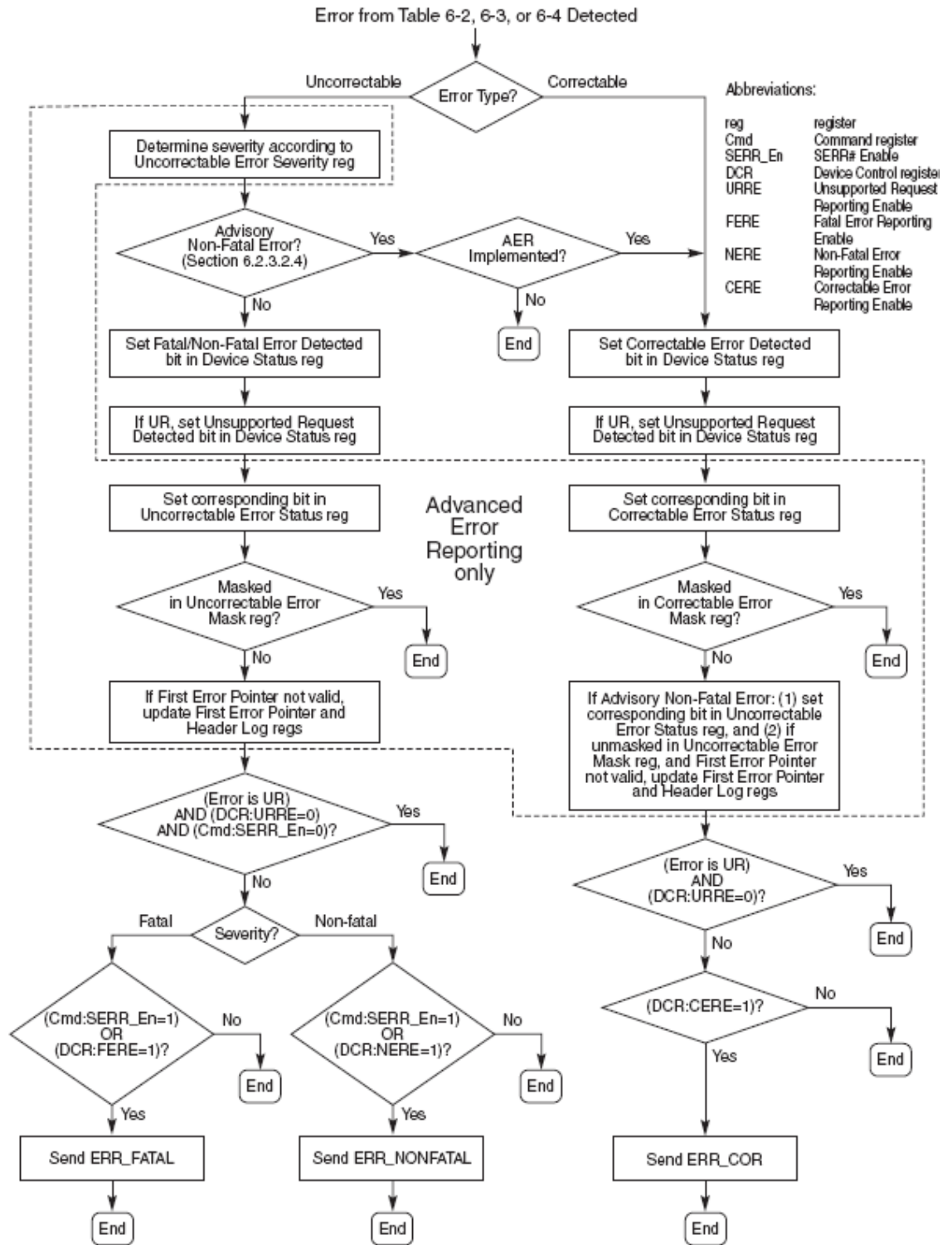
FTL\_ERR\_DTD, NFTL\_ERR\_DTD, and COR\_ERR\_DTD bits in “**PCIe Device Control and Status Register**” are set for the corresponding errors on the PCIe Interface, regardless of the error reporting enable bits.

The PEB383 also supports Advisory Non-Fatal error messages in the case where a TLP Error detected is a Advisory Non-Fatal Error and the Advisory Non-Fatal Error mask bit, ANFE, in the “**PCIe Correctable Error Mask Register**” is not masked then a Correctable error message is generated instead of a Non-Fatal error message.

**Figure 22** depicts the high-level flowchart for error handling on PCIe. This is taken from Table 6-2 of the *PCI Express Base Specification (Revision 1.1)*, and includes advanced error handling. Additional error handling requirements for a PCIe bridge are described in subsequent sections of the specification.



Figure 22: PCIe Flowchart of Device Error Signaling and Logging Operations



## 9.2 PCIe as Originating Interface

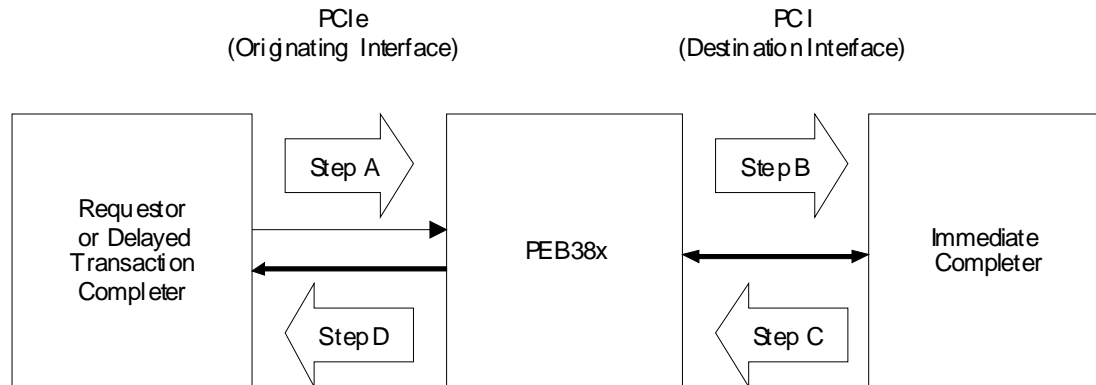
This section describes how the PEB383 handles error support for transactions that flow downstream from PCIe to PCI (see [Figure 23](#)).

In the case of reception of a Write Request or Read Completion with a Poisoned TLP, the entire data payload of the PCIe transaction is considered as corrupt and the parity is inverted on every data phase forwarded (see [Table 13](#)). In the case of reception of a request with ECRC error, the entire TLP is considered as corrupt and is dropped by the bridge.

**Table 13: Error Forwarding Requirements (Step A to Step B) for Received PCIe Errors**

Received PCIe Error (Step A)	Forwarded PCI Error Mode 1 (Parity) (Step B)
Write Request or Read Completion with Poisoned TLP	Poisoned Data Parity
Request with ECRC (Optional Support) Error	Do not forward

**Figure 23: Transaction Error Forwarding with PCIe as Originating Interface**



[Table 14](#) provides the translation a bridge has to perform when it forwards a non-posted PCIe request (read or write) to PCI and the request is completed immediately on PCI, either normally or with an error condition.

**Table 14: Bridge Requirements for Transactions Requiring a Completion (Immediate Response)**

Immediate PCI Termination	PCIe Completion Status
Data transfer with uncorrectable data error (reads)	Successful (Poisoned TLP)
Data transfer with uncorrectable data error (non-posted writes)	Unsupported Request

**Table 14: Bridge Requirements for Transactions Requiring a Completion (Immediate Response)**

Immediate PCI Termination	PCIe Completion Status
Master-Abort	Unsupported Request
Target-Abort	Completer Abort

In the case of an Advisory Non-Fatal Error detection, the following actions are taken by the PEB383:

1. If the severity of the TLP Error detected in “**PCIe Uncorrectable Error Severity Register**” is Non-Fatal then:
  - a. COR\_ERR\_DTD is set in the “**PCIe Device Control and Status Register**”
  - b. ANFE is set in the “**PCIe Correctable Error Status Register**”
2. And if the ANFE bit is not masked in the “**PCIe Correctable Error Mask Register**” then:
  - a. TLP Error Status bit is set in the “**PCIe Uncorrectable Error Status Register**”
  - b. If the corresponding TLP Error Mask bit is clear in the “**PCIe Uncorrectable Error Mask Register**” and ERR\_PTR is not valid in the “**PCIe Advanced Error Capabilities and Control Register**”, then the TLP header is logged in the “**PCIe Header Log 1 Register**” and ERR\_PTR is updated in the “**PCIe Advanced Error Capabilities and Control Register**”.
  - c. If COR\_ERR\_EN is set in the “**PCIe Device Control and Status Register**” then it sends a Correctable error message.

### 9.2.1 Received Poisoned TLPs

When the bridge receives a poisoned TLP it completes the following while forwarding it to the PCI Interface:

1. If the severity of the PTLP in the “**PCIe Uncorrectable Error Severity Register**” is Non-Fatal and the ANFE Mask bit is clear in “**PCIe Correctable Error Mask Register**” then:
  - A Correctable error message is generated if the COR\_ERR\_EN bit is set in the “**PCIe Device Control and Status Register**”
  - ANFE bit is set in the “**PCIe Correctable Error Status Register**”
  - COR\_ERR\_DTD bit is set in the “**PCIe Device Control and Status Register**”
  - PTLP bit is set in the “**PCIe Uncorrectable Error Status Register**”
  - TLP header is logged in the Header Log register and ERR\_PTR is updated if the PTLP Mask bit in “**PCIe Uncorrectable Error Mask Register**” is clear and the ERR\_PTR is not valid
2. If the severity of the PTLP bit in “**PCIe Uncorrectable Error Severity Register**” is Non-Fatal and the ANFE Mask bit is set in “**PCIe Correctable Error Mask Register**” then:
  - No error message is generated
  - COR\_ERR\_DTD bit is set in the “**PCIe Device Control and Status Register**”
  - ANFE bit is set in the “**PCIe Correctable Error Status Register**”

3. If it is not an AFNE then:
  - Fatal error message is generated if PTLP Mask bit is clear in the “PCIe Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN bit is set in the “PCIe Device Control and Status Register”
  - FTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”
  - PTLP bit is set in the “PCIe Uncorrectable Error Status Register”
  - TLP header is logged in the Header Log register and ERR\_PTR is updated if the PTLP Mask bit is clear and the ERR\_PTR is not valid.
  - S\_SERR bit is set in the “PCI Control and Status Register” if Fatal error message is generated and the SERR\_EN bit is set in the “PCI Control and Status Register”.
4. In all three of the previous cases the following actions are also taken by the PEB383:
  - D\_PE bit is set in “PCI Control and Status Register”
  - MDP\_D bit set in “PCI Control and Status Register” if the poisoned TLP is a read completion and the PERESP bit is set in the “PCI Control and Status Register”
  - Parity bit is inverted on the PCI bus with each associated data Dword
  - MDP\_D bit is set in the “PCI Secondary Status and I/O Limit and Base Register” if the S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”, and the bridge sees the PCI\_PERRn pin asserted when forwarding a write request transaction with bad parity to the PCI bus. The PERR\_AD bit in the “PCIe Secondary Uncorrectable Error Status Register” is set, Secondary Header is Logged and Secondary First Error Pointer is updated if enabled. No error message is generated when PCI\_PERRn is seen asserted by the bridge when forwarding a Poisoned TLP transaction from PCIe to PCI with bad parity.

## 9.2.2 Received ECRC Errors

When the PEB383 receives a TLP with ECRC error, it does the following:

1. Drops the transaction
2. D\_PE is set in the “PCI Control and Status Register”
3. ECRC bit is set in the “PCIe Uncorrectable Error Status Register”
4. Header is logged in the “PCIe Header Log 1 Register” and the ERR\_PTR field is updated in the “PCIe Advanced Error Capabilities and Control Register” if ECRC Error Mask bit is clear in the “PCIe Uncorrectable Error Mask Register” and ERR\_PTR is not valid.
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of ECRC bit in “PCIe Uncorrectable Error Severity Register” if the ECRC Mask bit is clear in “PCIe Uncorrectable Error Mask Register”, and either SERR\_EN bit is set in the “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN is set in the “PCIe Device Control and Status Register”
6. S\_SERR bit is set in the “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and SERR\_EN bit is set in the “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

## 9.2.3 PCI Uncorrectable Data Errors

This section describes the bridge requirements for error handling when forwarding downstream a non-poisoned PCIe transaction to PCI and the bridge detects an uncorrectable data error. The error is detected on the PCI Interface.

### 9.2.3.1 Immediate Reads

When the PEB383 forwards a read request (I/O, Memory, or Configuration) downstream, it does the following when it detects an uncorrectable data error on the destination interface while receiving an immediate response from the completer:

1. MDP\_D bit is set in the “PCI Secondary Status and I/O Limit and Base Register” if the S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”
2. D\_PE in the “PCI Control and Status Register” is set
3. PCI\_PERRn is asserted on the PCI Interface if the S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”
4. UDERR bit is set in “PCIe Secondary Uncorrectable Error Status Register”
5. Header is logged in the “PCIe Secondary Header Log 1 Register” and the SUFEP field is updated in the “PCIe Secondary Error Capabilities and Control Register” if UDERR Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register” and SUFEP is not valid
6. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of UDERR bit in “PCIe Secondary Uncorrectable Error Severity Register” if the UDERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in the “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in the “PCIe Device Control and Status Register”
7. S\_SERR bit is set in the “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and S\_SERR bit is set in the “PCI Control and Status Register”
8. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

For an immediate read transaction, if the PEB383 detects an uncorrectable data error on the destination bus it continues to fetch data until the byte count is satisfied, or the target on the destination bus ends the transaction. When the bridge creates the PCIe completion, it forwards it with successful completion status and poisons the TLP.

### 9.2.3.2 Non-Posted Writes

When the PEB383 detects PCI\_PERRn asserted on the PCI Interface while forwarding a non-poisoned non-posted write transaction from PCIe, it does the following:

1. If the target completes the transaction immediately with a data transfer, the PEB383 generates a PCIe completion with Unsupported Request status to report the error to the requester
2. PERR\_AD bit is set in the “PCIe Secondary Uncorrectable Error Status Register”
3. MDP\_D bit in the “PCI Secondary Status and I/O Limit and Base Register” is set if S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”

4. Header is logged in the “PCIe Secondary Header Log 1 Register” and the SUFEP field is updated in the “PCIe Secondary Error Capabilities and Control Register” if PERR\_AD Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register” and SUFEP is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of PERR\_AD bit in “PCIe Secondary Uncorrectable Error Severity Register” if the PERR\_AD Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in the “PCI Control and Status Register” or FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”
6. S\_SERR bit is set in the “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and SERR\_EN bit is set in the “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

### 9.2.3.3 Posted Writes

When the PEB383 detects PCI\_PERRn asserted on the PCI Interface while forwarding a non-poisoned posted write transaction from PCIe, it does the following:

1. Continues to forward the remainder of the transaction
2. MDP\_D bit in the “PCI Secondary Status and I/O Limit and Base Register” is set if S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”
3. PERRn Assertion Detected Status bit is set in the “PCIe Secondary Uncorrectable Error Status Register”
4. Header is logged in the “PCIe Secondary Header Log 1 Register” and the SUFEP field is updated in the “PCIe Secondary Error Capabilities and Control Register” if PERR\_AD Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register” and SUFEP is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of PERR\_AD bit in “PCIe Secondary Uncorrectable Error Severity Register” if the PERR\_AD Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register”, and either SERR\_EN bit is set in the “PCI Control and Status Register” or FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”
6. S\_SERR bit is set in the “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and SERR\_EN bit is set in the “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

### 9.2.4 PCI Uncorrectable Address/Attribute Errors

When the PEB383 forwards transactions from PCIe to PCI, address or attribute errors are reported through the PCI\_SERRn pin. When the PEB383 detects PCI\_SERRn asserted it does the following:

1. Continues forwarding transaction
2. S\_SERR System bit is set in the “PCI Secondary Status and I/O Limit and Base Register”
3. SERR\_AD bit is set in the “PCIe Secondary Uncorrectable Error Status Register”
4. In this case Header is not logged but the SUFEP is updated in the “PCIe Secondary Error Capabilities and Control Register” if the SUFEP bit is not valid and SERR\_AD Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register”

5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of SERR\_AD bit in “PCIe Secondary Uncorrectable Error Severity Register” if SERR\_AD Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” or SERR\_EN bit is set in “PCI Bridge Control and Interrupt Register”, and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
6. S\_SERR bit is set in the “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and SERR\_EN bit is set in the “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

## 9.2.5 Received Master-Abort on PCI Interface

This section describes the actions taken by the PEB383 when a Master-Abort is received on the PCI Interface.

### 9.2.5.1 Master Abort on a Posted Transaction

When the PEB383 receives a Master-Abort on the PCI bus while forwarding a posted write transaction from PCIe, it does the following:

1. Discards the entire transaction
2. R\_MA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
3. R\_MA bit is set in the “PCIe Secondary Uncorrectable Error Status Register”
4. Header is logged in the “PCIe Secondary Header Log 1 Register” and SUFEP is updated in the “PCIe Secondary Error Capabilities and Control Register” if R\_MA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of R\_MA bit in “PCIe Secondary Uncorrectable Error Severity Register” if R\_MA Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register” or MA\_ERR bit is set in “PCI Bridge Control and Interrupt Register”, and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
6. S\_SERR bit is set in “PCI Control and Status Register” if the R\_MA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” or MA\_ERR bit is set in “PCI Bridge Control and Interrupt Register” and the SERR\_EN bit is set
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in the “PCIe Device Control and Status Register”

### 9.2.5.2 Master-Abort On PCI Interface for Non-Posted Transaction

When the PEB383 receives a Master-Abort on the PCI bus while forwarding a non-posted PCIe request, it does the following:

1. Returns a completion with Unsupported Request status on the PCIe
2. R\_MA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
3. R\_MA bit is set in “PCIe Secondary Uncorrectable Error Status Register”

4. Header is logged in the “PCIe Secondary Header Log 4 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if R\_MA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of R\_MA bit in “PCIe Secondary Uncorrectable Error Severity Register” if R\_MA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
6. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR Enable bit is set in “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

## 9.2.6 Received Target-Abort On PCI Interface

This section describes the functionality of the PEB383 when a Target-Abort is received on the PCI Interface in response to posted, and non-posted transactions.

### 9.2.6.1 Target Abort On A Posted Transaction

When the PEB383 receives Target-Abort on the PCI Interface for posted requests, it takes the following actions:

1. Drops the entire transaction
2. R\_TA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
3. R\_TA bit is set in “PCIe Secondary Uncorrectable Error Status Register”
4. Header is logged in the “PCIe Secondary Header Log 1 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if R\_TA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of R\_TA bit in the “PCIe Secondary Uncorrectable Error Severity Register” if R\_TA Mask bit is clear in the “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in the “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in the “PCIe Device Control and Status Register”
6. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.2.6.2 Target-Abort On PCI Interface For Non-Posted Transaction

When the PEB383 receives a Target-Abort while forwarding a PCIe non-posted request to the PCI Interface, it takes the following actions:

1. Returns a completion with Completer Abort status on the PCIe link
2. R\_TA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
3. R\_TA bit is set in “PCIe Secondary Uncorrectable Error Status Register”



4. Header is logged in the “PCIe Secondary Header Log 1 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if R\_TA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
5. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of R\_TA bit in “PCIe Secondary Uncorrectable Error Severity Register” if R\_TA Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
6. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “PCI Control and Status Register”
7. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.3 PCI as Originating Interface

This section describes how the PEB383 handles errors for upstream transactions from PCI to PCIe (see Figure 24). The bridge supports TLP poisoning as a Transmitter to permit proper forwarding of parity errors that occur on the PCI Interface.

**Figure 24: Transaction Error Forwarding with PCI as Originating Interface**

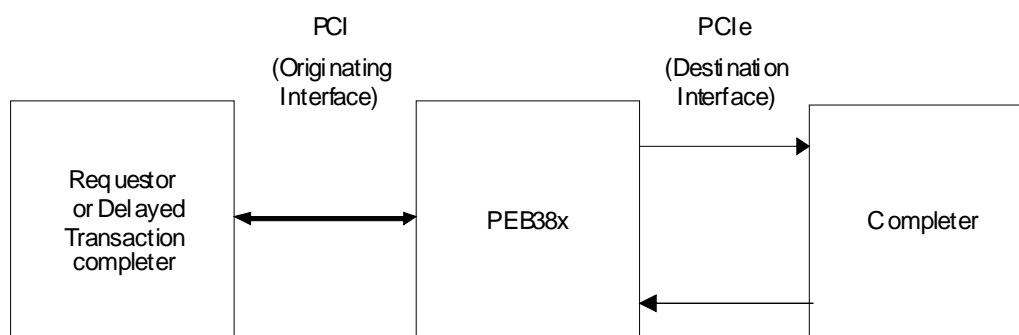


Table 15 provides the error forwarding requirements for Uncorrectable data errors detected by the PEB383 when a transaction targets the PCIe Interface. Posted and non-posted write data received on the secondary PCI Interface with bad parity are forwarded to PCIe as Poisoned TLPs.

**Table 15: Error Forwarding Requirements for Received PCI Errors**

Received PCI Error	Forwarded PCIe Error
Write with Uncorrectable Data Error	Write request with Poisoned TLP

**Table 16** describes the PEB383 behavior on a PCI Delayed transaction that is forwarded by a bridge to PCIe as a Memory Read request or an I/O Read/Write request, and the PCIe Interface returns a completion with Unsupported Request or Completer Abort Completion status for the request.

**Table 16: Error Forwarding Requirements for PCI Delayed Transaction**

PCIe Completion Status	PCI Immediate Response Master-Abort Mode = 1	PCI Immediate Response Master-Abort Mode = 0
Unsupported Request (on Memory or I/O Read)	Target Abort	Normal Completion, return 0xFFFF_FFFF
Unsupported Request (on I/O Write)	Target Abort	Normal Completion
Completer Abort	Target Abort	Target Abort

### 9.3.1 Received PCI Errors

This section describes how the PEB383 handles PCI errors.

#### 9.3.1.1 Uncorrectable Data Error on a Non-Posted Write Transaction PCI Mode

When the PEB383 receives non-posted write transaction that is addressed such that it crosses the bridge, and the bridge detects an uncorrectable data error on its PCI Interface, it does the following:

1. D\_PE bit is set in “PCI Secondary Status and I/O Limit and Base Register”
2. If S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”, then the transaction is discarded and is not forwarded to PCIe and the PERR# pin is asserted on the PCI bus
3. If S\_PERESP bit is not set in “PCI Bridge Control and Interrupt Register”, then the data is forwarded to PCIe as a Poisoned TLP. M\_DPE bit is set in “PCI Control and Status Register” if the S\_PERESP bit is set. The PERR# pin is not asserted on the PCI bus
4. UDERR bit is set in “PCIe Secondary Uncorrectable Error Status Register”
5. Header is logged in the “PCIe Secondary Header Log 1 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if UDERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
6. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of Uncorrectable Data Error bit in “PCIe Secondary Uncorrectable Error Severity Register”, if UDERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
7. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set
8. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.3.1.2 Uncorrectable Data Error on a Posted Write

When the PEB383 receives posted write transaction that is addressed such that it crosses the bridge and the bridge detects an uncorrectable data error on its secondary PCI Interface, it does the following:

1. D\_PE bit is set in “PCI Secondary Status and I/O Limit and Base Register”
2. If S\_PERESP bit is set in “PCI Bridge Control and Interrupt Register”, PERR# signal is asserted
3. MDP\_D bit is set in “PCI Secondary Status and I/O Limit and Base Register” if S\_PERESP bit is set in the “PCI Bridge Control and Interrupt Register”
4. UDERR bit is set in “PCIe Secondary Uncorrectable Error Status Register”
5. Header is logged in the “PCIe Secondary Header Log 1 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if UDERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
6. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of UDERR bit in “PCIe Secondary Uncorrectable Error Severity Register” if UDERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
7. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “PCI Control and Status Register”
8. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.3.1.3 Uncorrectable Data Error on PCI Delayed Read Completions

When the PEB383 detects PERR# asserted by the initiating PCI master while forwarding a non-poisoned read completion from PCIe to PCI, it does the following:

1. Forwards the remainder of completion
2. PERR\_AD bit is set in “PCIe Secondary Uncorrectable Error Status Register”
3. Header is logged in the “PCIe Secondary Header Log 1 Register” and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if, PERR\_AD Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
4. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of PERR\_AD bit in “PCIe Secondary Uncorrectable Error Severity Register”, if PERR\_AD Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
5. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “PCI Control and Status Register”
6. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

When the PEB383 detects PERR# asserted by the initiating PCI master while forwarding a poisoned read completion from PCIe to PCI, it does the above mentioned actions but no error message is generated.

### 9.3.1.4 Uncorrectable Address Error

When the PEB383 detects an Uncorrectable Address Error, and parity error detection is enabled using the S\_PERESP bit in “PCI Bridge Control and Interrupt Register”, the bridge takes the following actions:

1. Transaction is terminated with a Target Abort and discarded
2. D\_PE bit is set in “PCI Secondary Status and I/O Limit and Base Register” independent of S\_PERESP bit in “PCI Bridge Control and Interrupt Register”
3. S\_TA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
4. UADD\_ERR bit is set in “PCIe Secondary Uncorrectable Error Status Register”
5. Header is logged in the Secondary Header Log register and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if UADD\_ERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
6. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of UADD\_ERR bit in “PCIe Secondary Uncorrectable Error Severity Register” if UADD\_ERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”
7. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “PCI Control and Status Register”
8. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.3.1.5 Uncorrectable Attribute Error

When the PEB383 detects an Uncorrectable Attribute Error and parity error detection is enabled via the Parity Error Response Enable bit in “PCI Bridge Control and Interrupt Register” then the bridge takes the following actions:

1. Transaction is terminated with a Target Abort and discarded
2. D\_PE bit is set in “PCI Secondary Status and I/O Limit and Base Register” independent of S\_PERESP bit in “PCI Bridge Control and Interrupt Register”
3. S\_TA bit is set in “PCI Secondary Status and I/O Limit and Base Register”
4. UATT\_ERR bit is set in “PCIe Secondary Uncorrectable Error Status Register”
5. Header is logged in the Secondary Header Log register and ERR\_PTR is updated in the “PCIe Secondary Error Capabilities and Control Register” if UATT\_ERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and ERR\_PTR is not valid
6. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of UATT\_ERR bit in “PCIe Secondary Uncorrectable Error Severity Register” if UATT\_ERR Mask bit is clear in “PCIe Secondary Uncorrectable Error Mask Register” and either SERR\_EN bit is set in “PCI Control and Status Register” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “PCIe Device Control and Status Register”

7. S\_SERR bit is set in “PCI Control and Status Register” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “PCI Control and Status Register”
8. FTL\_ERR\_DTD/NFTL\_ERR\_DTD bit is set in “PCIe Device Control and Status Register”

### 9.3.2 Unsupported Request Completion Status

The PEB383 provides two methods for handling a PCIe completion received with Unsupported Request status in response to a request originated by a secondary interface in PCI mode. The bridge’s response to this completion is controlled by the MA\_ERR bit in “PCI Bridge Control and Interrupt Register”:

- MA\_ERR bit set – When MA\_ERR is set the PEB383 signals a Target-Abort to the originating master of an upstream read or a non-posted write transaction if the corresponding request on the PCIe link results in a completion with Unsupported Request status. The PEB383 also sets the S\_TA bit in the “PCI Secondary Status and I/O Limit and Base Register”.
- MA\_ERR bit is cleared – This is the default PCI compatible mode where an Unsupported Request Error is not considered an error. When a Read transaction initiated on the secondary interface results in a completion with Unsupported Request status, the PEB383 returns 0xFFFF\_FFFF to the originating master and normally terminates the read transaction on the originating interface (by asserting TRDY#). When a non-posted write transaction results in a completion with Unsupported Request status, the PEB383 normally completes the write transaction on the originating bus (by asserting TRDY#) and discards the write data.

In all cases of receiving Unsupported Request completion status on PCIe in response to a PCI request initiated on the secondary interface, the PEB383 sets the R\_MA in the “PCI Control and Status Register”.

### 9.3.3 Completer Abort Completion Status

When the PEB383 receives a completion with Completer Abort status on the PCIe link in response to a forwarded non-posted PCI transaction, it sets the R\_TA bit in the “PCI Secondary Status and I/O Limit and Base Register”.

A Completer Abort response on PCIe translates to a Delayed Transaction Target-Abort if the secondary interface is in PCI mode. The PEB383 provides data to the requesting agent up to the point where data was successfully returned from the PCIe interface, and then signals Target-Abort. R\_TA is set in “PCI Control and Status Register” when signaling a Target-Abort to a PCI agent.

## 9.4 Timeout Errors

This section discusses how the PEB383 handles PCIe and PCI timeout errors.

### 9.4.1 PCIe Completion Timeout Errors

The PCIe Completion Timeout function allows requestors to abort a non-posted request if the completion does not arrive within a reasonable period of time. When bridges act as initiators on PCIe on behalf of internally generated requests, and requests forwarded from a secondary interface in PCI mode, they act as endpoints for requests that they take ownership. When the PEB383 detects a completion timeout it responds as if a completion with Unsupported Request status has been received and follows the rules for handling Unsupported Request Completions as described in “**Unsupported Request Completion Status**”. In addition, the bridge takes the following actions:

1. CTO bit is set in “**PCIe Uncorrectable Error Status Register**”
2. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of the CTO bit in “**PCIe Uncorrectable Error Severity Register**” if CTO Mask bit is clear in “**PCIe Correctable Error Mask Register**” and either SERR\_EN bit is set in “**PCI Control and Status Register**” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “**PCIe Device Control and Status Register**”
3. S\_SERR bit is set in “**PCI Control and Status Register**” if an error message (Fatal/Non-Fatal) is generated and the SERR\_EN bit is set in “**PCI Control and Status Register**”

### 9.4.2 PCI Delayed Transaction Timeout Errors

If a delayed transaction timeout is detected the PEB383 does the following:

1. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of DTDTE bit in “**PCIe Secondary Uncorrectable Error Severity Register**”, if DTDTE Mask bit is clear in “**PCIe Secondary Uncorrectable Error Mask Register**” or DISCARD\_SERR bit is set “**PCI Bridge Control and Interrupt Register**” and either SERR\_EN bit is set in “**PCI Control and Status Register**” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “**PCIe Device Control and Status Register**”
2. No Header is logged
3. S\_SERR bit is set in “**PCI Control and Status Register**” if an error message (Fatal/Non-Fatal) is generated and SERR\_EN bit is set in “**PCI Control and Status Register**”

## 9.5 Other Errors

PCI devices can assert SERR# when detecting errors that compromise system integrity. When the PEB383 detects SERR# on the secondary interface, it does the following:

1. S\_SERR bit is set in “**PCI Secondary Status and I/O Limit and Base Register**”
2. Error Fatal or Non-Fatal message is generated on PCIe as per the severity level of SERR\_AD bit in “**PCIe Secondary Uncorrectable Error Severity Register**” if SERR\_AD Mask bit is clear in “**PCIe Secondary Uncorrectable Error Mask Register**” or SERR\_EN bit is set in “**PCI Bridge Control and Interrupt Register**” and either SERR\_EN bit is set in “**PCI Control and Status Register**” or FTL\_ERR\_EN/NFTL\_ERR\_EN bit is set in “**PCIe Device Control and Status Register**”
3. SERR\_AD bit is set in “**PCIe Secondary Uncorrectable Error Status Register**”
4. SUFEP field is updated in “**PCIe Secondary Error Capabilities and Control Register**”
5. No Header is Logged for SERR# assertion

## 9.6 Error Handling Tables

This section contains error handling information in a table format. Some of this information may overlap with error information discussed in previous sections of this chapter.

**Table 17: ECRC Errors**

Error Details	Primary Reporting Mechanism
ECRC Error	<ol style="list-style-type: none"> <li>1. "PCIe Uncorrectable Error Status Register" [ECRC].</li> <li>2. "PCI Control and Status Register" [D_PE].</li> <li>3. "PCI Control and Status Register" [S_SERR] if an error message is generated and [SERR_EN] bit is set in same register.</li> <li>4. "PCIe Device Control and Status Register" [FTL_ERR_DTD/NFTL_ERR_DTD].</li> <li>5. TLP is dropped.</li> </ol>

**Table 18: Poisoned TLP Errors**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
Poisoned TLP Error	<ol style="list-style-type: none"> <li>1. "PCIe Device Control and Status Register"[COR_ERR_DTD/FTL_ERR_DTD].</li> <li>2. "PCIe Correctable Error Status Register" [ANFE] in case of Advisory Non-Fatal condition.</li> <li>3. "PCIe Uncorrectable Error Status Register" [PTLP].</li> <li>4. "PCI Control and Status Register" [S_SERR] if a Fatal error message is sent and [SERR_EN] bit is set in same register.</li> <li>5. "PCI Control and Status Register" [D_PE].</li> <li>6. "PCI Control and Status Register" [MDP_D] is set if the Poisoned TLP is a read completion and [PERESP] is set in same register.</li> </ol>	<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [MDP_D] if [S_PERESP] is set in "PCI Bridge Control and Interrupt Register" and PCI_PERRn pin asserted when forwarding a write request transaction with bad parity to the PCI bus.</li> <li>2. "PCIe Secondary Uncorrectable Error Status Register" [PERR_AD].</li> </ol>

**Table 19: Malformed TLP Errors**

Error Details	Primary Reporting Mechanism
Payload exceeds max_payload_size	1. "PCIe Uncorrectable Error Status Register" [MAL_TLP]
Write TLP payload does not match length specified in	2. Optional ERR_FATAL or ERR_NONFATAL message sent.
Completion TLP payload does not match length	3. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].
Mismatch between TD and presence of ECRC	4. "PCI Control and Status Register" [S_SERR] if error message is generated and [SERR_EN] is set in same register.
Address/Length combination crosses 4KByte	5. TLP discarded.
Received INTx message with TC > 0	
Received Power Management message with TC > 0	
Received Error message with TC > 0	
Received Unlock message with TC > 0	
TLP Type field uses undefined value	
Illegal byte enables: <ol style="list-style-type: none"> <li>1. FBE = 0 when Length &gt; 1DW.</li> <li>2. LBE!= 0 when length = 1DW.</li> <li>3. LBE = 0 when length &gt; 1DW.</li> <li>4. Non-contiguous byte enables when length = 2DW, and non-Quadword aligned address.</li> <li>5. Non-contiguous byte enables when length &gt; 2DW.</li> </ol>	
IO request with TC > 0, or Attribute > 0 or Length > 1DW or LBE > 0	
Configuration request with TC>0, or Attribute > 0 or Length >1DW or LBE > 0	
Violations of RCB rules	
CRS response to non-configuration request	



**Table 20: Link and Flow Control Errors**

Error Details	Primary Reporting Mechanisms
Receiver Overflow on header or data	<ol style="list-style-type: none"> <li>1. "PCIe Uncorrectable Error Status Register" [RXO].</li> <li>2. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>3. Optional ERR_FATAL or ERR_NONFATAL message sent.</li> <li>4. "PCI Control and Status Register" [S_SERR] if error message is generated and [SERR_EN] is set in same register.</li> </ol>
Initial credits advertised are less than minimum	<ol style="list-style-type: none"> <li>1. "PCIe Uncorrectable Error Status Register" [FCPE].</li> </ol>
Received data credits > 2047, or header credits > 127	<ol style="list-style-type: none"> <li>2. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> </ol>
Initial infinite credit advertised, but subsequent UpdateFC contains non-zero credit value.	<ol style="list-style-type: none"> <li>3. Optional ERR_FATAL or ERR_NONFATAL message sent.</li> <li>4. "PCI Control and Status Register" [S_SERR] if error message is generated and [SERR_EN] is set in same register.</li> </ol>
Invalid (that is, non-outstanding) AckNack_Seq_Num in received Ack/Nak DLLP	<ol style="list-style-type: none"> <li>1. "PCIe Uncorrectable Error Status Register" [DLPE].</li> <li>2. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>3. Optional ERR_FATAL or ERR_NONFATAL message sent.</li> <li>4. "PCI Control and Status Register" [S_SERR] if error message is generated and [SERR_EN] is set same register.</li> </ol>
TLP ends with EDB, but LCRC is not inverted	<ol style="list-style-type: none"> <li>1. "PCIe Correctable Error Status Register" [B_TLP].</li> </ol>
TLP ends with END, but LCRC is incorrect	<ol style="list-style-type: none"> <li>2. "PCIe Device Control and Status Register" [COR_ERR_DTD].</li> </ol>
TLP ends with END, LCRC is correct, but has invalid	<ol style="list-style-type: none"> <li>3. Optional ERR_COR message sent.</li> </ol>
DLLP has invalid CRC	<ol style="list-style-type: none"> <li>1. "PCIe Correctable Error Status Register" [B_DLLP].</li> <li>2. "PCIe Device Control and Status Register" [COR_ERR_DTD].</li> <li>3. Optional ERR_COR message sent.</li> </ol>
Replay number rolls over	<ol style="list-style-type: none"> <li>1. "PCIe Correctable Error Status Register" [RN_RO].</li> <li>2. "PCIe Device Control and Status Register" [COR_ERR_DTD].</li> <li>3. Optional ERR_COR message sent.</li> </ol>
Replay timer expires	<ol style="list-style-type: none"> <li>1. "PCIe Correctable Error Status Register" [RT_TO].</li> <li>2. "PCIe Device Control and Status Register" [COR_ERR_DTD].</li> <li>3. Optional ERR_COR message sent.</li> </ol>

**Table 21: Uncorrectable Data/Address Errors**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
<b>PCIe as Originating Interface</b>		
Uncorrectable Data Error on the destination interface (PCI) while receiving an immediate response from the completer.	<ol style="list-style-type: none"> <li>1. "PCI Control and Status Register" [D_PE].</li> <li>2. PCI_PERRn is asserted on the PCI Interface if the [S_PERESP] is set in "PCI Bridge Control and Interrupt Register".</li> <li>3. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>4. "PCI Control and Status Register" [S_SERR] if an error message (Fatal/Non-Fatal) is generated and [S_SERR] is set in same register.</li> </ol>	<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [MDP_D] if "PCI Bridge Control and Interrupt Register" [S_PERESP] is set.</li> <li>2. "PCIe Secondary Uncorrectable Error Status Register" [UDERR].</li> </ol>
PCI_PERRn asserted on the PCI Interface while forwarding a non-posted write transaction from PCIe.	<ol style="list-style-type: none"> <li>1. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>2. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.</li> </ol>	<ol style="list-style-type: none"> <li>1. "PCIe Secondary Uncorrectable Error Status Register" [PERR_AD]</li> <li>2. "PCI Secondary Status and I/O Limit and Base Register" [MDP_D] if "PCI Bridge Control and Interrupt Register" [S_PERESP]</li> </ol>
PCI_PERRn asserted on the PCI Interface while forwarding a posted write transaction from PCIe.		<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [MDP_D] if "PCI Bridge Control and Interrupt Register" [S_PERESP]</li> <li>2. "PCIe Secondary Uncorrectable Error Status Register" [PERR_AD]</li> </ol>
PCI_SERRn detected on the PCI interface while forwarding transactions from PCIe.		<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [S_SERR].</li> <li>2. "PCIe Secondary Uncorrectable Error Status Register" [SERR_AD].</li> </ol>
<b>PCI as Originating Interface</b>		
Uncorrectable data error on a non-posted write transaction PCI mode.	<ol style="list-style-type: none"> <li>1. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>2. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.</li> </ol>	<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [D_PE].</li> <li>2. "PCIe Secondary Uncorrectable Error Status Register" [UDERR].</li> </ol>
Uncorrectable data error on a posted write transaction.	<ol style="list-style-type: none"> <li>1. If S_PERESP bit is set in "PCI Bridge Control and Interrupt Register", PERR# signal is asserted.</li> <li>2. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].</li> <li>3. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.</li> </ol>	<ol style="list-style-type: none"> <li>1. "PCI Secondary Status and I/O Limit and Base Register" [D_PE].</li> <li>2. "PCI Secondary Status and I/O Limit and Base Register" [MDP_D] if [S_PERESP] bit is set in the "PCI Bridge Control and Interrupt Register".</li> <li>3. "PCIe Secondary Uncorrectable Error Status Register" [UDERR].</li> </ol>

**Table 21: Uncorrectable Data/Address Errors (Continued)**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
Uncorrectable data error on PCI delayed read completions.	1. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].	1. "PCIe Secondary Uncorrectable Error Status Register" [PERR_AD]
Uncorrectable Address Error	2. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.	1. "PCI Secondary Status and I/O Limit and Base Register" [D_PE]. 2. "PCI Secondary Status and I/O Limit and Base Register" [S_TA]. 3. "PCIe Secondary Uncorrectable Error Status Register" [UADD_ERR].

**Table 22: Received Master/Target Abort Error**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
Master-Abort on the PCI bus while forwarding a posted write transaction from PCIe	1. "PCI Control and Status Register" [S_SERR] if R_MA Mask bit is clear in "PCIe Secondary Uncorrectable Error Mask Register" or MA_ERR bit is set in "PCI Bridge Control and Interrupt Register" and "PCI Control and Status Register" [SERR_EN] is set. 2. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD].	1. "PCI Secondary Status and I/O Limit and Base Register" [R_MA]. 2. "PCIe Secondary Uncorrectable Error Status Register" [R_MA].
Master-Abort on the PCI bus while forwarding a non-posted write transaction from PCIe	1. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD]. 2. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.	
Target-Abort on the PCI bus while forwarding a posted transaction from PCIe	1. "PCIe Device Control and Status Register" [FTL_ERR_DTD]/[NFTL_ERR_DTD]. 2. "PCI Control and Status Register" [S_SERR] if error message is sent and [SERR_EN] is set in same register.	1. "PCI Secondary Status and I/O Limit and Base Register" [R_TA]. 2. "PCIe Secondary Uncorrectable Error Status Register" [R_TA].
Target-Abort on the PCI bus while forwarding a non-posted transaction from PCIe		

**Table 23: Completion Errors**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
Completion received with Unsupported Request in response to a request originated by a secondary interface in PCI mode.	1. "PCI Control and Status Register" [R_MA].	1. "PCI Secondary Status and I/O Limit and Base Register" [S_TA] is set if [MA_ERR] bit in "PCI Bridge Control and Interrupt Register" is set.
Completion received with Completer Abort status on the PCIe link in response to a forwarded non-posted PCI transaction.	1. "PCI Control and Status Register" [R_TA].	1. "PCI Secondary Status and I/O Limit and Base Register" [S_TA].
Received Unexpected Completion Error	1. "PCIe Uncorrectable Error Status Register" [UXC] if not masked. 2. "PCIe Device Control and Status Register" [COR_ERR_DTD] if ANFE.	N/A
Completion Timeout Error	1. "PCIe Uncorrectable Error Status Register" [CTO] if not masked. 2. "PCIe Device Control and Status Register" [COR_ERR_DTD] if ANFE.	N/A

**Table 24: Request Errors**

Error Details	Primary Reporting Mechanism	Secondary Reporting Mechanism
Received vendor message (Type 0).	1. "PCIe Uncorrectable Error Status Register" [UR] if not masked. 2. "PCIe Device Control and Status Register" [UNS_REQ_DTD]. 3. "PCIe Device Control and Status Register" [COR_ERR_DTD] if ANFE.	N/A
Non-configuration or message received while in D1, D2 or D3 hot.		
Configuration Type 0 access with a non-zero function.		

## 10. Reset and Clocking

Topics discussed include the following:

- “Reset”
- “Clocking”

### 10.1 Reset

The PEB383 inputs resets from upstream devices, and drives reset to downstream devices. PCIE\_PERSTn is the reset input to the bridge, and is normally connected to a power-on reset controller at the system level. The PEB383 drives reset onto the PCI bus using PCI\_RSTn (see [Table 25](#)).

**Table 25: Reset Summary**

Reset Level	PCI Definition	Trigger	EEPROM Load	PEB383 Actions
0	Cold reset Warm reset	PCIE_PERSTn	Yes	<ul style="list-style-type: none"> <li>• Initialize all registers to known state (including sticky)</li> <li>• Drive and release PCI_RSTn 1 ms after PCIE_PERSTn is released</li> </ul>
1	Hot reset	Reset message or DL_down state	Yes	<ul style="list-style-type: none"> <li>• Initialize all registers to known state (except sticky)</li> <li>• Drive and release PCI_RSTn 1 ms after PEB383 is completed reset</li> </ul>
2	PCI bus reset	Set reset bit in CSR through configuration cycle	No	<ul style="list-style-type: none"> <li>• Hold PCI_RSTn low for 1 ms, or until bit is cleared by software, which ever is longer</li> <li>• Drain traffic</li> <li>• Drop request TLPs</li> <li>• Enumerate bus mode and clock speed (if clock master)</li> <li>• Do not initialize CSR</li> </ul>

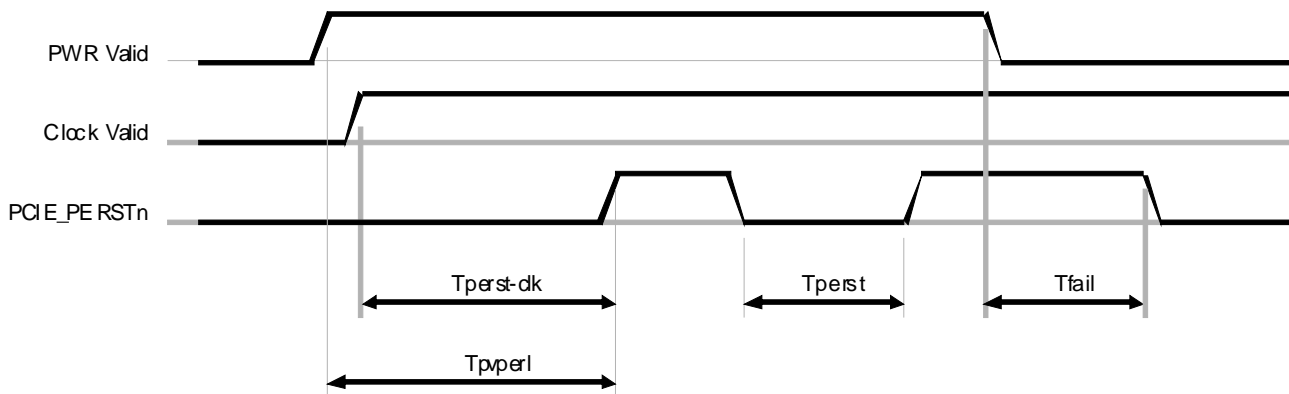
### 10.1.1 PCIe Link Reset

PCIe resets flow from upstream devices. The PCIe Interface is a slave to resets through a system-level power-on reset controller connected to PCIE\_PERSTn, or through inband messages from the root complex. After release of reset the external EEPROM is loaded. During the loading process, configuration requests will receive a “configuration request retry status” completion status.

#### 10.1.1.1 Cold Reset – Level 0

A cold reset is applied after power up. This is a traditional power-on reset that is generally driven at the system level by a power-on reset controller. After release of PCIE\_PERSTn, all of PEB383’s registers are in their power-on reset state, including sticky bits. Clock (PCIE\_REFCLK\_n/p) and power must be valid prior to the release of PCIE\_PERSTn. The timing diagram for a cold reset is displayed in [Figure 25](#), while its values are listed in [Table 26](#).

**Figure 25: Reset Timing**



**Table 26: Reset Timing**

Parameter	Value	Min./Max.	Description
$T_{pvperl}$	10 ms	Minimum	Power valid to release of reset
$T_{perst-clk}$	10 ms	Minimum	Clock valid to releases of reset
$T_{perst}$	1 ms	Minimum	Minimum pulse for reset (warm reset)
$T_{fail}$	1 ms	Maximum	Time to assert reset after power is not valid

#### 10.1.1.2 Warm Reset – Level 0

A warm reset occurs without cycling power. This is achieved by bringing PCIE\_PERSTn low for the minimum specified time,  $T_{perst}$ . After release of PCIE\_PERSTn, all of PEB383’s registers are in there power-on reset state, including sticky bits.

### 10.1.1.3 Hot Reset – Level 1

A hot reset is triggered by an in-band message from the root complex over the PCIe link. After application of hot reset, all registers are in their power-on reset state, except sticky bits which maintain their pre-reset values in order to aid in system diagnostics.

A hot reset is also be initiated during a DL\_down condition. DL\_down means that the PEB383 has lost communications at the physical or data link layer with the upstream device.

### 10.1.2 PCI Bus Reset

The PEB383 drives reset on the PCI bus using PCI\_RSTn. There are four conditions that cause the bridge to drive reset onto the PCI bus:

1. Assertion of PCIE\_PERSTn (cold/warm reset)
2. Receipt of a hot reset message on the PCIe link (hot reset)
3. PCIe link going into a DL\_down state (hot reset)
4. Setting the PCI bus reset bit, S\_RESET, in the “PCI Bridge Control and Interrupt Register” (level 2).

Software must ensure there are no requests pending in the device buffers before setting the PCI reset bit. If software fails to do so, the PEB383 drains its buffers as follows.

- Drops all upstream requests and associated completions pending in the PCI Core buffers. Requests pending in PCIe core buffers, however, are transmitted normally.
- Drops all downstream requests and returns the credits, and also returns completions with UR completion status for non-posted requests.

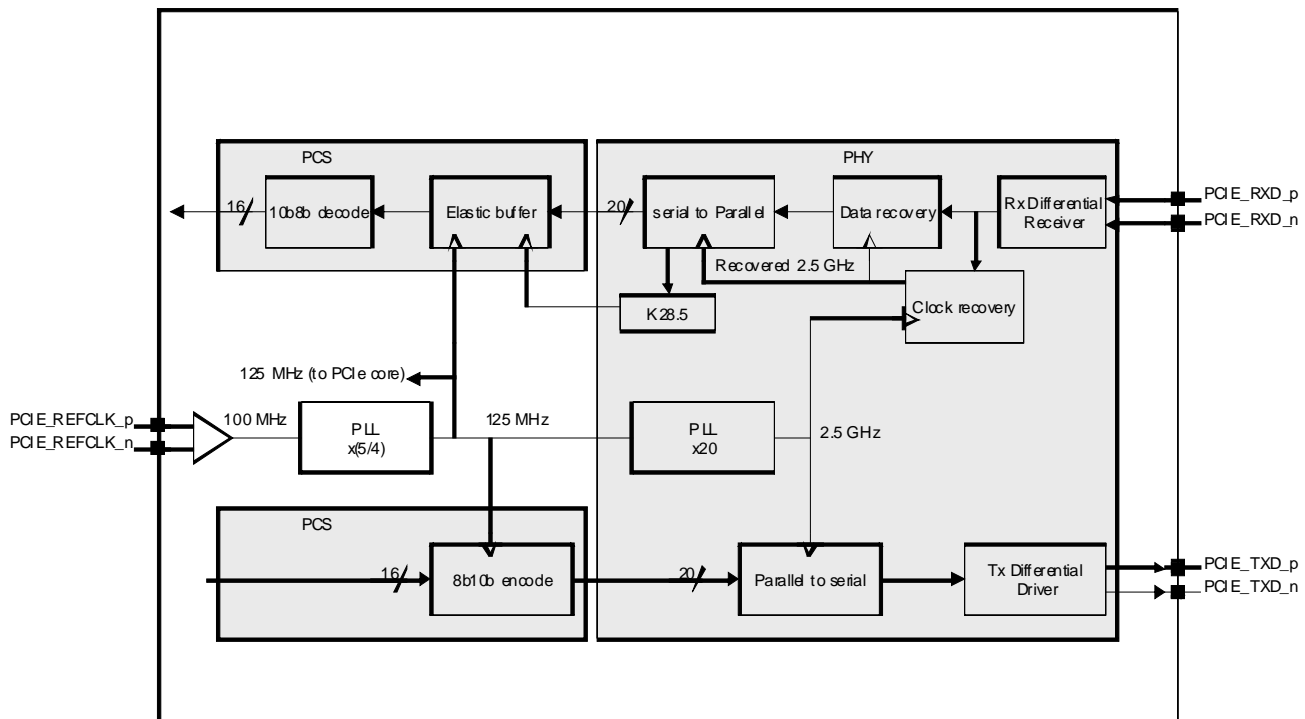
## 10.2 Clocking

This section discusses clocking information for the PEB383's PCIe and PCI Interfaces.

### 10.2.1 PCIe Clocking

The PCIe clocking is shown in **Figure 26**. The 100-MHz reference clock, PCIE\_REFCLK\_n/p, drives a  $\times(5/4)$  PLL to create a 125-MHz clock. The 125-MHz clock is further multiplied to create the Tx parallel to serial conversion, and clocking out the Tx pins, PCIE\_TXD\_n/p (The receive data is clocked into the PEB383 with the recovered clock. The elastic buffer operates on the recovered byte clock (from K28.5) and the internal generated 125-MHz clock. The two clocks can vary by twice the ppm tolerance of the reference clock tolerance on any one device (300ppm). Buffer overflow is prevented by discarding skip characters.

**Figure 26: PCIe Clocking**

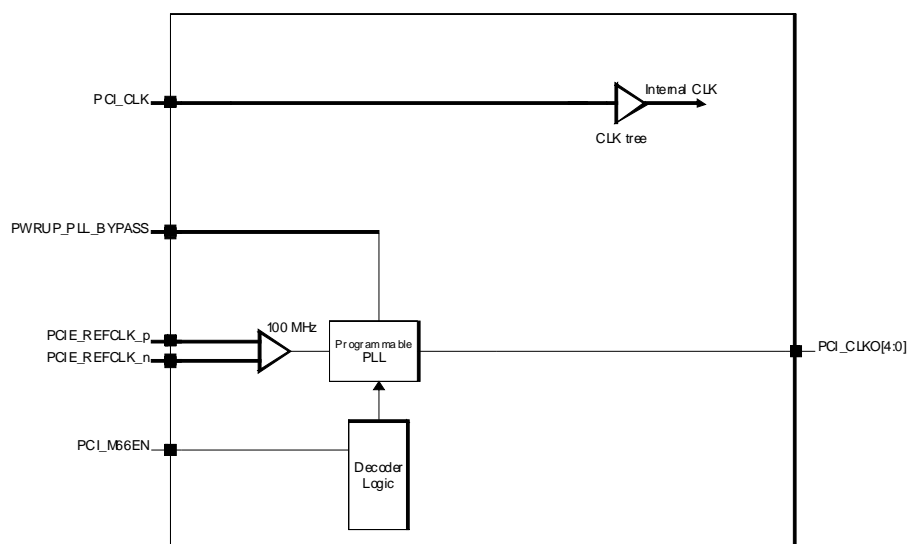




## 10.2.2 PCI Clocking

The PCI clocking for the PEB383 is shown in [Figure 27](#). The PEB383 supports clock master and slave mode, and is configured by the PCB design. The bridge drives up to four external clocks, PCI\_CLKO[3:0], which are individually enabled through the “[Clock Out Enable Function and Debug Register](#)”. PCI\_CLKO[4] can be used for external clock compensation.

**Figure 27: PCI Clocking**



### 10.2.2.1 Master Mode Clocking

Master mode clocking is provided by the PEB383. PCI\_CLKO[4:0] is generated from PCIE\_REFCLK and a programmable PLL. The decoder sets the divider ratios for programmable PLL as a function of PCI\_M66EN, and the “[PCI Miscellaneous Clock Straps Register](#)”. PCI\_M66EN selects 66 MHz when high, and 33 MHz when low. The “[PCI Miscellaneous Clock Straps Register](#)” allows this pin to be overwritten, and one of the following speeds used: 25, 33, 50, and 66 MHz.

Prior to the configuration of the PCI bus speed, the PCI clock is in bypass mode, which generates a 25-MHz clock on the PCI bus. After the release of reset, the PLL locks to a new frequency based on the value of the PCI\_M66EN signal (see [Table 27](#)).

**Table 27: PCI Clocking**

PCI Bus Rate	PCI_M66EN Signal
25 MHz	Requires software configuration <sup>a</sup>
33 MHz	0
50 MHz	Requires software configuration
66 MHz	1

- a. This setting is based on the value of CS\_MODE in the “PCI Miscellaneous Clock Straps Register”.

PCI\_CLKO[3:0] are connected to PCI devices, while PCI\_CLKO[4] is connected to the PCI\_CLK signal. The track length of the clock nets should be matched in length.

#### **10.2.2.2 Slave Mode Clocking**

In slave clocking, PCI\_CLKO[0] is disabled through the “Clock Out Enable Function and Debug Register”, and an external clock source drives the PEB383 (using PCI\_CLK) and the PCI devices.

---

# 11. Power Management

Topics discussed include the following:

- “Overview”
  - “Power Management Capabilities”
  - “Power States”
- 

## 11.1 Overview

The PEB383 provides basic power management support to its PCI bus and PCIe link. PCI power management states are mapped to specific PCIe link states. The bridge also supports Active State Power Management (ASPM), where the device enters into power saving state and initiates exit when needed. The PEB383 transmits power management messages during power management events.

The Power Management (PM) module connects with the Physical Layer sub block to transition the Link State into low-power states when it receives a power state change request from an upstream component, or when an internal event forces the link state entry into low-power states in ASPM. PCIe link states are not visible directly to legacy bus driver software but are derived from the Power Management state of the components residing on those links. Power saving increases as Link state transitions from L0 through L3.

### 11.1.1 Features

- Compliant with the *PCI Bus Power Management Interface Specification (Revision 1.2)*
- Supports the following PCI device power states:
  - D0
  - D3 hot
  - D3 cold
- Supports the following PCIe link power states:
  - L0
  - L0s
  - L1
  - L2/3 ready
  - L3

### 11.1.2 Unsupported Features

- PCI power states: D1 and D2
- PCIe link states: L2
- PCI bus states
- WAKE# to beacon
- PME in D3<sub>cold</sub>
- Auxiliary power

## 11.2 Power Management Capabilities

The PEB383 supports software driven D-state power management: D0, D3Hot, and D3Cold. It supports L0s state in Active state power management method; L0s entry should be enabled through configuration of ASPM\_CTL in the “PCIe Link Control Register”. It also support L1, L2/L3 Ready and L3 PCIe power saving link states.

Since the PEB383 does not support Auxiliary power it does not support power management events in the D3Cold state. The PEB383 enters into link power management states in response to the software driven D-state.

The power management related registers reside at “PCI Power Management Capability Register” and “PCI Power Management Control and Status Register”.

## 11.3 Power States

This section discusses the PEB383’s support of PCI and PCIe power states.

### 11.3.1 ASPM

Active state power management, or ASPM, enables power savings even when the PEB383 is in the D0 state. After a period of idle link time, the ASPM function engages the physical layer protocol that places idle link in the power saving state. Once in the lower power state, transitions to the fully operative L0 state can be triggered by transactions from the PCIe or PCI Interface. The L0/L1 entry capability of the PEB383 is determined by the Root Complex reading the PEB383 configuration space “PCIe Link Capabilities Register”. The Root Complex can enable entry into this state through configuration. L0s is not applicable to the PCI-PM compatible power management.

All main power supplies, component reference clocks, and component internal PLLs, must be active at all time during L0s. DLLP and TLP transmission through the PEB383 in L0s is prohibited. The PEB383’s PCIe Transmit module can be in L0s state while the Transmit module of the other device on the PCIe link is in the L0 state. In the PEB383, L0s entry is disabled by default. When L0s entry is enabled and the PEB383 Transmit module is in idle state for more then 6 micro seconds – that is, there is no transmission of packets for 6 micro seconds – the PEB383 Transmit module enters the L0s state. The bridge initiates exit from the L0s state when it has pending TLPs or DLLPs for transmission. The ASPM function of the PEB383 does support L1 entry.

### 11.3.2 L0 State

This is the normal operational mode.

### 11.3.3 L0s State

A low resume latency, energy-saving standby state. L0s support is required for ASPM. It is not applicable to PCI-PM compatible power management.

### 11.3.4 L1 State

L1 is a high latency and low-power standby state. It is required for PCI-PM compatible power management. The PEB383 does support L1 entry in ASPM. The L1 may be entered whenever the bridge is programmed to a D3 state. L1 is also entered by ASPM when there is no pending packet to transmit for 10us. TLP and DLLP communication over the link is prohibited when the PEB383 is in the L1 state. L1 exit can be initiated by the PEB383 or an upstream device.

### 11.3.5 L2/L3 Ready

The L2/L3 Ready state is a staging point for the L2 or L3 states. The process is initiated after the PM module software transitions the PEB383 into the D3 state and requests power management software to initiate the removal of power and clocks. After the PCIe link enters the L2/L3 Ready state the PEB383 is ready for power removal. TLP and DLLP communication over link cannot occur while the PEB383 is in this state. It is also possible to remove power without first placing the PEB383 in the D3Hot state. System software causes the root complex to broadcast the PME\_Turn\_Off message in preparation for removing the main power source, and the PEB383 responds in order to complete entry into the L2/L3 Ready state.

### 11.3.6 L3 State

When the PEB383 is in L2/L3 Ready state, the removal of main power and clocks places the device into the L3 state. The PEB383 does not support auxiliary power, therefore L2 power management state is not supported.

### 11.3.7 LDn State

This is a PCIe link down pseudo state prior to L0.

### 11.3.8 Link State Summary

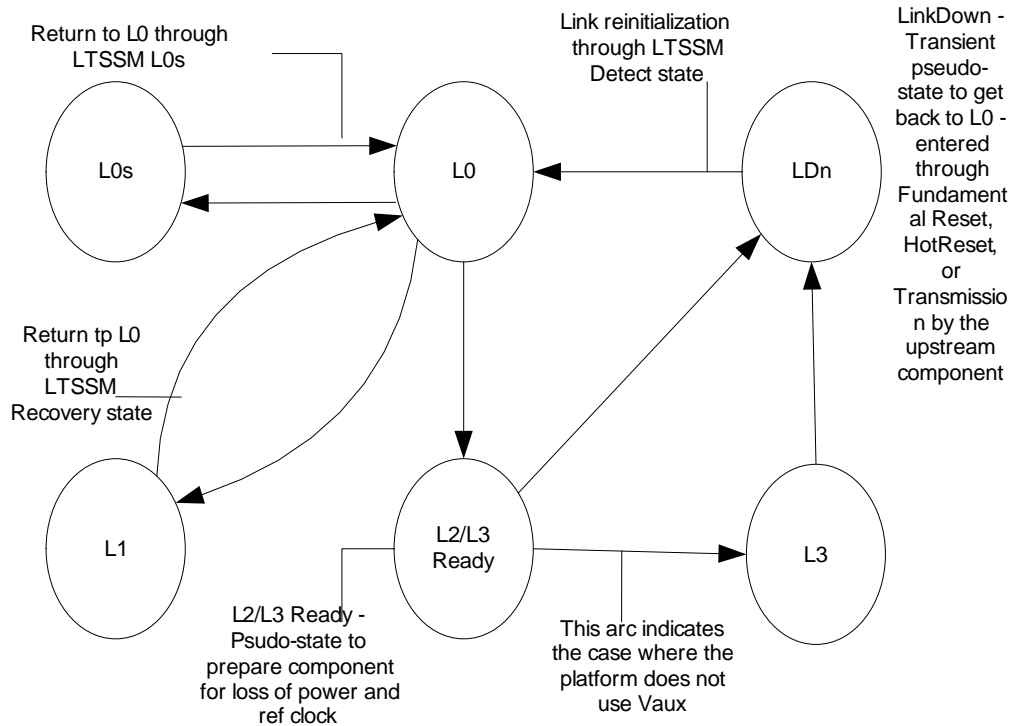
The link states are summarized in [Table 28](#).

**Table 28: PCIe Link States**

L state	Description	Software directed PM	ASPM	100-MHz Reference	Power	internal PLL
L0	Fully active link	Yes (D0)	Yes (D0)	On	On	On
L0s	Standby state	No	Yes (D0)	On	On	On
L1	Low-power standby	Yes (D3 <sub>hot</sub> )	Yes	On	On	On
L2/L3 ready	Stagging point for power removal	Yes	No	On	On	On
L3	Off	N/A	N/A	Off	Off	Off

The link state diagram is shown in [Figure 28](#).

**Figure 28: PCIe Link Power Management States**



### 11.3.9 Device Power States

The PEB383 supports the PCIe PCI-PM D0, D3Hot, and D3Cold (no Auxiliary power) device power management states. The bridge does not support the D1 and D2 power management states.

#### 11.3.10 D0 State

D0 is divided into two distinct sub states: the uninitialized sub-state and the active sub-state. When power is initially applied to the PEB383, it enters the D0\_uninitialized state. The bridge enters the D0\_active state when either of the following is set by system software:

- Memory space enable
- I/O space enable
- Bus Master enable

#### 11.3.11 D3<sub>Hot</sub> State

A device that is in the D3Hot state must be able to respond to configuration accesses so that it can be moved to the D0\_uninitialized state by software through configuration. Once in the D3Hot state, the device can later be transitioned into the D3Cold state by removing power from the device. D3Hot is a useful state for reducing power consumption by idle components in an otherwise running system.

Once the PEB383 is programmed to the D3Hot state, it initiates L1 entry process. The NO\_SOFT\_RST bit in the “PCI Power Management Control and Status Register” is set to 1 in the PEB383 when software programs the bridge back to the D0 state. L1 exit can be initiated by the PEB383 or an upstream device.

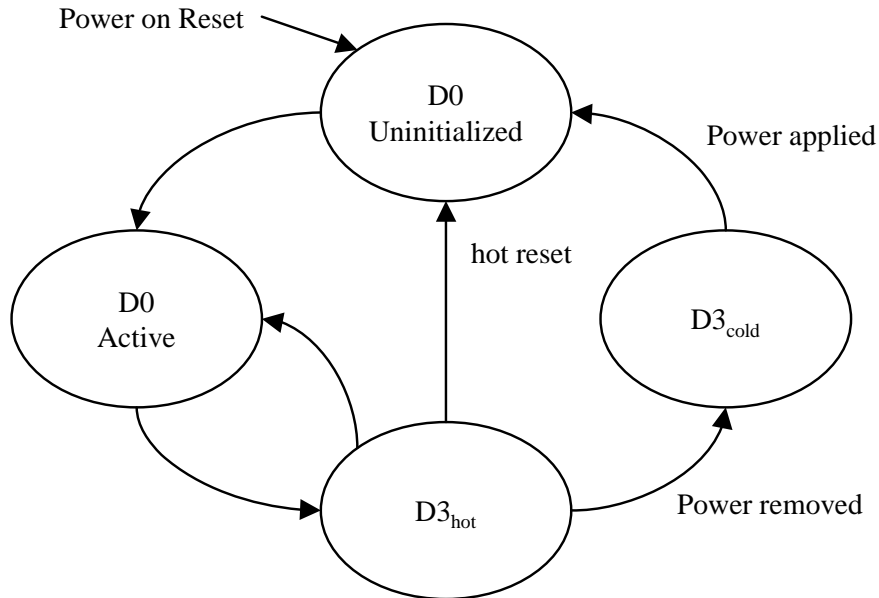
#### 11.3.12 D3<sub>Cold</sub> State

The PEB383 transitions to the D3Cold state when its power is removed. Re-applying power causes the device to transition from the D3Cold state into the D0\_uninitialized state. The D3Cold state assumes that all previous contexts are lost, so software must save the necessary context while the device is still in the D3Hot state. A power-on sequence with its associated cold reset transitions the PEB383 from the D3Cold state to the D0 uninitialized state. Software must perform a full initialization of the PEB383 in order to restore the function to its D0 active state.

### 11.3.13 D State Transitions

The device power state transitions are shown in Figure 29. Software is responsible for controlling the state diagram through PWR\_ST in the “PCI Power Management Control and Status Register”.

**Figure 29: D State Transitions**



### 11.3.14 Power Management Event

Power management events are generated by the PEB383 as a means of requesting a PM state change. The PEB383 sends a PM\_PME message to the root complex during a power management event. The bridge does not support a wake-up function through Beacon and WAKE#. It does not support PME generation from the D3Cold state since the PEB383 does not support Auxiliary power. A PM\_PME message are posted TLP packets that are always routed in the direction of the root complex. To send a PM\_PME message on its upstream link, the PEB383 must transition the link to the L0 state if the link is not already in the L0 state. The PCI\_PME<sub>en</sub> pin is sampled every 100 microseconds for PM\_PME message generation.



### 11.3.15 Power State Summary

The state summary is shown in [Table 29](#).

**Table 29: Power Management State Summary**

PEB383 State	Link State	Upstream State	PCI Bus	Description
D0	L0	D0	Operational	Fully operational
D0	L0s	D0	Operational	PCIe link in standby
D0	L1	D0	Operational	PCIe Link in L1
D3 <sub>hot</sub>	L0	D3 <sub>hot</sub> -D0	PME only <sup>a</sup>	PEB383 sending PME message when in D3 <sub>hot</sub> or when injecting a PME_TO_Ack TLP when PEB383 transitions between L1 and L2/L3 ready.
D3 <sub>hot</sub>	L1	D3 <sub>hot</sub> -D0	PME only	Power saving mode, or waiting to transition to L2/L3 ready
D3 <sub>hot</sub>	L2/L3 ready	D3 <sub>hot</sub> -D0	Not operational	Ready to remove power, will not respond to PME
D3 <sub>cold</sub>	N/A	D3 <sub>cold</sub> -D0	N/A	Power removed

- a. The PEB383 drives PCI\_CLKO[4:0], does not assert PCI\_RSTn, responds to PCI\_PME<sub>n</sub>, does not participate in bus transactions.

## 11.4 Power Saving Modes

The PEB383 provides several low power modes of operation, as described in [Table 30](#).

**Table 30: Power saving modes**

Input Conditions					power saving activities		
Mode	state	ASPM <sup>a</sup>	PCI_CLK[3:0] gate enable <sup>b</sup>	traffic	PCI_CLK[3:0]	link state	internal clock
1	DO	X	X	active	on	L0	on
2	DO	none	X	idle	on	L0	on
3	DO	L0s	X	idle	on	L0s	on
4	DO	L1	X	idle	on	L1	gated
5	D3_hot	X	no	idle	on	L1	gated
6	D3_hot	X	yes	idle	gated	L1	gated

a. ASPM enabled via “ASPM\_CTL” bit of “[PCIe Link Control Register](#)”

b. PCI\_CLK[3:0] gating enabled via “PCGE” bit “[PCI Miscellaneous Clock Straps Register](#)”

Mode1 is fully operational, no power saving modes used.

Mode2 has ASPM disabled, no power saving modes used.

Mode3 Has ASPM L0s enabled, link power is saved.

Mode4 has ASPM L1 enabled, additional link power is saved, and internal core logic clock is gated for additional power savings

Mode5 is D3\_hot, link is in L1, and internal clock is gated

Mode6 is D3\_hot, link in L1, internal clock is gated, and external PCI\_CLK[3:0] is gated.

---

## 12. Serial EEPROM

Topics discussed include the following:

- “Overview”
- “System Diagram”
- “EEPROM Image”
- “Functional Timing”

---

### 12.1 Overview

The PEB383 uses an internal serial EEPROM Controller to configure its configuration space register (CSR) block with the values stored in an external serial EEPROM. The Controller is compatible with EEPROM devices that use the Serial Peripheral Interface, such as the Atmel AT25010A, AT25020A, AT25040A, AT25080A, AT25160A, AT25320A, and AT25640A.

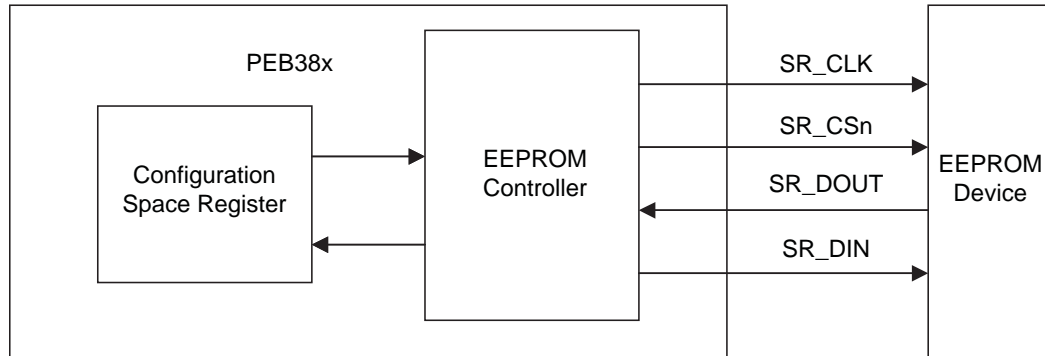
The primary purpose of the EEPROM Controller is to modify some of the default values of the Read-only and Read/Write registers in the PEB383’s CSR space (for more information, see “[Register Descriptions](#)”). After reset is de-asserted, the Controller initiates the read instructions to the external EEPROM and reads its contents. If an EEPROM is present the Controller writes its data into the PEB383’s register space depending on the offset address provided in the EEPROM location.

The EEPROM Controller can write data into an external EEPROM using the “[EEPROM Control Register](#)”. It supports 9-bit and 16-bit addressing modes to read and write the external EEPROM.

## 12.2 System Diagram

Figure 30 shows the EEPROM Controller interfacing an external EEPROM to the PEB383 configuration space.

Figure 30: EEPROM Interface



The PEB383 internal clock block generates an EEPROM clock of 7.8 MHz to supply to the external EEPROM. This clock is derived from the PCIe clock of frequency 125 MHz.

The first two locations in the EEPROM – byte address 0x0000 and 0x0001 – contain the identification code. The next two locations contain the byte count, which indicates the number of bytes to be read from the EEPROM locations. After this, the next two locations of the EEPROM contain the CSR address, and the byte enables to indicate the valid byte locations to be loaded from the EEPROM. The next four locations after this contain the 4 bytes of data to be loaded into configuration space. Thereafter, the data structure is maintained in the EEPROM, per register, as 2 bytes of address and byte enables followed by 4 bytes of data. Therefore, the value in the third and fourth locations of the EEPROM, which is the byte count, should always be a multiple of 6 since 6 bytes of information (which includes address, byte enables, and data) is required to program one CSR register. Table 31 describes the data structure to be maintained by the external EEPROM.



If the byte count value is programmed to 0 or greater and is a non-multiple of 6, then the EEPROM Controller rounds up this value to the next nearest value (which is a multiple of 6). The EEPROM Controller then proceeds to program the CSR as per this new byte count value.

After the reset is de-asserted, the EEPROM Controller initiates a read of the first two locations of the external EEPROM to get the identification code. The identification code must be 0x28AB. Initially, it initiates a read transaction with 9-bit address, and reads the identification code. If the identification code results in a wrong value – that is, other than above value – then it initiates another read transaction with a 16-bit address to read the identification code. If the value read is other than the identification code, then it determines that an EEPROM is not present. It then sets this information in ADD\_WIDTH of the “EEPROM Control Register”, and aborts the programming of the configuration space by signaling the completion of the loading.



If a blank EEPROM is used, the ADD\_WIDTH bits in the “EEPROM Control Register” must be written with the correct bit pattern for the type of EEPROM *before* accessing the EEPROM.

If the identification code obtained through the first read is a correct value, then the EEPROM Controller determines that the EEPROM supports 9-bit addressing. The Controller then initiates one more read transaction to read the third and fourth locations of the EEPROM, where the value of the total number of bytes to be read (byte count) is located. Thereafter, it continuously reads all the bytes and programs the CSR registers depending on the address provided in the EEPROM location. The PEB383 has now determined the EEPROM Controller supports 9-bit addressing (it uses this mode for writes as well).

If the identification code read after first read is a wrong value, and after the second read is a correct value, then it initiates one more read transaction to get the value of total number of bytes to be read (byte count). Thereafter it reads all the bytes from the EEPROM locations and programs the CSR registers according to the addresses given in the EEPROM locations. The PEB383 has now determined the EEPROM Controller supports 16-bit addressing (it uses this mode for writes as well).

In both cases just discussed, the Controller updates the “**EEPROM Control Register**” with the address width of the EEPROM detected and signals the completion of the loading to the CSR block. During the process of programming the CSR by the EEPROM, any configuration transactions on the PCIe Interface that are initiated by the root complex are completed with CRRS completions (Configuration Request Retry Status completions). All other transactions are completed with UR completions.

The root complex can access the external EEPROM through the EEPROM Controller; that is, EEPROM locations can be written and read by the root complex. The root complex initiates configuration write transactions to program the “**EEPROM Control Register**” using a write command. The EEPROM Controller initiates a WREN (Write Enable) instruction first, followed by a WRITE instruction. The Controller sets the BUSY bit in the register when it initiates a write instruction to the external EEPROM. It obtains the status of the write cycle from the external EEPROM by initiating RDSR (Read Status Register) instruction to it after every write instruction. If the external EEPROM finishes the write operation it would return the status in the form of BUSY bit as 1'b0. This information from the external EEPROM is updated in the “**EEPROM Control Register**”; that is, this bit would reset once the external EEPROM completes the WRITE operation. Therefore, software should poll this bit to get BUSY status before initiating another transaction to the serial EEPROM. As a result, this bit should indicate 1'b0 before initiating any other instruction to the external EEPROM. Software should ensure that the CMD\_VLD bit in this register is high in order to trigger the EEPROM Controller to initiate Read/Write instructions. If a configuration write is initiated to overwrite the command in the “**EEPROM Control Register**” during the busy state, the EEPROM Controller will ignore the command.

To read the EEPROM location, the root complex initiates a configuration write transaction to the “**EEPROM Control Register**” with the READ command; this prompts the EEPROM to initiate a READ instruction to the external EEPROM.



The EEPROM Controller does not support the WRDI (Write Disable) and WRSR (Write Status Register) instructions.

When the PCIe reset signal is asserted, all the CSR register values are set to their default values. When this reset is de-asserted, the EEPROM Controller starts the EEPROM loading process in order to re-program its CSR registers.

## 12.3 EEPROM Image

The data structure to be maintained in the external EEPROM for successful operation of the EEPROM Controller is shown in [Table 31](#). Note that the *m* and *n* in the Description column indicate the register number: they can point to any register in the entire CSR space.

The byte enable[3:0] is active high; a 1 enables the byte. For example, a byte enable of 0b0001 would enable the low order byte, bits[7:0] of the DWORD.

**Table 31: EEPROM Image**

Serial EEPROM Location	Description	Value
0000h	Identification code [7:0]	0xAB
0001h	Identification code [15:8]	0x28
0002h	Byte count [7:0]	Any value
0003h	Byte count [15:8]	Any value, but total value of Byte count[15:0] should be multiple of 6
0004h	CSR register m Address [7:0]	Any number
0005h	CSR register m byte enable [3:0], CSR register m Address [11:8]	Any number
0006h	CSR register m Data [7:0]	Any number
0007h	CSR register m Data [15:8]	Any number
0008h	CSR register m Data [23:16]	Any number
0009h	CSR register m Data [31:24]	Any number
000Ah	CSR register n Address [7:0]	Any number
000Bh	CSR register n byte enable [3:0], CSR register n Address [11:8]	Any number
000Ch	CSR register n Data [7:0]	Any number
000Dh	CSR register n Data [15:8]	Any number
000Eh	CSR register n Data [23:16]	Any number
000Fh	CSR register n Data [31:24]	Any number
...	...	...
FFFAh	CSR register r Address [7:0]	Any number
FFFBh	CSR register r byte enable [3:0], CSR register r Address [11:8]	Any number
FFFCh	CSR register r Data [7:0]	Any number
FFFDh	CSR register r Data [15:8]	Any number

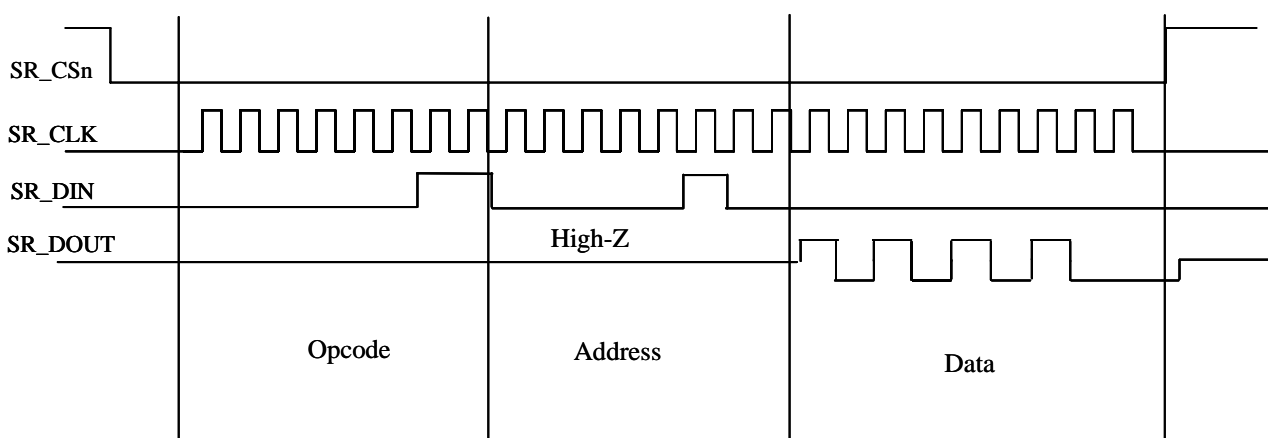
**Table 31: EEPROM Image (Continued)**

Serial EEPROM Location	Description	Value
FFFEh	CSR register r Data [23:16]	Any number
FFFFh	CSR register r Data [31:24]	Any number

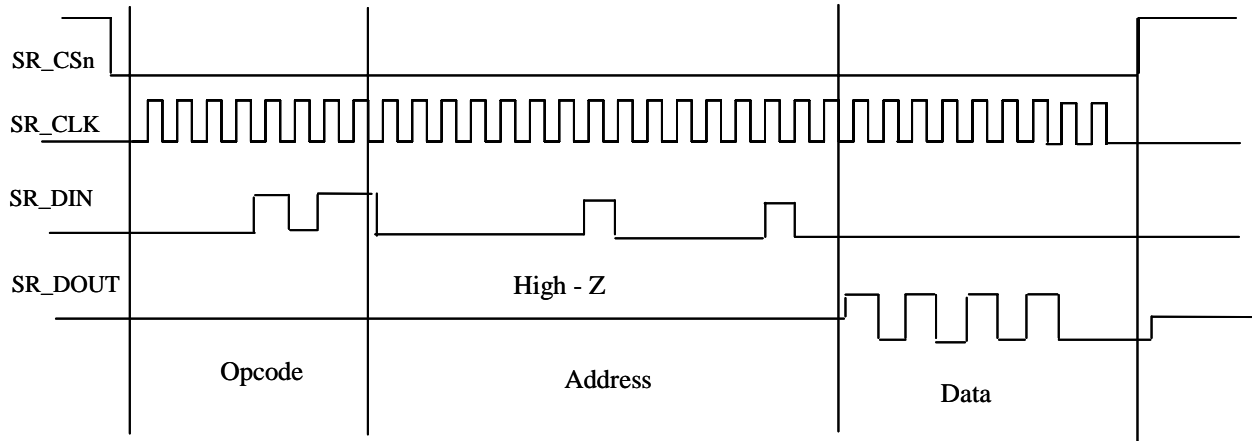
## 12.4 Functional Timing

The EEPROM Controller outputs the data on the SR\_DIN signal on every negative edge of the SR\_CLK clock. The external EEPROM samples this output on every positive edge of SR\_CLK. Similarly, the external EEPROM outputs the data on SR\_DOUT on every negative edge of SR\_CLK, while the Controller samples it on every positive edge of the clock.

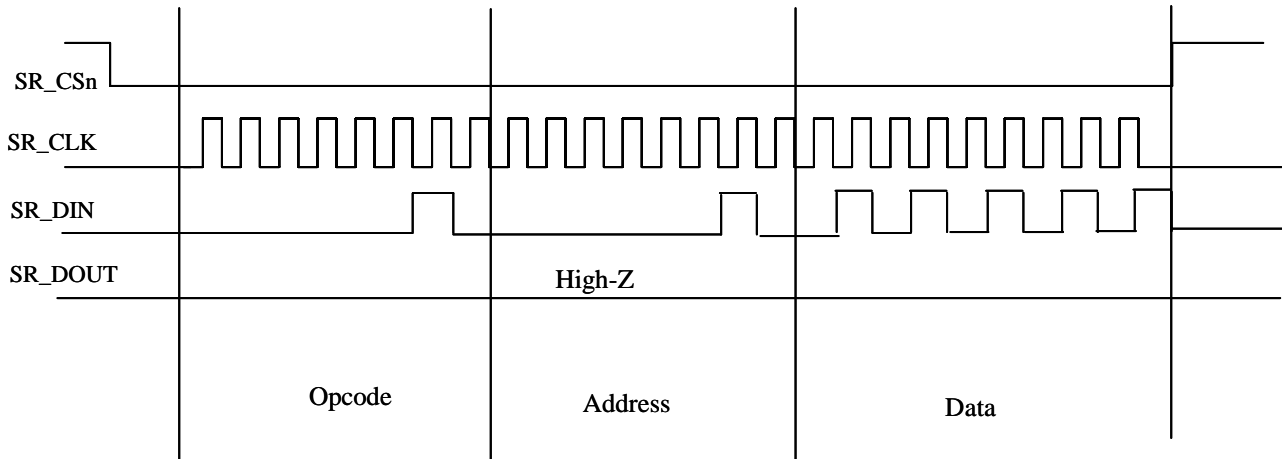
For read or write instructions in support of addresses greater than 0xFFH (in 9-bit addressing mode), the 8th bit of the address is transmitted in place of the third bit of the opcode of that instruction; thus, the address phase consists of 8 clock cycles. The timing for different instructions of the EEPROM Controller are provided in the following figures.

**Figure 31: 9-bit EEPROM Read Timing**

**Figure 32: 16-bit EEPROM Read Timing**

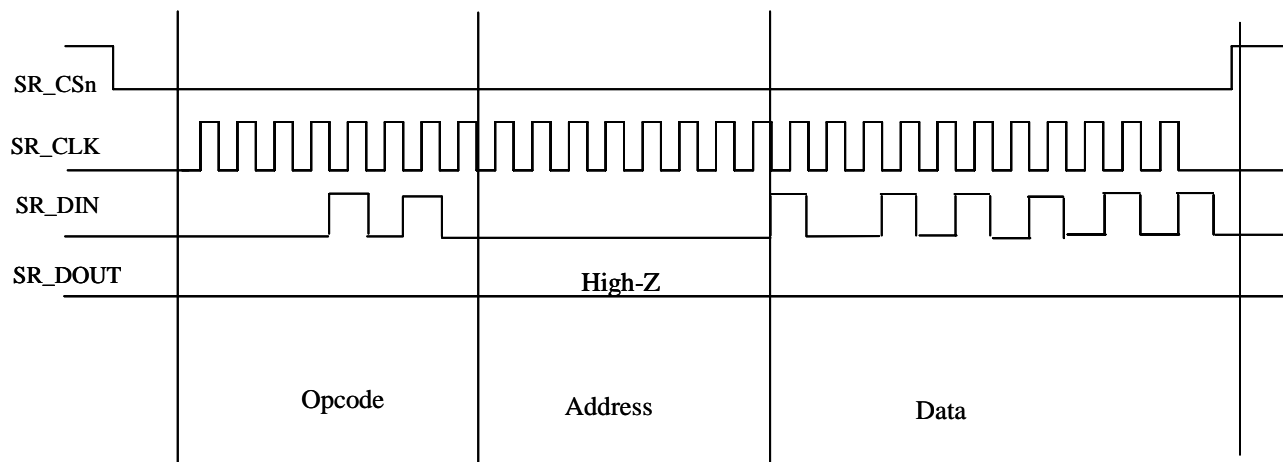


**Figure 33: 9-bit EEPROM Write Timing**

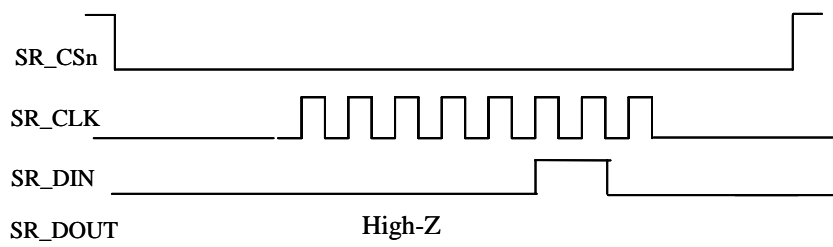




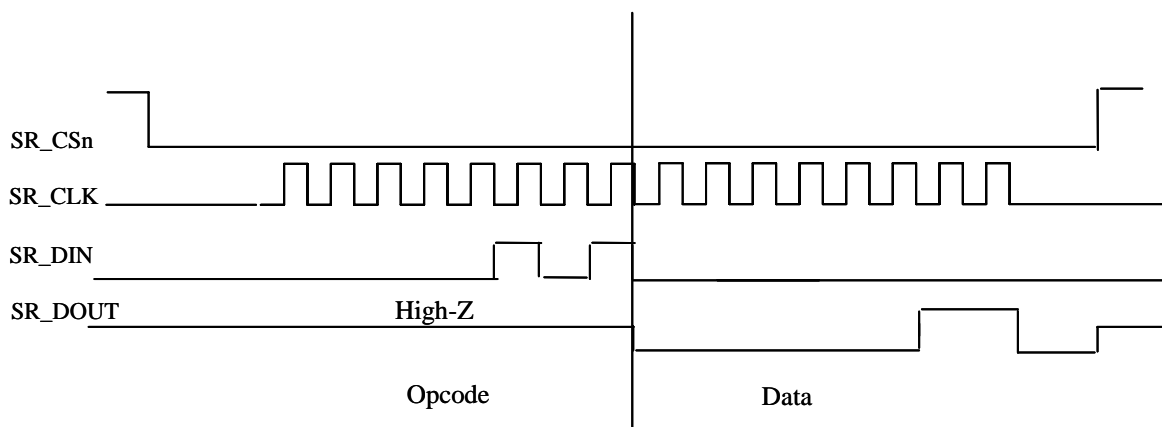
**Figure 34: 16-bit EEPROM Write Timing**



**Figure 35: EEPROM WREN Instruction Timing**



**Figure 36: EEPROM RDSR Instruction Timing**



Note: RDSR means Read Status Register Instruction.



---

## 13. JTAG

Topics discussed include the following:

- “Overview”
- “TAP Controller Initialization”
- “Instruction Register”
- “Bypass Register”
- “JTAG Device ID Register”
- “JTAG Register Access”
- “Dedicated Test Pins”
- “Accessing SerDes TAP Controller”

---

### 13.1 Overview

The JTAG Interface is compliant with IEEE 1149.6 *Boundary Scan Testing of Advanced Digital Networks*, as well as IEEE 1149.1 *Standard Test Access Port and Boundary Scan Architecture* standards. There are five standard pins associated with the interface (JTAG\_TMS, JTAG\_TCK, JTAG\_TDI, JTAG\_TDO, and JTAG\_TRSTn) that allow full control of the internal TAP (Test Access Port) controller.

The JTAG Interface has the following features:

- Contains a 5-pin Test Access Port (TAP) controller, with support for the following registers
  - Instruction register (IR)
  - Boundary scan register
  - Bypass register
  - Device ID register
  - User test data register (DR)
- Supports debug access of the PEB383's configuration registers
  - During mission mode or not
  - Bus arbitration with configuration cycles
- Supports the following instruction opcodes
  - Sample/Preload
  - Extest
  - EXTEST\_PULSE (1149.6)
  - EXTEST\_TRAIN (1149.6)

- Bypass
- IDCODE
- Clamp
- User data select

## 13.2 TAP Controller Initialization

After power-up of the PEB383, the TAP controller must be put into its test-logic-reset state to disable the JTAG logic and allow the bridge to function normally. This can be completed by driving the JTAG\_TMS signal high and pulsing the JTAG\_TCK signal five or more times, or by asserting the JTAG\_TRSTn signal.

## 13.3 Instruction Register

The PEB383 uses an Instruction register to control the operation of the JTAG logic. Bit combinations that are not equivalent to any instruction are equivalent to the BYPASS instruction.

## 13.4 Bypass Register

This register is a 1-bit shift register that provides a single bit scan path between the JTAG\_TDI input and the JTAG\_TDO output. This abbreviated scan path is selected by the BYPASS instruction code, and is used to shorten the overall scan ring length during board-level testing when the PEB383 is not involved.

## 13.5 JTAG Device ID Register

The JTAG device identification number for the PEB383 is as follows:

- Version [31:28] – 0000
- Part number [27:12] – 0000\_0011\_1000\_0011
- Manufacturer identity [11:1] – 000\_1011\_0011
- Mandatory LSB [0] – 1

## 13.6 JTAG Register Access

The JTAG Interface can be used for debug purposes in order to perform read and write access of the PEB383's configuration registers. It also can perform read accesses on the performance registers without impacting active transactions.

A user-defined command enables the read and write capabilities of the JTAG Interface. This is in the User Test Data Register (DR) set in the PEB383.



For more information about the test data register, see Test Technology Standards Committee: IEEE Computer Society, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std. 1149.1-1990, 1149.1a-1993, October, 1993., Section 8.3.

### 13.6.1 Register Access from JTAG

The format for access the PEB383's DR register using JTAG is shown in the following figures. The same DR register is used for read and write access.

**Figure 37: Read/Write Access from JTAG — Serial Data In**



**Figure 38: Observe from JTAG — Serial Data Out**



### 13.6.2 Write Access to Registers from the JTAG Interface

Complete the following steps to write to a device register through the JTAG Interface:

1. Move to the TAP controller “Shift-IR” state and program the instruction register with the instruction of the DR by writing into Instruction Register bits with 0xFFFF\_FFFF\_FFFF\_FFFD.
2. Move to the “Shift-DR” state and shift the data[31:0], R/W = 1 and the address[9:0] serially in the TDI pin. To prevent corruption of unused bits, the full DR bits have to be written as follows (see also [Figure 37](#)):
  - DR[66:62] = 5b'0
  - DR[61:52] = ADDR[9:0]<sup>1</sup>
  - DR[51] = R/W
  - DR[50:19] = DATA[31:0]
  - DR[18:17] = 2b'0

1. Note that the address here is the DWORD address, not the byte address. Take the byte address and remove the 2 LSBs, >>2.

- $DR[16:0] = 17b'0$   
*Note:* Bit 0 is shifted first, and bit 66 is shifted last.
3. Move to the “Run-test idle” state and loop in this state for a minimum of 20 TCK cycles.
  4. Move to the “Shift-DR” state again and shift the Ready bit and Error bit through JTAG\_TDO (see [Figure 38](#)).
    - First bit shifted out is the Ready bit.
    - Second bit shifted out is the Error bit.
    - Verify that the Ready bit is at logic high and the Error bit is at logic low.

*Note:* To prevent corruption, the DR register must be loaded as described in step 2 while shifting out through JTAG\_TDO for observation.
  5. Go back to step 2 to perform another write.

### 13.6.3 Read Access to Registers from JTAG Interface

Complete the following steps to read a device register through the JTAG Interface:

1. Move to the TAP controller “Shift-IR” state and program the instruction register with IRAC instruction by writing into Instruction Register bits with 0xFFFF\_FFFF\_FFFF\_FFFD.  
This step is optional if the instruction register is already programmed during the write cycle.
2. Move to the “Shift-DR” state and shift the R/W = 0 and the address[9:0] serially in the TDI pin. To prevent corruption of unused bits, the full DR bits have to be written as follows (see also [Figure 37](#)):
  - $DR[66:62] = 5b'0$
  - $DR[61:52] = ADDR[9:0]^1$
  - $DR[51] = R/W$
  - $DR[50:19] = DATA[31:0]$
  - $DR[18:17] = 2b'0$
  - $DR[16:0] = 17b'0$

*Note:* Bit 0 is shifted first, and bit 66 is shifted last.
3. Move to the “Run-test idle” state and loop in this state for a minimum of 20 TCK cycles.
4. Move to the “Shift-DR” state again and shift the Ready bit, Error bit, and data[31:0] out through JTAG\_TDO (see [Figure 38](#)).
  - First bit shifted out is the Ready bit.
  - Second bit shifted out is the Error bit.

---

1. Note that the address here is the DWORD address, not the byte address. Take the byte address and remove the 2 LSBs, >>2.

- Verify that the Ready bit is at logic high and the Error bit is at logic low.

*Note:* To prevent corruption, the DR register must be loaded as described in step 2 while shifting out through JTAG\_TDO for observation.

5. Go back to step 2 to perform another read.

## 13.7 Dedicated Test Pins

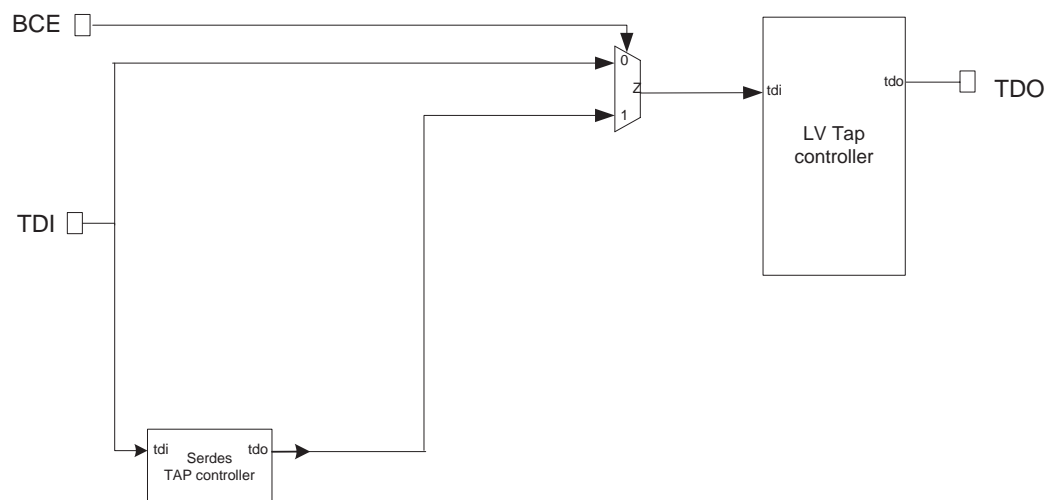
The following pins are dedicated to test:

- TEST\_ON (Scan shift enable; this signal is tied low for normal operation)
- TEST\_BCE (Boundary scan compliance enable; this signal is tied low for normal operation) – This pin configures the SerDes built-in TAP controller and the PEB383 top-level TAP controller into a daisy chain. TEST\_BCE uses a pad with a built-in pull-up. When TEST\_BCE is low, the bridge's JTAG pins access only the top-level TAP controller. When TEST\_BCE is high, the daisy chain mode is selected (see [Figure 39](#)).

## 13.8 Accessing SerDes TAP Controller

The SerDes has an internal TAP controller that uses IDCODE instruction for the IP identification and CRSEL instruction for writing and reading registers in the IP. To access the SerDes TAP controller through JTAG pins, JTAG\_TDI pin of SerDes is connected to the JTAG\_TDI pin and the TDO of SerDes is connected to the JTAG\_TDI of the PEB383's top-level TAP controller through a mux with JTAG\_BCE pin as selector. [Figure 39](#) shows the connections between the bridge's TAP controller and the SerDes TAP controller.

**Figure 39: PCIe SerDes Connections**







---

## 14. Register Descriptions

Topics discussed include the following:

- “Overview”
- “PCI Configuration Space”
- “Register Map”
- “Upstream Non-transparent Address Remapping Registers”
- “PCI Capability Registers”
- “PCIe Capability Registers”
- “Downstream Non-transparent Address Remapping Registers”
- “Advanced Error Reporting Capability Registers”
- “PCIe and SerDes Control and Status Registers”

---

### 14.1 Overview

The following terms describe the PEB383’s register attributes:

- R - Read only.
- RWL - Read and write when unlocked. Values can always be modified via serial EEPROM or JTAG. Values can be written from TLPs when the UNLOCK bit is high.
- HwInitWO - Hardware Initialized Write Once. The field may be written once, EEPROM or CFG, and then it becomes read only. Hot reset does not reset read only attribute. Cold or warm reset does reset read only attribute. All HwInitWO bits in the same 32 bit register must be written at the same time.
- R/W - Read/write.
- R/W1C - Read/Write 1 to clear; writing a 0 has no effect. These register bits are only set by the PEB383.
- RW1CS - Sticky Read Only, Write-1-to-Clear - Not initialized or modified by hot reset.
- R/WS Sticky Read / Write - Not initialized or modified by hot reset.
- R/W1S - Read 0/Write 1 to set (writing a 1 triggers an event such as an interrupt). These register bits are only cleared by the PEB383.
- RC - Clear after read.
- RS - Sticky Read Only. Not initialized or modified by hot reset.
- Reserved - Do not write any value other than 0 to this field. Reads return 0.

- ReservedP - The value in this field must be preserved during a write access.
- Undefined - This value is undefined after reset because it is based on a bit setting, a pin setting, or a power-up setting.

## 14.2 PCI Configuration Space

The PEB383 device uses a standard PCI Type 1 configuration header. [Table 32](#) shows the PCI 3.0 compatible Type 1 configuration space with constant values shown populated in the appropriate header fields. The PCIe 1.1 compatible capabilities options are located later in the configuration space starting at offset 0xC0 (see [Table 35](#)).

**Table 32: PCI Type 1 Configuration Header**

31			0	Offset	Page
Device ID		Vendor ID		0x000	123
Status		Command		0x004	124
Class Code			Revision ID	0x008	128
BIST	Header Type	Master Latency Timer	CacheLine Size	0x00C	129
Base Address Register 0(Reserved 0x00000000)				0x010	
Base Address Register 1 (Reserved 0x00000000)				0x014	-
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	0x018	130
Secondary Status		I/O Limit	I/O Base	0x01C	131
Memory Status		Memory Base		0x020	134
Prefetchable Memory Limit		Prefetchable Memory Base		0x024	135
Prefetchable Base Upper 32 Bits				0x028	136
Prefetchable Limit Upper 32 Bits				0x02C	136
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		0x030	137
Reserved			Capability Pointer	0x034	138
Expansion ROM Base Address (Reserved 0x00000000)				0x038	-
Bridge Control		Interrupt Pin	Interrupt Line	0x03C	139

The SSID capability registers are shown below.

**Table 33: SSID Capability Registers**

31			0	Offset	Page
Reserved		Next Pointer	Capability ID	0x060	160
SSID		SSVID		0x064	161

The power management capability registers are shown below.

**Table 34: Power Management Capability Registers**

31			0	Offset	Page
Power Management Capabilities		Next Pointer	Capability ID	0x0A0	162
Data (Reserved 0x00)	bridge support extensions (Reserved 0x00)	PMCSR		0x0A4	164

The PCIe capability registers are shown below.

**Table 35: PCIe Capability Registers**

31			0	Offset	Page
PCIe Capability Register		Next Pointer	Capability ID	0x0C0	173
Device Capability				0x0C4	175
Device Status		Device Control		0x0C8	177
Link Capability				0x0CC	180
Link Status		Link Control		0x0D0	182

The advanced error reporting capability register is shown below.

**Table 36: Advanced Error Reporting Capability Registers**

31			0	Offset	Page
PCIe Enhanced Capability Header				0x100	188
Uncorrectable Error Status Register				0x104	189
Uncorrectable Error Mask Register				0x108	190
Uncorrectable Error Severity Register				0x10C	191
Correctable Error Status Register				0x110	192
Correctable Error Mask Register				0x114	193
Advanced Error Capabilities and Control Register				0x118	194

**Table 36: Advanced Error Reporting Capability Registers (Continued)**

31			0	Offset	Page
Header Log Register				0x11C	195
				0x120	195
				0x124	196
				0x128	196
Secondary Uncorrectable Error Status Register				0x12C	197
Secondary Uncorrectable Error Mask Register				0x130	198
Secondary Uncorrectable Error Severity Register				0x134	199
Secondary Error Capabilities and Control Register				0x138	200
Secondary Header Log Register				0x13C	200
				0x140	201
				0x144	202
				0x148	202

## 14.3 Register Map

The following table lists the register map for the PEB383.

**Table 37: Register Map**

Offset	Name	See
0x000	PCI_ID	"PCI Identification Register"
0x004	PCI_CSR	"PCI Control and Status Register"
0x008	PCI_CLASS	"PCI Class Register"
0x00C	PCI_MISC0	"PCI Miscellaneous 0 Register"
0x010	Reserved	
0x014	Reserved	
0x018	PCI_BUSNUM	"PCI Bus Number Register"
0x01C	PCI_MISC1	"PCI Secondary Status and I/O Limit and Base Register"
0x020	PCI_MIO_BL	"PCI Memory Base and Limit Register"
0x024	PCI_PFM_BL	"PCI PFM Base and Limit Register"
0x028	PCI_PFM_B_UPPER	"PCI PFM Base Upper 32 Address Register"
0x02C	PCI_PFM_L_UPPER	"PCI PFM Limit Upper 32 Address Register"
0x030	PCI_IO_UPPER	"PCI I/O Address Upper 16 Register"
0x034	PCI_CAP	"PCI Capability Pointer Register"
0x038	Reserved	
0x03C	PCI_MISC2	"PCI Bridge Control and Interrupt Register"
0x040	SEC_RETRY_CNT	"Secondary Retry Count Register"
0x044	PCI_MISC_CSR	"PCI Miscellaneous Control and Status Register"
0x048	PCI_MISC_CLK_STRAPS	"PCI Miscellaneous Clock Straps Register"
0x04C	UPST_PWR_THRES	"Upstream Posted Write Threshold Register"
0x050	CPL_TIMEOUT	"Completion Timeout Register"
0x054	CLKOUT_ENB_FUNC_DBG	"Clock Out Enable Function and Debug Register"
0x058	SERRDIS_OPQEN_DTC	"SERRDIS_OPQEN_DTC Register"
0x05C	Reserved	
0x060	SSID_CAP	"SSID Capability Register"
0x064	SSID_ID	"SSID ID Register"

**Table 37: Register Map (Continued)**

Offset	Name	See
0x068	NTMA_CTRL	"NTMA Control Register"
0x06C	NTMA_PRI_BASEUPPER	"NTMA Primary Upper Base Register"
0x070	NTMA_SEC_LBASE	"NTMA Secondary Lower Base Register"
0x074	NTMA_SEC_BASEUPPER	"NTMA Secondary Upper Base Register"
0x078	NTMA_SEC_LIMIT	"NTMA Secondary Lower Limit Register"
0x07C	NTMA_SEC_UPPER_LIMIT	"NTMA Secondary Upper Limit Register"
0x0A0	PCI_PMC	"PCI Power Management Capability Register"
0x0A4	PCI_PMCS	"PCI Power Management Control and Status Register"
0x0A8	Reserved	
0x0AC	EE_CTRL	"EEPROM Control Register"
0x0B0	SBUS_DEVMSK	"Secondary Bus Device Mask Register"
0x0B4	STC_PERIOD	"Short-term Caching Period Register"
0x0B8	RTIMER_STATUS	"Retry Timer Status Register"
0x0BC	PREF_CTRL	"Prefetch Control Register"
0x0C0	PCIE_CAP	"PCIe Capabilities Register"
0x0C4	PCIE_DEV_CAP	"PCIe Device Capabilities Register"
0x0C8	PCIE_DEV_CSR	"PCIe Device Control and Status Register"
0x0CC	PCIE_LNK_CAP	"PCIe Link Capabilities Register"
0x0D0	PCIE_LNK_CSR	"PCIe Link Control Register"
0x0E4	AR_SBNPCTRL	"Secondary Bus Non-prefetchable Address Remap Control Register"
0x0E8	AR_SBNPBASE	"Secondary Bus Non-prefetchable Upper Base Address Remap Register"
0x0EC	AR_SBPPRECTRL	"Secondary Bus Prefetchable Address Remap Control Register"
0x0F0	AR_SBPBASEUPPER	"Secondary Bus Prefetchable Upper Base Address Remap Register"
0x0F4	AR_PBNPBASEUPPER	"Primary Bus Non-prefetchable Upper Base Address Remap Register"
0x0F8	AR_PBNPLIMITUPPER	"Primary Bus Non-prefetchable Upper Limit Remap Register"
0x0FC	Reserved	
0x100	PCIE_AERR_CAP	"PCIe Advanced Error Reporting Capability Register"
0x104	PCIE_UERR_STAT	"PCIe Uncorrectable Error Status Register"

**Table 37: Register Map (Continued)**

Offset	Name	See
0x108	PCIE_UERR_MASK	"PCIe Uncorrectable Error Mask Register"
0x10C	PCIE_UERR_SEV	"PCIe Uncorrectable Error Severity Register"
0x110	PCIE_COR_ERR	"PCIe Correctable Error Status Register"
0x114	PCIE_COR_MASK	"PCIe Correctable Error Mask Register"
0x118	PCIE_AERR_CAP_CTRL	"PCIe Advanced Error Capabilities and Control Register"
0x11C	PCIE_HL1	"PCIe Header Log 1 Register"
0x120	PCIE_HL2	"PCIe Header Log 2 Register"
0x124	PCIE_HL3	"PCIe Header Log 3 Register"
0x128	PCIE_HL4	"PCIe Header Log 4 Register"
0x12C	PCIE_SERR_STAT	"PCIe Secondary Uncorrectable Error Status Register"
0x130	PCIE_SERR_MASK	"PCIe Secondary Uncorrectable Error Mask Register"
0x134	PCIE_SERR_SEV	"PCIe Secondary Uncorrectable Error Severity Register"
0x138	PCIE_ECAP_CTRL	"PCIe Secondary Error Capabilities and Control Register"
0x13C	PCIE_SEC_HL1	"PCIe Secondary Header Log 1 Register"
0x140	PCIE_SEC_HL2	"PCIe Secondary Header Log 2 Register"
0x144	PCIE_SEC_HL3	"PCIe Secondary Header Log 3 Register"
0x148	PCIE_SEC_HL4	"PCIe Secondary Header Log 4 Register"
0x14C-204	Reserved	
0x208	REPLAY_LATENCY	"Replay Latency Register"
0x20C	ACKNAK_UPD_LAT	"ACK/NACK Update Latency Register"
0x210	N_FTS	"N_FTS Register"



### 14.3.1 PCI Identification Register

This register contains device and vendor identifiers.

Register name: PCI_ID Reset value: 0x8113_10E3	Register offset: 0x000
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	DID							
23:16	DID							
15:08	VID							
07:00	VID							

Bits	Name	Description	Type	Reset value
31:16	DID	Device ID This field indicates the silicon device identification number.	RWL	0x8113
15:0	VID	Vendor ID This field indicates the silicon vendor identification number. By default, the PEB383 device reports a value of 0x10E3 indicating the vendor as IDT (formerly Tundra).	RWL	0x10E3

### 14.3.2 PCI Control and Status Register

This register defines configurable parameters for how devices interact with the PCI bus, and indicates status information for PCI bus events.

<b>Register name: PCI_CSR</b> <b>Reset value: 0x_0010_0000</b>	<b>Register offset: 0x004</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	D_PE	S_SERR	R_MA	R_TA	S_TA	DEVSEL		MDP_D
23:16	TFBBC	Reserved	DEV66	CAP_L	INT_STAT	Reserved		
15:08	Reserved					INT_DIS	MFBBC	SERR_EN
07:00	WAIT	PERESP	VGAPS	MWI_EN	SC	BM	MS	IOS

Bits	Name	Description	Type	Reset value
31	D_PE	Detected Parity Error This bit is set by the bridge whenever it receives a poisoned TLP or a TLP with bad ECRC (Read Completion or Write Request) on the PCIe Interface, regardless of the state the Parity Error Response bit in the Command register. 0 = Data poisoning and bad ECRC not detected by the bridge on its PCIe Interface 1 = Data poisoning or bad ECRC detected by the bridge on its PCIe Interface	R/W1C	0
30	S_SERR	Signaled System Error This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message to the Root Complex and the SERR# Enable bit is set in the Command register. 0 = Neither ERR_FATAL nor ERR_NONFATAL transmitted on the PCIe Interface 1 = ERR_FATAL or ERR_NONFATAL transmitted on the PCIe Interface	R/W1C	0
29	R_MA	Received Master-Abort This bit is set when the bridge receives a Completion with Unsupported Request Completion Status on its PCIe Interface. 0 = Unsupported Request Completion Status not received on the PCIe Interface 1 = Unsupported Request Completion Status received on the PCIe Interface	R/W1C	0

*(Continued)*

Bits	Name	Description	Type	Reset value
28	R_TA	Received Target-Abort This bit is set when the bridge receives a Completion with Completer Abort Completion Status on its PCIe Interface. 0 = Completer Abort Completion Status not received on the PCIe Interface 1 = Completer Abort Completion Status received on the PCIe Interface	R/W1C	0
27	S_TA	Signaled Target-Abort This bit is set when the bridge generates a Completion with Completer Abort Completion Status in response to a request received on its PCIe Interface. 0 = Completer Abort Completion not transmitted on the PCIe Interface 1 = Completer Abort Completion transmitted on the PCIe Interface	R/W1C	0
26:25	DEVSEL	DEVSEL# Timing This field is not applicable for PCIe. It always reads 0.	R	00
24	MDP_D	Master Data Parity Error 0 = No uncorrectable data error detected on the PCIe Interface 1 = Uncorrectable data error detected on the PCIe Interface This field is set by the PEB383 if its Parity Error Response Enable bit is set and either of the following conditions occurs: <ul style="list-style-type: none"> <li>The PEB383 receives a Completion marked poisoned on the PCIe Interface.</li> <li>The PEB383 poisons a write request on the PCIe Interface</li> </ul> Note: If the Parity Error Response Enable bit is cleared, this bit is never set.	R/W1C	0
23	TFBBC	Fast Back-to-Back Capable This field is not applicable for PCIe. It always reads 0.	R	0
22	Reserved	Status Reserved 1. It always reads 0.	R	0
21	DEV66	66-MHz Capable This field is not applicable for PCIe. It always reads 0.	R	0
20	CAP_L	Capabilities List 1 = Capabilities list is supported	R	1
19	INT_STAT	Interrupt Status The PEB383 does not generate internal interrupts.	R	0
18:11	Reserved	Reserved	R	0x0

*(Continued)*

Bits	Name	Description	Type	Reset value
10	INT_DIS	Interrupt Disable The PEB383 does not generate internal interrupts.	R	0
09	MFBBC	Fast Back-to-Back Enable This field does not apply for PCIe bridges. It always reads 0.	R	0
08	SERR_EN	SERR# Enable This bit enables reporting of non-fatal and fatal errors to the Root Complex. In addition, this bit enables transmission by the PCIe Interface of ERR_NONFATAL and ERR_FATAL error messages on behalf of SERR# assertions detected on the PCI Interface. Note that errors are reported if enabled either through this bit or through the PCIe specific bits in the Device Control register. 0 = Disable the reporting of bridge non-fatal errors and fatal errors to the Root Complex. 1 = Enable the reporting of bridge non-fatal errors and fatal errors to the Root Complex.	R/W	0
07	WAIT	IDSEL Stepping / Wait Cycle Control This field does not apply for PCIe bridges. It always reads 0.	R	0
06	PERESP	Parity Error Response Enable This bit controls the PEB383's setting of the Master Data Parity Error bit in the Status register in response to a received poisoned TLP from PCIe. 0 = Disable the setting of the Master Data Parity Error bit. 1 = Enable the setting of the Master Data Parity Error bit.	R/W	0
05	VGAPS	VGA Palette Snoop This field does not apply for PCIe bridges. It always reads 0.	R	0
04	MWI_EN	Memory Write Invalidate Enable This bit controls the PEB383's ability to translate PCIe Memory Write Requests into PCI Memory Write and Invalidate transactions. 0 = Do not translate Memory Write requests into PCI Memory Write and Invalidate transactions. 1 = Promote Memory Write requests to PCI Memory Write and Invalidate transactions.	R/W	0
03	SC	Special Cycles This field does not apply for PCIe bridges. It always reads 0.	R	0
02	BM	Bus Master Enable This field allows the PEB383 to perform bus-mastered transactions on the PCIe link. The host or software driver must ensure this bit is set to 1 for correct NTMA operation.	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
01	MS	<p>Memory Space Enable</p> <p>This bit controls the PEB383's response as a target to memory accesses on the PCIe Interface that address a device that resides behind the bridge in both the non-prefetchable and prefetchable memory ranges, or targets a memory-mapped location within the bridge itself.</p> <p>0 = Respond to all Memory Requests on the PCIe Interface as Unsupported Request Received. Forward all memory requests from the PCI Interface to the PCIe Interface.</p> <p>1 = Enable forwarding of memory transactions to the PCI Interface and any internal function.</p>	R/W	0
00	IOS	<p>I/O Space Enable</p> <p>This bit controls the PEB383's response as a target to I/O transactions on the PCIe Interface that address a device that resides behind the bridge.</p> <p>0 = Respond to all I/O Requests on the PCIe Interface with an Unsupported Request Completion.</p> <p>1 = Enable forwarding of I/O Requests to the PCI Interface.</p>	R/W	0

### 14.3.3 PCI Class Register

This register indicates the PCI classification of the PEB383.

Register name: PCI_CLASS Reset value: 0x0604_0001	Register offset: 0x008
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	BASE							
23:16	SUB							
15:08	PROG							
07:00	RID							

Bits	Name	Description	Type	Reset value
31:24	BASE	Base Class This field indicates the device is a bridge.	R	0x06
23:16	SUB	Sub Class This field indicates the device is a PCI-to-PCI bridge.	R	0x04
15:08	PROG	Program Interface This field reads 0 when the LEGACY bit is clear (see "PCI Miscellaneous Clock Straps Register"), and reads 0x1 when the legacy bit is set. When set to 0x1, it indicates to software that a subtractive decode bridge is present. For more information about Legacy mode, see "Legacy Mode".	R	0x00
07:00	RID	Revision ID This field indicates the hardware silicon revision identifier.	RWL	0x01

### 14.3.4 PCI Miscellaneous 0 Register

This register controls miscellaneous PCI functions, such as the latency timer value and cacheline size.

<b>Register name: PCI_MISC0</b> <b>Reset value: 0x0001_0000</b>	<b>Register offset: 0x00C</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	BISTC	SBIST	Reserved		CCODE			
23:16	H_TYPE							
15:08	Reserved							
07:00	CLINE							

Bits	Name	Description	Type	Reset value
31	BISTC	BIST Capable; 0 = PEB383 is not BIST capable	R	0
30	SBIST	Start BIST; 0 = PEB383 is not BIST capable	R	0
29:28	Reserved	Reserved	R	0
27:24	CCODE	Completion Code; 0 = PEB383 is not BIST capable	R	0
23:16	H_TYPE	Header Type This field indicates the PEB383 is a single-function bridge.	R	0x01
15:08	Reserved	Reserved (Latency timer in PCI Interface)	R	0
07:00	CLINE	Cacheline Size <sup>a</sup> 04 = 4 x 32-bit word (16 bytes) 08 = 8 x 32-bit word (32 bytes) 10 = 16 x 32-bit word (64 bytes) 20 = 32 x 32-bit word (128 bytes)  This field specifies the system cacheline size in units of 32-bit words. It is used by the PCI master to determine the PCI read transaction - that is, memory read, memory read line, or memory read multiple - it should generate on the PCI bus. CLINE is also used by the PCI target to decide how much data to read on the destination bus.  Note: This field is set to 0 if CLINE is programmed to a value not specified above.	R/W	0x0

- a. Software programs the system cacheline size in DWORD counts. The value programmed is used by the PEB383 for prefetching data from memory for Memory Read Line and Memory Line Multiple transactions on the primary bus interface. Software should set only one bit at anytime. If multiple bits are set, the register defaults to 0.

### 14.3.5 PCI Bus Number Register

Register name: PCI_BUSNUM Reset value: Undefined	Register offset: 0x018
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	S_LTIMER					S_LTIMER_8		
23:16	SUB_BUS_NUM							
15:08	S_BUS_NUM							
07:00	P_BUS_NUM							

Bits	Name	Description	Type	Reset value
31:27	S_LTIMER	<p>Secondary Latency Timer</p> <p>This value is used by the PEB383 to perform burst transfers on the PCI Interface. The lower 3 bits are hardwired to 0 so that the timer is limited to 8-cycle granularity.</p> <p>This field defines the minimum amount of time in PCI clock cycles that the PEB383 can retain ownership as a bus master on the PCI Interface.</p> <p>00000 = PCI reset value</p>	R/W	Undefined
26:24	S_LTIMER_8	Set to 000 to force 8-cycle increments for the Secondary Latency Timer.	R	000
23:16	SUB_BUS_NUM	<p>Subordinate Bus Number</p> <p>The system software programs this field with the PEB383's highest-numbered downstream secondary bus number. This value is used by the PEB383 to respond to Type 1 Configuration transactions on the primary bus interface.</p>	R/W	0x00
15:08	S_BUS_NUM	<p>Secondary Bus Number</p> <p>The system software programs this field with the number of the bridge's immediate downstream secondary bus. This value is used by the PEB383 to convert Type 1 Configuration transactions received on its primary bus interface to Type 0 Configuration transactions.</p>	R/W	0x00
07:00	P_BUS_NUM[7:0]	<p>Primary Bus Number</p> <p>The system software writes to this field with the primary bus number of the PEB383.</p>	R/W	0x00



### 14.3.6 PCI Secondary Status and I/O Limit and Base Register

Register name: PCI_MISC1_P Reset value: 0x02A0_0101	Register offset: 0x01C
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	D_PE	S_SERR	R_MA	R_TA	S_TA	DEVSEL		MDP_D
23:16	TFBBC	Reserved	DEV66	Reserved				
15:08	IO_LA				ADD_CAP1			
07:00	IO_BA				ADD_CAP2			

Bits	Name	Description	Type	Reset value
31	D_PE	Data Parity Error Detected This bit reports the detection of an address or data parity error on the PEB383's PCI Interface. The PEB383 sets this bit when it detects one of the following: <ul style="list-style-type: none"> <li>Address parity error as a potential target</li> <li>Data parity error as a target of a write transaction</li> <li>Data parity error as a master of a read transaction</li> </ul> 0 = Device did not detect a parity error. 1 = Device detected a parity error.	R/W1C	0
30	S_SERR	Received System Error This bit reports the assertion of PCI_SERRn on the PCI Interface. 1 = PCI_SERRn was detected on the PCI Interface. 0 = PCI_SERRn was not detected.	R/W1C	0
29	R_MA	Received Master Abort This bit reports the detection of a Master-Abort termination by the PEB383 when it is the master of a transaction on its PCI Interface. 0 = No Master-Abort detected. 1 = Master-Abort detected on the PCI Interface.	R/W1C	0
28	R_TA	Received Target Abort This bit reports the detection of a Target-Abort termination by the PEB383 when it is the master of a transaction on its PCI Interface. 0 = No Target-Abort detected. 1 = Target-Abort detected on the PCI Interface.	R/W1C	0

*(Continued)*

Bits	Name	Description	Type	Reset value
27	S_TA	Signaled Target Abort The PEB383 sets this bit to report the signaling of Target-Abort as target of a transaction on the PCI Interface. 0 = No Target-Abort signaled. 1 = Target-Abort signaled by the PEB383 on its PCI Interface.	R/W1C	0
26:25	DEVSEL	Device Select Timing The PEB383 uses medium-speed decoding on its PCI Interface.	R	01
24	MDP_D	Master Data Parity Error This bit reports the detection of an uncorrectable data error by the PEB383. 0 = No uncorrectable data error detected on the PCI Interface. 1 = Uncorrectable data error detected on the PCI Interface.	R/W1C	0
23	TFBBC	Fast Back-to-Back Capability 0 = Not supported 1 = Supported This bit is hardwired to 1 when the secondary bus interface operates in PCI mode, indicating that the bridge can decode fast back-to-back transactions when the transactions are from the same master but to different targets.	R	1
22	Reserved	Reserved	R	0
21	DEV66	66-MHz Capable PCI Bus This bit is hardwired to 1, indicating that the secondary bus interface can operate at a 66-MHz clock rate.	R	1
20:16	Reserved	Reserved	R	00000
15:12	IO_LA[3:0]	I/O Limit Address The PEB383 uses this field for I/O address decoding. These bits define the upper bound of the address range used by the bridge to forward an I/O transaction from one interface to the other. These 4 bits correspond to address bits <15:12>. The address bits <11:0> are assumed equal to 12'hFFF.	R/W	0x0
11:08	ADD_CAP1	Addressing Capability The PEB383 supports 32-bit I/O addressing.	R	0x1
07:04	IO_BA[3:0]	I/O Base Address The PEB383 uses this field for I/O address decoding. These bits define the lower bound of address range used by the bridge to forward an I/O transaction from one interface to the other. These 4 bits correspond to address bits <15:12>. The address bits <11:0> are assumed equal to 12'h0.	R/W	0x0

---

*(Continued)*

Bits	Name	Description	Type	Reset value
03:00	ADD_CAP2	Addressing Capability The PEB383 supports 32-bit I/O addressing.	R	0x1

### 14.3.7 PCI Memory Base and Limit Register

Register name: PCI_MIO_BL Reset value: 0x0000_0000	Register offset: 0x020
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	LA							
23:16	LA				Reserved			
15:08	BA							
07:00	BA				Reserved			

Bits	Name	Description	Type	Reset value
31:20	LA	Memory Limit Address This field is used in conjunction with the Memory Base Address for forwarding memory-mapped I/O transactions. These bits define the upper bound for the memory address range. The upper 12 bits correspond to address bits <31:20> of the address range. Bits <19:0> of the address range are 0xFFFFF.	R/W	0
19:16	Reserved	Reserved	R	0
15:04	BA	Memory Base Address This field defines the lower bound of the address range for forwarding memory-mapped I/O transactions. These bits correspond to address bits <31:20> of the address range. The lower 20 address bits (19:0) are 20'h0.	R/W	0
03:00	Reserved	Reserved	R	0

### 14.3.8 PCI PFM Base and Limit Register

Register name: PCI_PFM_BL Reset value: 0x0001_0001	Register offset: 0x024
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	LA							
23:16	LA				ADD_LA_64			
15:08	BA							
07:00	BA				ADD_BA_64			

Bits	Name	Description	Type	Reset value
31:20	LA	Prefetchable Memory Limit Address This field is used in conjunction with Memory Base Address for forwarding memory-mapped I/O transactions. These bits define the upper bound for the memory address range. The upper 12 bits correspond to address bits <31:20> of the address range. Bits <19:0> of the address range are 0xFFFFF.	R/W	0
19:16	ADD_LA_64	Addressing Capability — Memory Base Address The PEB383 supports 64-bit addressing.	R	0x1
15:04	BA	Prefetchable Memory Base Address This field defines the lower bound of the prefetchable memory address range. These bits correspond to address bits <31:20> of the Prefetchable Address range. The lower 20 address bits (19:0) are 20'h0.	R/W	0
03:00	ADD_BA_64	Addressing Capability — Memory Range Limit Address The PEB383 supports 64-bit addressing.	R	0x1

### 14.3.9 PCI PFM Base Upper 32 Address Register

Register name: PCI_PFM_B_UPPER Reset value: 0x0000_0000	Register offset: 0x028
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	BA							
23:16	BA							
15:08	BA							
07:00	BA							

Bits	Name	Description	Type	Reset value
31:00	BA	Prefetchable Memory Base Upper 32-bit Address This field is used in conjunction with BA in the “PCI PFM Base and Limit Register” to specify the lower bound of the 64-bit prefetchable address range. The 32 bits relate to address bits <63:32> of the Prefetchable Base Address bits.	R/W	0x0

### 14.3.10 PCI PFM Limit Upper 32 Address Register

Register name: PCI_PFM_L_UPPER Reset value: 0x0000_0000	Register offset: 0x02C
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	LA							
23:16	LA							
15:08	LA							
07:00	LA							

Bits	Name	Description	Type	Reset value
31:00	LA	Prefetchable Memory Limit Upper 32-bit Address This field is used in conjunction with LA in the “PCI PFM Base and Limit Register” to specify the upper bound of the 64-bit prefetchable address range. The 32 bits relate to address bits <63:32> of the Prefetchable Limit Address.	R/W	0x0

### 14.3.11 PCI I/O Address Upper 16 Register

Register name: PCI_IO_UPPER Reset value: 0x0000_0000	Register offset: 0x030
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	IO_LA							
23:16	IO_LA							
15:08	IO_BA							
07:00	IO_BA							

Bits	Name	Description	Type	Reset value
31:16	IO_LA	I/O Limit Address Upper 16-bits This field is used in conjunction with IO_LA in the “PCI Secondary Status and I/O Limit and Base Register” to define the upper bound 32-bit address range used for decoding I/O transactions from the PCIe Interface to the PCI Interface. These bits relate to address bits <31:16> of I/O Limit Address.	R/W	0x0000
15:00	IO_BA	I/O Base Address Upper 16-bits This field is used in conjunction with IO_BA in the “PCI Secondary Status and I/O Limit and Base Register” to define the lower bound 32-bit address range used for decoding I/O transaction from the PCIe Interface to the PCI Interface. These bits relate to address bits <31:16> of I/O Base Address.	R/W	0x0000

### 14.3.12 PCI Capability Pointer Register

Register name: PCI_CAP Reset value: 0x0000_00A0	Register offset: 0x034
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							
07:00	CAP_PTR							

Bits	Name	Description	Type	Reset value
31:08	Reserved	Reserved	R	0x0
07:00	CAP_PTR	Capabilities Pointer By default the next capability pointer is 0xA0 "PCI Power Management Capability Register". If it is desired to link in "SSID Capability Register" then this value should be changed to 0x60.	RWL	0x0A0



### 14.3.13 PCI Bridge Control and Interrupt Register

Register name: PCI_MISC2 Reset value: 0x0000_00FF	Register offset: 0x03C
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved				DISCARD_SERR	DISCARD_STAT	DISCARD2	DISCARD1
23:16	S_FFTP_EN	S_RESET	MA_ERR	VGA_16BIT_EN	VGA_EN	ISA_EN	SERR_EN	S_PERESP
15:08	INT_PIN							
07:00	INT_LINE							

Bits	Name	Description	Type	Reset value
31:28	Reserved	Reserved	R	0x0
27	DISCARD_SERR	<p>Discard Timer SERR# Enable</p> <p>This bit only applies in PCI mode. It enables the PEB383 to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the PCIe Interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. The severity is selectable only if Advanced Error Reporting is supported.</p> <p>0 = Do not generate ERR_NONFATAL or ERR_FATAL on the PCIe Interface as a result of the expiration of the Secondary Discard Timer. Note that an error message can still be sent if Advanced Error Reporting is supported and the Delayed Transaction Discard Timer Expired Mask bit is clear.</p> <p>1 = Generate ERR_NONFATAL or ERR_FATAL on the PCIe Interface if the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge.</p>	R/W	0
26	DISCARD_STAT	<p>Discard Timer Status</p> <p>It is set to 1 when the Secondary Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge.</p> <p>0 = No discard timer error</p> <p>1 = Discard timer error</p>	R/W1C	0

*(Continued)*

Bits	Name	Description	Type	Reset value
25	DISCARD2	<p>Secondary Discard Timer</p> <p>This bit determines the number of PCI clocks that the bridge waits for a master on the PCI Interface to repeat a Delayed Transaction request. The counter starts once the Completion (PCIe Completion associated with the Delayed Transaction Request) has reached the head of the downstream queue of the bridge (that is, all ordering requirements have been satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the secondary bus). If the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets the Discard Timer Status bit.</p> <p>0 = Secondary Discard Timer counts <math>2^{15}</math> PCI clock cycles  1 = Secondary Discard Timer counts <math>2^{10}</math> PCI clock cycles</p>	R/W	0
24	DISCARD1	<p>Primary Discard Timer</p> <p>This bit does not apply to PCIe. It always reads 0.</p>	R	0
23	S_FFTP_EN	<p>Fast Back-to-Back Enable</p> <p>The PEB383 cannot generate fast back-to-back transactions as a master on the PCI Interface.</p>	R	0
22	S_RESET	<p>Secondary Bus Reset</p> <p>This bit forces the assertion of PCI_RST# on the PCI Interface. The secondary PCI_RST# is asserted by the bridge whenever this bit is set. The bridge's secondary bus interface and any buffers between the two interfaces (primary and secondary) must be initialized back to their default state whenever this bit is set. The primary bus interface and all configuration space registers must not be affected by the setting of this bit. Because PCI_RST# is asserted for as long as this bit is set, software must observe proper PCI reset timing requirements.</p> <p>0 = Do not force the assertion of the PCI Interface PCI_RST#.  1 = Force the assertion of the PCI Interface PCI_RST#.</p>	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
21	MA_ERR	<p>Master-Abort Mode</p> <p>This bit controls the behavior of a bridge when it receives a Master-Abort termination (for example, an Unsupported Request on PCIe) on either interface.</p> <p>0 = Do not report Master-Aborts. When a UR response is received from PCIe for non-posted transactions, and when the secondary side is operating in PCI mode, return 0xFFFF_FFFF on reads and complete I/O writes normally. When a Master-Abort is received on the PCI Interface for posted transactions initiated from the PCIe Interface, no action is taken (that is, all data is discarded).</p> <p>1 = Report UR Completions from PCIe by signaling Target-Abort on the PCI Interface when the PCI Interface is operating in PCI mode. For posted transactions initiated from the PCIe Interface and Master-Aborted on the PCI Interface, the bridge must return an ERR_NONFATAL (by default) or ERR_FATAL transaction (provided the SERR# Enable bit is set in the Command register). The severity is selectable only if Advanced Error Reporting is supported.</p>	R/W	0
20	VGA_16BIT_EN	<p>VGA 16-Bit Enable</p> <p>This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit has meaning only if VGA Enable bit is set.</p> <p>1 = Executes 16-bit address decodes on VGA I/O accesses 0 = Executes 10-bit address decodes on VGA I/O accesses</p>	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
19	VGA_EN	<p>VGA Enable</p> <p>This bit modifies the response of the bridge to VGA-compatible addresses. If this bit is set, the bridge forwards the following accesses on the PCIe Interface to the PCI Interface (and, conversely, block the forwarding of these addresses from the secondary interface to the PCIe Interface):</p> <ul style="list-style-type: none"> <li>• Memory accesses in the range 0x000A_0000 to 000B_FFFF</li> <li>• I/O addresses in the first 64 Kbytes of the I/O address space (Address[31:16] for PCIe are 0x0000) and where Address[9:0] is in the range of 0x3B0 to 0x3BB or 0x3C0 to 0x3DF (inclusive of ISA address aliases - Address[15:10] may possess any value and is not used in the decoding)</li> </ul> <p>If this bit is set, the forwarding of VGA addresses is independent of the following:</p> <ul style="list-style-type: none"> <li>• The value of the ISA Enable bit</li> <li>• The I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Prefetchable Memory Base and Limit registers of the bridge</li> </ul> <p>The forwarding of VGA addresses is qualified by the I/O Enable and Memory Enable bits in the “<b>PCI Control and Status Register</b>”.</p> <p>0 = Do not forward VGA compatible memory and I/O addresses from PCIe to the PCI (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges.</p> <p>1 = Forward VGA compatible memory and I/O addresses (addresses defined above) from PCIe to PCI (if the I/O Enable and Memory Enable bits are set) independent of the I/O and memory address ranges, and independent of the ISA Enable bit.</p>	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
18	ISA_EN	<p>ISA Enable</p> <p>This bit modifies the response by the PEB383 to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block.</p> <p>0 = Forward downstream all I/O addresses in the address range defined by the I/O Base and Limit registers.</p> <p>1 = Forward upstream ISA I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block).</p>	R/W	0
17	SERR_EN	<p>SERR# Enable</p> <p>This bit controls the forwarding of PCI SERR# assertions to the PCIe Interface. The PEB383 transmits an ERR_FATAL or ERR_NONFATAL cycle on the PCIe Interface when PCI_SERRn is asserted on the PCI Interface.</p> <p>This bit is set when Advanced Error Reporting is supported and the SERR# Assertion Detected Mask bit is clear in the "PCIe Secondary Uncorrectable Error Mask Register".</p> <p>The SERR# Enable bit is set in the "PCI Control and Status Register" or the PCIe-specific bits are set in the "PCIe Device Control and Status Register" of the PCIe Capability Structure.</p> <p>0 = Disable the forwarding of SERR# from the PCI Interface to ERR_FATAL and ERR_NONFATAL (SERR# can still be forwarded if the SERR Advanced Error mask bit is cleared).</p> <p>1 = Enable the forwarding of secondary SERR# to ERR_FATAL or ERR_NONFATAL.</p>	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
16	S_PERESP	<p>Parity Error Response Enable</p> <p>This bit controls the PEB383's response to uncorrectable address, attribute, and data errors on the PCI Interface. If this bit is set, the bridge must take its normal action when one of these errors is detected. If this bit is cleared, the bridge must ignore any uncorrectable address, attribute, and data errors that it detects and continue normal operation.</p> <p>Note: A bridge must generate parity (or ECC, if applicable) even if parity error reporting is disabled. Also, a bridge must always forward data with poisoning from PCI to PCIe on an uncorrectable PCI data error, regardless of the setting of this bit.</p> <p>0 = Ignore uncorrectable address, attribute, and data errors on the PCI Interface.</p> <p>1 = Enable uncorrectable address, attribute, and data error detection and reporting on the PCI Interface.</p>	R/W	0
15:08	INT_PIN [7:0]	<p>Interrupt Pin</p> <p>The PEB383 does not generate interrupts. Therefore, this register is hardwired to 0x00.</p>	R	0x00
07:00	INT_LINE [7:0]	<p>Interrupt Line</p> <p>The PEB383 does not generate an interrupt. Therefore, the register is read only.</p>	R	0xFF

### 14.3.14 Secondary Retry Count Register

Register name: SEC_RETRY_CNT Reset value: 0x0000_AA00	Register offset: 0x040
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							CGD
23:16	Reserved			ARB	Reserved			PARK
15:8	DTL3		DTL2		DTL1		DTL0	
7:0	Reserved				SEC_RT_CNT			

Bits	Name	Description	Type	Reset value
31:25	Reserved	Reserved	R	0
24	CGD	Clock gating disable 1: clock gating disabled 0: clock gating enabled When in L1 state internal clocks are gated off by default.	R/W	0
23:21	Reserved	Reserved	R	0
20	ARB	External arbiter control 0b0: disable external arbiter 0b1: enable external arbiter	HwInitWO	0
19:17	Reserved	Reserved	R	0
16	PARK	PARK bus parking policy 0b0: park on last served device 0b1: park on the bridge	HwInitWO	0
15:14	DTL0	Delayed Transaction Limit for PCI Device 3: 0b01; max one delayed transaction for device 3 0b10; max two delayed transaction for device 3 0b11; max three delayed transaction for device 3 0b00; max four delayed transaction for device 3	R/W	0b10
13:12	DTL0	Delayed Transaction Limit for PCI Device 2: 0b01; max one delayed transaction for device 2 0b10; max two delayed transaction for device 2 0b11; max three delayed transaction for device 2 0b00; max four delayed transaction for device 2	R/W	0b10

*(Continued)*

Bits	Name	Description	Type	Reset value
11:10	DTL0	Delayed Transaction Limit for PCI Device 1: 0b01; max one delayed transaction for device 1 0b10; max two delayed transaction for device 1 0b11; max three delayed transaction for device 1 0b00; max four delayed transaction for device 1	R/W	0b10
9:8	DTL0	Delayed Transaction Limit for PCI Device 0: 0b01; max one delayed transaction for device 0 0b10; max two delayed transaction for device 0 0b11; max three delayed transaction for device 0 0b00; max four delayed transaction for device 0	R/W	0b10
7:4	Reserved	Reserved	R	0
3:0	SEC_RT_CNT	This field defines the number of retries that the PEB383 will receive on the secondary bus for a requested transaction, before its internal retry counter expires. When the counter expires, the bridge discards the request. 0000 = Counting disabled (No expiration) 0001 = 256 retries before expiration 0010 = 64K retries before expiration 0100 = 16M retries before expiration 1000 = 2G retries before expiration	R/W	0000



### 14.3.15 PCI Miscellaneous Control and Status Register

Register name: PCI_MISC_CSR Reset value: 0x7D10_1900	Register offset: 0x044
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved	EN_ARB	EN_ARB3	EN_ARB2	EN_ARB1	EN_ARB0	Reserved	P_ERR
23:16	STC_EN	Reserved		ARB_PRI	ARB_PRI3	ARB_PRI2	ARB_PRI1	ARB_PRI0
15:08	Reserved	CPL_INIT_COUNT				CFG_RT		
07:00	Reserved							

Bits	Name	Description	Type	Reset value
31	Reserved	Reserved	R	0
30	EN_ARB	Enable Internal Arbiter This bit enables arbitration for PEB383 requests. 0 = PEB383 disables internal requests. 1 = PEB383 enables internal requests. 0	R/W	1
29	EN_ARB3	Enable Arbiter 3 0 = PEB383 disables PCI_REQ3n for arbitration. 1 = The bridge enables PCI_REQ3n for arbitration.	R/W	1
28	EN_ARB2	Enable Arbiter 2 0 = PEB383 disables PCI_REQ2# for arbitration. 1 = PEB383 enables PCI_REQ2# for arbitration.	R/W	1
27	EN_ARB1	Enable Arbiter 1 0 = PEB383 disables PCI_REQ1# for arbitration. 1 = PEB383 enables PCI_REQ1# for arbitration.	R/W	1
26	EN_ARB0	Enable Arbiter 0 0 = PEB383 disables PCI_REQ0# for arbitration. 1 = PEB383 enables PCI_REQ0# for arbitration.	R/W	1
25	Reserved	Reserved	R	0
24	P_ERR	Parity Error Behavior This bit controls the behavior of the PEB383 when it detects a data parity error during a non-posted write transaction. 0 = PCI_PERRn is asserted and the corrupted data is passed. 1 = PCI_PERRn is asserted and the transaction is asserted on the originating bus, appropriate status bits are set, data is discarded, and the request is not enqueued.	R	1

*(Continued)*

Bits	Name	Description	Type	Reset value
23	STC_EN	Short-term Caching Enable 0 = Disable short-term caching 1 = Enable short-term caching	R/W	0
22:21	Reserved	Reserved	R	00
20	ARB_PRI	Internal Arbiter Priority This bit sets priority for PEB383 requests. 0 = Internal requests from the PEB383 are assigned low priority 1 = Internal requests from the PEB383 are assigned high priority	R/W	1
19	ARB_PRI3	Arbiter Priority 3 0 = PEB383 assigns low priority to PCI_REQ3#. 1 = PEB383 assigns high priority to PCI_REQ3#.	R/W	0
18	ARB_PRI2	Arbiter Priority 2 0 = PEB383 assigns low priority to PCI_REQ2#. 1 = PEB383 assigns high priority to PCI_REQ2#.	R/W	0
17	ARB_PRI1	Arbiter Priority 1 0 = PEB383 assigns low priority to PCI_REQ1#. 1 = PEB383 assigns high priority to PCI_REQ1#.	R/W	0
16	ARB_PRI0	Arbiter Priority 0 0 = PEB383 assigns low priority to PCI_REQ0#. 1 = PEB383 assigns high priority to PCI_REQ0#.	R/W	0
15	Reserved	Reserved	R	0
14:11	CPL_INIT_COUNT	This is applicable for upstream Non-Posted requests in PCI mode. It indicates the number of Dwords of response data to be accumulated before starting the data transfer. 0000 = 8 Dwords 0001 = 16 Dwords 0010 = 24 Dwords 0011 = 32 Dwords 0100 = 40 Dwords 0101 = 48 Dwords 0110 = 56 Dwords 0111 = 64 Dwords 1000 = 72 Dwords 1001 = 80 Dwords 1010 = 88 Dwords	R/W	0011

*(Continued)*

Bits	Name	Description	Type	Reset value
10:08	CFG_RT	<p>Configuration Retry Timer</p> <p>The PEB383 returns the Completion with CRS completion status for the received Type 1 configuration requests if this timer is expired before receiving the Completion from the targeted secondary device.</p> <p>000 = 25 us            001 = 40 us            010 = 50 us            011 = 100 us            100 = 200 us            101 = 500 us            110 = 1 ms            111 = 10 ms</p>	R/W	001
07:00	Reserved	Reserved	R	0x00

### 14.3.16 PCI Miscellaneous Clock Straps Register

Register name: PCI_MISC_CLK_STRAPS Reset value: 0x0000_0100	Register offset: 0x048
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							CSR_SEL_400
07:00	LEGACY	Reserved		PCGE	OP_MODE	CS_MODE		

Bits	Name	Description	Type	Reset value
31:9	Reserved	Reserved	R	0
8	CSR_SEL_400	This bit programs the PLL clock: 1 = PLL Clock is 400MHz. This generates 50/50% nominal PCI_CLKO. 0 = PLL Clock is 200MHz. This generates 33/66% nominal PCI_CLKO. Note: For normal operation, leave this bit in its default state.	R/W	1
7	LEGACY	Legacy Mode When set to 1, the PEB383 operates in legacy mode (for more information, see "Legacy Mode").	R/W	0
6:5	Reserved	Reserved	R	0
4	PCGE	PCI clock gate enable 0b0: PCI_CLK[3:0] clock gating disabled 0b1: PCI_CLK[3:0] clock gating enabled when in D3_hot, and in 33MHZ mode. In addition the bits "BPCCE" and "B2B3S" in the "PCI Power Management Control and Status Register" is updated to reflect this <b>Note:</b> Setting this bit to a 1 has no effect if clock rate is higher than 33MHz.	R/W	0
3	OP_MODE	Operating Mode 0 = PEB383 provides the clock on PCI_CLKO with the speed defined by the M66_EN signal (33/66 MHz) 1 = PEB383 provides the clock on PCI_CLKO with the speed defined by the CS_MODE bits. (25/33/50/60 MHz)	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
2:0	CS_MODE	Clock Speed Mode This field defines the clock speed when OP_MODE is set to 1 according to the following code points: 0bX00 = 25-MHz PCI mode 0bX01 = 33-MHz PCI mode 0bX10 = 50-MHz PCI mode 0bX11 = 66-MHz PCI mode	R/W	000

### 14.3.17 Upstream Posted Write Threshold Register

Register name: UPST_PWR_THRES Reset value: 0x0000_0307	Register offset: 0x04C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:8	Reserved						MAX_BUF_ALOC	
7:0	Reserved			UPST_PWR_THRES				

Bits	Name	Description	Type	Reset value
31:10	Reserved	Reserved.	R	0
9:8	MAX_BUF_ALOC	<p>Maximum Buffer Allocation</p> <p>This field determines the maximum completion buffer allocation that a single, upstream non-posted read request will create. The amount of completion buffer allocated is the MIN of these bits and the read request.</p> <p>11 = 1024 bytes 10 = 512 bytes 01 = 256 bytes 00 = 256 bytes</p>	R/W	11
7:5	Reserved	Reserved.	R	0
4:0	UPST_PWR_THRES	<p>This field defines the threshold for the upstream posted writes, and indicates the length of posted write data to be accumulated in the upstream posted buffer that triggers forwarding of a posted request onto the PCIe core.</p> <p>Note: Other events may also trigger forwarding. For more information, see <a href="#">"Upstream Posted Buffer"</a>.</p> <p>This field is defined as follows:</p> <p>00000 = 16 bytes 00001 = 32 bytes 00010 = 48 bytes 00011 = 64 bytes 00100 = 80 bytes 00101 = 96 bytes 00110 = 112 bytes 00111 = 128 bytes</p>	R/W	00111

### 14.3.18 Completion Timeout Register

Register name: CPL_TIMEOUT Reset value: 0x8009_8968	Register offset: 0x050
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	CPL_TO_EN	CPL_TO_VALUE						
23:16	CPL_TO_VALUE							
15:08	CPL_TO_VALUE							
07:00	CPL_TO_VALUE							

Bits	Name	Description	Type	Reset value
31	CPL_TO_EN	Completion Timeout Enable This bit enables/disables the Completion Timeout function. The PEB383 handles an upstream non-posted request as if completion is returned with UR if the completion is not returned before its Completion Timeout Timer is expired. 0 = Disable Completion Timeout Timer 1 = Enable Completion Timeout Timer	R/W	1
30:00	CPL_TO_VALUE	Completion Timeout Value This 31-bit register defines the Completion Timeout Value as follows: 0x0000_0000 = 0 ns 0x0000_0001 = 16 ns 0x0000_0002 = 32 ns 0x0000_0003 = 48 ns ----- 0x0009_8968 = 10 ms (default value) 0x7FFF_FFFF = 34 s	R/W	0x009_8968

### 14.3.19 Clock Out Enable Function and Debug Register

Register name: CLKOUT_ENB_FUNC_DBG Reset value: 0x0000_1F00	Register offset: 0x054
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved			CLKOUT_ENB				
07:00	Reserved						FUNC_DBG	

Bits	Name	Description	Type	Reset value
31:13	Reserved	Reserved.	R	0
12:08	CLKOUT_ENB	This field enables and disables the five clocks (PCI_CLK_OUT[4:0]) supplied to the PCI secondary devices. <u>CLKOUT_ENB[0]</u> 0 = Disable PCI_CLK_OUT[0] 1 = Enable PCI_CLK_OUT[0] <u>CLKOUT_ENB[1]</u> 0 = Disable PCI_CLK_OUT[1] 1 = Enable PCI_CLK_OUT[1] <u>CLKOUT_ENB[2]</u> 0 = Disable PCI_CLK_OUT[2] 1 = Enable PCI_CLK_OUT[2] <u>CLKOUT_ENB[3]</u> 0 = Disable PCI_CLK_OUT[3] 1 = Enable PCI_CLK_OUT[3] <u>CLKOUT_ENB[4]</u> 0 = Disable PCI_CLK_OUT[4] 1 = Enable PCI_CLK_OUT[4]	R/W	11111
07:02	Reserved	Reserved	R	0
01	UNLOCK	Setting this bit to 0b1 allows register bits with an RWL attribute to be written from TLPs, i.e. configuration or memory writes. Register bits with RWL attribute can always be written from EEPROM or JTAG regardless of the setting of this bit.	R/W	0
00	FUNC_DBG	This bit is for functional testing. Setting to 0b1 disables scrambling.	R/W	0



### 14.3.20 SERRDIS\_OPQEN\_DTC Register

Register name: SERRDIS_OPQEN_DTC Reset value: 0x0000_0100	Register offset: 0x058
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved					ST_DIST_EN	Reserved	SEC_DIST_EN
07:00	Reserved							

Bits	Name	Description	Type	Reset value
31:11	Reserved	Reserved	R	0
10	ST_DIST_EN	Short Term Discard Timer Enable 0 = Secondary discard timer value sets to either 0x03FF (1K PCI clock cycles) or 0x7FFF (32 K PCI clock cycles) 1 = Secondary discard timer value sets to 0x003F (64 PCI clock cycles)	R/W	0
9	Reserved	Reserved	R	0
8	SEC_DIST_EN	Secondary Discard Timer Enable 0 = Disable Secondary Discard Timer 1 = Enable Secondary Discard Timer	R/W	1
7:0	Reserved	Reserved	R	0

## 14.4 Upstream Non-transparent Address Remapping Registers

The PEB383 supports address remapping, which is one of the requirements of non-transparent bridging. All transactions that fall in the non-transparent address range are mapped to different address locations according to following device-specific registers.

### 14.4.1 NTMA Control Register

Register name: NTMA_CTRL Reset value: 0x0000_0000	Register offset: 0x068
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_LBA							
23:16	NTMA_LBA				Reserved			
15:08	Reserved							
07:00	Reserved				NTMA_RMP	Reserved		

Bits	Name	Description	Type	Reset value
31:20	NTMA_LBA	NTMA primary lower base address.	R/W	0x0
19:04	Reserved	Reserved	R	0x0
03	NTMA_RMP	0 = Disable NTMA address remapping. 1 = Enable NTMA address remapping.	R/W	0x0
02:00	Reserved	Reserved	R	0x0

### 14.4.2 NTMA Primary Upper Base Register

Register name: NTMA_PRI_BASEUPPER Reset value: 0x0000_0000	Register offset: 0x06C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_UBA							
23:16	NTMA_UBA							
15:08	NTMA_UBA							
07:00	NTMA_UBA							

Bits	Name	Description	Type	Reset value
31:00	NTMA_UBA	NTMA Primary upper base address.	R/W	0x0

### 14.4.3 NTMA Secondary Lower Base Register

Register name: NTMA_SEC_LBASE Reset value: 0x0000_0000	Register offset: 0x070
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_LBA							
23:16	NTMA_LBA				Reserved			
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset value
31:20	NTMA_LBA	NTMA Secondary lower base address.	R/W	0x0
19:00	Reserved	Reserved	R	0x0

#### 14.4.4 NTMA Secondary Upper Base Register

Register name: NTMA_SEC_BASEUPPER Reset value: 0x0000_0000	Register offset: 0x074
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_UBA							
23:16	NTMA_UBA							
15:08	NTMA_UBA							
07:00	NTMA_UBA							

Bits	Name	Description	Type	Reset value
31:00	NTMA_UBA	NTMA Secondary upper base address.	R/W	0x0

#### 14.4.5 NTMA Secondary Lower Limit Register

Register name: NTMA_SEC_LOWER_LIMIT Reset value: 0x0000_0000	Register offset: 0x078
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_LLA							
23:16	NTMA_LLA				Reserved			
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset value
31:20	NTMA_LLA	NTMA Secondary lower limit address.	R/W	0x0
19:00	Reserved	Reserved	R	0x0

### 14.4.6 NTMA Secondary Upper Limit Register

Register name: NTMA_SEC_UPPER_LIMIT Reset value: 0x0000_0000	Register offset: 0x07C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NTMA_ULA							
23:16	NTMA_ULA							
15:08	NTMA_ULA							
07:00	NTMA_ULA							

Bits	Name	Description	Type	Reset value
31:00	NTMA_ULA	NTMA Secondary Upper limit address.	R/W	0x0

## 14.5 PCI Capability Registers

The PEB383 device supports PCI and PCIe extended capabilities options. The Capabilities Pointer field in the “[PCI Capability Pointer Register](#)” (0x034) points to the first PCI capabilities option, while the first PCIe extended capability option is always located at 0x100 (see “[PCIe Advanced Error Reporting Capability Register](#)”).



When the PEB383 operates in “[Legacy Mode](#)” the following registers are not supported and are treated as reserved:

- “[PCIe Capability Registers](#)”
- “[Advanced Error Reporting Capability Registers](#)”

### 14.5.1 SSID/SSVID Capability

The optional “[SSID ID Register](#)” — Subsystem ID (SSID) and Subsystem Vendor ID (SSVID) ID — uniquely identifies the add-in card or subsystem where the PCI device resides. It provides a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI bridge on them (and, therefore, the same Vendor ID and Device ID).

Values in this register must be loaded and valid prior to system software accessing the PCI configuration space.

Note that by default, the SSID capability is not linked in via “[PCI Capability Pointer Register](#)”. This capability must be linked in first, before the SSID ID Register can be written.

## 14.5.2 SSID Capability Register

Register name: SSID_CAP Reset value: 0x0000_A00D	Register offset: 0x060
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	CAP_PTR							
07:00	CAP_ID							

Bits	Name	Description	Type	Reset value
31:16	Reserved	Reserved	R	0x0
15:08	CAP_PTR	Capabilities Pointer This register contains the head pointer for the capability list in PCI configuration space.	R	0xA0
07:00	CAP_ID	Capability ID	R	0x0D

### 14.5.3 SSID ID Register

The values in this register can be written by EEPROM.

Register name: <b>SSID_ID</b> Reset value: <b>0x0000_0000</b>	Register offset: <b>0x064</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	SSID							
23:16	SSID							
15:08	SSVID							
07:00	SSVID							

Bits	Name	Description	Type	Reset value
31:16	SSID	Sub System ID This value identifies the add-in card or subsystem, and is assigned by the vendor.	RWL	0
15:0	SSVID	Sub System vendor ID This value identifies the manufacturer of the add-in card or subsystem.	RWL	0

### 14.5.4 PCI Power Management Capability Register

This register defines bytes 0 to 3 of the power management capability option.

Register name: PCI_PMC Reset value: 0x7803_C001	Register offset: 0x0A0
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	PME_SUP					D2_SP	D1_SP	AUX_CUR
23:16	AUX_CUR	DSI	Reserved	PME_CK	PM_VER			
15:08	NXT_PTR							
07:00	CAP_ID							

Bits	Name	Description	Type	Reset value
31:27	PME_SUP	<p>PME Support</p> <p>This field indicates the power management states from which the PEB383 device can indicate PME#.</p> <p>The value reported by this field is based on Serial EEPROM programming that indicates how auxiliary power is routed to the PEB383 device in the system.</p> <p>Given the right power supplies, the PEB383 can assert the PME# signals in D3<sub>COLD</sub>.</p> <p>In the absence of Serial EEPROM information, the PEB383 will report PME support for power levels down to D3<sub>HOT</sub>.</p>	RWL	01111
26	D2_SP	<p>D2 Support</p> <p>This field always returns 0 since the PEB383 does not support the D2 power management state.</p>	R	0
25	D1_SP	<p>D1 Support</p> <p>This field always returns 0 since the PEB383 does not support the D1 power management state.</p>	R	0
24:22	AUX_CUR	<p>Aux Current</p> <p>This field returns a value 0 indicating the device is self powered.</p>	R	000
21	DSI	<p>Device Specific Initialization</p> <p>Hardwired to 0. No special initialization is required.</p>	R	0
20	Reserved	Reserved. It always reads 0.	R	0
19	PME_CK	<p>PME Clock</p> <p>This field is not applicable to devices with a PCIe Interface. It always reads 0.</p>	R	0



*(Continued)*

Bits	Name	Description	Type	Reset value
18:16	PM_VER	Version This field indicates a version number of 011 indicating it supports the <i>PCI Bus Power Management Interface Specification (Revision 1.2)</i> .	R	011
15:8	NXT_PTR	Next Pointer This field points to the next capability option: " <b>PCIe Capabilities Register</b> " (0x0C0). Note: This read-only value will be changed to 0x00 when the LEGACY bit is set to 1 in the " <b>PCI Miscellaneous Clock Straps Register</b> ".	R	0xC0
7:0	CAP_ID	Capability ID This field contains the value 0x01 indicating a power management capability option.	R	0x01

### 14.5.5 PCI Power Management Control and Status Register

This register defines the control and status registers of the power management capability option.

Register name: PCI_PMCS Reset value: 0x0000_0008	Register offset: 0x0A4
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	DATA							
23:16	BPCCE	B2B3S	Reserved					
15:08	PME_ST	DATA_SC		DATA_SEL			PME_EN	
07:00	Reserved			NO_SOFT_RST	Reserved	PWR_ST		

Bits	Name	Description	Type	Reset value
31:24	DATA	Power Data The PEB383 does not support the Power Data field.	R	0x00
23	BPCCE	BPCC_En (Bus Power/Clock Control Enable) - A "1" indicates that the bus power/clock control mechanism as defined in Section 4.7.1 is enabled. A "0" indicates that the bus power/clock control policies defined in Section 4.7.1 have been disabled. When the Bus Power/Clock Control mechanism is disabled, the bridge's PMCSR PowerState field cannot be used by the system software to control the power or clock of the bridge's secondary bus. This bit will be set if "PCGE" is set in "PCI Miscellaneous Clock Straps Register", and the PCI_CLK is 33MHz or less.	R	0x0
22	B2B3S	B2_B3# (B2/B3 support for D3hot) - The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A "1" indicates that when the bridge function is programmed to D3hot, its secondary bus's PCI clock will be stopped (B2). A "0" indicates that when the bridge function is programmed to D3hot, its secondary bus will have its power removed (B3). This bit is only meaningful if bit 7 (BPCC_En) is a "1". This bit will be set if "PCGE" is set in "PCI Miscellaneous Clock Straps Register", and the PCI_CLK is 33MHz or less.	R	0x0
21:16	Reserved	Reserved. It always reads 0.	R	0x0

*(Continued)*

Bits	Name	Description	Type	Reset value
15	PME_ST	<p>Power PME Status</p> <p>This field indicates whether this device can generate PME#. This field's value is independent of whether the Power PME Enable field is set to 1.</p> <p>0 = No PME# is being asserted by this PCI function.</p> <p>1 = A PME# status is reported by this PCI function. If PME_EN is also set to 1, this PCI function is also asserting the PME# signal. Writing 1 to this field clears the field.</p> <p>Note: The PEB383 does not support this feature; this bit always returns a 0.</p>	R	0
14:13	DATA_SC	<p>Power Data Scale</p> <p>This field always returns 0 since the PEB383 device does not support the DATA field.</p>	R	00
12:9	DATA_SEL	<p>Power Data Select</p> <p>This field always returns 0 since the PEB383 device does not support the DATA field.</p>	R	0x0
8	PME_EN	<p>Power PME Enable</p> <p>This field enables PME# assertion. The initial value of this field depends on whether the device woke from power-off or D3<sub>COLD</sub>.</p> <ul style="list-style-type: none"> <li>From power-off, this field starts disabled.</li> <li>From D3<sub>COLD</sub>, this field contains the enable condition going into the D3<sub>COLD</sub> state.</li> </ul> <p>0 = Disable PME# generation.</p> <p>1 = Enable PME# generation.</p>	R/W	0
7:4	Reserved	Reserved 1. It always reads 0.	R	0x0
3	NO_SOFT_RST	<p>Power No Soft Reset</p> <p>This field indicates whether the device needs a soft reset after transitioning from D3<sub>HOT</sub> to D0. This field always returns 1 indicating a soft reset is not required.</p>	R	1
2	Reserved	Power Reserved 0. It always reads 0.	R	0
1:0	PWR_ST	<p>Power State</p> <p>This field determines the current power state of the PCI function, and sets a new state. If the new state is not supported, the change is ignored.</p> <p>00 = D0</p> <p>01 = D1</p> <p>10 = D2</p> <p>11 = D3<sub>HOT</sub></p>	R/W	0

### 14.5.6 EEPROM Control Register

Register name: EE_CTRL Reset value: Undefined	Register offset: 0x0AC
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		CMD		ADD_WIDTH		BUSY	CMD_VLD
23:16	ADD							
15:08	ADD							
07:00	DATA							

Bits	Name	Description	Type	Reset value
31:30	Reserved	Reserved	R	0x0
29:28	CMD	Command 01 = Read 10 = Write	R/W	0x0
27:26	ADD_WIDTH	Address width This field indicates the address width of the serial EEPROM, and whether or not an EEPROM device is present. 00 = No EEPROM 01 = 9-bit address 10 = 16-bit address Note: A blank EEPROM is indicated with 0b00. If this occurs, these bits must be written with the appropriate values before the EEPROM can be accessed.	R/W	Undefined
25	BUSY	This bit indicates the serial EEPROM is busy with Read/Write operation. Software must poll this bit before initiating a write/read to the external EEPROM through a configuration write to the "EEPROM Control Register". For information on software polling, see "System Diagram".	R	0x0
24	CMD_VLD	This bit validates the command and side-band signals to the serial EEPROM.	R/W	0x0
23:08	ADD	Address This is the EEPROM address to be read from or written into.	R/W	0x0000
07:00	DATA	DATA This is the data to be written into the EEPROM.	R/W	0x00

### 14.5.7 Secondary Bus Device Mask Register

This register provides a method to support private devices on the PCI bus. The process of converting Type 1 configuration transactions to Type 0 configuration transactions is modified by the contents of this register. A configuration transaction that targets a device masked by this register is rerouted to device 15. Setting this register to all zeros disables device masking.

<b>Register name: SBUS_DEVMSK</b> <b>Reset value: 0x0000_0000</b>	<b>Register offset: 0x0B0</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		DEVMSK_13	Reserved			DEVMSK_9	Reserved
23:16	DEVMSK_7	DEVMSK_6	DEVMSK_5	DEVMSK_4	Reserved		DEVMSK_1	Reserved
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset Value
31:30	Reserved	Reserved	R	0
29	DEVMSK_13	Device Mask 13 0 = Rerouting disabled for device 13. 1 = Block assertion of PCI_AD (Pin 29) for configuration transactions to device 13, assert pin PCI_AD (Pin 31) instead.	R/W	0
28:26	Reserved	Reserved. Masking for devices 12, 11, and 10 is not implemented. Operation of the PEB383 is unaffected by the value of these bits.	R	0
25	DEVMSK_9	Device Mask 9 0 = Rerouting disabled for device 9. 1 = Block assertion of PCI_AD (Pin 25) for configuration transactions to device 9, assert pin PCI_AD (Pin 31) instead.	R/W	0
24	Reserved	Reserved. Masking for device 8 is not implemented. Operation of the PEB383 is unaffected by the value of this bit.	R	0
23	DEVMSK_7	Device Mask 7 0 = Rerouting disabled for device 7. 1 = Block assertion of PCI_AD (Pin 23) for configuration transactions to device 7, assert pin PCI_AD (Pin 31) instead.	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset Value
22	DEVMSK_6	Device Mask 6 0 = Rerouting disabled for device 6. 1 = Block assertion of PCI_AD (Pin 22) for configuration transactions to device 6, assert pin PCI_AD (Pin 31) instead.	R/W	0
21	DEVMSK_5	Device Mask 5 0 = Rerouting disabled for device 5. 1 = Block assertion of PCI_AD (Pin 21) for configuration transactions to device 5, assert pin PCI_AD (Pin 31) instead.	R/W	0
20	DEVMSK_4	Device Mask 4 0 = Rerouting disabled for device 4. 1 = Block assertion of PCI_AD (Pin 20) for configuration transactions to device 4, assert pin PCI_AD (Pin 31) instead.	R/W	0
19:18	Reserved	Reserved. Masking for devices 3 and 2 is not implemented. Operation of the PEB383 is unaffected by the value of these bits.	R	0
17	DEVMSK_1	Device Mask 1 0 = Rerouting disabled for device 1. 1 = Block assertion of PCI_AD (Pin 17) for configuration transactions to device 1, assert pin PCI_AD (Pin 31) instead.	R/W	0
16:0	Reserved	Reserved. Operation of the PEB383 is unaffected by the value of these bits.	R	0

### 14.5.8 Short-term Caching Period Register

Register name: <b>STERM_CACHING_PERIOD</b> Reset value: <b>0x0000_0040</b>	Register offset: <b>0x0B4</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	ST_CACHE							
23:16	ST_CACHE							
15:08	ST_CACHE							
07:00	ST_CACHE							

Bits	Name	Description	Type	Reset value
31:00	ST_CACHE	Short Term caching period This field indicates the number of PCI clock cycles allowed before short-term caching is discarded.	R/W	0x0000_0040

### 14.5.9 Retry Timer Status Register

Register name: <b>TIMER_STATUS</b> Reset value: <b>0x0000_0000</b>	Register offset: <b>0x0B8</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							
07:00	Reserved					SEC_DIS_STAT	Reserved	SEC_R_STAT

Bits	Name	Description	Type	Reset value
31:03	Reserved	Reserved	R	0x0
2	SEC_DIS_STAT	Secondary Discard Timer status For more information on this timer, see DISCARD2 in "PCI Bridge Control and Interrupt Register". 0 = Secondary discard timer has not expired. 1 = Secondary discard timer has expired.	R	0
1	Reserved	Reserved	R	0
0	SEC_R_STAT	Secondary Retry timer status For more information on this timer, see "Secondary Retry Count Register". 0 = Secondary retry timer has not expired 1 = Secondary retry timer has expired	R	0



### 14.5.10 Prefetch Control Register

Register name: <b>PREF_CTRL</b> Reset value: <b>0x0300_0041</b>	Register offset: <b>0x0BC</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved					P_MR	P_MRL	P_MRM
23:16	MRL_66						MRL_33	
15:08	MRL_33				MRM_66			
07:00	MRM_66			MRM_33				

Bits	Name	Description	Type	Reset value
31:27	Reserved	Reserved	R	0x00
26	P_MR	0 = The PEB383 fetches a Dword of data in case of 32-bit PCI data bus mode. 1 = The PEB383 prefetches as per the value specified in MRL_66/MRL_33 fields on behalf of the PCI master for memory read command.	R/W	0
25	P_MRL	0 = The PEB383 prefetches one cacheline of data. 1 = The PEB383 prefetches as per the value specified in MRL_66/MRL_33 fields on behalf of the PCI master for memory read line command.	R/W	1
24	P_MRM	0 = The PEB383 prefetches two cachelines of data. 1 = The PEB383 prefetches as per the value specified in MRM_66/MRM_33 fields on behalf of PCI master for memory read multiple command.	R/W	1
23:18	MRL_66	This bit indicates the threshold parameter for Memory read line and memory read commands in 66-MHz PCI mode. Unit is 64-byte chunk. 6'h00 = 64 bytes 6'h01 = 128 bytes ... 6'h3F = 4096 bytes	R/W	0x00
17:12	MRL_33	This bit indicates the threshold parameter for Memory read line and memory read commands in 33-MHz PCI mode. Unit is 64-byte chunk. 6'h00 = 64 bytes 6'h01 = 128 bytes ... 6'h3F = 4096 bytes	R/W	0x00

*(Continued)*

Bits	Name	Description	Type	Reset value
11:6	MRM_66	This bit indicates the threshold parameter for Memory read multiple command in 66-MHz PCI mode. Unit is 64-byte chunk. 6'h00 = 64 bytes 6'h01 = 128 bytes ... 6'h3F = 4096 bytes	R/W	0x01
5:0	MRM_33	This bit indicates the threshold parameter for Memory read multiple command in 33-MHz PCI mode. Unit is 64-byte chunk. 6'h00 = 64 bytes 6'h01 = 128 bytes ... 6'h3F = 4096 bytes	R/W	0x01

## 14.6 PCIe Capability Registers

In the PEB383, the PCIe capability is located in PCI 2.3 configuration space at 0x0C0 and contains 20 bytes.



When the PEB383 operates in “Legacy Mode” the following registers are not supported and are treated as reserved:

- “PCIe Capability Registers”
- “Advanced Error Reporting Capability Registers”

### 14.6.1 PCIe Capabilities Register

The PCIe capabilities register defines bytes 0 to 3 of the PCIe capability option.

<b>Register name:</b> PCIE_CAP <b>Reset value:</b> 0x0071_0010	<b>Register offset:</b> 0x0C0
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		INT_MN				SLOT_IMP	
23:16	DP_TYPE			CAP_VER				
15:08	NXT_PTR							
07:00	CAP_ID							

Bits	Name	Description	Type	Reset value
31:30	Reserved	PCIe Reserved. It always reads 0.	R	00
29:25	INT_MN	PCIe Interrupt Message Number The PEB383 device does not have slot status or root port status. It always reads 0.	R	00000
24	SLOT_IMP	PCIe Slot Implemented This field is not applicable for a bridge device. It always reads 0.	R	0
23:20	DP_TYPE	PCIe Device Port Type This field indicates the device is a PCIe bridge device.	R	0111
19:16	CAP_VER	PCIe Capability Version This field returns a version number of 1 indicating it supports PCIe 1.1 capabilities.	R	0001
15:08	NXT_PTR	Next Pointer This field points to the next capability option. In the PEB383, this will contain a value of 0x00 indicating there are no more PCI compatible capabilities options.	R	0x00

*(Continued)*

Bits	Name	Description	Type	Reset value
07:00	CAP_ID	Capability ID This field contains the value 0x10 indicating a PCIe capability option.	R	0x10

## 14.6.2 PCIe Device Capabilities Register

This register defines bytes 4 to 7 of the PCIe capability option.

Register name: PCIE_DEV_CAP Reset value: 0x0000_8000	Register offset: 0x0C4
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved			PL_SCL		PL_VAL		
23:16	PL_VAL						Reserved	
15:08	ROL_BAS_ERR_REP	Reserved			L1_LAT			LOS_LAT
07:00	LOS_LAT		EXT_TAG	PH_FUNC		MAX_SIZE		

Bits	Name	Description	Type	Reset value
31:28	Reserved	PCIe Reserved. It always reads 0.	R	0000
27:26	PL_SCL	PCIe Captured Slot Power Limit Scale This field specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x This value is set by the Set_Slot_Power_Limit Message. The default value is 00.	R	00
25:18	PL_VAL	PCIe Captured Slot Power Limit Value In combination with the Slot Power Limit Scale value, this field specifies the upper limit on power supplied by the slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message. The default value is 0x00.	R	0x00
17:16	Reserved	PCIe Reserved. It always reads 0.	R	000
15	ROL_BAS_ERR_REP	Role-based Error Reporting This bit, when set, indicates that the device uses the functionality defined in the Error Reporting ECN for the <i>PCIe Base Specification, (Revision 1.0a)</i> , and later incorporated into the <i>PCI Express Base Specification (Revision 1.1)</i> . This bit must be set by all devices conforming to the ECN, PCIe 1.1 Specification, or subsequent PCIe Base Specification revisions.	R	1

*(Continued)*

Bits	Name	Description	Type	Reset value
14:12	Reserved	The Value read from these bits is 0b000. Previous version of the PCI specification had defined these bits, they are now defined as read only, and return 0b000. System software is permitted to write any value to these bits.	R	000
11:9	L1_LAT	PCIe Endpoint L1 Acceptable Latency This field indicates the acceptable latency for transition from L1 to L0 state. This field is set to 0b000 since the PEB383 is not an endpoint.	R	000
8:6	L0S_LAT	PCIe Endpoint L0s Acceptable Latency This field indicates the acceptable latency for transition from L0s to L0 state. This field is set to 0b000 since the PEB383 is not an endpoint.	R	000
5	EXT_TAG	PCIe Extended Tag Field Supported This field contains the value 0 indicating 5-bit tag fields are supported.	R	0
4:3	PH_FUNC	PCIe Phantom Functions Supported This field is 0 indicating no phantom functions are used.	R	00
2:0	MAX_SIZE	PCIe Maximum Payload Size Supported 000 = 128 bytes	R	000

### 14.6.3 PCIe Device Control and Status Register

This register defines bytes 8 to 11 of the PCIe capability option.

Register name: PCIE_DEV_CSR Reset value: 0x0000_2000	Register offset: 0x0C8
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved		TRAN_PND	AUX_PWR_DTD	UNS_REQ_DTD	FTL_ERR_DTD	NFTL_ERR_DTD	COR_ERR_DTD
15:08	CFG_RETR_Y_EN	MAX_RD_SIZE			EN_SNP_NREQ	AUX_PWR_PM_EN	PHN_EN	EXT_TAG_EN
07:00	MAX_PAY_SIZE			EN_RLX_ORD	UNS_REQ_EN	FTL_ERR_EN	NFTL_ERR_EN	COR_ERR_EN

Bits	Name	Description	Type	Reset value
31:22	Reserved	PCIe Reserved. It always reads 0.	R	0x000
21	TRAN_PND	PCIe Transaction Pending This field indicates the PEB383 issued Non-Posted Requests that have not been completed. 0 = No pending completion of Non-Posted Requests. 1 = Pending completion of Non-Posted Requests.	R	0
20	AUX_PWR_DTD	PCIe Aux Power Detected This field indicates whether the PEB383 detected AUX power. The PEB383, however, does not require the Auxiliary Power. 0 = No Aux power detected. 1 = Aux power detected.	R	0
19	UNS_REQ_DTD	PCIe Unsupported Request Detected This field indicates whether an unsupported request was detected. 0 = No error detected. 1 = Error detected. Writing 1 clears this error.	R/W1C	0
18	FTL_ERR_DTD	PCIe Fatal Error Detected This field indicates whether a fatal error was detected. 0 = No error detected. 1 = Error detected. Writing 1 clears this error.	R/W1C	0

*(Continued)*

Bits	Name	Description	Type	Reset value
17	NFTL_ERR_DTD	PCIe Non-Fatal Error Detected This field indicates whether a non-fatal error was detected. 0 = No error detected. 1 = Error detected. Writing 1 clears this error.	R/W1C	0
16	COR_ERR_DTD	PCIe Correctable Error Detected This field indicates whether a correctable error was detected. 0 = No error detected. 1 = Error detected. Writing 1 clears this error.	R/W1C	0
15	CFG_RETRY_EN	Bridge Configuration Retry Enable 0 = Disable the PEB383 to return Configuration Request Retry Status (CRS) in response to Configuration Requests to the target devices below the bridge. 1 = Enable the PEB383 to return Configuration Request Retry Status (CRS) in response to Configuration Requests to the target devices below the bridge.	R/W	0
14:12	MAX_RD_SIZE	PCIe Max Read Request Size This field sets the maximum read request size for the PEB383 as a requestor. 000 = 128 bytes 001 = 256 bytes 010 = 512 bytes 011 = 1024 bytes 100 = 2048 bytes 101 = 4096 bytes 110-111 = Reserved.	R/W	010
11	EN_SNP_NREQ	PCIe Enable Snoop Not Required The PEB383 does not set the No Snoop attribute. This bit is hardwired to 0.	R	0
10	AUX_PWR_PM_EN	PCIe Aux Power PM Enable When this bit is set the PEB383 can draw AUX power independent of PME AUX power. 0 = Do not allow use of AUX power other than PME AUX. 1 = Allow use of AUX power other than PME AUX.	R/W	0
9	PHN_EN	PCIe Phantom Functions Enable The PEB383 does not use phantom functions. This bit always returns 0.	R	0
8	EXT_TAG_EN	PCIe Extended Tag Field Enable The PEB383 does not support extended tag fields. This bit always returns 0.	R	0



*(Continued)*

Bits	Name	Description	Type	Reset value
7:5	MAX_PAY_SIZE	PCIe Maximum Payload Size This field indicates the maximum payload size that can be used for data transmission by the PEB383. This must be a subset of the size reported by MAX_SIZE in “ <a href="#">PCIe Device Capabilities Register</a> ”. 000-111 = 128 bytes	R/W	000
4	EN_RLX_ORD	PCIe Enable Relaxed Ordering This field controls whether relaxed ordering for transactions is enabled. 0 = Relaxed ordering is disabled. 1 = Relaxed ordering is enabled.	R	0
3	UNS_REQ_EN	PCIe Unsupported Request Reporting Enable This field controls reporting of unsupported requests. 0 = No error reporting. 1 = Error reporting enabled.	R/W	0
2	FTL_ERR_EN	PCIe Fatal Error Reporting Enable This bit, in conjunction with other bits, controls sending ERR_FATAL messages (for more information, see <a href="#">Figure 22</a> ). 0 = No error reporting. 1 = Error reporting enabled.	R/W	0
1	NFTL_ERR_EN	PCIe Non-Fatal Error Reporting Enable This bit, in conjunction with other bits, controls sending ERR_NONFATAL messages (for more information, see <a href="#">Figure 22</a> ). 0 = No error reporting. 1 = Error reporting enabled.	R/W	0
0	COR_ERR_EN	PCIe Correctable Error Reporting Enable This bit, in conjunction with other bits, controls sending ERR_COR messages (for more information, see <a href="#">Figure 22</a> ). 0 = No error reporting. 1 = Error reporting enabled.	R/W	0

### 14.6.4 PCIe Link Capabilities Register

Register name: PCIE_LNK_CAP Reset value: 0x0001_3C11	Register offset: 0x0CC
---	------------------------

Bits	7	6	5	4	3	2	1	0	
31:24	PORT_NUM								
23:16	Reserved			DLL_LNK_ ACT_REP_ CAP	SRP_DWN_ _ERR_REP_ _CAP	CLK_PWR_ MGT	L1_EXIT		
15:08	L1_EXIT	LOS_EXIT			ASPM		MAX_WIDTH		
07:00	MAX_WIDTH				MAX_SPEED				

Bits	Name	Description	Type	Reset value
31:24	PORT_NUM	PCIe Port Number The PEB383 always reports a port number of 0 for this field.	R	0x00
23:21	Reserved	PCIe Reserved. This field always reads 0.	R	0x00
20	DLL_LNK_ACT_ REP_CAP	Data Link Layer Link Active Reporting Capable For a downstream port, this bit must be set to 1 if the component can report the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable downstream port, this bit must be set to 1. For upstream ports and components that do not support this capability, this bit must be hardwired to 0. Note: The PEB383 does not support DLL_LNK_ACT_REP_CAP. This field always reads 0.	R	0
19	SRP_DWN_ERR_ REP_CAP	Surprise Down Error Reporting Capable For a downstream port, this bit must be set to 1 if the component can detect and report a Surprise Down error condition. For upstream ports and components that do not support this capability, this bit must be hardwired to 0. Note: The PEB383 does not support SRP_DWN_ERR_REP_CAP. This field always reads 0.	R	0

*(Continued)*

Bits	Name	Description	Type	Reset value
18	CLK_PWR_MGT	<p>Clock Power Management</p> <p>0 = The component does not have this capability, and the reference clock(s) must not be removed in these link states.</p> <p>1 = The component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the link is in the L1 and L2/3 Ready link states.</p> <p>This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability.</p> <p>For a multifunction device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicates a 1 in this bit.</p> <p>Note: The PEB383 does not support CLK_PWR_MGT. This field always reads 0.</p>	R	0
17:15	L1_EXIT	<p>PCIe L1 Exit Latency</p> <p>L1 exit latency is between 2 and 4 us.</p>	RWL	010
14:12	L0S_EXIT	<p>PCIe L0s Exit Latency</p> <p>The PEB383 L0s exit latency will be as 256-512ns which will be reported as 0b011. This value can be overwritten by the serial EEPROM.</p> <p>000 = Less than 64 ns  001 = 64 ns to less than 128 ns  010 = 128 ns to less than 256 ns  011 = 256 ns to less than 512 ns  100 = 512 ns to less than 1 us  101 = 1 us to less than 2us  110 = 2-4 us  111 = More than 4 us</p>	RWL	011
11:10	ASPM	<p>PCIe ASPM Support</p> <p>The PEB383 supports the L0s and L1 ASPM state. This field always returns 11.</p>	R	11
09:04	MAX_WIDTH	<p>PCIe Maximum Link Width</p> <p>This field indicates the maximum number of PCIe lanes that can be used for communicating with the PEB383.</p> <p>0x01 = 1 PCIe lane</p>	R	0x01
03:00	MAX_SPEED	<p>PCIe Maximum Link Speed</p> <p>This field is always 1 indicating a 2.5-Gbps link.</p>	R	0x1

### 14.6.5 PCIe Link Control Register

This register defines bytes 16 to 17 of the PCIe capability option.

<b>Register name: PCIE_LNK_CSR</b> <b>Reset value: 0x0011_0000</b>	<b>Register offset: 0x0D0</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		DLL_LNK_ACT	SLT_CLK_CONFIG	Reserved		NEG_LNK_WIDTH	
23:16	NEG_LNK_WIDTH				LNK_SPEED			
15:08	Reserved							
07:00	E_SYNC	COM_CLK	RETRAIN	LNK_DIS	RCB	Reserved	ASPM_CTL	

Bits	Name	Description	Type	Reset value
31:30	Reserved	Reserved	R	00
29	DLL_LNK_ACT	Data Link Layer Active. This bit indicates the status of the Data Link Control and Management State Machine. This bit is hardwired to 0.	R	0
28	SLT_CLK_CONFIG	Slot Clock Configuration. This bit indicates the PEB383 uses the same physical reference clock that the platform provides on the connector.  This bit can be loaded from the serial EEPROM as part of the PCB configuration information.	R	0
27:26	Reserved	Reserved	R	0
25:20	NEG_LNK_WIDTH	Negotiated Link Width. This field indicates the negotiated width of the PCIe Link. 000001 = x1 lane	R	0x01
19:16	LNK_SPEED	Link Speed. This field indicates the negotiated Link Speed of the PCIe Link. 0001 = 2.5-Gbps PCIe Link	R	0x1
15:8	Reserved	Reserved	R	0x00
7	E_SYNC	PCIe Extended Synchronization  This field is normally only used when attempting to capture the PCIe link on an analyzer since it allows the synchronization cycle to be extended allowing the analyzer to synchronize to the link.  0 = Normal operation. 1 = Enable extended synchronization	R/W	0

*(Continued)*

Bits	Name	Description	Type	Reset value
6	COM_CLK	<p>PCIe Common Clock Configuration</p> <p>This field selects between a distributed common reference clock or an asynchronous reference clock. After setting both ends of the link to the same value, the link must be retrained from the bridge side of the link.</p> <p>Components use this common clock configuration information to report the correct L0s and L1 Exit Latencies.</p> <p>0 = Asynchronous reference clock 1 = Distributed common reference clock</p>	R/W	0
5	RETRAIN	<p>PCIe Retrain Link</p> <p>This field is reserved for a bridge device. It always reads 0.</p>	R	0
4	LNK_DIS	<p>PCIe Link Disable</p> <p>This field is reserved for a bridge device. It always reads 0.</p>	R	0
3	RCB	<p>PCIe Read Completion Boundary</p> <p>This field is set by system software to indicate the read completion boundary value of the upstream root port.</p> <p>0 = 64 bytes 1 = 128 bytes</p>	R/W	0
2	Reserved	PCIe Reserved. It always reads 0.	R	0
1:0	ASPM_CTL	<p>PCIe ASPM Control</p> <p>This field enables different levels of ASPM.</p> <p>00: Disabled 01 :L0s Entry enabled 10: L1 entry enabled 11: L0s and L1 entry enabled</p>	R/W	00

## 14.7 Downstream Non-transparent Address Remapping Registers

### 14.7.1 Secondary Bus Non-prefetchable Address Remap Control Register

Register name: AR_SBNPCTRL Reset value: 0x0000_0000	Register offset: 0x0E4
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	SEC_NP_LBASE							
23:16	SEC_NP_LBASE				Reserved			
15:08	Reserved			IO_SIZE				
07:00	Reserved			NP_REMA PP_EN		Reserved		

Bits	Name	Description	Type	Reset value
31:20	SEC_NP_LBASE	Secondary non-prefetchable lower base.	R/W	0x000
19:13	Reserved	Reserved.	R	0x00
12:8	IO_SIZE	This field describes how many upper bits of a downstream I/O address are discarded.	R/W	0x00
7:4	Reserved	Reserved.	R	0x0
3	NP_REMAP_EN	1 = Enable non-prefetchable address remapping	R/W	0x0
2:0	Reserved	Reserved.	R	0x0

### 14.7.2 Secondary Bus Non-prefetchable Upper Base Address Remap Register

Register name: AR_SBNPBASE Reset value: 0x0000_0000	Register offset: 0x0E8
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	SEC_NP_UBA							
23:16	SEC_NP_UBA							
15:08	SEC_NP_UBA							
07:00	SEC_NP_UBA							

Bits	Name	Description	Type	Reset value
31:00	SEC_NP_UBA	Secondary bus non-prefetchable upper base.	R/W	0x000

### 14.7.3 Secondary Bus Prefetchable Address Remap Control Register

Register name: AR_SBPPRECTRL Reset value: 0x0000_0000	Register offset: 0x0EC
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	SEC_PRE_LBA							
23:16	SEC_PRE_LBA				Reserved			
15:08	Reserved							
07:00	Reserved				PRE_REMAP AP_EN	Reserved		

Bits	Name	Description	Type	Reset value
31:20	SEC_PRE_LBA	Secondary bus prefetchable lowerbase.	R/W	0x000
19:4	Reserved	Reserved.	R	0x0000
3	PRE_REMAP_EN	0 = Disable prefetchable address remapping 1 = Enable prefetchable address remapping	R/W	0x0
2:0	Reserved	Reserved.	R	0x0

### 14.7.4 Secondary Bus Prefetchable Upper Base Address Remap Register

Register name: AR_SBPBASEUPPER Reset value: 0x0000_0000	Register offset: 0x0F0
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	SEC_PRE_UBA							
23:16	SEC_PRE_UBA							
15:08	SEC_PRE_UBA							
07:00	SEC_PRE_UBA							

Bits	Name	Description	Type	Reset value
31:00	SEC_PRE_UBA	Secondary bus non-prefetchable upper base.	R/W	0x000

### 14.7.5 Primary Bus Non-prefetchable Upper Base Address Remap Register

Register name: AR_PBNPBASEUPPER Reset value: 0x0000_0000	Register offset: 0x0F4
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	PRI_NP_UBA							
23:16	PRI_NP_UBA							
15:08	PRI_NP_UBA							
07:00	PRI_NP_UBA							

Bits	Name	Description	Type	Reset value
31:00	PRI_NP_UBA	Primary bus non-prefetchable upper base.	R/W	0x0000_000 0



### 14.7.6 Primary Bus Non-prefetchable Upper Limit Remap Register

Register name: AR_PBNPLIMITUPPER Reset value: 0x0000_0000	Register offset: 0x0F8
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	PRI_NP_ULA							
23:16	PRI_NP_ULA							
15:08	PRI_NP_ULA							
07:00	PRI_NP_ULA							

Bits	Name	Description	Type	Reset value
31:00	PRI_NP_ULA	Primary bus non-prefetchable upper Limit	R/W	0x0000_000 0

## 14.8 Advanced Error Reporting Capability Registers



When the PEB383 operates in “Legacy Mode” the following registers are not supported and are treated as reserved:

- “PCIe Capability Registers”
- “Advanced Error Reporting Capability Registers”

### 14.8.1 PCIe Advanced Error Reporting Capability Register

Register name: PCIE_ADV_ERR_CAP Reset value: 0x0001_0001	Register offset: 0x100
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	NXT_CAP_OFF							
23:16	NXT_CAP_OFF				CAP_VER			
15:08	EXT_CAP_ID							
07:00	EXT_CAP_ID							

Bits	Name	Description	Type	Reset value
31:20	NXT_CAP_OFF	Next Capability Offset This field contains the offset to the next PCIe capability structure or 0x000 if no other items exist in the linked list of capabilities. For Extended Capabilities implemented in device configuration space, this offset is relative to the beginning of PCI compatible configuration space and thus must always be either 0x000 (for terminating list of capabilities) or greater than 0x0FF.	R	0x000
19:16	CAP_VER	Capability Version This field is a PCI-SIG defined version number that indicates the version of the capability structure present.	R	0x1
15:0	EXT_CAP_ID	PCIe Extended Capability ID This field is a PCI-SIG defined ID number that indicates the function and format of the extended capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0x0001.	R	0x0001

## 14.8.2 PCIe Uncorrectable Error Status Register

Register name: PCIE_UNC_ERR_STAT Reset value: 0x0000_0000	Register offset: 0x104
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved			UR	ECRC	MAL_TLP	R XO	U XC
15:08	CA	CTO	FCPE	PTLP	Reserved			
07:00	Reserved			DLPE	Reserved			Undefined

Bits	Name	Description	Type	Reset value
31:21	Reserved	Reserved	R	0x000
20	UR	Unsupported Request Error Status	R/W1CS	0
19	ECRC	ECRC Error Status	R/W1CS	0
18	MAL_TLP	Malformed TLP Status	R/W1CS	0
17	R XO	Receiver Overflow Status	R/W1CS	0
16	U XC	Unexpected Completion Status	R/W1CS	0
15	CA	Completer Abort Status	R/W1CS	0
14	CTO	Completion Timeout Status	R/W1CS	0
13	FCPE	Flow Control Protocol Error Status	R/W1CS	0
12	PTLP	Poisoned TLP Status	R/W1CS	0
11:5	Reserved	Reserved	R	0x00
4	DLPE	Data Link Protocol Error Status	R/W1CS	0
3:1	Reserved	Reserved	R	000
0	Undefined	Undefined	R	0

### 14.8.3 PCIe Uncorrectable Error Mask Register

Register name: PCIE_UERR_MASK Reset value: 0x0000_0000	Register offset: 0x108
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved			UR	ECRC	MAL_TLP	R XO	U XC
15:08	CA	CTO	FCPE	PTLP	Reserved			
07:00	Reserved			DLPE	Reserved			Undefined

Bits	Name	Description	Type	Reset value
31:21	Reserved	Reserved	R	0x000
20	UR	Unsupported Request Error Mask	R/WS	0
19	ECRC	ECRC Error Mask	R/WS	0
18	MAL_TLP	Malformed TLP Mask	R/WS	0
17	R XO	Receiver Overflow Mask	R/WS	0
16	U XC	Unexpected Completion Mask	R/WS	0
15	CA	Completer Abort Mask	R/WS	0
14	CTO	Completion Timeout Mask	R/WS	0
13	FCPE	Flow Control Protocol Error Mask	R/WS	0
12	PTLP	Poisoned TLP Mask	R/WS	0
11:5	Reserved	Reserved	R	0x00
4	DLPE	Data Link Protocol Error Mask	R/WS	0
3:1	Reserved	Reserved	R	000
0	Undefined	Undefined	R	0

### 14.8.4 PCIe Uncorrectable Error Severity Register

Register name: PCIE_UNC_ERR_SEV Reset value: 0x0006_2030	Register offset: 0x10C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved			UR	ECRC	MAL_TLP	R XO	UXC
15:08	CA	CTO	FCPE	PTLP	Reserved			
07:00	Reserved		SDES	DLPE	Reserved			Unused

Bits	Name	Description	Type	Reset value
31:21	Reserved	Reserved	R	0x000
20	UR	Unsupported Request Error Severity	R/WS	0
19	ECRC	ECRC Error Severity	R/WS	0
18	MAL_TLP	Malformed TLP Severity	R/WS	1
17	R XO	Receiver Overflow Severity	R/WS	1
16	UXC	Unexpected Completion Severity <b>Note:</b> In the <i>PCI Express Base Specification (Revision 1.1)</i> , Unexpected Completions are only reported as correctable errors: this bit should not be set to 1.	R/WS	0
15	CA	Completer Abort Severity	R/WS	0
14	CTO	Completion Timeout Severity	R/WS	0
13	FCPE	Flow Control Protocol Error Severity	R/WS	1
12	PTLP	Poisoned TLP Severity	R/WS	0
11:6	Reserved	Reserved	R	0x00
5	SDES	Surprise Down Error Severity	R/WS	1
4	DLPE	Data Link Protocol Error Severity	R/WS	1
3:1	Reserved	Reserved	R	000
0	Unused	Reserved <b>Note:</b> Bit 0 is Training Error Status for PCIe 1.0a, but is not defined for the <i>PCI Express Base Specification (Revision 1.1)</i> .	R	0

### 14.8.5 PCIe Correctable Error Status Register

Register name: PCIE_COR_ERR Reset value: 0x0000_0000	Register offset: 0x110
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		ANFE	RT_TO	Reserved			RN_RO
07:00	B_DLLP	B_TLP	Reserved					RXE

Bits	Name	Description	Type	Reset value
31:14	Reserved	Reserved	R	0x00000
13	ANFE	Advisory Non-Fatal Error Status	R/W1CS	0
12	RT_TO	Replay Timer Timeout Status	R/W1CS	0
11:9	Reserved	Reserved	R	000
8	RN_RO	REPLAY_NUM Rollover Status	R/W1CS	0
7	B_DLLP	Bad DLLP Status This bit is set to indicate the following conditions: <ul style="list-style-type: none"> <li>Calculated CRC was not equal to received CRC.</li> </ul>	R/W1CS	0
6	B_TLP	Bad TLP Status This bit is set to indicate the following conditions: <ul style="list-style-type: none"> <li>Physical layer indicated errors with the TLP</li> <li>TLP ended with EDB, but calculated CRC was not the logical NOT of the received CRC</li> <li>Calculated CRC was not equal to the received CRC</li> </ul>	R/W1CS	0
5:1	Reserved	Reserved	R	0x0
0	RXE	Receiver Error Status	R/W1CS	0

### 14.8.6 PCIe Correctable Error Mask Register

Register name: PCIE_COR_MASK Reset value: 0x0000_2000	Register offset: 0x114
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		ANFE	RT_TO	Reserved			RN_RO
07:00	B_DLLP	B_TLP	Reserved					RXE

Bits	Name	Description	Type	Reset value
31:14	Reserved	Reserved	R	0x00000
13	ANFE	Advisory Non-Fatal Error Mask	R/WS	1
12	RT_TO	Replay Timer Timeout Mask	R/WS	0
11:9	Reserved	Reserved	R	000
8	RN_RO	REPLAY_NUM Rollover Mask	R/WS	0
7	B_DLLP	Bad DLLP Mask	R/WS	0
6	B_TLP	Bad TLP Mask	R/WS	0
5:1	Reserved	Reserved	R	0x0
0	RXE	Receiver Error Mask	R/WS	0

### 14.8.7 PCIe Advanced Error Capabilities and Control Register

Register name: PCIE_ADV_ERR_CAP_CTRL Reset value: 0x0000_00A0	Register offset: 0x118
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							EC_EN
07:00	EC_CAP	EG_EN	EG_CAP	ERR_PTR				

Bits	Name	Description	Type	Reset value
31:9	Reserved	Reserved	R	0x0000_00
8	EC_EN	ECRC Check Enable 0 = Disable 1 = Enable	R/WS	0
7	EC_CAP	ECRC Check Capable This bit indicates the PEB383 can check ECRC.	R	1
6	EG_EN	ECRC Generation Enable 0 = Disable 1 = Enable	R/WS	0
5	EG_CAP	ECRC Generation Capable This bit indicates the PEB383 can generate ECRC.	R	1
4:0	ERR_PTR	First Error Pointer This pointer is a read-only field that identifies the bit position of the first error reported in the "PCIe Uncorrectable Error Status Register".	RS	0



### 14.8.8 PCIe Header Log 1 Register

Register name: PCIE_HL1 Reset value: 0x0000_0000	Register offset: 0x11C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	HEADER[127:120]							
23:16	HEADER[119:112]							
15:08	HEADER[111:104]							
07:00	HEADER[103:96]							

Bits	Name	Description	Type	Reset value
31:00	HEADER[127:96]	Header of TLP associated with error.	RS	0

### 14.8.9 PCIe Header Log 2 Register

Register name: PCIE_HL2 Reset value: 0x0000_0000	Register offset: 0x120
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	HEADER[95:88]							
23:16	HEADER[87:80]							
15:08	HEADER[79:72]							
07:00	HEADER[71:64]							

Bits	Name	Description	Type	Reset value
31:00	HEADER[95:64]	Header of TLP associated with error.	RS	0

### 14.8.10 PCIe Header Log 3 Register

Register name: PCIE_HL3 Reset value: 0x0000_0000	Register offset: 0x124
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	HEADER[63:56]							
23:16	HEADER[55:48]							
15:08	HEADER[47:40]							
07:00	HEADER[39:32]							

Bits	Name	Description	Type	Reset value
31:00	HEADER[63:32]	Header of TLP associated with error.	RS	0

### 14.8.11 PCIe Header Log 4 Register

Register name: PCIE_HL4 Reset value: 0x0000_0000	Register offset: 0x128
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	HEADER[31:24]							
23:16	HEADER[23:16]							
15:08	HEADER[15:08]							
07:00	HEADER[07:00]							

Bits	Name	Description	Type	Reset value
31:00	HEADER[31:00]	Header of TLP associated with error.	RS	0

### 14.8.12 PCIe Secondary Uncorrectable Error Status Register

Register name: PCIE_SEC_UERR_STAT Reset value: 0x0000_0000	Register offset: 0x12C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		IB_ERR	SERR_AD	PERR_AD	DTDTE	UADD_ERR	UATT_ERR
07:00	UDERR	USCM	USCE	Reserved	R_MA	R_TA	MA_SC	TA_SC

Bits	Name	Description	Type	Reset value
31:14	Reserved	Reserved	R	0x0000_0
13	IB_ERR	Internal Bridge Error Status (No Header Log). The PEB383 never sets this bit.	R	0
12	SERR_AD	SERR# Assertion Detected (No Header Log)	R/W1CS	0
11	PERR_AD	PERR# Assertion Detected	R/W1CS	0
10	DTDTE	Delayed Transaction Discard Timer Expired Status (No Header Log)	R/W1CS	0
9	UADD_ERR	Uncorrectable Address Error Status	R/W1CS	0
8	UATT_ERR	Uncorrectable Attribute Error Status	R/W1CS	0
7	UDERR	Uncorrectable Data Error Status	R/W1CS	0
6	USCM	Uncorrectable Split Completion Message Data Error Status <sup>a</sup>	R/W1CS	0
5	USCE	Unexpected Split Completion Error Status <sup>a</sup>	R/W1CS	0
4	Reserved	Reserved	R	0
3	R_MA	Received Master-Abort Status	R/W1CS	0
2	R_TA	Received Target-Abort Status	R/W1CS	0
1	MA_SC	Master-Abort on Split Completion Status <sup>a</sup>	R/W1CS	0
0	TA_SC	Target-Abort on Split Completion Status <sup>a</sup>	R/W1CS	0

a. The PEB383 never sets this bit since it does not support PCI-X.

### 14.8.13 PCIe Secondary Uncorrectable Error Mask Register

Register name: PCIE_SEC_UERR_MASK Reset value: 0x0000_17A8	Register offset: 0x130
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		IB_ERR	SERR_AD	PERR_AD	DTDTE	UADD_ERR	UATT_ERR
07:00	UDERR	USCM	USCE	Reserved	R_MA	R_TA	MA_SC	TA_SC

Bits	Name	Description	Type	Reset value
31:14	Reserved	Reserved	R	0x0000_0
13	IB_ERR	Internal Bridge Error Mask (No Header Log)	R/WS	0
12	SERR_AD	SERR# Assertion Detected Mask (No Header Log)	R/WS	1
11	PERR_AD	PERR# Assertion Detected Mask	R/WS	0
10	DTDTE	Delayed Transaction Discard Timer Expired Mask (No Header Log)	R/WS	1
9	UADD_ERR	Uncorrectable Address Error Mask	R/WS	1
8	UATT_ERR	Uncorrectable Attribute Error Mask	R/WS	1
7	UDERR	Uncorrectable Data Error Mask	R/WS	1
6	USCM	Uncorrectable Split Completion Message Data Error Mask <sup>a</sup>	R/WS	0
5	USCE	Unexpected Split Completion Error Mask <sup>a</sup>	R/WS	1
4	Reserved	Reserved	R	0
3	R_MA	Received Master-Abort Mask	R/WS	1
2	R_TA	Received Target-Abort Mask	R/WS	0
1	MA_SC	Master-Abort on Split Completion Mask <sup>a</sup>	R/WS	0
0	TA_SC	Target-Abort on Split Completion Mask <sup>a</sup>	R/WS	0

a. This bit has no effect on the PEB383 since it does not support PCI-X.

### 14.8.14 PCIe Secondary Uncorrectable Error Severity Register

Register name: PCIE_SEC_UERR_SEV Reset value: 0x0000_1340	Register offset: 0x134
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		IB_ERR	SERR_AD	PERR_AD	DTDTE	UADD_ERR	UATT_ERR
07:00	UDERR	USCM	USCE	Reserved	R_MA	R_TA	MA_SC	TA_SC

Bits	Name	Description	Type	Reset value
31:14	Reserved	Reserved	R	0x0000_0
13	IB_ERR	Internal Bridge Error Severity (No Header Log)	R/WS	0
12	SERR_AD	SERR# Assertion Detected Severity (No Header Log)	R/WS	1
11	PERR_AD	PERR# Assertion Detected Severity	R/WS	0
10	DTDTE	Delayed Transaction Discard Timer Expired Severity (No Header Log)	R/WS	0
9	UADD_ERR	Uncorrectable Address Error Severity	R/WS	1
8	UATT_ERR	Uncorrectable Attribute Error Severity	R/WS	1
7	UDERR	Uncorrectable Data Error Severity	R/WS	0
6	USCM	Uncorrectable Split Completion Message Data Error Severity <sup>a</sup>	R/WS	1
5	USCE	Unexpected Split Completion Error Severity <sup>a</sup>	R/WS	0
4	Reserved	Reserved	R	0
3	R_MA	Received Master-Abort Severity	R/WS	0
2	R_TA	Received Target-Abort Severity	R/WS	0
1	MA_SC	Master-Abort on Split Completion Severity	R/WS	0
0	TA_SC	Target-Abort on Split Completion Severity	R/WS	0

a. This bit has no effect on the PEB383 since it does not support PCI-X.

### 14.8.15 PCIe Secondary Error Capabilities and Control Register

Register name: PCIE_ERR_CAP_CTRL Reset value: 0x0000_0000	Register offset: 0x138
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							
07:00	Reserved				SUFEP			

Bits	Name	Description	Type	Reset value
31:05	Reserved	Reserved	R	0
04:00	SUFEP	Secondary Uncorrectable First Error Pointer.	RS	0x00

### 14.8.16 PCIe Secondary Header Log 1 Register

Register name: PCIE_SEC_HL1 Reset value: 0x0000_0000	Register offset: 0x13C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	TRAN_ATT[31:24]							
23:16	TRAN_ATT[23:16]							
15:08	TRAN_ATT[15:08]							
07:00	TRAN_ATT[07:00]							

Bits	Name	Description	Type	Reset value
31:00	TRAN_ATT[31:00]	Transaction Attribute This field is [31:0] of the 36-bit value transferred on C/BE[3:0]# and AD[31:0] during the attribute phase.	RS	0x0

### 14.8.17 PCIe Secondary Header Log 2 Register

Register name: PCIE_SEC_HL2 Reset value: 0x0000_0000	Register offset: 0x140
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved				TRAN_CU			
07:00	TRAN_CL				TRAN_ATT[35:32]			

Bits	Name	Description	Type	Reset value
31:12	Reserved	Reserved	R	0
11:08	TRAN_CU	Transaction Command Upper This value is transferred on C/BE[3:0]# during the second address phase of a DAC transaction.	RS	0x0
07:04	TRAN_CL	Transaction Command Lower This value is transferred on C/BE[3:0]# during the first address phase.	RS	0x0
3:0	TRAN_ATT[35:32]	Transaction Attribute This field is [35:32] of the 36-bit value transferred on C/BE[3:0]# and AD[31:0] during the attribute phase.	RS	0x0

### 14.8.18 PCIe Secondary Header Log 3 Register

Register name: PCIE_SEC_HL3 Reset value: 0x0000_0000	Register offset: 0x144
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	TRAN_ADD[31:24]							
23:16	TRAN_ADD[23:16]							
15:08	TRAN_ADD[15:08]							
07:00	TRAN_ADD[07:00]							

Bits	Name	Description	Type	Reset value
31:00	TRAN_ADD[31:00]	Transaction Address This is the first 32 bits of the 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged in this field, and the second address is logged in "PCIe Secondary Header Log 4 Register".	RS	0x0

### 14.8.19 PCIe Secondary Header Log 4 Register

Register name: PCIE_SEC_HL4 Reset value: 0x0000_0000	Register offset: 0x148
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	TRAN_ADD[63:56]							
23:16	TRAN_ADD[55:48]							
15:08	TRAN_ADD[47:40]							
07:00	TRAN_ADD[39:32]							

Bits	Name	Description	Type	Reset value
31:00	TRAN_ADD[63:32]	Transaction Address This is the second 32 bits of the 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged in "PCIe Secondary Header Log 3 Register", and the second address phase is logged in this field. In the case of a 32-bit address, this field is set to 0.	RS	0x0



## 14.8.20 Replay Latency Register

Register name: <b>REPLAY_LATENCY</b> Reset value: <b>0x0000_0000</b>	Register offset: <b>0x208</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	REPLAY_L AT_EN	REPLAY_LATENCY						
07:00	REPLAY_LATENCY							

Bits	Name	Description	Type	Reset value
31:16	Reserved	Reserved	R	0
15	REPLAY_LAT_EN	Replay Latency Enable	R/W	0
14:00	REPLAY_LATENCY	Replay Latency timer value is overwritten by this value if REPLAY_LAT_EN is set to b1.	R/W	0x0000

### 14.8.21 ACK/NACK Update Latency Register

Register name: ACKNAK_UPD_LAT Reset value: 0x0009_0009	Register offset: 0x20C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	UPDATE_LAT_EN	Reserved			UPDATE_LATENCY			
23:16	UPDATE_LATENCY							
15:08	ACKNAK_LAT_EN	Reserved		ACKNAK_LATENCY				
07:00	ACKNAK_LATENCY							

Bits	Name	Description	Type	Reset value
31	UPDATE_LAT_EN	Update Latency Enable	R/W	0x0
30:28	Reserved	Reserved.	R	0
27:16	UPDATE_LATENCY	Update Latency timer value is overwritten with this value if UPDATE_LAT_EN is set to b1.	R/W	0x009
15	ACKNAK_LAT_EN	Ack/Nak Latency Enable	R/W	0x0
14:13	Reserved	Reserved.	R	0
12:00	ACKNAK_LATENCY	Ack/Nak Latency timer value is overwritten with this value if ACKNAK_LAT_EN is set to b1.	R/W	0x0009

## 14.8.22 N\_FTS Register

Register name: N_FTS Reset value: 0x0000_0020	Register offset: 0x210
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved							
07:00	N_FTS							

Bits	Name	Description	Type	Reset value
31:08	Reserved	Reserved	R	0x0
07:00	N_FTS	This register indicates the N_FTS count value to be advertised to the other end component. Note: This value should fall in the L0s exit latency value range reported by the PEB383.	R/W	0x20



## 14.9 PCIe and SerDes Control and Status Registers

The following table outlines the PCIe SerDes and PCS layer registers. These registers are mainly for status reporting and testing. Caution should be taken when modifying any of these registers during normal operation. Any unused offset space should be treated as reserved.



The SerDes Control and Status Registers must not be accessed if the SerDes is in reset nor when the reference clock is stopped.

### 14.9.1 Base Offset Address Calculation

The PCIe SerDes control register addressees are calculated according to the following formula.

$$\text{Address} = \text{Base} + \text{Offset}$$

$$\text{Base} = 0x800$$

**Table 38: SerDes Per-lane and Clock Control and Status Register Map**

Offset	Register Name	See
<b>“PCIe Per-Lane Transmit and Receive Registers”</b>		
0x000	PCIE_TXRX_STAT_0	“PCIe Transmit and Receive Status Register”
0x004	PCIE_OUT_STAT_0	“PCIe Output Status and Transmit Override Register”
0x008	PCIE_RX_OVRD_0	“PCIe Receive and Output Override Register”
0x00C	PCIE_DBG_CTL	“PCIe Debug and Pattern Generator Control Register”
0x02C	PCIE_PM_CTL	“PCIe Pattern Matcher Control and Error Register”
0x030	PCIE_SS_EC_CTL	“PCIe SS Phase and Error Counter Control Register”
0x034	PCIE_SCTL_FI	“PCIe Scope Control and Frequency Integrator Register”
<b>“PCIe Clock Module Control and Status Registers”</b>		
0x420	PCIE_CTL_STAT	“PCIe Control and Level Status Register”
0x428	PCIE_CTL_OVRD	“PCIe Control and Level Override Register”

## 14.9.2 PCIe Per-Lane Transmit and Receive Registers

### 14.9.3 PCIe Transmit and Receive Status Register

This register reflects the default state of the SerDes transmit and receive control inputs at power-up. Its reset value depends on various inputs. When its accompanying override registers are used, however (see “[PCIe Output Status and Transmit Override Register](#)” and “[PCIe Receive and Output Override Register](#)”), the relevant status bits are no longer valid.

<b>Register name: PCIE_TXRX_STAT</b> <b>Reset value: Undefined</b>	<b>Register offset: 0x000</b>
---	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		LOS_CTL		Reserved			
23:16	RX_EQ_VAL			Reserved	RX_ALIGN_EN	Reserved		HALF_RATE
15:08	Reserved						TX_BOOST	
07:00	TX_BOOST		Reserved					

Bits	Name	Description	Type	Reset Value
31:30	Reserved	Reserved	R	01
29:28	LOS_CTL	LOS filtering mode control	R	Undefined
27:24	Reserved	Reserved	R	Undefined
23:21	RX_EQ_VAL	Receive Equalization control	R	0b010
20	Reserved	Reserved	R	0
18:17	Reserved	Reserved	R	Undefined
16	HALF_RATE	Digital half-rate data control	R	Undefined
15:10	Reserved	Reserved	R	100000
9:6	TX_BOOST	Transmit Boost control Programmed boost value (ratio of drive level of transition bit to non-transition bit) is: $\text{boost} = -20 \cdot \log(1 - (\text{tx\_boost}[3:0] + 0.5) / 32) \text{dB}$ , except that setting TX_BOOST to 0 produces 0dB of boost. This produces results up to 5.75dB in steps of ~0.37dB.	R	0b1011
5:0	Reserved	Reserved	R	Undefined

### 14.9.4 PCIe Output Status and Transmit Override Register

This register indicates the status of output signals. Its reset value depends on various inputs. The register also provides a method for overriding the value of TX\_BOOST in the “**PCIe Transmit and Receive Status Register**”.

<b>Register name: PCIE_OUT_STAT</b> <b>Reset value: Undefined</b>	<b>Register offset: 0x004</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	OVRD	Reserved				TX_BOOST		
23:16	TX_BOOST		ReservedP					
15:08	ReservedP							
07:00	ReservedP				LOS		Reserved	

Bits	Name	Description	Type	Reset Value
31	OVRD	Enable override of relevant bits 16:30 in this register.	R/W	0
30:26	Reserved	Reserved	R/W	00000
25:22	TX_BOOST	Transmit Boost control Programmed boost value (ratio of drive level of transition bit to non-transition bit) is: $boost = -20 * \log(1 - (tx\_boost[3:0] + 0.5) / 32) \text{dB}$ , except that setting TX_BOOST to 0 produces 0dB of boost. This produces results up to 5.75dB in steps of -0.37dB.	R/W	0x0
21:3	ReservedP	Preserve state on writes.	R/W	Undefined
2	LOS	Loss of signal output	R	Undefined
1:0	Reserved	Reserved	R	Undefined

## 14.9.5 PCIe Receive and Output Override Register

This register provides a method for overriding the values of LOS\_CTL, RX\_EQ\_VAL, and RX\_ALIGN\_EN in the “PCIe Transmit and Receive Status Register”.

Register name: PCIE_RX_OVRD Reset value: Undefined	Register offset: 0x008
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	ReservedP							
23:16	ReservedP							
15:08	ReservedP	OVRD_2	LOS_CTL		ReservedP			
07:00	RX_EQ_VAL			ReservedP	RX_ALIGN_EN	ReservedP		HALF_RATE

Bits	Name	Description	Type	Reset Value
31:15	ReservedP	Preserve state on writes.	R	Undefined
14	OVRD_2	Enable override of relevant bits 0:13 in this register.	R/W	0
13:12	LOS_CTL	LOS filtering mode control 00 = Disabled 01-10 = Reserved 11 = Heavy filtering. The LOS signal is synchronous to the output of the prescaler. Heavy filtering means 128 +/- 5 cycles of no signal for LOS to be asserted.	R/W	01
11:8	ReservedP	Preserve state on writes.	R/W	Undefined
7:5	RX_EQ_VAL	Receive Equalization control Internal linear equalizer boost is approximately = (rx_eq_val+1)*0.5dB Example: 3'b100 = 2.5dB boost	R/W	000
4	ReservedP	Preserve state on writes.	R/W	1
3	RX_ALIGN_EN	Enable Word Alignment 0 = Alignment (framer) disabled 1 = Alignment enabled	R/W	1
2:1	ReservedP	Preserve state on writes.	R/W	11
0	HALF_RATE	Digital half-rate data control	R/W	0



### 14.9.6 PCIe Debug and Pattern Generator Control Register

This register controls the pattern generator in the SerDes.

Register name: PCIE_DBG_CTL Reset value: 0x0000_0000	Register offset: 0x00C
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved		PATO					
23:16	PATO			TRIGGER_ERR		MODE		
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset Value
31:30	Reserved	Reserved	R	0
29:20	PATO	Pattern for modes 3–5 Program the desired pattern in these 10 bits when using modes 3-5. Note: This field returns to its reset value on reset.	R/W	0x00
19	TRIGGER_ERR	Insert a single error into a LSB Note: This field returns to its reset value on reset.	R/W	0
18:16	MODE	Pattern to generate: 0 = Disabled 1 = lfsr15 ( $x^{15}+x^{14}+1$ ) 2 = lfsr7 ( $x^7+x^6+1$ ) 3 = Fixed word (PATO) 4 = DC balanced word (PATO, ~PATO) 5 = Fixed pattern: (000, PAT0, 3ff, ~PATO) 6–7 = Reserved	R/W	000
15:0	Reserved	Reserved	R	0

## 14.9.7 PCIe Pattern Matcher Control and Error Register

This register controls the pattern matcher in the SerDes.

Register name: PCIE_PM_CTL Reset value: Undefined	Register offset: 0x02C
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	OV14	COUNT						
23:16	COUNT							
15:08	Reserved							
07:00	Reserved				SYNC	MODE		

Bits	Name	Description	Type	Reset Value
31	OV14	Overflow 14 0 = Inactive 1 = Multiply COUNT by 128 If OV14 is 1 and COUNT=2 <sup>15</sup> -1, signals overflow of counter. Note: This bit may require two reads to get a stable value. <sup>a</sup>	R/W	Undefined
30:16	COUNT	Current error count If OV14 field is active, then multiply count by 128. <sup>a</sup>	R/W	Undefined
15:4	Reserved	Reserved	R	0
3	SYNC	Synchronize pattern matcher LFSR with incoming data must be turned on then off to enable checking. Note: This bit returns to its reset value on reset	R/W	0
2:0	MODE	Pattern to match: 0 = Disabled 1 = lfsr15 2 = lfsr7 3 = d[n] = d[n-10] 4 = d[n] = !d[n-10] 5-7 = Reserved	R/W	000

a. Read operation on this register is pipelined. Two reads may be needed to get "current" value. The value is volatile; that is, the value may change at any time. The second read resets the counter.

### 14.9.8 PCIe SS Phase and Error Counter Control Register

This register holds the current MPLL phase selector value and information for the associated error counter in the SerDes.

Register name: PCIE_SS_EC_CTL Reset value: Undefined	Register offset: 0x030
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved				SS_PVAL			
23:16	SS_PVAL							DTHR
15:08	OV14	COUNT						
07:00	COUNT							

Bits	Name	Description	Type	Reset Value
31:28	Reserved	Reserved	R	0
27:17	SS_PVAL	Phase value from zero reference <sup>a</sup>	R/W	0x000
16	DTHR	Bits below the useful resolution <sup>a</sup>	R/W	0
15	OV14	Overflow 14 0 = Inactive 1 = Multiply COUNT by 128. If OV14=1 and COUNT=2 <sup>15</sup> -1, signals overflow of counter. <sup>a</sup>	R/W	Undefined
14:0	COUNT	Current error count If OV14 field is active, then multiply count by 128. <sup>a</sup>	R/W	Undefined

a. Read operation on this register is pipelined. Two reads may be needed to get “current” value. The value is volatile; that is, the value may change at any time. The second read resets the counter.

### 14.9.9 PCIe Scope Control and Frequency Integrator Register

Register name: PCIE_SCTL_FI Reset value: 0000_0000	Register offset: 0x034
---	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved							
23:16	Reserved							
15:08	Reserved		FVAL					
07:00	FVAL							DTHR_F

Bits	Name	Description	Type	Reset Value
31:14	Reserved	Reserved	R/W	0
13:1	FVAL	Frequency is $1.526 \cdot \text{VAL}$ ppm from the reference. Value is a signed integer format (2's complement). Note: This field may require two "reads" to get a stable value.	R/W	0
0	DTHR_F	Bits below the useful resolution. Note: This bit may require two "reads" to get a stable value.	R/W	0

## 14.9.10 PCIe Clock Module Control and Status Registers

### 14.9.11 PCIe Control and Level Status Register

This register indicates the status of various control inputs. Its reset value depends on inputs. When its accompanying override register is used, however (see “[PCIe Control and Level Override Register](#)”), the relevant status bits are no longer valid.

<b>Register name: PCIE_CTL_STAT</b> <b>Reset value: Undefined</b>	<b>Register offset: 0x420</b>
--	-------------------------------

Bits	7	6	5	4	3	2	1	0
31:24	Reserved	TX_LVL				LOS_LVL		
23:16	LOS_LVL			ACJT_LVL				
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset Value
31	Reserved	Reserved	R	1
30:26	TX_LVL	Fine Resolution setting of Tx signal level. Equation: Pk-Pk output level (without attenuation) = 1230 x (48 + tx_lvl/2)/63.5 mV Vdiff-pp Note: TX_LVL should be set to >= 0x1010 (which results in an output of 1Vp-p). For more information on available settings, see <a href="#">Table 39</a> .	R	0x10
25:21	LOS_LVL	Loss of Signal Detector level.	R	0x12
20:16	ACJT_LVL	AC JTAG Comparator level.	R	0x00
15:0	Reserved	Reserved	R	1

## 14.9.12 PCIe Control and Level Override Register

The register provides a method for overriding the value of TX\_LVL, LOS\_LVL, and ACJT\_LVL in the “PCIe Control and Level Status Register”.

Register name: PCIE_CTL_OVRD Reset value: Undefined	Register offset: 0x428
--	------------------------

Bits	7	6	5	4	3	2	1	0
31:24	OVRD	TX_LVL				LOS_LVL		
23:16	LOS_LVL			ACJT_LVL				
15:08	Reserved							
07:00	Reserved							

Bits	Name	Description	Type	Reset Value
31	OVRD	Override all level controls.	R/W	0
30:26	TX_LVL	Fine Resolution setting of Tx signal level. Equation: Pk-Pk output level (without attenuation) = 1230 x (48 + tx_lvl/2)/63.5 mV Vdiff-pp Note: TX_LVL should be set to >= 0x1010 (which results in an output of 1Vp-p). For more information on available settings, see Table 39.	R/W	0x10
25:21	LOS_LVL	Loss of Signal Detector level	R/W	0x10
20:16	ACJT_LVL	AC JTAG Receiver Comparator level This sets the hysteresis level for AC JTAG. For information on setting the correct voltage levels, see IEEE 1149.6.	R/W	0x10
15:0	ReservedP	Preserve state on writes.	R/W	Undefined

**Table 39: TX\_LVL Values**

TX_LVL	Value	TX_LVL[0:4]	Vdiff-pp (mV)
0	0x00	5'b00000	929.8
1	0x01	5'b00001	939.4
2	0x02	5'b00010	949.1
3	0x03	5'b00011	958.8
4	0x04	5'b00100	968.5
5	0x05	5'b00101	978.2

**Table 39: TX\_LVL Values (Continued)**

TX_LVL	Value	TX_LVL[0:4]	Vdiff-pp (mV)
6	0x06	5'b00110	987.9
7	0x07	5'b00111	997.6
8	0x08	5'b01000	1007.2
9	0x09	5'b01001	1016.9
10	0xA	5'b01010	1026.6
11	0xB	5'b01011	1036.3
12	0xC	5'b01100	1046.0
13	0xD	5'b01101	1055.7
14	0xE	5'b01110	1065.4
15	0xF	5'b01111	1075.0
16	0x10	5'b10000	1084.7
17	0x11	5'b10001	1094.4
18	0x12	5'b10010	1104.1
19	0x13	5'b10011	1113.8
20	0x14	5'b10100	1123.5
21	0x15	5'b10101	1133.1
22	0x16	5'b10110	1142.8
23	0x17	5'b10111	1152.5
24	0x18	5'b11000	1162.2
25	0x19	5'b11001	1171.9
26	0x1A	5'b11010	1181.6
27	0x1B	5'b11011	1191.3
28	0x1C	5'b11100	1200.9
29	0x1D	5'b11101	1210.6
30	0x1E	5'b11110	1220.3
31	0x1F	5'b11111	1230.0





## 15. Electrical Characteristics

Topics discussed include the following:

- “Absolute Maximum Ratings”
- “Recommended Operating Conditions”
- “Power Characteristics”
- “Power Supply Sequencing”
- “DC Operating Characteristics”
- “AC Timing Specifications”
- “AC Timing Waveforms”

### 15.1 Absolute Maximum Ratings

Table 40: Absolute Maximum Ratings – PCI

Symbol	Parameter	Minimum	Maximum	Units
$T_{STG}$	Storage temperature	-55	125	°C
$T_C$	Case temperature under bias	-40	120	°C
<b>Voltage with respect with ground</b>				
$V_{DD}$	1.05V DC core logic supply voltage	-0.5	2.0	V
$V_{DD\_PCIE}$	1.05V DC PCIe digital supply voltage	-0.3	1.7	V
$V_{DDA\_PLL}$	1.05V DC PLL analog supply voltage	-0.5	2.0	V
$V_{DD\_PCI}$	3.3V DC I/O supply voltage	-0.5	4.1	V
$V_{DDA\_PCIE}$	3.3V DC PCIe analog supply voltage	-0.5	4.6	V
$V_{IO\_PCI}$	PCI Interface I/O voltage	-0.5	6.6	V
$V_{IL}$	Minimum signal input voltage	-0.5	-	V
$V_{IH}$	Maximum signal input voltage	-	$V_{DD}^a + 0.5$	V

a. The  $V_{DD}$  reference is dependent on the input pad supply rail.

## 15.2 Recommended Operating Conditions

**Table 42: Recommended Operating Conditions**

Symbol	Parameter	Minimum	Maximum	Units	Notes
V <sub>DD_PCI</sub>	3.3V DC I/O supply voltage	3.0	3.6	V	-
V <sub>DDA_PCIE</sub>	3.3V DC PCIe supply voltage	3.0	3.6	V	-
V <sub>DD</sub>	1.05V DC core supply voltage	0.945	1.155	V	-
V <sub>DD_PCIE</sub>	1.05V DC PCIe digital supply voltage	0.945	1.155	V	-
V <sub>DDA_PLL</sub>	1.05V DC PLL supply voltage	0.945	1.155	V	-
V <sub>IO_PCI</sub>	PCI Interface I/O voltage	V <sub>DD_PCI</sub>	5.25	V	-
V <sub>ripple1</sub>	Power Supply Ripple for Voltage Supplies: V <sub>DD</sub> and V <sub>DD_PCI</sub>	-	100	mV <sub>pp</sub>	-
V <sub>ripple2</sub>	Power Supply Ripple for Voltage Supplies: V <sub>DD_PCIE</sub> , V <sub>DDA_PCIE</sub> , V <sub>DDA_PLL</sub>	-	50	mV <sub>pp</sub>	-
T <sub>A</sub>	Ambient temperature	0	85	°C	a, b
T <sub>JUNC</sub>	Junction temperature	-40	125	°C	-

- a. No heat sink, no air flow.
- b. Higher ambient temperatures are permissible provided T<sub>JUNC</sub> is not violated. For heat sink and air flow requirements for higher temperature operation, see [“Thermal Characteristics”](#).

## 15.3 Power Characteristics

**Table 43: PEB383 Power Dissipation**

Device State	ASPM Link State	Bridge Activity	Typical Power (W)	Max Power (W)
D0	L0	Fully Active Links	0.398	0.458
D0	L0	50% Link Activity	0.312	0.359
D0	L0	0% Link Activity	0.225	0.259
D0	L0s	PCIe Link in Active Standby	0.185	0.213
D3hot	L1	Power Saving Mode	0.132	0.151

**Table 43: PEB383 Power Dissipation (Continued)**

Device State	ASPM Link State	Bridge Activity	Typical Power (W)	Max Power (W)
D3hot	L1	Power Saving Mode. All PCI Clocks Gated	0.128	0.148
D3cold	N/A	Power Removed	0.060	0.069

**Table 44: PEB383 Power Dissipation per Supply**

Device State	ASPM Link State	Bridge Activity	Typical Power (W)	1.0V_A (W)	3.3V_A (W)	1.0V (W)	3.3V (W)
D0	L0	Fully Active Links	0.398	0.022	0.065	0.036	0.275
D0	L0	0% Link Activity	0.225	0.022	0.065	0.031	0.108

## 15.4 Power Supply Sequencing

The PEB383 does not have any power sequencing constraints.

## 15.5 DC Operating Characteristics

**Table 45: DC Operating Characteristics**

Symbol	Parameter	Condition	Minimum	Maximum	Units	Notes
V <sub>OL_PCI</sub>	PCI Output Low Voltage	I <sub>OL</sub> = 1500uA	-	0.1V <sub>DD_PCI</sub>	V	-
V <sub>OH_PCI</sub>	PCI Output High Voltage	I <sub>OH</sub> = -500uA	0.9V <sub>DD_PCI</sub>	-	V	-
V <sub>OH_33</sub>	3.3 CMOS Output High Voltage	I <sub>OH</sub> = -6mA	V <sub>DD_PCI</sub> - 0.5	-	V	-
V <sub>OL_33</sub>	3.3 CMOS Output Low Voltage	I <sub>OL</sub> = 6mA	-	0.4	V	-
V <sub>IH_33</sub>	3.3 CMOS Input High Voltage	-	2	V <sub>DD_PCI</sub> + 0.5	V	-

**Table 45: DC Operating Characteristics (Continued)**

Symbol	Parameter	Condition	Minimum	Maximum	Units	Notes
$V_{IL\_33}$	3.3 CMOS Input Low Voltage	-	-0.5	0.8	V	-
$C_{IN\_PCI}$	Input Pin Capacitance	-	-	8.8	pF	-
$C_{CLK\_PCI}$	Clock Pin Capacitance PCI_CLK	-	-	7.5	pF	-
$L_{IN\_PCI}$	Input Pin Inductance	-	-	8.3	nH	-
$L_{CLK\_PCI}$	Clock Pin Inductance PCI_CLK	-	-	4.9	nH	-

## 15.6 AC Timing Specifications

This section discusses AC timing specifications for the PEB383.

### 15.6.1 PCI Interface AC Signal Timing

**Table 46: PCI Clock (PCI\_CLK) Specification**

Symbol	Parameter	Min	Max	Units	Notes
$T_{F\_PCI}$	PCI Clock Frequency	25	66	MHz	<sup>a</sup>
$T_{C\_PCI}$	PCI Clock Cycle Time	15	40	ns	<sup>a</sup> <sup>b</sup>
$T_{CH\_PCI}$	PCI Clock High Time	6	-	ns	-
$T_{CL\_PCI}$	PCI Clock Low Time	6	-	ns	-
$T_{SR\_PCI}$	PCI Clock Slew Rate	1	6	V/ns	<sup>c</sup>
$T_{SKEW}$	PCI Output Clock Skew	-	0.5	ns	-
<b>Spread Spectrum Requirements</b>					
$f_{MOD\_PCI}$	PCI_CLK Clock modulation frequency	30	33	kHz	-
$f_{SPREAD\_PCI}$	PCI_CLK Clock frequency spread	-1	0	%	-

- The clock frequency may not change beyond the spread-spectrum limits except while device reset is asserted.
- The minimum clock period must not be violated for any single clock cycle.
- This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

## 15.6.2 PCIe Differential Transmitter Output Specification

The following table lists the specification of parameters for the differential output of the PCIe lanes.

**Table 47: PCIe Differential Transmitter Output Specification**

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400ps +/-300ppm. UI does not account for SSC dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage programmed to tx_lvl=5b'01001 and tx_boost = 0	0.800	-	1.2	V	$V_{TX-DIFFp-p} = 2 *  V_{TX-D+} - V_{TX-D-} $ See Note 1.
$V_{TX-DE-RATIO}$	De-emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2
$T_{TX-EYE}$	Minimum TX Eye Width	0.75	-	-	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. This parameter is measured with the equivalent of a zero jitter reference clock. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFF} = 0V$ ) in relation to recovered TX UI. To be measured after the clock recovery function in Section 4.3.3.2 of the <i>PCI Express Base Specification Rev 1.1</i> . See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV	$V_{TX-CM-ACp} = RMS( V_{TX-D+} + V_{TX-D-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(AVG)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV	$ V_{TX-CM-DC} [during L0] - V_{TX-CM-DC} [during electrical idle]  \leq 100mV$ $V_{TX-CM-DC} = DC_{(AVG)}$ of $ V_{TX-D+} + V_{TX-D-} /2 [L0]$ $V_{TX-CM-idle-DC} = DC_{(AVG)}$ of $ V_{TX-D+} + V_{TX-D-} /2 [Electrical Idle]$ See Note 2

**Table 47: PCIe Differential Transmitter Output Specification (Continued)**

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments
$V_{TX\_CM-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}  \leq 25mV$ $V_{TX-CM-DC-D+} = DC_{(AVG)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = DC_{(AVG)}$ of $ V_{TX-D-} $ See Note 2
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV	$V_{TX-IDLE-DIFFp} =  V_{TX-IDLE-D+} - V_{TX-IDLE-D-}  \leq 20mV$ See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	-	-	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Section 4.3.1.8 of the <i>PCI Express Base Specification (Revision 1.1)</i> .
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V	The maximum DC Common Mode voltage under any conditions. See Section 4.3.1.8 of the <i>PCI Express Base Specification (Revision 1.1)</i> .
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	-	-	UI	Minimum time a Transmitter must be in Electrical Idle. Used by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set.
$T_{TX-IDLE-SET-to-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set	-	-	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle specifications within this time. This is considered a de-bounce time for the transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-to-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition	-	-	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a de-bounce time for the TX to meet all TX specifications after leaving Electrical Idle.
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX-CM}$	Common Mode Return Loss	6	-	-	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	-	120	Ohms	TX DC Differential Mode low impedance. See Note 6.

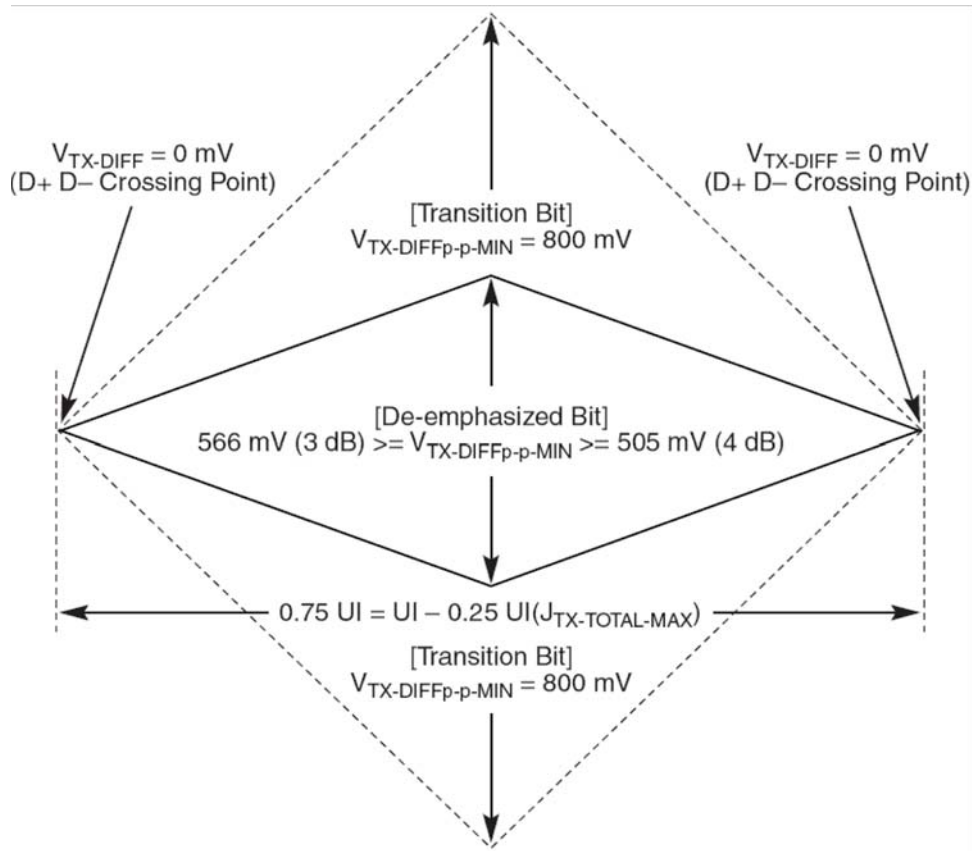
**Table 47: PCIe Differential Transmitter Output Specification (Continued)**

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-2.8	-	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
$C_{TX}$	AC Coupling Capacitor	75	-	200	nF	All Transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Section 4.2.6.3 of the <i>PCI Express Base Specification (Revision 1.1)</i> .

Note that all Figure and Section references are to the *PCI Express Base Specification (Revision 1.1)*.

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 and measured using the clock recovery function in Section 4.3.3.2. (also see the transmitter compliance eye diagram in Figure 4-24).
3. A  $T_{TX-EYE} = 0.75$  UI provides for a total sum of deterministic and random jitter of  $T_{TX-JITTER-MAX} = 0.25$  UI for the Transmitter using clock recovery function specified in Section 4.3.3.2. The  $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half the total TX jitter budget using the clock recovery function specified in section 4.3.3.2. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed the averaged time value. This parameter is to be met at the target bit error rate. The  $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$  is to be met using the compliance pattern at a sample size of 1,000,000 UI.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 10 dB with a differential test input signal no less than 200mV (peak value, 400 mV differential peak to peak) swing around ground applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. the reference impedance for return loss measurements is 50 Ohms to ground for both D+ and D- line (that is, as measured by a vector Network Analyzer with 50 Ohm probes - see Figure 4-25). Note that the series capacitors  $C_{TX}$  is optional for the return loss measurement.
5. Measured between 20-80% at the Transmitter package pins into a test load as shown in Figure 4-25 for both  $V_{TX-D+}$  and  $V_{TX-D-}$ .
6.  $Z_{TX-DIFF-DC}$  is the small signal resistance of the transmitter measured at a DC operating point that is equivalent to that established by connecting a 100-Ohm resistor from D+ and D- while the TX is driving a static logic one or logic zero. Equivalently, this parameter can be derived by measuring the RMS voltage of the TX while transmitting a test pattern into two different differential terminations that are near 100 Ohms. Small signal resistance is measured by forcing a small change in differential voltage and dividing this by the corresponding change in current.

**Figure 40: Transmitter Eye Voltage and Timing Diagram<sup>1</sup>**



1. This diagram is an excerpt from *PCI Express Base Specification (Revision 1.1), Revision 1.1*, “Transmitter Compliance Eye Diagrams,” page 225.



### 15.6.3 PCIe Differential Receiver Input Specifications

The following table lists the specification of parameters for the differential output of the PCIe lanes.

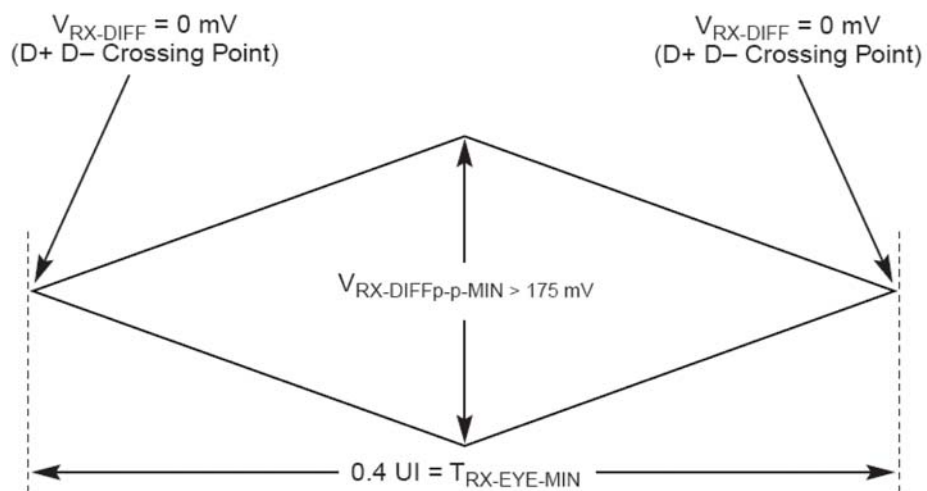
**Table 48: PCIe Differential Receiver Input Specifications**

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400ps +/-300ppm. Ui does not account for SSC dictated variations. See Note 7.
$V_{RX-DIFFp-p}$	Differential Peak to Peak Input Voltage	0.175	-	1.200	V	$V_{RX-DIFFp-p} = 2 *  V_{RX-D+} - V_{RX-D-} $ See Note 8.
$T_{RX-EYE}$	Minimum RX Eye Width	0.4	-	-	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 8, 9, and 10.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFF} = 0V$ ) in relation to recovered TX UI. To be measured after the clock recovery function in Section 4.3.3.2 of the <i>PCI Express Base Specification (Revision 1.1)</i> . See Notes 8 and 9.
$V_{RX-CM-ACp}$	RMS AC Peak Common Mode Input Voltage	-	-	150	mV	$V_{RX-CM-AC} =  V_{RX-D+} + V_{RX-D-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(AVG)}$ of $ V_{RX-D+} + V_{RX-D-} /2$ See Note 8.
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB	Measured over 50 MHz to 1.25 GHz. See Note 11.
$RL_{RX-CM}$	Common Mode Return Loss	6	-	-	dB	Measured over 50 MHz to 1.25 GHz. See Note 11.
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	-	120	Ohms	RX DC Differential Mode impedance. See Note 12.
$Z_{RX-DC}$	DC Input Impedance	40	50	60	Ohms	Required RX D+ as well as D- DC impedance (50 Ohm +/- 20% tolerance). See Notes 8 and 12.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200K	-	-	Ohms	Required RX D+ as well as D- DC impedance when the Receiver terminations do not have power. See Note 13.

**Table 48: PCIe Differential Receiver Input Specifications (Continued)**

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments
$V_{RX-IDLE-DET-DIFFp}$	Electrical Idle Detect Threshold	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp} = 2 *  V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms	An unexpected Electrical Idle ( $V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$ ) must be longer than $T_{RX-IDLE-DET-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Skew	-	-	20	ns	Skew across all lanes on a link. This includes variation in the length of a SKP ordered set (for example, COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.

7. No test load is necessarily associated with this value.
8. Specified at the measurement point and measured using the clock recovery function specified in Section 4.3.3.2. The test load in Figure 4-25 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 4-26). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.
9. The  $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. This parameter is measured with the equivalent of a zero jitter reference clock. The  $T_{RX-EYE}$  measurement is to be met at the target bit error rate. The  $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$  specification is to be met using the compliance pattern at a sample size of 1,000,000 UI.
10. For more information on the RX-EYE measurement, see the *PCI Express Jitter and BER* white paper.
11. The receiver input impedance shall result in a differential return loss greater than or equal to 10 dB with a differential test input signal of no less than 200 mV (peak value, 400mV differential peak to peak) swing around ground applied to D+ and D- lines and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for the return loss measurements is 50 Ohms to ground for both D+ and D- lines (that is, as measured by a Vector Network Analyzer with 50-Ohm probes - see Figure 4-25). Note that the series capacitors  $C_{TX}$  is optional for the return loss measurement.
12. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5ms transition time before the Receiver termination values must be met on all un-configured lanes of a port.
13. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit does not falsely assume a Receiver is powered on when it is not. This term must be measured at 200mV above the RX ground.

**Figure 41: Minimum Receiver Eye Timing and Voltage Compliance Specification<sup>1</sup>**

1. This diagram is an excerpt from *PCI Express Base Specification, Revision 1.1*, "Differential Receiver (RX) Input Specifications," page 230.

## 15.6.4 Reference Clock

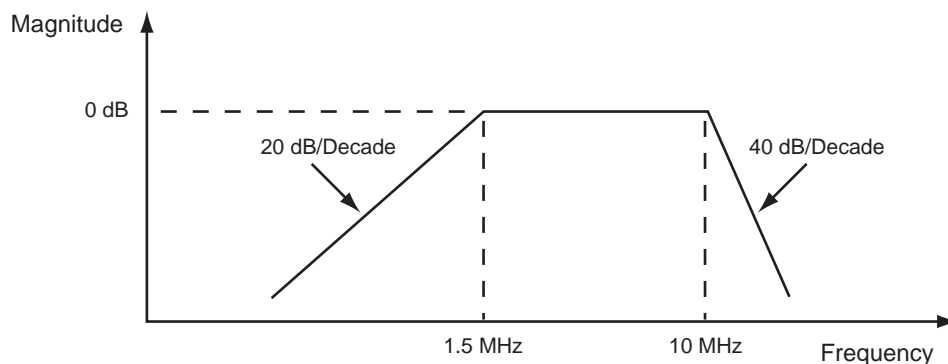
The following table lists the PEB383's electrical characteristics for the differential SerDes reference clock input (PCIE\_REFCLK\_n/p).

**Table 49: Reference Clock (PCIE\_REFCLK\_n/p) Electrical Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{DIFF}$	Differential Input Voltage	350	710	850	mV	-
$V_{CM}$	Differential Input Common Mode Range [(PCIE_REFCLK_p + PCIE_REFCLK_n)/2]	175	-	2000	mV	-
$F_{in}$	Input Clock Frequency	-	100	-	MHz	-
$F_{PCIE\_REFCLK\_P/N}$	Reference Clock Frequency Tolerance	-300	-	+300	ppm	ppm with respect to 100 MHz, based on the PCIe Specification.
$F_{in\_DC}$	Reference Clock Duty Cycle	40	50	60	%	-
$J_{CLK-REF}$	Total Phase Jitter (rms)	-	-	3	ps <sub>rms</sub>	See <sup>a</sup> .
$Z_{in}$	Input Impedance	-	-	-	-	PCIE_REFCLK_p/n is a high-impedance input.

- a. Total Permissible Phase Jitter on the Reference Clock is 3 ps rms. This value is specified with assumption that the measurement is performed with a 20 GSamples/s scope with more than 1 million samples. The zero-crossing times of each rising edges are recorded and an average Reference Clock is calculated. This average period may be subtracted from each sequential, instantaneous period to find the difference between each reference clock rising edge and the ideal placement to produce the Phase Jitter Sequence. The PSD of the phase jitter is calculated and integrated after being weighted with the transfer function shown in [Figure 42](#). The square root of the resulting integral is the rms Total Phase Jitter.

**Figure 42: Weighing Function for RMS Phase Jitter Calculation**



### 15.6.5 Boundary Scan Test Signal Timing

The following table lists the test signal timings for the PEB383.

**Table 50: Boundary Scan Test Signal Timings**

Symbol	Parameter	Min	Max	Units	Notes
$T_{BSF}$	JT_TCK Frequency	0	10	MHz	-
$T_{BSCH}$	JT_TCK High Time	50	-	ns	Measured at 1.5V, <sup>a</sup>
$T_{BSCL}$	JT_TCK Low Time	50	-	ns	Measured at 1.5V, <sup>a</sup>
$T_{BSCR}$	JT_TCK Rise Time	-	25	ns	0.8V to 2.0V, <sup>a</sup>
$T_{BSCF}$	JT_TCK Fall Time	-	25	ns	2.0V to 0.8V, <sup>a</sup>
$T_{SIS1}$	Input Setup to JT_TCK	10	-	ns	<sup>b</sup>
$T_{BSIH1}$	Input Hold from JT_TCK	10	-	ns	<sup>b</sup>
$T_{BSOV1}$	JT_TDO Output Valid Delay from falling edge of JT_TCK.	-	15	ns	<sup>c, d</sup>
$T_{OF1}$	JT_TDO Output Float Delay from falling edge of JT_TCK	-	15	ns	<sup>c, e</sup>

a. Not tested.

b. See [Figure 43](#).

c. Outputs precharged to  $V_{DD33}$ .

d. See [Figure 44](#).

e. A float condition occurs when the output current becomes less than  $I_{LO}$ . Float delay is not tested (see [Figure 44](#)).

### 15.6.6 Reset Timing

The following table lists the reset signal timings for the PEB383.

**Table 51: Reset Timing**

Symbol	Parameter	Min	Max	Units	Notes
$T_{POR}$	Power supplies in recommended operating range to de-assertion of device reset	100	-	ms	The PCIe specification requires reset (PCIE_PERSTn) to remain asserted for 100 ms after power supplies are valid.
$T_{ACTIVE}$	Reset active time	1	-	ms	-

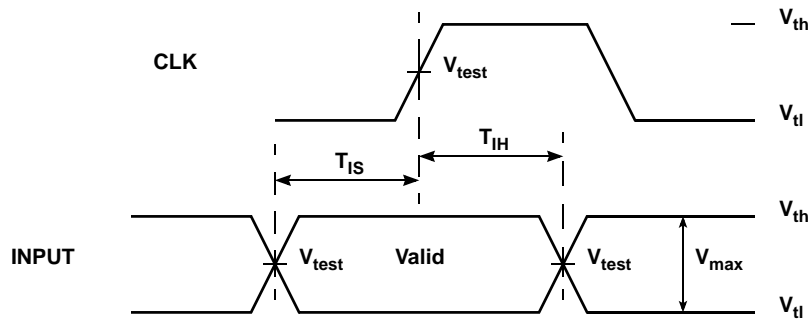
**Table 51: Reset Timing (Continued)**

Symbol	Parameter	Min	Max	Units	Notes
-	PCI_CLK clock stable to de-assertion of device reset	100	-	us	-
-	Power-up strapping hold from de-assertion of device reset	0	-	ns	-
$T_{HIZ}$	Assertion of reset to outputs tri-state	-	10	ns	-

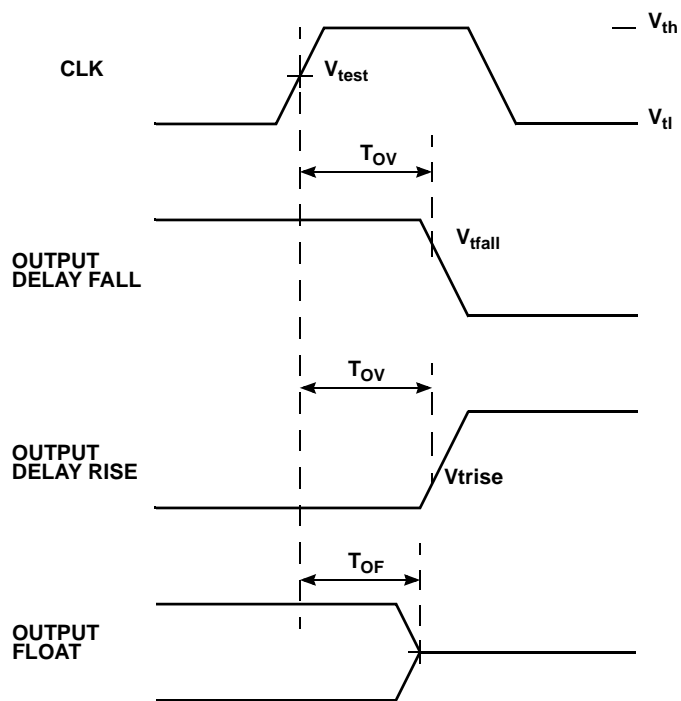
## 15.7 AC Timing Waveforms

This section contains AC timing waveforms for the PEB383.

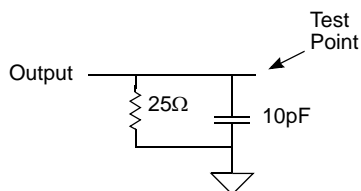
**Figure 43: Input Timing Measurement Waveforms**



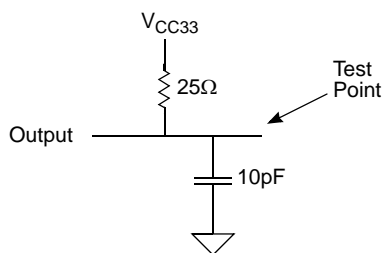
**Figure 44: Output Timing Measurement Waveforms**

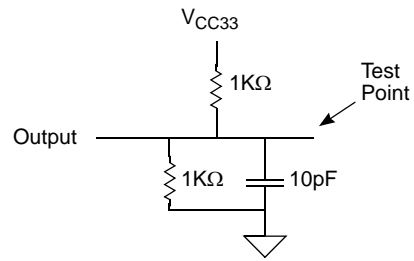


**Figure 45: PCI  $T_{OV(max)}$  Rising Edge AC Test Load**



**Figure 46: PCI  $T_{OV(max)}$  Falling Edge AC Test Load**



**Figure 47: PCI  $T_{OV}$  (min) AC Test Load**



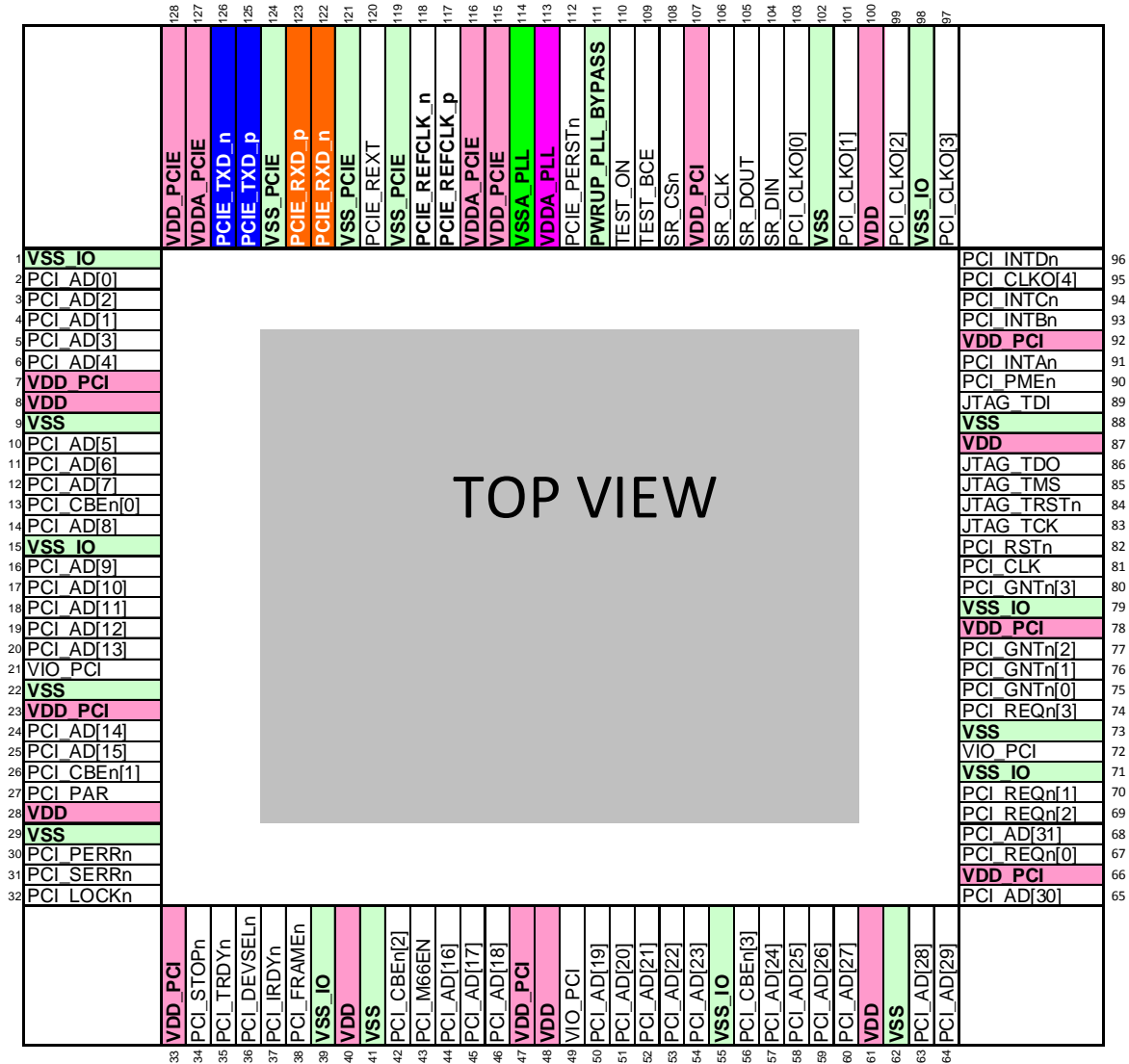
## 16. Packaging

Topics discussed include the following:

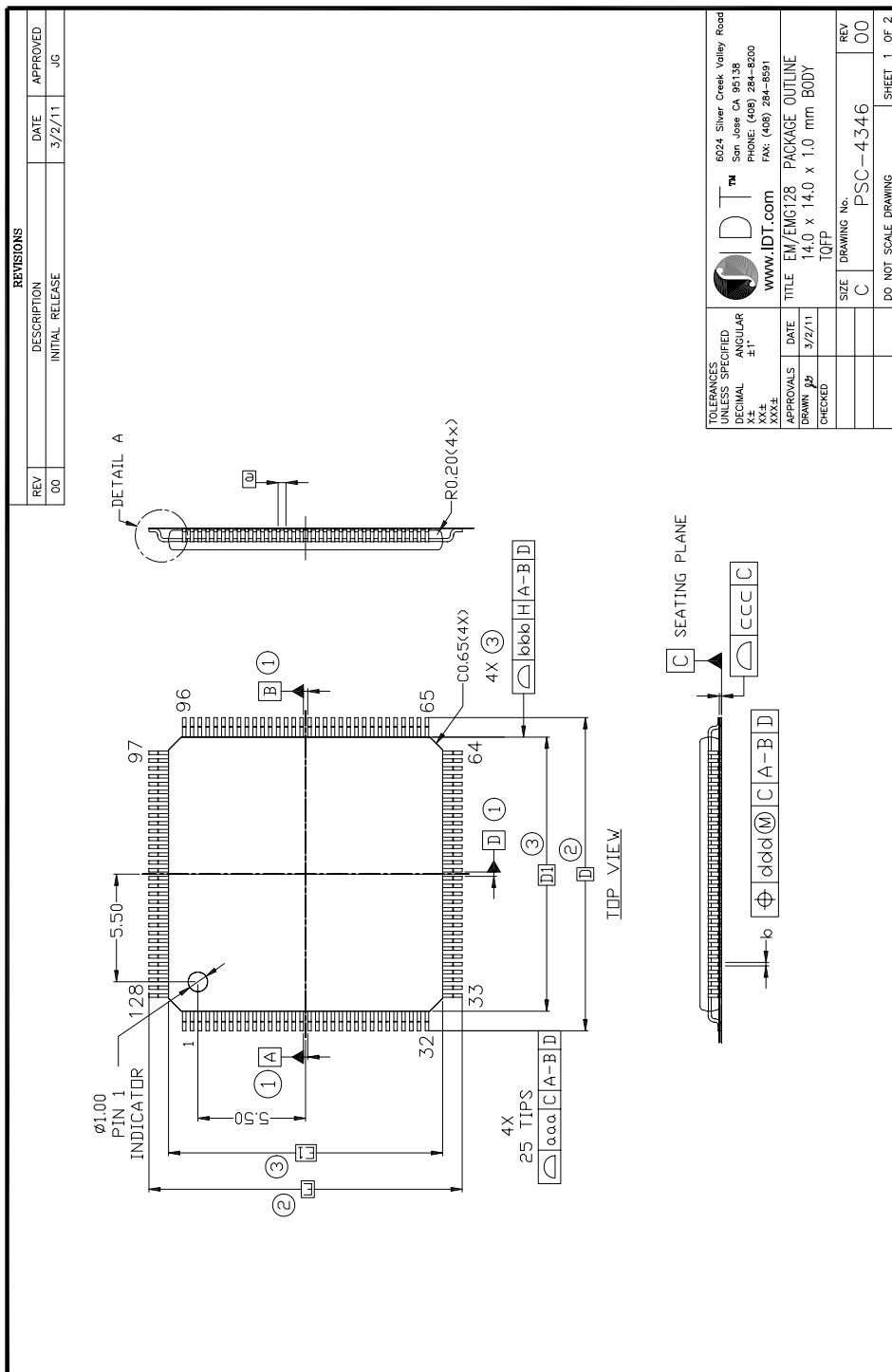
- “Pinouts and Mechanical Diagrams”
  - “Thermal Characteristics”
  - “Moisture Sensitivity”
-

# 16.1 Pinouts and Mechanical Diagrams

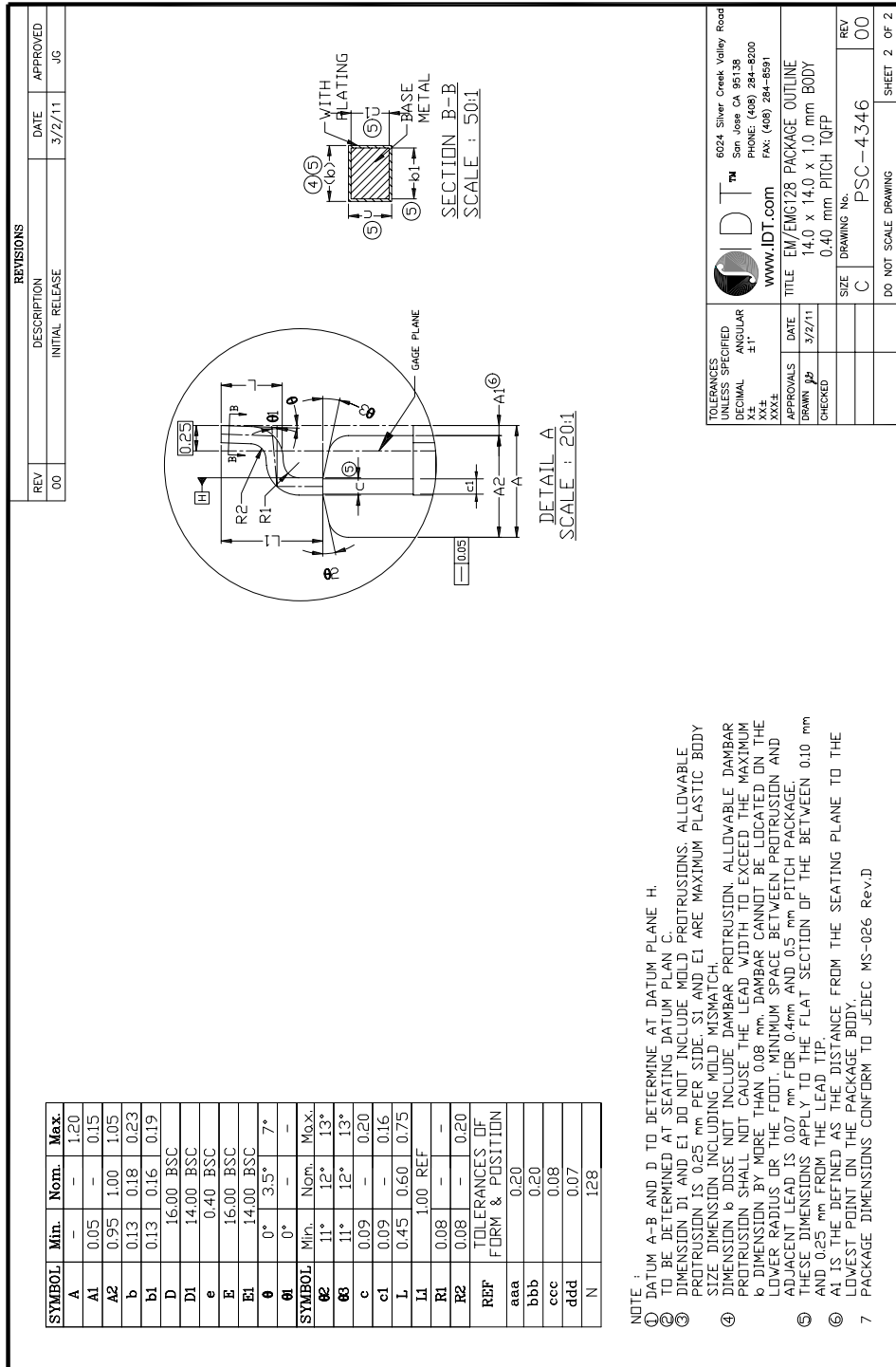
## 16.1.1 QFP Package Pinout



### 16.1.2 QFP Package Drawing



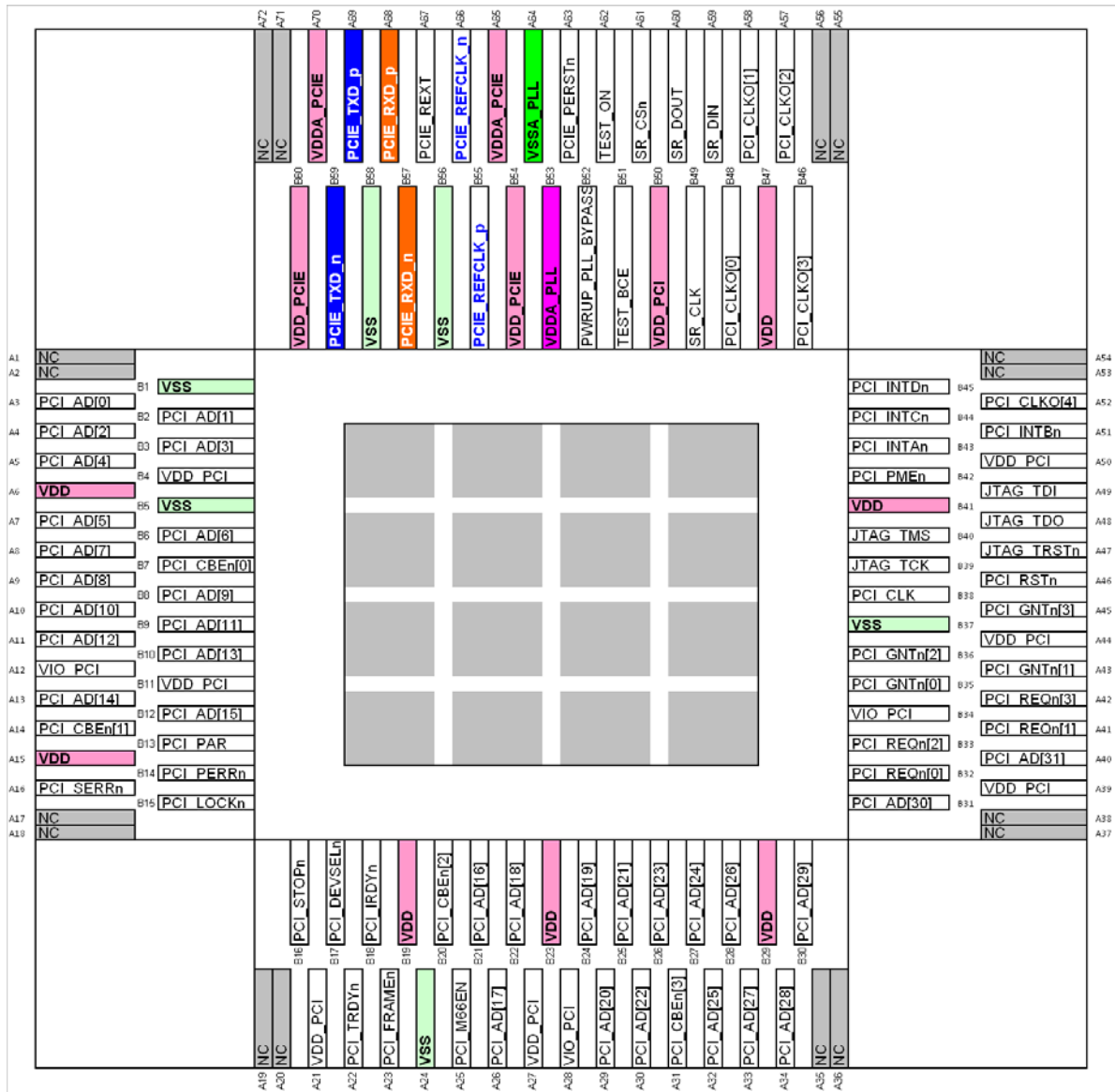
16.1.2.1 QFP Package Drawing — Page 2



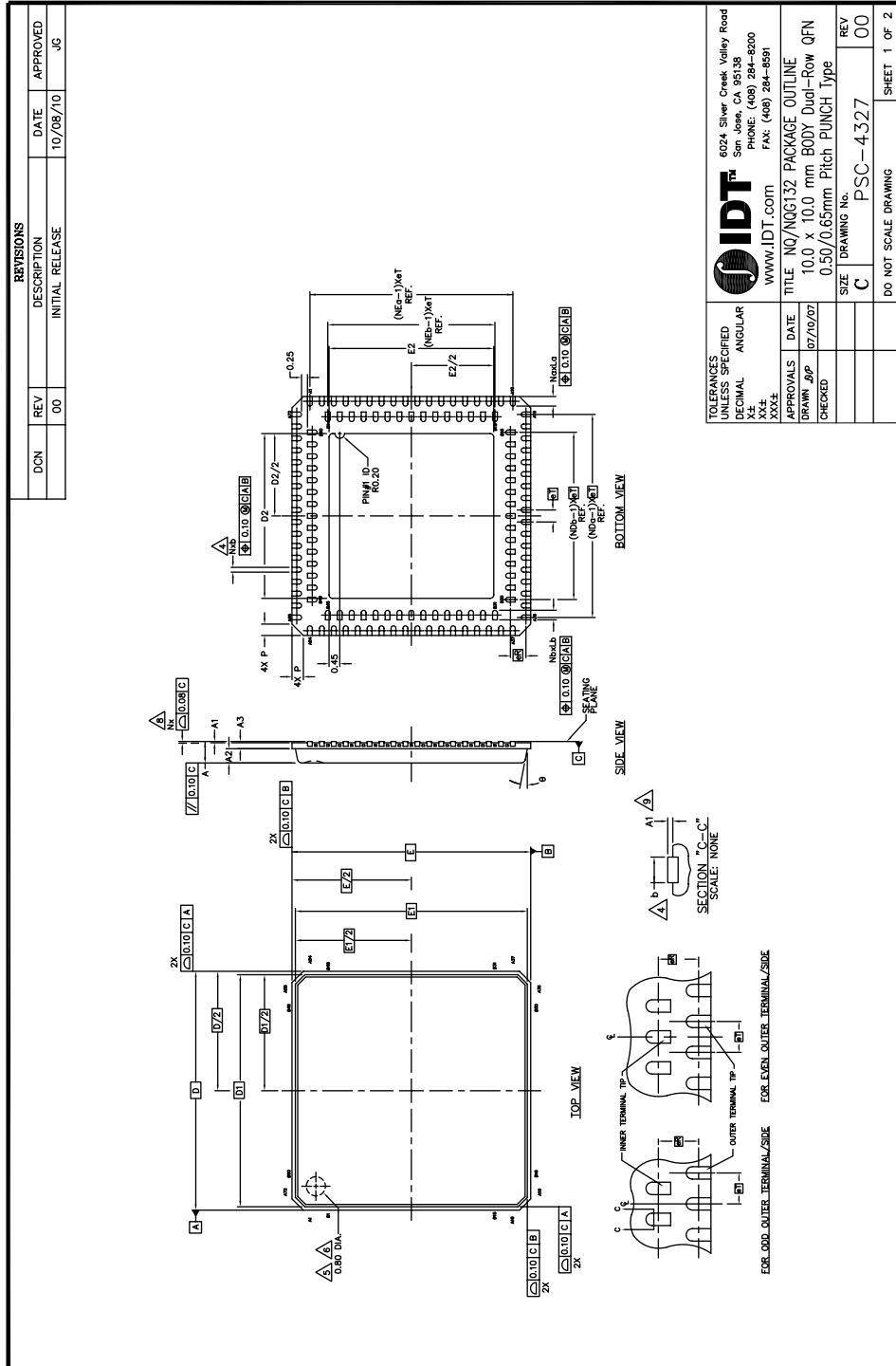
NOTE :

- ① DATUM A-B AND D TO DETERMINE AT DATUM PLANE H.
- ② TO BE DETERMINED AT SEATING DATUM PLAN C.
- ③ DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. S1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- ④ DIMENSION b DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 mm FOR 0.4mm AND 0.5 mm PITCH PACKAGE. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
- ⑤ A1 IS THE DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- ⑦ PACKAGE DIMENSIONS CONFORM TO JEDEC MS-026 Rev.D

### 16.1.3 QFN Package Pinout



### 16.1.4 QFN Package Drawing



16.1.4.1 QFN Package Drawing — Page 2

REVISIONS			
DCN	REV	DESCRIPTION	DATE
	00	INITIAL RELEASE	10/08/10
			APPROVED JG

COMMON DIMENSIONS		
MIN.	NOM.	MAX.
A	0.80	0.95
A <sub>1</sub>	0.90	0.90
A <sub>2</sub>	0.90	0.60
A <sub>3</sub>	0.35	0.60
A <sub>4</sub>	0.25	REF
D	10.00	BSC
D1	9.73	BSC
E	10.00	BSC
E1	9.73	BSC

PITCH VARIATION		
MIN.	NOM.	MAX.
e <sub>1</sub>	0.50	BSC
e <sub>2</sub>	0.65	BSC
N	1.32	
NDg	18	3
NDb	15	3
NEg	18	3
NEb	15	3
Lg	0.30	0.40
Lb	0.30	0.40
b	0.17	0.22
D2	5.45	
E2	5.45	
θ	—	12°
P	0.24	0.42
		0.60

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. — 1994.
3. N IS THE NUMBER OF TERMINALS.
- NDg, NDb ARE THE NUMBER OF TERMINALS IN X-DIRECTION & NEG, NEb ARE THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN # IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
9. APPLIED ONLY FOR TERMINALS.
- <STANDARD>

GENERAL : NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION-0.20

TOLERANCES UNLESS SPECIFIED	DECIMAL	ANGULAR
XX±		
XX°±		
APPROVALS	DATE	
DRAWN JAP	07/10/07	
CHECKED		
TITLE INQ/NGG132 PACKAGE OUTLINE		
10.0 x 10.0 mm BODY Dual-Row QFN		
0.50/0.65mm Pitch PUNCH Type		
SIZE DRAWING NO. PSC-4327		
REV 00		
DO NOT SCALE DRAWING SHEET 2 OF 2		

## 16.2 Thermal Characteristics

Heat generated by the packaged silicon must be removed from the package to ensure the silicon is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the silicon temperature may exceed the temperature limits. A consequence of this is that the silicon may fail to meet the performance specifications and the reliability objectives may be affected.

Failure mechanisms and failure rate of a device has an exponential dependence on the silicon operating temperatures. Therefore, the control of the package, and by extension the Junction temperature, is essential to ensure product reliability. The PEB383 is specified safe for operation when the Junction temperature is within the recommended limits as shown in [Table 42](#).

**Table 52: Thermal Specifications — 66MHz**

Power estimates are based on simulations — 0.894 W @ 66MHz					
Package	Parameter	Air Flow			Unit
		0 m/s	1 m/s	2 m/s	
QFP — EM128	$\theta_{JA}$	43.9	36.9	33.7	C/W
	$T_j$ Max @ $T_{AMB}=85^\circ\text{C}$	124	118	115	C
	$T_j$ Max @ $T_{AMB}=70^\circ\text{C}$	109	103	100	C
	$\theta_{JC}$	14	—	—	C/W
QFN — NQ132	$\theta_{JA}$	23.4	18.5	17	C/W
	$T_j$ Max @ $T_{AMB}=85^\circ\text{C}$	106	102	100	C
	$T_j$ Max @ $T_{AMB}=70^\circ\text{C}$	91	87	85	C
	$\theta_{JC}$	11.5			C/W
	$\theta_{JB}$	0.42			C/W



**Table 53: Thermal Specifications — 33MHz**

Power estimates are based on simulations — 0.511 W @ 33MHz					
Package	Parameter	Air Flow			Unit
		0 m/s	1 m/s	2 m/s	
<b>QFP — EM128</b>	$\theta_{JA}$	43.9	36.9	33.7	C/W
	$T_j$ Max @ $T_{AMB}=85^{\circ}\text{C}$	107	104	102	C
	$T_j$ Max @ $T_{AMB}=70^{\circ}\text{C}$	92	89	87	C
	$\theta_{JC}$	14	—	—	C/W
	<b>QFN — NQ132</b>	$\theta_{JA}$	23.4	18.5	17
$T_j$ Max @ $T_{AMB}=85^{\circ}\text{C}$		97	94	94	C
$T_j$ Max @ $T_{AMB}=70^{\circ}\text{C}$		82	79	79	C
$\theta_{JC}$		11.5			C/W
$\theta_{JB}$		0.42			C/W

Table 52 and Table 53 show the simulated thermal characteristics ( $\theta_{JA}$ ,  $\theta_{JB}$ , and  $\theta_{JC}$ ) of the PEB383 package at 66MHz and 33MHz respectively. The thermal resistance  $\theta_{JA}$  characteristics of a package depends of multiple variables other than just the package. In a typical application, designers must take into account various system-level and environmental characteristics, such as:

- Package mounting (vertical/horizontal)
- System airflow conditions (laminar/turbulent)
- Heat sink design and thermal characteristics
- Heat sink attachment method
- PWB size, layer count, and conductor thickness
- Influence of the heat dissipating components assembled on the PWB (neighboring effects)

The results in Table 53 and Table 52 are based on a JEDEC Thermal Test Board configuration (JESD51-9), and does not factor in the system-level characteristics described above. As such, these values are for reference only.

#### Example of Thermal Data Usage

Based on above  $\theta_{JA}$  data and specified conditions, the Junction temperature of the PEB383 with a 0 m/s airflow can be determined using the following formula:

$$T_J = \theta_{JA} * P + T_{AMB}$$

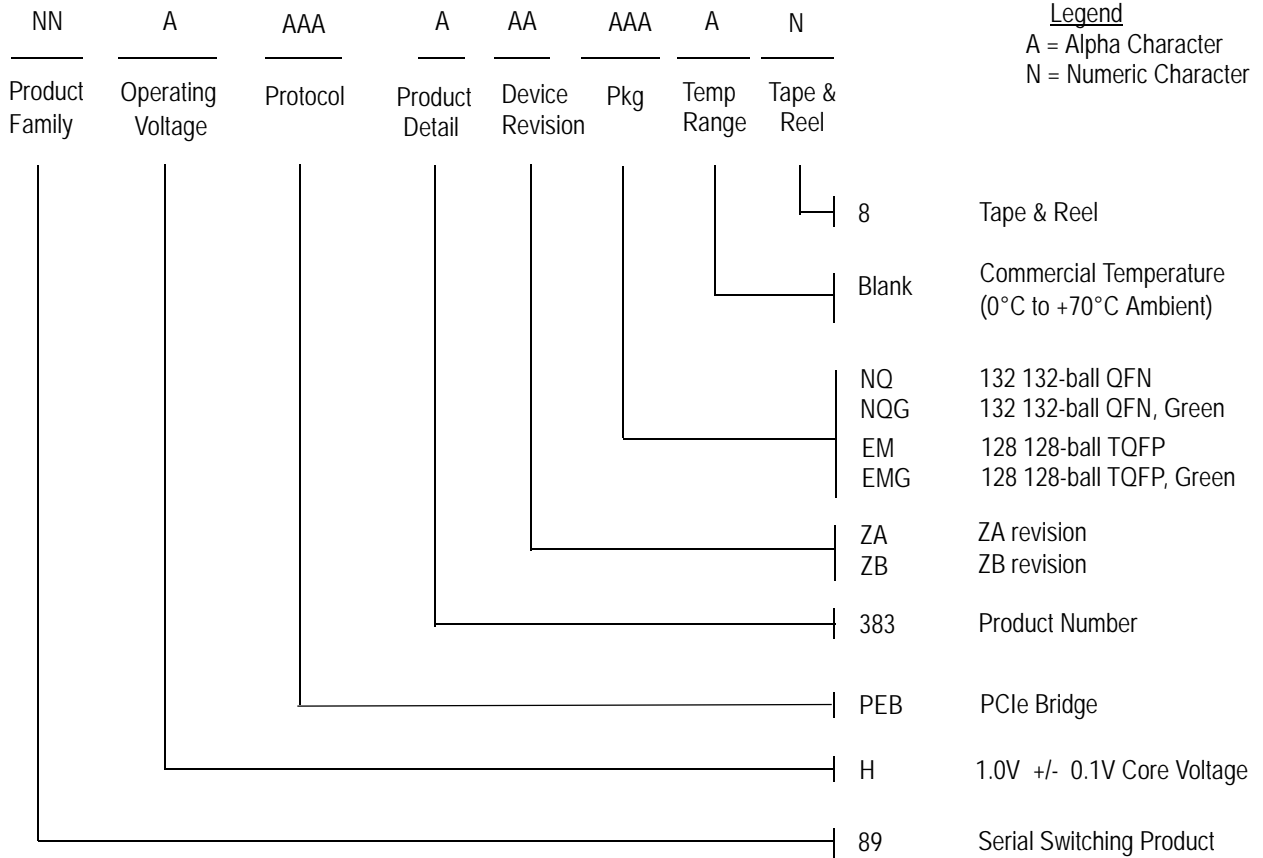
Where:

- $T_J$  is the Junction temperature
- P is the Power consumption
- $T_{AMB}$  is the Ambient temperature

## 16.3 Moisture Sensitivity

The moisture sensitivity level (MSL) for the PEB383 is 3.

# 17. Ordering Information



## Valid Combinations

89HPEB383ZANO 89HPEB383ZANO8	132-ballQFN package, Commercial Temp.	89HPEB383ZBNO 89HPEB383ZBNO8	132-ballQFN package, Commercial Temp.
89HPEB383ZANQG 89HPEB383ZANQG8	132-ball Green QFN package, Commercial Temp.	89HPEB383ZBNQG 89HPEB383ZBNQG8	132-ball Green QFN package, Commercial Temp.
89HPEB383ZAEM 89HPEB383ZAEM8	128-ball TQFP package,Commercial Temp.	89HPEB383ZBEM 89HPEB383ZBEM8	128-ball TQFP package,Commercial Temp.
89HPEB383ZAEMG 89HPEB383ZAEMG8	128-ball Green TQFP package, Commercial Temp.	89HPEB383ZBEMG 89HPEB383ZBEMG8	128-ball Green TQFP package, Commercial Temp.



---

# Glossary

<b>Address decode window</b>	The address range defined by a device's base address registers when operating in non-transparent addressing mode. If a transaction address on the bus falls within a device's address decode window, the device claims the transaction.
<b>Base and limit register</b>	A configuration register that stores memory or I/O address decode information in a device. If the address of a transaction falls within the window defined by a device's base and limit registers, the device claims the transaction. Base and Limit registers are used only by transparent bridges.
<b>Compact PCI</b>	cPCI. It is an adaptation of the <i>PCI Local Bus Specification (Revision 2.2)</i> for Industrial and/or embedded applications that require a more robust mechanical form factor than desktop PCI.
<b>Completer (PCIe)</b>	The device that is targeted by a requester during a PCIe transaction. A requester reads data from a completer, or writes data to a completer. A requester can be either a root complex or an endpoint device.
<b>Completer ID</b>	This value uniquely identifies the completer of a transaction request. It consists of a completer's bus number, device number, and function number.
<b>Configuration transaction</b>	A read or write access of a PCI device's configuration registers.
<b>Downstream port</b>	A PCIe port that points in the direction away from the root complex (for example, a root complex port).
<b>Egress port</b>	A PCIe port that transmits a packet to another PCIe device.
<b>Endpoint</b>	A type of PCIe device, or mode of operation, that function as requesters or completers of PCIe transactions (examples include Ethernet, USB, and graphic devices). If a PCIe port is not configured as a root complex or a switch then it is considered an endpoint. An endpoint can support up to eight functions.
<b>Fairness algorithm</b>	Arbitration logic that helps low and high priority devices gain fair access to a peripheral bus. This logic also helps prevent deadlocks among bus-mastering devices in a system.
<b>Flow control</b>	The method of communicating receive buffer status from a receiver to a transmitter to prevent receive buffer overflow and to allow transmitter compliance with ordering rules.
<b>Hierarchy</b>	A PCIe fabric of all devices and links associated with a root complex. The devices can be connected either directly or indirectly (through switches and bridges) to the root complex.
<b>Hot swap</b>	This refers to the process of inserting and extracting CompactPCI boards from an active system without adversely affecting system operation.
<b>Ingress port</b>	A PCIe port that receives a packet from another PCIe device.
<b>Link</b>	An interconnection between two PCIe devices. A link consists of either x1, x2, x4, x8, x16, or x32 pairs of signals between two devices. Each grouping of signals is referred to as a <i>lane</i> .
<b>Memory-mapped I/O</b>	MIO. Memory-mapped I/O is used for non-prefetchable PCI memory transactions.

<b>Message</b>	A TLP used to communicate information outside of the memory, I/O, and configuration spaces. Message TLPs are always posted, and may or may not contain data.
<b>Non-transparent addressing</b>	This type of addressing is used by a PCI bridging device to isolate the primary address map from the secondary address map. It provides address translation for PCI devices located in separate address domains with multiple host processors. This mode of operation, which is sometimes called embedded bridging, allows for distinct PCI memory spaces to be connected through defined windows with address translation from one memory domain to another.
<b>PCI extended capabilities</b>	Optional features supported by the <i>PCI Local Bus Specification</i> . Some examples of extended capabilities include: Vital Product Data, Message Signaled Interrupts, and Slot Numbering. A device that supports extended capabilities uses a PCI capability list to access the features located in its PCI configuration space.
<b>Prefetchable memory</b>	The process of prefetching memory occurs when a line of information from memory is read before a bus master requests it. If a bus master later requests the memory line, the bus target can supply it immediately. This type of memory access minimizes the time required to retrieve target memory.
<b>Requester (PCIe)</b>	The device that originates a PCIe transaction. A requester can be either a root complex or an endpoint device.
<b>Requester ID (PCIe)</b>	This value uniquely identifies the requester of a transaction. It consists of a requester's bus number, device number, and function number.
<b>Root complex</b>	<p>This is a type of PCIe device, or mode of operation, that connects a host processor and memory sub-system to a PCIe fabric. The root complex generates transaction requests on behalf of the host processor — such as configuration, memory, and I/O — to other devices in the PCIe hierarchy. It also handles interrupts and power management events.</p> <p>The root complex appears as P2P bridge(s) to the PCIe links, and can support one or more PCIe ports.</p>
<b>Transparent addressing</b>	This type of PCI addressing is used by a bridging device to support configuration mapping but not perform address translation between two buses. When a device is configured in transparent mode, it provides standard PCI bus bridging support through its base and limit registers. These registers define address decode windows for multiple bridges so that transactions can be passed transparently in a system. This enables devices that are connected to multiple bridging devices to share a single, unified address space.
<b>Upstream port</b>	A PCIe port that points in the direction of the root complex (for example, an endpoint port).

# Index

## A

absolute maximum ratings 219  
 AC timing  
   PCI Interface 222  
 AC timing specifications 222  
 AC timing waveforms 232  
 address decoding  
   I/O memory 32  
   ISA 35  
   memory-mapped I/O 29  
   non-transparent 37  
   prefetchable memory 31  
   VGA 34  
 advanced error reporting capability registers 188  
 arbitration 59  
 ASPM 94

## B

buffer  
   downstream non-posted 26  
   downstream posted 26  
   upstream non-posted 24  
   upstream posted 25  
 buffer management 50  
 bus arbiter 59

## C

clocking  
   PCI 91  
   PCIe 90  
 cold reset 88  
 completer abort completion status errors 79  
 configuration retry 47  
 configuration transaction  
   overview 43  
   Type 0 44  
   Type 1 44  
   Type 1 to special cycle 46  
   Type 1 to Type 0 45  
   Type 1 to Type 1 45

## D

D state transitions 98  
 D0 state 97  
 D3cold state 97  
 D3hot state 97  
 DC and operating characteristics 221  
 device power states 97  
 device register map 120  
 document conventions  
   document status 2

  numeric conventions 2  
   symbols 2  
 downstream  
   data path 22  
   non-transparent registers 184

## E

ECRC error 70  
 EEPROM controller 101  
 EEPROM device 102  
 EEPROM image 104  
 error handling 65  
   PCI 75  
   PCIe 68  
 exclusive access 57

## F

flow control  
   advertisements 49  
   credits 27  
   overview 26

## H

hot reset 89

## I

I/O addressing 32  
 IEEE 1149.1 Interface 111  
 interrupt handling 63  
 interrupt routing 64  
 interrupt sources 64  
 ISA addressing 35

## J

JTAG 109  
   read access 112  
   write access 111  
 JTAG test pins 113  
 JTAG\_TCK signal 19  
 JTAG\_TDI signal 19  
 JTAG\_TDO signal 19  
 JTAG\_TMS signal 19  
 JTAG\_TRSTn signal 19

## L

L0 state 95  
 L1 state 95  
 L2/L3 ready 95  
 L3 state 95  
 LDn state 95  
 LOs state 95

## M

master-abort errors 73

mechanical diagram 236  
 memory-mapped I/O addressing 29  
 message signaled interrupts (MSI) 63  
 message signaled interrupts (MSI-X) 63  
 message transactions 55  
 message-based interrupts  
   enhanced message signaled interrupts 63  
   message signaled interrupts 63

## N

non-transparent addressing 37  
 non-transparent registers  
   downstream 184  
   upstream 156

## O

ordering information 245

## P

PCI capability registers 159  
 PCI clocking 91  
 PCI errors 76  
 PCI Interface  
   AC timing 222  
 PCI reset 89  
 PCI transactions 53  
 PCIe capability registers 173  
 PCIe clocking 90  
 PCIe configuration space 117  
 PCIe enhanced configuration 46  
 PCIe link states 96  
 PCIe reset 88  
 PCIe transactions 54  
 poisoned TLP 69  
 power characteristics 220  
 power management 93  
 power management event 98  
 power states 94  
 power supply sequencing 221  
 prefetchable memory addressing 31  
 prefetching algorithm 27

## R

recommended operating conditions 220  
 register map 120  
 requestor ID 50  
 reset  
   PCI 89  
   PCIe 88  
 round-robin arbitration 60

## S

SerDes TAP controller 113  
 short term caching 28  
 system errors 80

## T

TAP controller 110  
 target-abort errors 74  
 TCK signal 19  
 TDI signal 19  
 TDO signal 19  
 thermal characteristics 242  
 timeout errors 79  
 timing waveforms 232  
 TMS signal 19  
 transaction forwarding  
   PCI to PCIe 51  
   PCIe to PCI 50  
 transaction management  
   downstream 24  
   upstream 23  
 transaction ordering 56  
 transactions supported  
   PCI 53  
   PCIe 54  
 TRSTn signal 19  
 Type 0 configuration transaction 44  
 Type 1 configuration transaction 44  
 Type 1 to special cycle configuration transaction 46  
 Type 1 to Type 0 configuration transaction 45  
 Type 1 to Type 1 configuration transaction 45  
 typical applications 10

## U

uncorrectable address/attribute errors 72  
 uncorrectable data error 71  
 Undefined 116  
 unsupported request completion status errors 79  
 upstream  
   data path 21  
   non-transparent registers 156

## V

VGA addressing 34

## W

warm reset 88