32-Lane 8-Port PCI Express® System Interconnect Switch

89HPES32H8
Data Sheet

Device Overview

The 89HPES32H8 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES32H8 is a 32-lane, 8-port system interconnect switch optimized for PCI Express packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, and embedded systems.

Features

- High Performance PCI Express Switch
  - *Eight maximum switch ports*
    - Four main ports each of which consists of eight SerDes
    - Each x8 main port can further bifurcate to 2 x4-ports
  - *Thirty-two 2.5 Gbps embedded SerDes*
    - Supports pre-emphasis and receive equalization on per-port basis
  - *Delivers 128 Gbps (16 GBps) aggregate switching capacity*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *Supports two virtual channels and eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Port arbitration schemes utilizing round robin algorithms*
  - *Virtual channels arbitration based on priority*
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all ports*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
  - *Ability to control device via SMBus*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates thirty-two 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Redundant upstream port failover capability*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*

Block Diagram

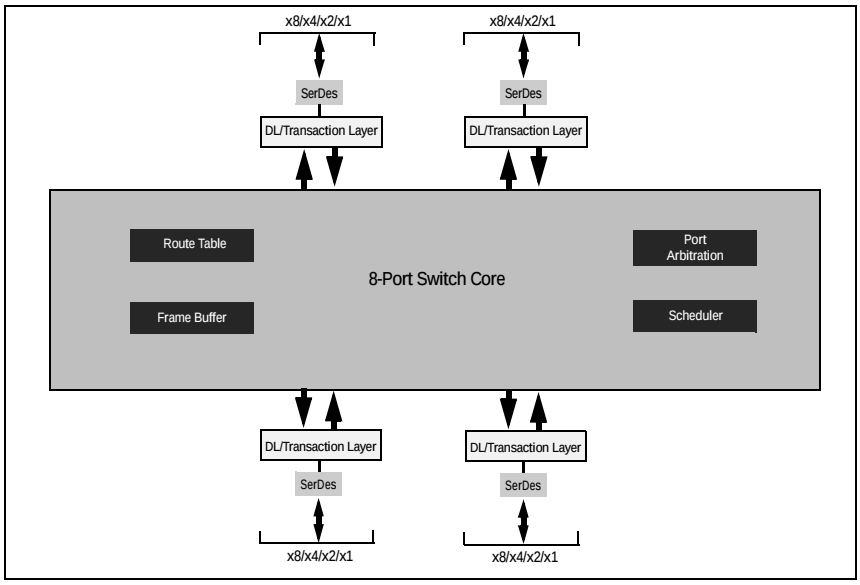


Figure 1 Internal Block Diagram

- *Supports optional PCI Express end-to-end CRC checking*
- *Supports optional PCI Express Advanced Error Reporting*
- *Supports PCI Express Hot-Plug*
  - Compatible with Hot-Plug I/O expanders used on PC motherboards
- *Supports Hot-Swap*

◆ Power Management

- *Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)*
  - Supports powerdown modes at the link level (L0, L0s, L1, L2/L3 Ready and L3) and at the device level (D0, $D3_{hot}$)
- *Unused SerDes disabled*

◆ Testability and Debug Features

- *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
- *Ability to read and write any internal register via the SMBus*
- *Ability to bypass link training and force any link into any mode*
- *Provides statistics and performance counters*

◆ Thirty-two General Purpose Input/Output pins

- *Each pin may be individually configured as an input or output*
- *Each pin may be individually configured as an interrupt input*
- *Some pins have selectable alternate functions*

◆ Packaged in a 31mm x 31mm 900-ball Flip Chip BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES32H8 provides the most efficient system interconnect switching solution for applications requiring maximum throughput, low latency, and simple board layout with a minimum number of board layers. It provides 128 Gbps of aggregated, full-duplex switching capacity through 32 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES32H8 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES32H8 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and two Virtual Channels (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded applications.

SMBus Interface

The PES32H8 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES32H8, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES32H8 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

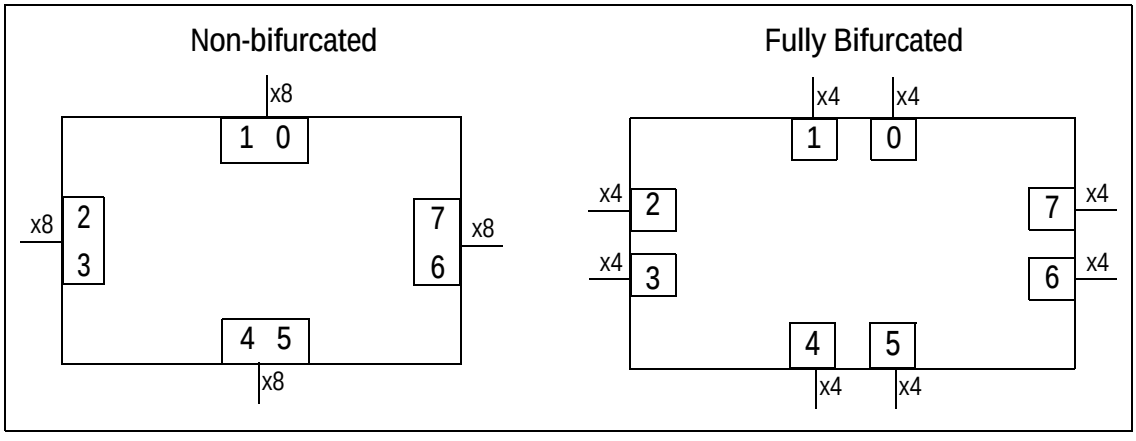


Figure 2 Port Configuration Examples

Note: The configurations in the above diagram show the maximum port widths. The PES32H8 can negotiate to narrower port widths — x4, x2, or x1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES32H8 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES32H8 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES32H8 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES32H8 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

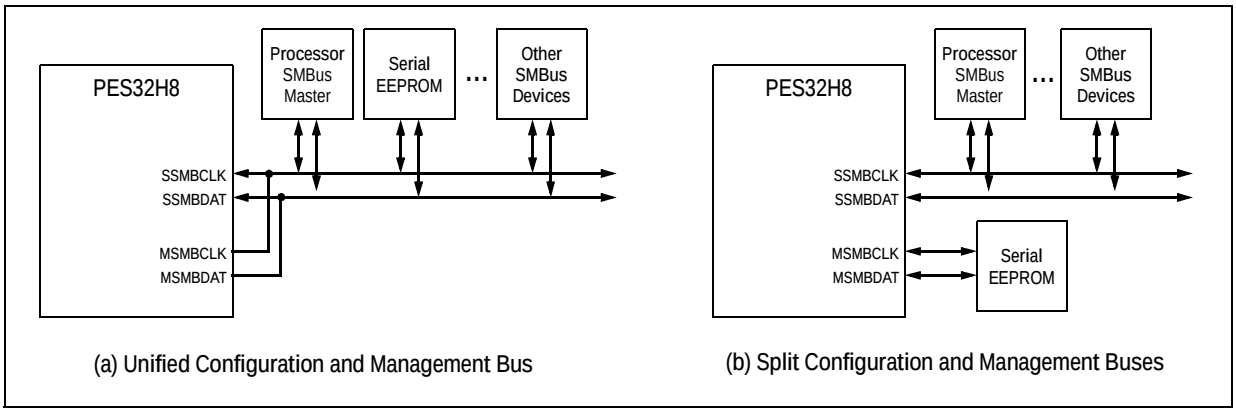


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES32H8 supports PCI Express Hot-Plug on each downstream port (ports 1 through 7). To reduce the number of pins required on the device, the PES32H8 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32H8 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES32H8. In response to an I/O expander interrupt, the PES32H8 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES32H8 provides 32 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES32H8. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix “N” or “P.” The differential signal ending in “P” is the positive portion of the differential pair and the differential signal ending in “N” is the negative portion of the differential pair.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE1TP[3:0] PE1TN[3:0]	O	PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE2RP[3:0] PE2RN[3:0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2.
PE3RP[3:0] PE3RN[3:0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE3TP[3:0] PE3TN[3:0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pairs for port 2. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE4RP[3:0] PE4RN[3:0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4.
PE5RP[3:0] PE5RN[3:0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE5TP[3:0] PE5TN[3:0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE6RP[3:0] PE6RN[3:0]	I	PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pairs for port 6.
PE6TP[3:0] PE6TN[3:0]	O	PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pairs for port 6.
PE7RP[3:0] PE7RN[3:0]	I	PCI Express Port 7 Serial Data Receive. Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE7TP[3:0] PE7TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz
PEREFCLKP[3:0] PEREFCLKN[3:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins (Part 1 of 3)

Signal	Type	Name/Description
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P7RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 7
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[15]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[16]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[17]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[18]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[19]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 2 of 3)

Signal	Type	Name/Description
GPIO[20]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[21]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 0
GPIO[22]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 1
GPIO[23]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 2
GPIO[24]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 3
GPIO[25]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[26]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[27]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[28]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[29]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[30]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[31]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN10 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 10

Table 4 General Purpose I/O Pins (Part 3 of 3)

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	Common Clock Upstream. When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	Port 0 and 1 Merge. When this pin is asserted, port 1 is merged with port 0 to form a single x8 port. The SerDes lanes associated with port B become lanes 4 through 7 of port 0.
P23MERGEN	I	Port 2 and 3 Merge. When this pin is asserted, port 3 is merged with port 2 to form a single x8 port. The SerDes lanes associated with port D become lanes 4 through 7 of port 2.
P45MERGEN	I	Port 4 and 5 Merge. When this pin is asserted, port 5 is merged with port 4 to form a single x8 port. The SerDes lanes associated with port F become lanes 4 through 7 of port 4.
P67MERGEN	I	Port 6 and 7 Merge. When this pin is asserted, port 7 is merged with port 6 to form a single x8 port. The SerDes lanes associated with port H become lanes 4 through 7 of port 6.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES32H8 and initiates a PCI Express fundamental reset.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES32H8 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	Switch Mode. These configuration pins determine the PES32H8 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD**. Power supply for core logic.
V_{DD}IO	I	**I/O VDD**. LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power**. PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power**. PCI Express analog power used by the PLL and bias generator.
V_{SS}	I	**Ground**.
V_{TT}PE		**PCI Express Serial Data Transmit Termination Voltage**. This pin allows the driver termination voltage to be set, enabling the system designer to control the Common Mode Voltage and output voltage swing of the corresponding PCI Serial Data Transmit differential pair.

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES32H8 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE3RN[3:0]	I				
	PE3RP[3:0]	I				
	PE3TN[3:0]	O				
	PE3TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE5RN[3:0]	I				
	PE5RP[3:0]	I				
	PE5TN[3:0]	O				
	PE5TP[3:0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PE7RN[3:0]	I				
	PE7RP[3:0]	I				
	PE7TN[3:0]	O				
	PE7TP[3:0]	O				

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface (cont.)	PEREFCLKN[3:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[3:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	STI[1]	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I			pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[31:0]	I/O	LVTTL		pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Schmitt Trigger Input (STI).

Logic Diagram — PES32H8

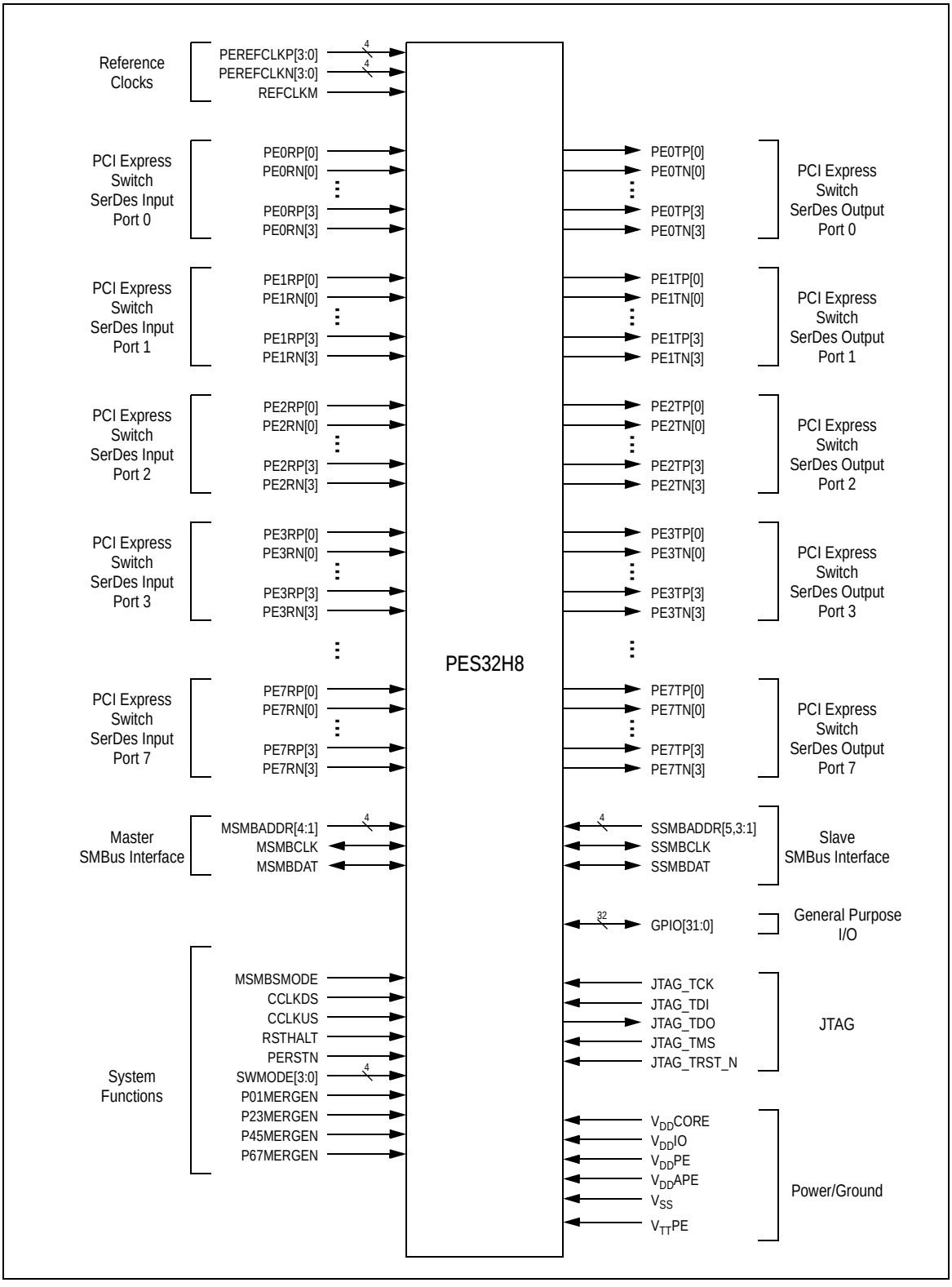


Figure 4 PES32H8 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX-IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[31:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 5.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

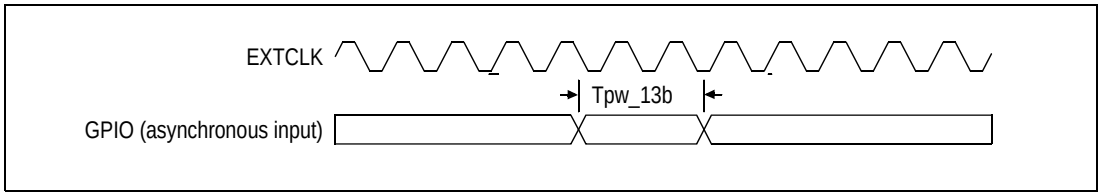


Figure 5 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

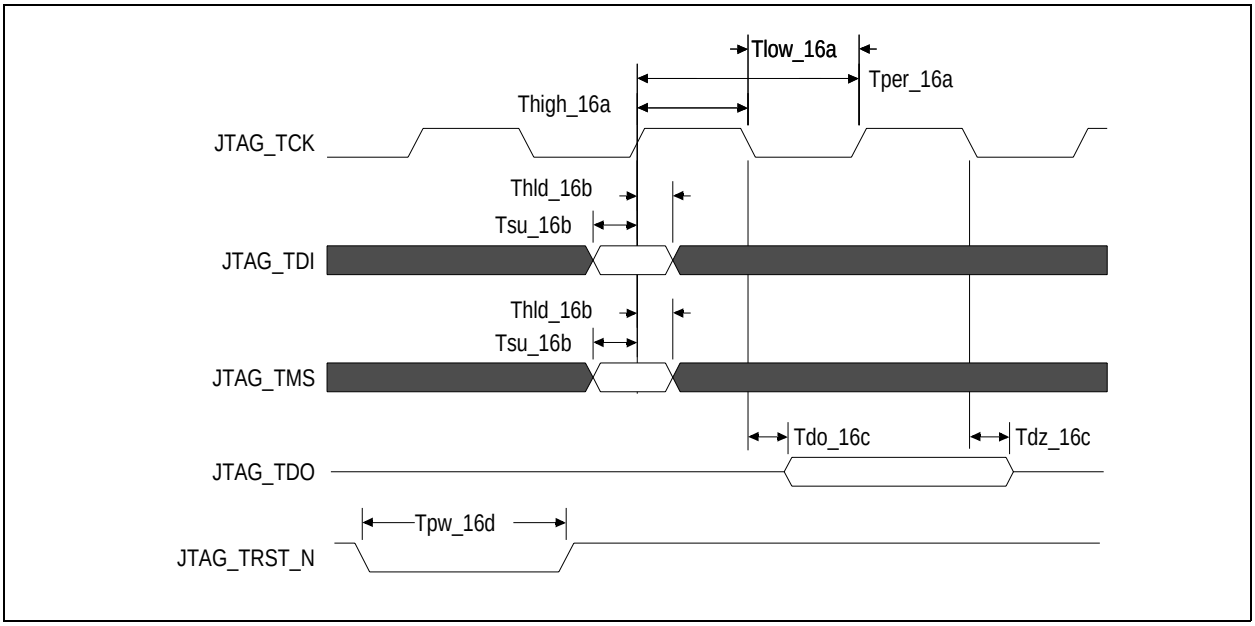


Figure 6 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES32H8 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES32H8, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES32H8 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
8/8/8/8	mA	1800	2100	1677	1990	792	909	804	826	1	2	5.5W	6.81W
	Watts	1.81	2.31	1.68	2.19	0.79	1.0	1.21	1.3	0.003	0.01		

Table 15 PES32H8 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES32H8 (31mm^2 FCBGA900 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES32H8 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum
θ_{JC}	Thermal Resistance, Junction-to-Case	0.2	^{0}C/W	
P	Power Dissipation of the Device	6.81	Watts	Maximum

Table 16 Thermal Specifications for PES32H8, 31x31 mm FCBGA900 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 16. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 16), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 10 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 1 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 17 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 17 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

Package Pinout — 900-BGA Signal Pinout for PES32H8

The following table lists the pin numbers and signal names for the PES32H8 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B5	V_{SS}		C9	V_{SS}		D13	V_{SS}	
A2	V_{SS}		B6	V_{SS}		C10	V_{SS}		D14	PE3RP01	
A3	GPIO_19		B7	V_{SS}		C11	V_{SS}		D15	PE3RP00	
A4	$V_{DD}IO$		B8	V_{SS}		C12	V_{SS}		D16	V_{SS}	
A5	V_{SS}		B9	V_{SS}		C13	V_{SS}		D17	PE2RP03	
A6	V_{SS}		B10	V_{SS}		C14	V_{SS}		D18	PE2RP02	
A7	V_{SS}		B11	PE3TN03		C15	V_{SS}		D19	V_{SS}	
A8	V_{SS}		B12	PE3TN02		C16	V_{SS}		D20	PE2RP01	
A9	V_{SS}		B13	V_{SS}		C17	V_{SS}		D21	PE2RP00	
A10	V_{SS}		B14	PE3TN01		C18	V_{SS}		D22	V_{SS}	
A11	PE3TP03		B15	PE3TN00		C19	V_{SS}		D23	V_{SS}	
A12	PE3TP02		B16	V_{SS}		C20	V_{SS}		D24	V_{SS}	
A13	V_{SS}		B17	PE2TN03		C21	V_{SS}		D25	V_{SS}	
A14	PE3TP01		B18	PE2TN02		C22	V_{SS}		D26	JTAG_TMS	
A15	PE3TP00		B19	V_{SS}		C23	V_{SS}		D27	$V_{DD}IO$	
A16	V_{SS}		B20	PE2TN01		C24	V_{SS}		D28	SSMBADDR_5	
A17	PE2TP03		B21	PE2TN00		C25	V_{SS}		D29	SSMBADDR_3	
A18	PE2TP02		B22	V_{SS}		C26	MSMBADDR_4		D30	$V_{DD}IO$	
A19	V_{SS}		B23	V_{SS}		C27	JTAG_TDI		E1	$V_{DD}IO$	
A20	PE2TP01		B24	V_{SS}		C28	JTAG_TRST_N		E2	GPIO_30	
A21	PE2TP00		B25	V_{SS}		C29	SSMBADDR_2		E3	GPIO_31	1
A22	V_{SS}		B26	MSMBADDR_3		C30	SSMBADDR_1		E4	GPIO_24	1
A23	V_{SS}		B27	MSMBADDR_2		D1	GPIO_28	1	E5	V_{SS}	
A24	V_{SS}		B28	PERSTN		D2	GPIO_26	1	E6	V_{SS}	
A25	V_{SS}		B29	$V_{DD}IO$		D3	$V_{DD}IO$		E7	V_{SS}	
A26	$V_{DD}IO$		B30	V_{SS}		D4	GPIO_23	1	E8	V_{SS}	
A27	MSMBADDR_1		C1	GPIO_29		D5	V_{SS}		E9	PEREFCLKP1	
A28	MSMBSMODE		C2	GPIO_27	1	D6	V_{SS}		E10	V_{SS}	
A29	V_{SS}		C3	GPIO_21	1	D7	V_{SS}		E11	PE3RN03	
A30	V_{SS}		C4	GPIO_16		D8	V_{SS}		E12	PE3RN02	
B1	V_{SS}		C5	V_{SS}		D9	PEREFCLKN1		E13	V_{SS}	
B2	$V_{DD}IO$		C6	V_{SS}		D10	V_{SS}		E14	PE3RN01	
B3	GPIO_18		C7	V_{SS}		D11	PE3RP03		E15	PE3RN00	
B4	GPIO_17		C8	V_{SS}		D12	PE3RP02		E16	V_{SS}	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 1 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
E17	PE2RN03		F23	V_{SS}		G29	V_{SS}		J5	PEREFCLKN2	
E18	PE2RN02		F24	MSMBDAT		G30	V_{SS}		J6	V_{SS}	
E19	V_{SS}		F25	V_{DD}IO		H1	V_{SS}		J7	V_{SS}	
E20	PE2RN01		F26	SSMBCLK		H2	V_{SS}		J8	V_{SS}	
E21	PE2RN00		F27	V_{SS}		H3	V_{SS}		J9	V_{SS}	
E22	V_{SS}		F28	V_{SS}		H4	V_{SS}		J10	V_{SS}	
E23	V_{SS}		F29	V_{SS}		H5	V_{SS}		J11	V_{DD}PE	
E24	V_{SS}		F30	V_{SS}		H6	V_{SS}		J12	V_{DD}PE	
E25	MSMBCLK		G1	V_{SS}		H7	V_{DD}IO		J13	V_{DD}PE	
E26	V_{SS}		G2	V_{SS}		H8	GPIO_22	1	J14	V_{SS}	
E27	V_{SS}		G3	V_{SS}		H9	V_{SS}		J15	V_{DD}PE	
E28	V_{SS}		G4	V_{SS}		H10	V_{SS}		J16	V_{DD}PE	
E29	V_{SS}		G5	V_{SS}		H11	V_{TT}PE		J17	V_{SS}	
E30	V_{SS}		G6	V_{SS}		H12	V_{SS}		J18	V_{DD}PE	
F1	V_{SS}		G7	GPIO_25	1	H13	V_{DD}APE		J19	V_{DD}PE	
F2	V_{SS}		G8	V_{SS}		H14	V_{SS}		J20	V_{DD}PE	
F3	V_{SS}		G9	V_{SS}		H15	V_{TT}PE		J21	V_{SS}	
F4	V_{SS}		G10	V_{SS}		H16	V_{TT}PE		J22	V_{SS}	
F5	V_{SS}		G11	V_{SS}		H17	V_{SS}		J23	V_{SS}	
F6	GPIO_20		G12	V_{DD}PE		H18	V_{DD}APE		J24	V_{SS}	
F7	V_{DD}IO		G13	V_{SS}		H19	V_{SS}		J25	V_{SS}	
F8	V_{SS}		G14	V_{SS}		H20	V_{TT}PE		J26	V_{SS}	
F9	V_{SS}		G15	V_{TT}PE		H21	V_{SS}		J27	V_{SS}	
F10	V_{SS}		G16	V_{TT}PE		H22	V_{SS}		J28	V_{SS}	
F11	V_{SS}		G17	V_{SS}		H23	CCLKDS		J29	V_{SS}	
F12	V_{SS}		G18	V_{SS}		H24	JTAG_TCK		J30	V_{SS}	
F13	V_{SS}		G19	V_{DD}PE		H25	V_{SS}		K1	V_{SS}	
F14	V_{SS}		G20	V_{SS}		H26	V_{SS}		K2	V_{SS}	
F15	V_{SS}		G21	V_{SS}		H27	V_{SS}		K3	V_{SS}	
F16	V_{SS}		G22	V_{SS}		H28	V_{SS}		K4	V_{SS}	
F17	V_{SS}		G23	JTAG_TDO		H29	V_{SS}		K5	V_{SS}	
F18	V_{SS}		G24	V_{DD}IO		H30	V_{SS}		K6	V_{SS}	
F19	V_{SS}		G25	SSMBDAT		J1	V_{SS}		K7	V_{SS}	
F20	V_{SS}		G26	V_{SS}		J2	V_{SS}		K8	V_{SS}	
F21	V_{SS}		G27	V_{SS}		J3	V_{SS}		K9	V_{SS}	
F22	V_{SS}		G28	V_{SS}		J4	PEREFCLKP2		K10	V_{SS}	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 2 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
K11	V_{DD}PE		L17	V_{DD}CORE		M23	V_{SS}		N29	PE1TN01	
K12	V_{SS}		L18	V_{DD}CORE		M24	V_{DD}PE		N30	PE1TP01	
K13	V_{DD}PE		L19	V_{DD}CORE		M25	V_{SS}		P1	PE4TP02	
K14	V_{SS}		L20	V_{DD}CORE		M26	V_{SS}		P2	PE4TN02	
K15	V_{DD}PE		L21	V_{DD}PE		M27	V_{SS}		P3	V_{SS}	
K16	V_{DD}PE		L22	V_{DD}PE		M28	V_{SS}		P4	PE4RP02	
K17	V_{SS}		L23	V_{TT}PE		M29	V_{SS}		P5	PE4RN02	
K18	V_{DD}PE		L24	V_{SS}		M30	V_{SS}		P6	V_{SS}	
K19	V_{SS}		L25	V_{SS}		N1	V_{SS}		P7	V_{SS}	
K20	V_{DD}PE		L26	PE1RN02		N2	V_{SS}		P8	V_{SS}	
K21	V_{SS}		L27	PE1RP02		N3	V_{SS}		P9	V_{SS}	
K22	V_{SS}		L28	V_{SS}		N4	V_{SS}		P10	V_{SS}	
K23	V_{SS}		L29	PE1TN02		N5	V_{SS}		P11	V_{SS}	
K24	V_{SS}		L30	PE1TP02		N6	V_{SS}		P12	V_{SS}	
K25	V_{SS}		M1	PE4TP01		N7	V_{SS}		P13	V_{DD}CORE	
K26	PE1RN03		M2	PE4TN01		N8	V_{DD}APE		P14	V_{SS}	
K27	PE1RP03		M3	V_{SS}		N9	V_{DD}PE		P15	V_{DD}CORE	
K28	V_{SS}		M4	PE4RP01		N10	V_{DD}PE		P16	V_{SS}	
K29	PE1TN03		M5	PE4RN01		N11	V_{DD}CORE		P17	V_{DD}CORE	
K30	PE1TP03		M6	V_{SS}		N12	V_{DD}CORE		P18	V_{SS}	
L1	PE4TP00		M7	V_{DD}PE		N13	V_{SS}		P19	V_{DD}CORE	
L2	PE4TN00		M8	V_{SS}		N14	V_{DD}CORE		P20	V_{DD}CORE	
L3	V_{SS}		M9	V_{DD}PE		N15	V_{SS}		P21	V_{SS}	
L4	PE4RP00		M10	V_{SS}		N16	V_{DD}CORE		P22	V_{SS}	
L5	PE4RN00		M11	V_{DD}CORE		N17	V_{SS}		P23	V_{SS}	
L6	V_{SS}		M12	V_{SS}		N18	V_{DD}CORE		P24	V_{SS}	
L7	V_{SS}		M13	V_{DD}CORE		N19	V_{SS}		P25	V_{SS}	
L8	V_{TT}PE		M14	V_{SS}		N20	V_{DD}CORE		P26	PE1RN00	
L9	V_{DD}PE		M15	V_{DD}CORE		N21	V_{DD}PE		P27	PE1RP00	
L10	V_{DD}PE		M16	V_{SS}		N22	V_{DD}PE		P28	V_{SS}	
L11	V_{DD}CORE		M17	V_{DD}CORE		N23	V_{DD}APE		P29	PE1TN00	
L12	V_{DD}CORE		M18	V_{SS}		N24	V_{SS}		P30	PE1TP00	
L13	V_{DD}CORE		M19	V_{DD}CORE		N25	V_{SS}		R1	PE4TP03	
L14	V_{SS}		M20	V_{DD}CORE		N26	PE1RN01		R2	PE4TN03	
L15	V_{DD}CORE		M21	V_{SS}		N27	PE1RP01		R3	V_{SS}	
L16	V_{SS}		M22	V_{DD}PE		N28	V_{SS}		R4	PE4RP03	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 3 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
R5	PE4RN03		T11	V_{SS}		U17	V_{SS}		V23	V_{DD}APE	
R6	V_{SS}		T12	V_{SS}		U18	V_{DD}CORE		V24	V_{SS}	
R7	V_{TT}PE		T13	V_{DD}CORE		U19	V_{SS}		V25	V_{SS}	
R8	V_{TT}PE		T14	V_{SS}		U20	V_{SS}		V26	V_{SS}	
R9	V_{DD}PE		T15	V_{DD}CORE		U21	V_{SS}		V27	V_{SS}	
R10	V_{DD}PE		T16	V_{SS}		U22	V_{SS}		V28	V_{SS}	
R11	V_{DD}CORE		T17	V_{DD}CORE		U23	V_{SS}		V29	V_{SS}	
R12	V_{DD}CORE		T18	V_{SS}		U24	V_{SS}		V30	V_{SS}	
R13	V_{SS}		T19	V_{DD}CORE		U25	V_{SS}		W1	V_{SS}	
R14	V_{DD}CORE		T20	V_{DD}CORE		U26	PE0RN02		W2	V_{SS}	
R15	V_{SS}		T21	V_{DD}PE		U27	PE0RP02		W3	V_{SS}	
R16	V_{DD}CORE		T22	V_{DD}PE		U28	V_{SS}		W4	V_{SS}	
R17	V_{SS}		T23	V_{TT}PE		U29	PE0TN02		W5	V_{SS}	
R18	V_{DD}CORE		T24	V_{TT}PE		U30	PE0TP02		W6	V_{SS}	
R19	V_{SS}		T25	V_{SS}		V1	PE5TP01		W7	V_{DD}PE	
R20	V_{SS}		T26	PE0RN03		V2	PE5TN01		W8	V_{SS}	
R21	V_{DD}PE		T27	PE0RP03		V3	V_{SS}		W9	V_{DD}PE	
R22	V_{DD}PE		T28	V_{SS}		V4	PE5RP01		W10	V_{SS}	
R23	V_{TT}PE		T29	PE0TN03		V5	PE5RN01		W11	V_{DD}CORE	
R24	V_{TT}PE		T30	PE0TP03		V6	V_{SS}		W12	V_{DD}CORE	
R25	V_{SS}		U1	PE5TP00		V7	V_{SS}		W13	V_{SS}	
R26	V_{SS}		U2	PE5TN00		V8	V_{DD}APE		W14	V_{DD}CORE	
R27	V_{SS}		U3	V_{SS}		V9	V_{DD}PE		W15	V_{SS}	
R28	V_{SS}		U4	PE5RP00		V10	V_{DD}PE		W16	V_{DD}CORE	
R29	V_{SS}		U5	PE5RN00		V11	V_{DD}CORE		W17	V_{SS}	
R30	V_{SS}		U6	V_{SS}		V12	V_{SS}		W18	V_{DD}CORE	
T1	V_{SS}		U7	V_{SS}		V13	V_{DD}CORE		W19	V_{SS}	
T2	V_{SS}		U8	V_{SS}		V14	V_{SS}		W20	V_{DD}CORE	
T3	V_{SS}		U9	V_{SS}		V15	V_{DD}CORE		W21	V_{SS}	
T4	V_{SS}		U10	V_{SS}		V16	V_{SS}		W22	V_{DD}PE	
T5	V_{SS}		U11	V_{DD}CORE		V17	V_{DD}CORE		W23	V_{SS}	
T6	V_{SS}		U12	V_{DD}CORE		V18	V_{SS}		W24	V_{DD}PE	
T7	V_{TT}PE		U13	V_{SS}		V19	V_{DD}CORE		W25	V_{SS}	
T8	V_{TT}PE		U14	V_{DD}CORE		V20	V_{DD}CORE		W26	PE0RN01	
T9	V_{DD}PE		U15	V_{SS}		V21	V_{DD}PE		W27	PE0RP01	
T10	V_{DD}PE		U16	V_{DD}CORE		V22	V_{DD}PE		W28	V_{SS}	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 4 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
W29	PE0TN01		AA5	PE5RN03		AB11	V_{DD}PE		AC17	V_{SS}	
W30	PE0TP01		AA6	V_{SS}		AB12	V_{DD}PE		AC18	V_{DD}APE	
Y1	PE5TP02		AA7	V_{SS}		AB13	V_{DD}PE		AC19	V_{SS}	
Y2	PE5TN02		AA8	V_{SS}		AB14	V_{SS}		AC20	V_{TT}PE	
Y3	V_{SS}		AA9	V_{SS}		AB15	V_{DD}PE		AC21	V_{SS}	
Y4	PE5RP02		AA10	V_{SS}		AB16	V_{DD}PE		AC22	V_{SS}	
Y5	PE5RN02		AA11	V_{DD}PE		AB17	V_{SS}		AC23	GPIO_06	1
Y6	V_{SS}		AA12	V_{SS}		AB18	V_{DD}PE		AC24	V_{DD}IO	
Y7	V_{SS}		AA13	V_{DD}PE		AB19	V_{DD}PE		AC25	V_{SS}	
Y8	V_{TT}PE		AA14	V_{SS}		AB20	V_{DD}PE		AC26	V_{SS}	
Y9	V_{DD}PE		AA15	V_{DD}PE		AB21	V_{SS}		AC27	V_{SS}	
Y10	V_{DD}PE		AA16	V_{DD}PE		AB22	V_{SS}		AC28	V_{SS}	
Y11	V_{DD}CORE		AA17	V_{SS}		AB23	V_{SS}		AC29	V_{SS}	
Y12	V_{DD}CORE		AA18	V_{DD}PE		AB24	V_{SS}		AC30	V_{SS}	
Y13	V_{DD}CORE		AA19	V_{SS}		AB25	V_{SS}		AD1	V_{SS}	
Y14	V_{DD}CORE		AA20	V_{DD}PE		AB26	PEREFCLKN0		AD2	V_{SS}	
Y15	V_{SS}		AA21	V_{SS}		AB27	PEREFCLKP0		AD3	V_{SS}	
Y16	V_{DD}CORE		AA22	V_{SS}		AB28	V_{SS}		AD4	V_{SS}	
Y17	V_{SS}		AA23	V_{SS}		AB29	V_{SS}		AD5	V_{SS}	
Y18	V_{DD}CORE		AA24	V_{SS}		AB30	V_{SS}		AD6	V_{SS}	
Y19	V_{DD}CORE		AA25	V_{SS}		AC1	V_{SS}		AD7	V_{DD}IO	
Y20	V_{DD}CORE		AA26	V_{SS}		AC2	V_{SS}		AD8	V_{DD}IO	
Y21	V_{DD}PE		AA27	V_{SS}		AC3	V_{SS}		AD9	V_{SS}	
Y22	V_{DD}PE		AA28	V_{SS}		AC4	V_{SS}		AD10	V_{SS}	
Y23	V_{TT}PE		AA29	V_{SS}		AC5	V_{SS}		AD11	V_{SS}	
Y24	V_{SS}		AA30	V_{SS}		AC6	V_{SS}		AD12	V_{DD}PE	
Y25	V_{SS}		AB1	V_{SS}		AC7	V_{DD}IO		AD13	V_{SS}	
Y26	PE0RN00		AB2	V_{SS}		AC8	V_{DD}IO		AD14	V_{SS}	
Y27	PE0RP00		AB3	V_{SS}		AC9	V_{SS}		AD15	V_{TT}PE	
Y28	V_{SS}		AB4	V_{SS}		AC10	V_{SS}		AD16	V_{TT}PE	
Y29	PE0TN00		AB5	V_{SS}		AC11	V_{TT}PE		AD17	V_{SS}	
Y30	PE0TP00		AB6	V_{SS}		AC12	V_{SS}		AD18	V_{SS}	
AA1	PE5TP03		AB7	V_{SS}		AC13	V_{DD}APE		AD19	V_{DD}PE	
AA2	PE5TN03		AB8	V_{SS}		AC14	V_{SS}		AD20	V_{SS}	
AA3	V_{SS}		AB9	V_{SS}		AC15	V_{TT}PE		AD21	V_{SS}	
AA4	PE5RP03		AB10	V_{SS}		AC16	V_{TT}PE		AD22	V_{SS}	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 5 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AD23	V_{SS}		AE29	V_{SS}		AG5	V_{SS}		AH11	V_{SS}	
AD24	GPIO_09	1	AE30	V_{SS}		AG6	V_{SS}		AH12	V_{SS}	
AD25	V_{SS}		AF1	V_{SS}		AG7	V_{SS}		AH13	V_{SS}	
AD26	V_{SS}		AF2	V_{SS}		AG8	V_{SS}		AH14	V_{SS}	
AD27	V_{SS}		AF3	V_{SS}		AG9	V_{SS}		AH15	V_{SS}	
AD28	V_{SS}		AF4	V_{SS}		AG10	PE6RP00		AH16	V_{SS}	
AD29	V_{SS}		AF5	V_{SS}		AG11	PE6RP01		AH17	V_{SS}	
AD30	V_{SS}		AF6	REFCLKM		AG12	V_{SS}		AH18	V_{SS}	
AE1	V_{SS}		AF7	V_{SS}		AG13	PE6RP02		AH19	V_{SS}	
AE2	V_{SS}		AF8	V_{SS}		AG14	PE6RP03		AH20	V_{SS}	
AE3	V_{SS}		AF9	V_{SS}		AG15	V_{SS}		AH21	V_{SS}	
AE4	V_{SS}		AF10	PE6RN00		AG16	PE7RP00		AH22	V_{SS}	
AE5	CCLKUS		AF11	PE6RN01		AG17	PE7RP01		AH23	V_{SS}	
AE6	V_{DD}IO		AF12	V_{SS}		AG18	V_{SS}		AH24	V_{SS}	
AE7	V_{SS}		AF13	PE6RN02		AG19	PE7RP02		AH25	V_{SS}	
AE8	V_{SS}		AF14	PE6RN03		AG20	PE7RP03		AH26	V_{SS}	
AE9	V_{SS}		AF15	V_{SS}		AG21	V_{SS}		AH27	GPIO_00	
AE10	V_{SS}		AF16	PE7RN00		AG22	PEREFCLKN3		AH28	GPIO_05	1
AE11	V_{SS}		AF17	PE7RN01		AG23	V_{SS}		AH29	GPIO_11	1
AE12	V_{SS}		AF18	V_{SS}		AG24	V_{SS}		AH30	GPIO_13	
AE13	V_{SS}		AF19	PE7RN02		AG25	V_{SS}		AJ1	V_{SS}	
AE14	V_{SS}		AF20	PE7RN03		AG26	V_{SS}		AJ2	V_{DD}IO	
AE15	V_{SS}		AF21	V_{SS}		AG27	GPIO_07	1	AJ3	V_{SS}	
AE16	V_{SS}		AF22	PEREFCLKP3		AG28	V_{DD}IO		AJ4	SWMODE_0	
AE17	V_{SS}		AF23	V_{SS}		AG29	GPIO_10	1	AJ5	SWMODE_2	
AE18	V_{SS}		AF24	V_{SS}		AG30	GPIO_12	1	AJ6	V_{SS}	
AE19	V_{SS}		AF25	V_{SS}		AH1	P23MERGEN		AJ7	V_{SS}	
AE20	V_{SS}		AF26	V_{SS}		AH2	P67MERGEN		AJ8	V_{SS}	
AE21	V_{SS}		AF27	GPIO_08	1	AH3	V_{SS}		AJ9	V_{SS}	
AE22	V_{SS}		AF28	GPIO_15		AH4	V_{SS}		AJ10	PE6TN00	
AE23	V_{SS}		AF29	GPIO_14		AH5	SWMODE_3		AJ11	PE6TN01	
AE24	V_{DD}IO		AF30	V_{DD}IO		AH6	V_{SS}		AJ12	V_{SS}	
AE25	GPIO_04		AG1	V_{DD}IO		AH7	V_{SS}		AJ13	PE6TN02	
AE26	V_{SS}		AG2	P01MERGEN		AH8	V_{SS}		AJ14	PE6TN03	
AE27	V_{SS}		AG3	P45MERGEN		AH9	V_{SS}		AJ15	V_{SS}	
AE28	V_{SS}		AG4	V_{DD}IO		AH10	V_{SS}		AJ16	PE7TN00	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 6 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AJ17	PE7TN01		AJ28	GPIO_02		AK9	V_{SS}		AK20	PE7TP03	
AJ18	V_{SS}		AJ29	$V_{DD}IO$		AK10	PE6TP00		AK21	V_{SS}	
AJ19	PE7TN02		AJ30	V_{SS}		AK11	PE6TP01		AK22	V_{SS}	
AJ20	PE7TN03		AK1	V_{SS}		AK12	V_{SS}		AK23	V_{SS}	
AJ21	V_{SS}		AK2	V_{SS}		AK13	PE6TP02		AK24	V_{SS}	
AJ22	V_{SS}		AK3	RSTHALT		AK14	PE6TP03		AK25	V_{SS}	
AJ23	V_{SS}		AK4	SWMODE_1		AK15	V_{SS}		AK26	V_{SS}	
AJ24	V_{SS}		AK5	$V_{DD}IO$		AK16	PE7TP00		AK27	$V_{DD}IO$	
AJ25	V_{SS}		AK6	V_{SS}		AK17	PE7TP01		AK28	GPIO_03	
AJ26	V_{SS}		AK7	V_{SS}		AK18	V_{SS}		AK29	V_{SS}	
AJ27	GPIO_01		AK8	V_{SS}		AK19	PE7TP02		AK30	V_{SS}	

Table 18 PES32H8 900-pin Signal Pin-Out (Part 7 of 7)

Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
AH28	GPIO_05	GPEN	H8	GPIO_22	IOEXPINTN1
AC23	GPIO_06	P1RSTN	D4	GPIO_23	IOEXPINTN2
AG27	GPIO_07	P2RSTN	E4	GPIO_24	IOEXPINTN3
AF27	GPIO_08	P3RSTN	G7	GPIO_25	IOEXPINTN4
AD24	GPIO_09	P4RSTN	D2	GPIO_26	IOEXPINTN5
AG29	GPIO_10	P5RSTN	C2	GPIO_27	IOEXPINTN6
AH29	GPIO_11	P6RSTN	D1	GPIO_28	IOEXPINTN7
AG30	GPIO_12	P7RSTN	E3	GPIO_31	IOEXPINTN10
C3	GPIO_21	IOEXPINTN0			

Table 19 PES32H8 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}PE	V_{DD}APE	V_{TT}PE
L11	T17	A4	G12	T9	H13	G15
L12	T19	A26	G19	T10	H18	G16
L13	T20	B2	J11	T21	N8	H11
L15	U11	B29	J12	T22	N23	H15
L17	U12	D3	J13	V9	V8	H16
L18	U14	D27	J15	V10	V23	H20
L19	U16	D30	J16	V21	AC13	L8
L20	U18	E1	J18	V22	AC18	L23
M11	V11	F7	J19	W7		R7
M13	V13	F25	J20	W9		R8
M15	V15	G24	K11	W22		R23
M17	V17	H7	K13	W24		R24
M19	V19	AC7	K15	Y9		T7
M20	V20	AC8	K16	Y10		T8
N11	W11	AC24	K18	Y21		T23
N12	W12	AD7	K20	Y22		T24
N14	W14	AD8	L9	AA11		Y8
N16	W16	AE6	L10	AA13		Y23
N18	W18	AE24	L21	AA15		AC11
N20	W20	AF30	L22	AA16		AC15
P13	Y11	AG1	M7	AA18		AC16
P15	Y12	AG4	M9	AA20		AC20
P17	Y13	AG28	M22	AB11		AD15
P19	Y14	AJ2	M24	AB12		AD16
P20	Y16	AJ29	N9	AB13		
R11	Y18	AK5	N10	AB15		
R12	Y19	AK27	N21	AB16		
R14	Y20		N22	AB18		
R16			R9	AB19		
R18			R10	AB20		
T13			R21	AD12		
T15			R22	AD19		

Table 20 PES32H8 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C8	E13	F30	H21	K8	M29	R13
A2	C9	E16	G1	H22	K9	M30	R15
A5	C10	E19	G2	H25	K10	N1	R17
A6	C11	E22	G3	H26	K12	N2	R19
A7	C12	E23	G4	H27	K14	N3	R20
A8	C13	E24	G5	H28	K17	N4	R25
A9	C14	E26	G6	H29	K19	N5	R26
A10	C15	E27	G8	H30	K21	N6	R27
A13	C16	E28	G9	J1	K22	N7	R28
A16	C17	E29	G10	J2	K23	N13	R29
A19	C18	E30	G11	J3	K24	N15	R30
A22	C19	F1	G13	J6	K25	N17	T1
A23	C20	F2	G14	J7	K28	N19	T2
A24	C21	F3	G17	J8	L3	N24	T3
A25	C22	F4	G18	J9	L6	N25	T4
A29	C23	F5	G20	J10	L7	N28	T5
A30	C24	F8	G21	J14	L14	P3	T6
B1	C25	F9	G22	J17	L16	P6	T11
B5	D5	F10	G26	J21	L24	P7	T12
B6	D6	F11	G27	J22	L25	P8	T14
B7	D7	F12	G28	J23	L28	P9	T16
B8	D8	F13	G29	J24	M3	P10	T18
B9	D10	F14	G30	J25	M6	P11	T25
B10	D13	F15	H1	J26	M8	P12	T28
B13	D16	F16	H2	J27	M10	P14	U3
B16	D19	F17	H3	J28	M12	P16	U6
B19	D22	F18	H4	J29	M14	P18	U7
B22	D23	F19	H5	J30	M16	P21	U8
B23	D24	F20	H6	K1	M18	P22	U9
B24	D25	F21	H9	K2	M21	P23	U10
B25	E5	F22	H10	K3	M23	P24	U13
B30	E6	F23	H12	K4	M25	P25	U15
C5	E7	F27	H14	K5	M26	P28	U17
C6	E8	F28	H17	K6	M27	R3	U19
C7	E10	F29	H19	K7	M28	R6	U20

Table 21 PES32H8 Ground Pins (Part 1 of 2)

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U21	W17	AA27	AC9	AD23	AE28	AG25	AJ9
U22	W19	AA28	AC10	AD25	AE29	AG26	AJ12
U23	W21	AA29	AC12	AD26	AE30	AH3	AJ15
U24	W23	AA30	AC14	AD27	AF1	AH4	AJ18
U25	W25	AB1	AC17	AD28	AF2	AH6	AJ21
U28	W28	AB2	AC19	AD29	AF3	AH7	AJ22
V3	Y3	AB3	AC21	AD30	AF4	AH8	AJ23
V6	Y6	AB4	AC22	AE1	AF5	AH9	AJ24
V7	Y7	AB5	AC25	AE2	AF7	AH10	AJ25
V12	Y15	AB6	AC26	AE3	AF8	AH11	AJ26
V14	Y17	AB7	AC27	AE4	AF9	AH12	AJ30
V16	Y24	AB8	AC28	AE7	AF12	AH13	AK1
V18	Y25	AB9	AC29	AE8	AF15	AH14	AK2
V24	Y28	AB10	AC30	AE9	AF18	AH15	AK6
V25	AA3	AB14	AD1	AE10	AF21	AH16	AK7
V26	AA6	AB17	AD2	AE11	AF23	AH17	AK8
V27	AA7	AB21	AD3	AE12	AF24	AH18	AK9
V28	AA8	AB22	AD4	AE13	AF25	AH19	AK12
V29	AA9	AB23	AD5	AE14	AF26	AH20	AK15
V30	AA10	AB24	AD6	AE15	AG5	AH21	AK18
W1	AA12	AB25	AD9	AE16	AG6	AH22	AK21
W2	AA14	AB28	AD10	AE17	AG7	AH23	AK22
W3	AA17	AB29	AD11	AE18	AG8	AH24	AK23
W4	AA19	AB30	AD13	AE19	AG9	AH25	AK24
W5	AA21	AC1	AD14	AE20	AG12	AH26	AK25
W6	AA22	AC2	AD17	AE21	AG15	AJ1	AK26
W8	AA23	AC3	AD18	AE22	AG18	AJ3	AK29
W10	AA24	AC4	AD20	AE23	AG21	AJ6	AK30
W13	AA25	AC5	AD21	AE26	AG23	AJ7	
W15	AA26	AC6	AD22	AE27	AG24	AJ8	

Table 21 PES32H8 Ground Pins (Part 2 of 2)

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	H23	System
CCLKUS	I	AE5	
GPIO_00	I/O	AH27	General Purpose I/O
GPIO_01	I/O	AJ27	
GPIO_02	I/O	AJ28	
GPIO_03	I/O	AK28	
GPIO_04	I/O	AE25	
GPIO_05	I/O	AH28	
GPIO_06	I/O	AC23	
GPIO_07	I/O	AG27	
GPIO_08	I/O	AF27	
GPIO_09	I/O	AD24	
GPIO_10	I/O	AG29	
GPIO_11	I/O	AH29	
GPIO_12	I/O	AG30	
GPIO_13	I/O	AH30	
GPIO_14	I/O	AF29	
GPIO_15	I/O	AF28	
GPIO_16	I/O	C4	
GPIO_17	I/O	B4	
GPIO_18	I/O	B3	
GPIO_19	I/O	A3	
GPIO_20	I/O	F6	
GPIO_21	I/O	C3	General Purpose I/O (cont.)
GPIO_22	I/O	H8	
GPIO_23	I/O	D4	
GPIO_24	I/O	E4	
GPIO_25	I/O	G7	
GPIO_26	I/O	D2	
GPIO_27	I/O	C2	
GPIO_28	I/O	D1	
GPIO_29	I/O	C1	
GPIO_30	I/O	E2	
GPIO_31	I/O	E3	

Table 22 89PES32H8 Alphabetical Signal List (Part 1 of 6)

Signal Name	I/O Type	Location	Signal Category
JTAG_TCK	I	H24	Test
JTAG_TDI	I	C27	
JTAG_TDO	O	G23	
JTAG_TMS	I	D26	
JTAG_TRST_N	I	C28	
MSMBADDR_1	I	A27	SMBus Interface
MSMBADDR_2	I	B27	
MSMBADDR_3	I	B26	
MSMBADDR_4	I	C26	
MSMBCLK	I/O	E25	
MSMBDAT	I/O	F24	
MSMBSMODE	I	A28	System
P01MERGEN	I	AG2	
P23MERGEN	I	AH1	
P45MERGEN	I	AG3	
P67MERGEN	I	AH2	
PE0RN00	I	Y26	PCI Express
PE0RN01	I	W26	
PE0RN02	I	U26	
PE0RN03	I	T26	
PE0RP00	I	Y27	
PE0RP01	I	W27	
PE0RP02	I	U27	
PE0RP03	I	T27	
PE0TN00	O	Y29	
PE0TN01	O	W29	
PE0TN02	O	U29	
PE0TN03	O	T29	
PE0TP00	O	Y30	
PE0TP01	O	W30	
PE0TP02	O	U30	
PE0TP03	O	T30	
PE1RN00	I	P26	
PE1RN01	I	N26	
PE1RN02	I	L26	

Table 22 89PES32H8 Alphabetical Signal List (Part 2 of 6)

Signal Name	I/O Type	Location	Signal Category
PE1RN03	I	K26	PCI Express (cont.)
PE1RP00	I	P27	
PE1RP01	I	N27	
PE1RP02	I	L27	
PE1RP03	I	K27	
PE1TN00	O	P29	
PE1TN01	O	N29	
PE1TN02	O	L29	
PE1TN03	O	K29	
PE1TP00	O	P30	
PE1TP01	O	N30	
PE1TP02	O	L30	
PE1TP03	O	K30	
PE2RN00	I	E21	
PE2RN01	I	E20	
PE2RN02	I	E18	
PE2RN03	I	E17	
PE2RP00	I	D21	
PE2RP01	I	D20	
PE2RP02	I	D18	
PE2RP03	I	D17	
PE2TN00	O	B21	
PE2TN01	O	B20	
PE2TN02	O	B18	
PE2TN03	O	B17	
PE2TP00	O	A21	
PE2TP01	O	A20	
PE2TP02	O	A18	
PE2TP03	O	A17	
PE3RN00	I	E15	
PE3RN01	I	E14	
PE3RN02	I	E12	
PE3RN03	I	E11	
PE3RP00	I	D15	
PE3RP01	I	D14	
PE3RP02	I	D12	

Table 22 89PES32H8 Alphabetical Signal List (Part 3 of 6)

Signal Name	I/O Type	Location	Signal Category
PE3RP03	I	D11	PCI Express (cont.)
PE3TN00	O	B15	
PE3TN01	O	B14	
PE3TN02	O	B12	
PE3TN03	O	B11	
PE3TP00	O	A15	
PE3TP01	O	A14	
PE3TP02	O	A12	
PE3TP03	O	A11	
PE4RN00	I	L5	
PE4RN01	I	M5	
PE4RN02	I	P5	
PE4RN03	I	R5	
PE4RP00	I	L4	
PE4RP01	I	M4	
PE4RP02	I	P4	
PE4RP03	I	R4	
PE4TN00	O	L2	
PE4TN01	O	M2	
PE4TN02	O	P2	
PE4TN03	O	R2	
PE4TP00	O	L1	
PE4TP01	O	M1	
PE4TP02	O	P1	
PE4TP03	O	R1	
PE5RN00	I	U5	
PE5RN01	I	V5	
PE5RN02	I	Y5	
PE5RN03	I	AA5	
PE5RP00	I	U4	
PE5RP01	I	V4	
PE5RP02	I	Y4	
PE5RP03	I	AA4	
PE5TN00	O	U2	
PE5TN01	O	V2	
PE5TN02	O	Y2	

Table 22 89PES32H8 Alphabetical Signal List (Part 4 of 6)

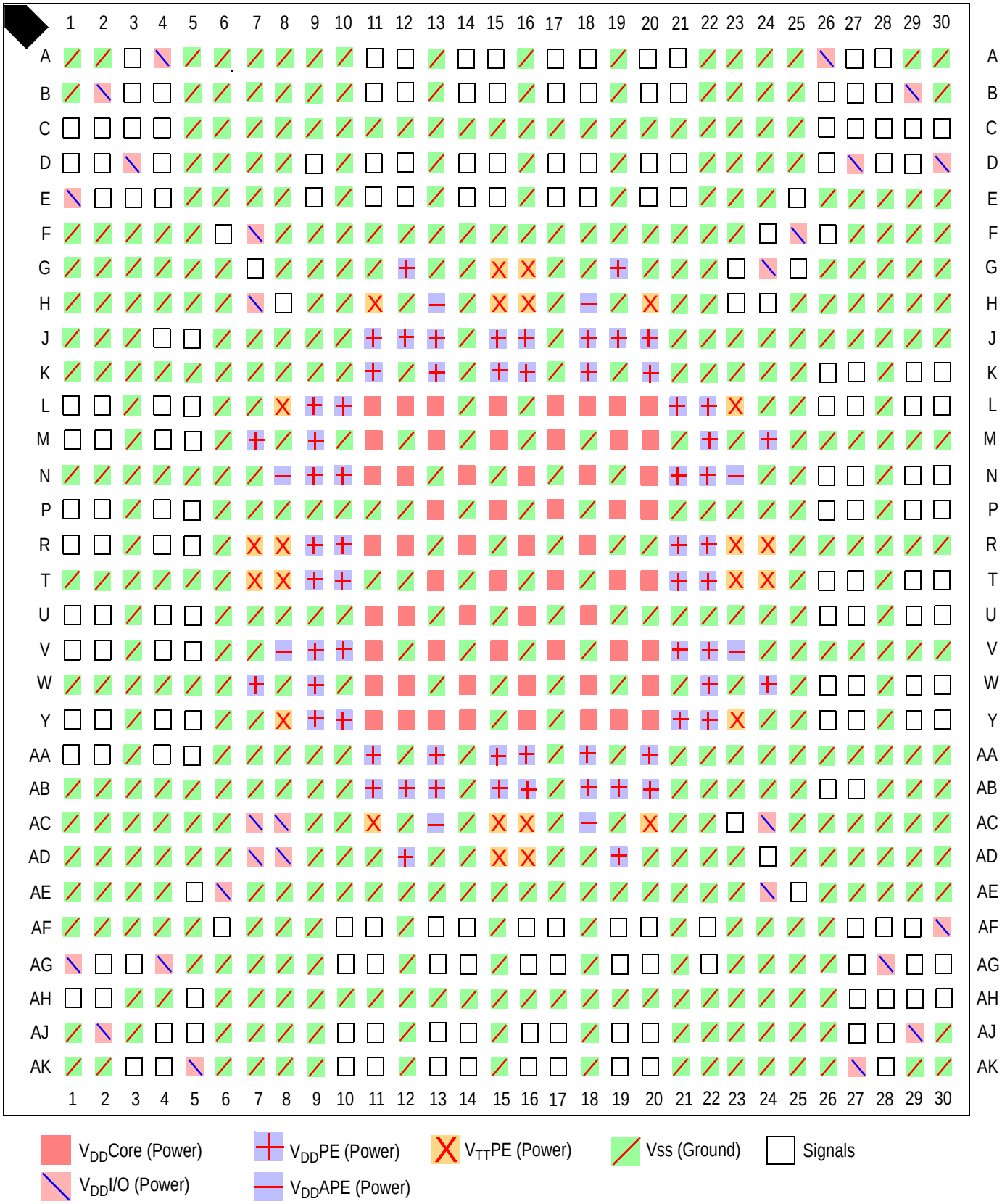
Signal Name	I/O Type	Location	Signal Category
PE5TN03	O	AA2	PCI Express (cont.)
PE5TP00	O	U1	
PE5TP01	O	V1	
PE5TP02	O	Y1	
PE5TP03	O	AA1	
PE6RN00	I	AF10	
PE6RN01	I	AF11	
PE6RN02	I	AF13	
PE6RN03	I	AF14	
PE6RP00	I	AG10	
PE6RP01	I	AG11	
PE6RP02	I	AG13	
PE6RP03	I	AG14	
PE6TN00	O	AJ10	
PE6TN01	O	AJ11	
PE6TN02	O	AJ13	
PE6TN03	O	AJ14	
PE6TP00	O	AK10	
PE6TP01	O	AK11	
PE6TP02	O	AK13	
PE6TP03	O	AK14	
PE7RN00	I	AF16	
PE7RN01	I	AF17	
PE7RN02	I	AF19	
PE7RN03	I	AF20	
PE7RP00	I	AG16	
PE7RP01	I	AG17	
PE7RP02	I	AG19	
PE7RP03	I	AG20	
PE7TN00	O	AJ16	
PE7TN01	O	AJ17	
PE7TN02	O	AJ19	
PE7TN03	O	AJ20	
PE7TP00	O	AK16	
PE7TP01	O	AK17	
PE7TP02	O	AK19	

Table 22 89PES32H8 Alphabetical Signal List (Part 5 of 6)

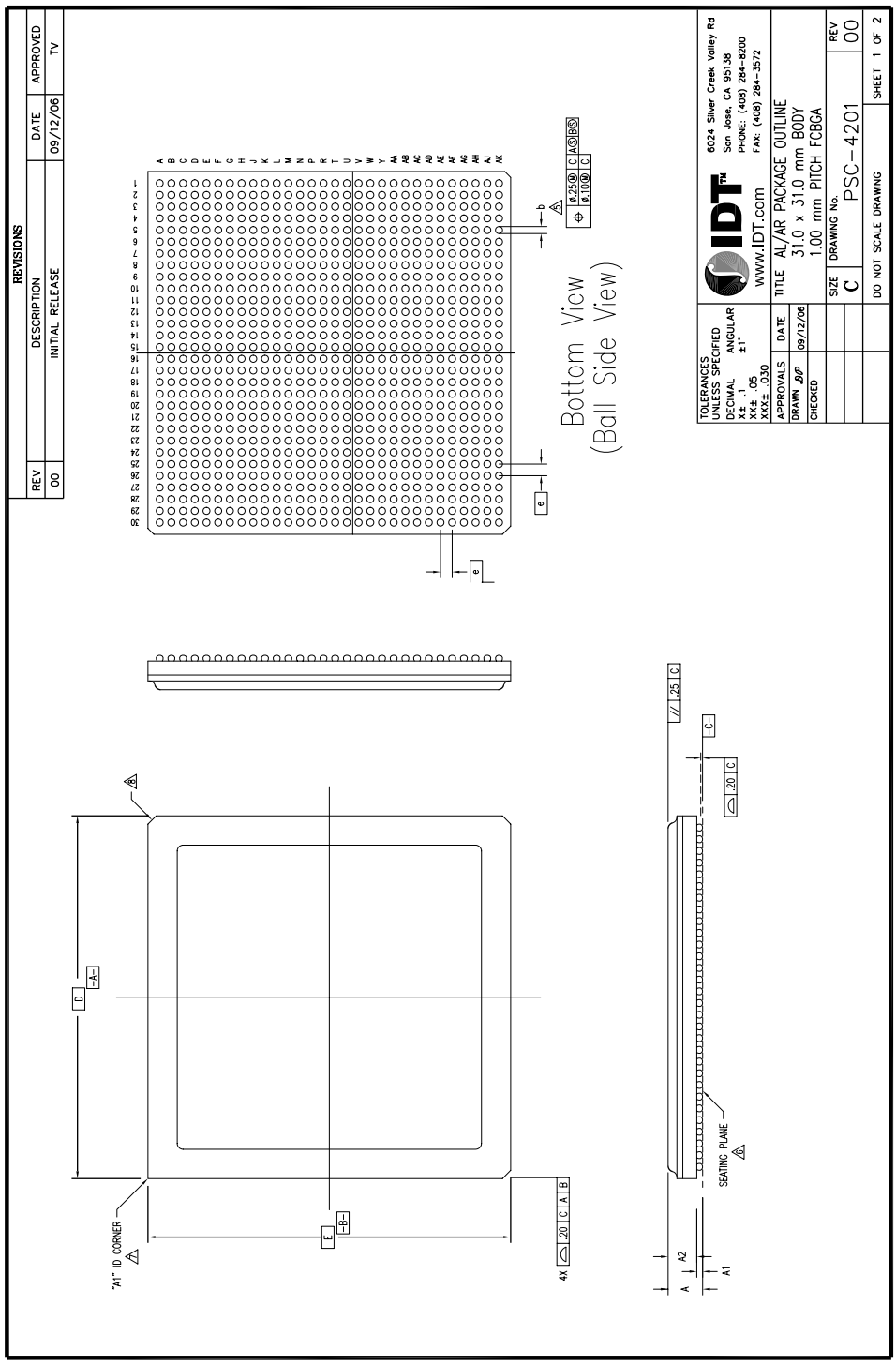
Signal Name	I/O Type	Location	Signal Category
PE7TP03	O	AK20	PCI Express (cont.)
PEREFCLKN0	I	AB26	
PEREFCLKN1	I	D9	
PEREFCLKN2	I	J5	
PEREFCLKN3	I	AG22	
PEREFCLKP0	I	AB27	
PEREFCLKP1	I	E9	
PEREFCLKP2	I	J4	
PEREFCLKP3	I	AF22	
PERSTN	I	B28	System
REFCLKM	I	AF6	PCI Express
RSTHALT	I	AK3	System
SSMBADDR_1	I	C30	SMBus Interface
SSMBADDR_2	I	C29	
SSMBADDR_3	I	D29	
SSMBADDR_5	I	D28	
SSMBCLK	I/O	F26	
SSMBDAT	I/O	G25	
SWMODE_0	I	AJ4	System
SWMODE_1	I	AK4	
SWMODE_2	I	AJ5	
SWMODE_3	I	AH5	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 20 for a listing of power pins.		
V_{SS}	See Table 21 for a listing of ground pins.		

Table 22 89PES32H8 Alphabetical Signal List (Part 6 of 6)

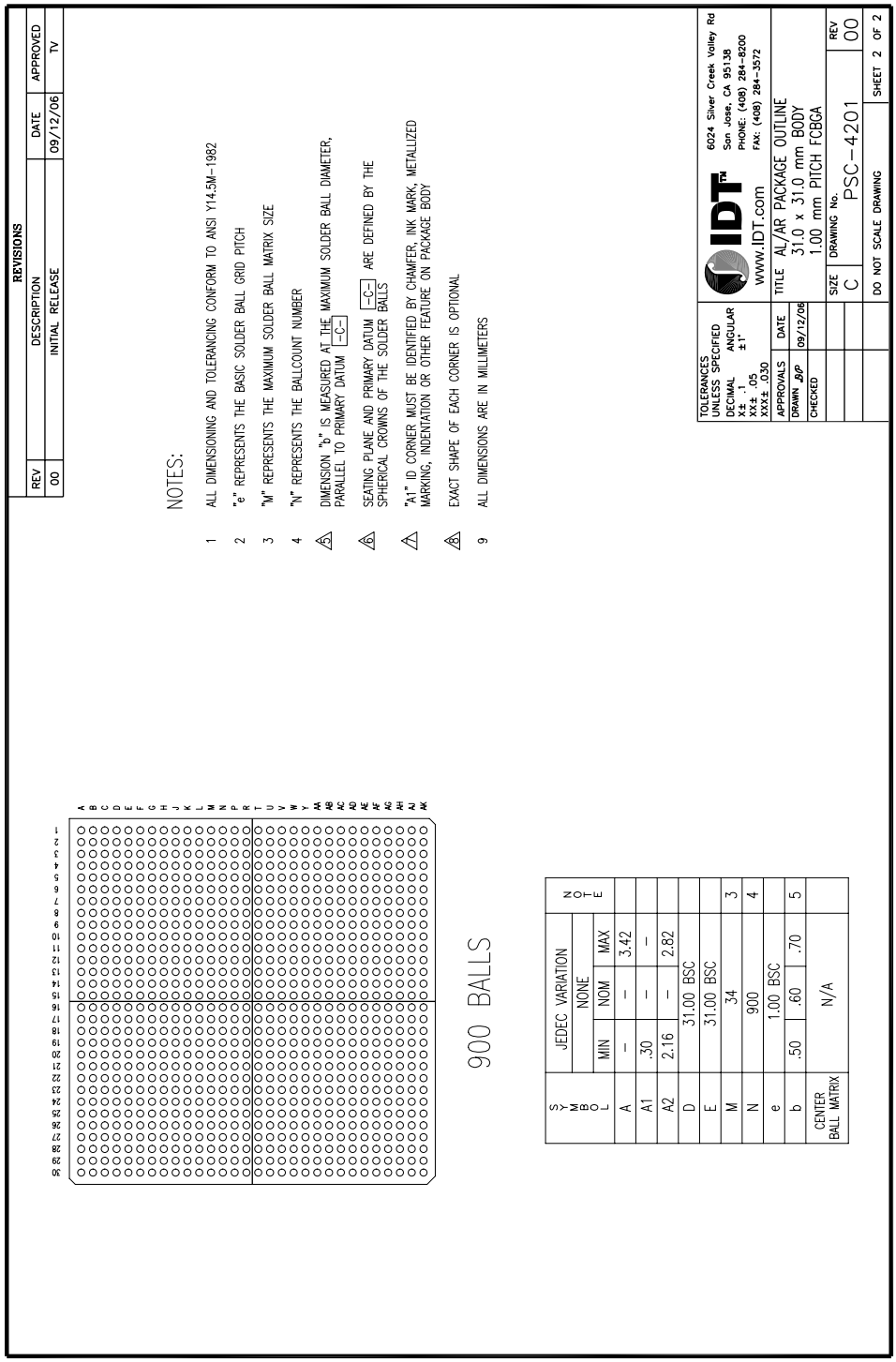
PES32H8 Pinout — Top View



PES32H8 Package Drawing — 900-Pin AL900/AR900



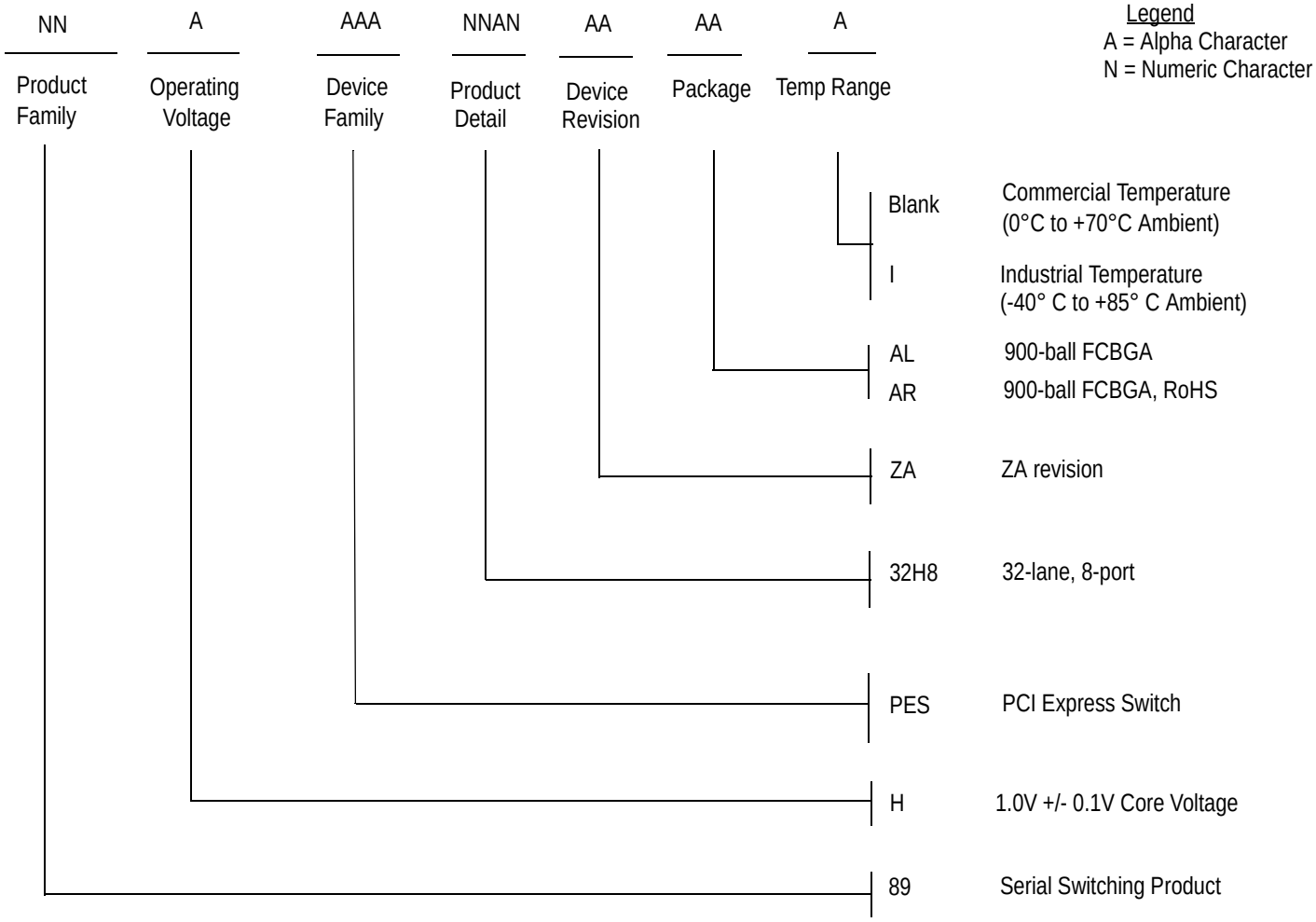
PES32H8 Package Drawing — Page Two



Revision History

July 19, 2007: Initial publication of data sheet.

Ordering Information



Valid Combinations

89HPES32H8ZAAL	900-ball FCBGA package, Commercial Temperature
89HPES32H8ZAAR	900-ball RoHS FCBGA package, Commercial Temperature
89HPES32H8ZAALI	900-ball FCBGA package, Industrial Temperature
89HPES32H8ZAARI	900-ball RoHS FCBGA package, Industrial Temperature

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