



8N50H

Power MOSFET

8A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

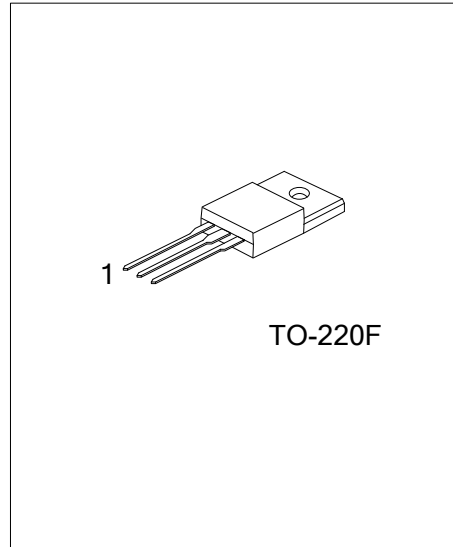
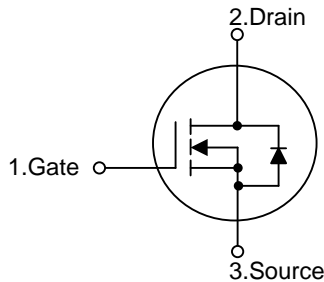
The UTC **8N50H** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **8N50H** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

FEATURES

- * $R_{DS(ON)} \leq 1.0 \Omega$ @ $V_{GS}=10V, I_D=3.5A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



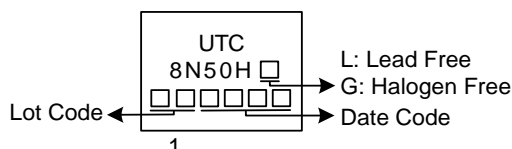
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
8N50HL-TF3-T	8N50HG-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>8N50HG-TF3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TF3: TO-220F</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	7 (Note 2)	A
	Pulsed (Note 2)	I_{DM}	14	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	270	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2	V/ns
Power Dissipation		P_D	35	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=10\text{mH}$, $I_{AS}=8.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD}\leq 8.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.57	$^\circ\text{C}/\text{W}$

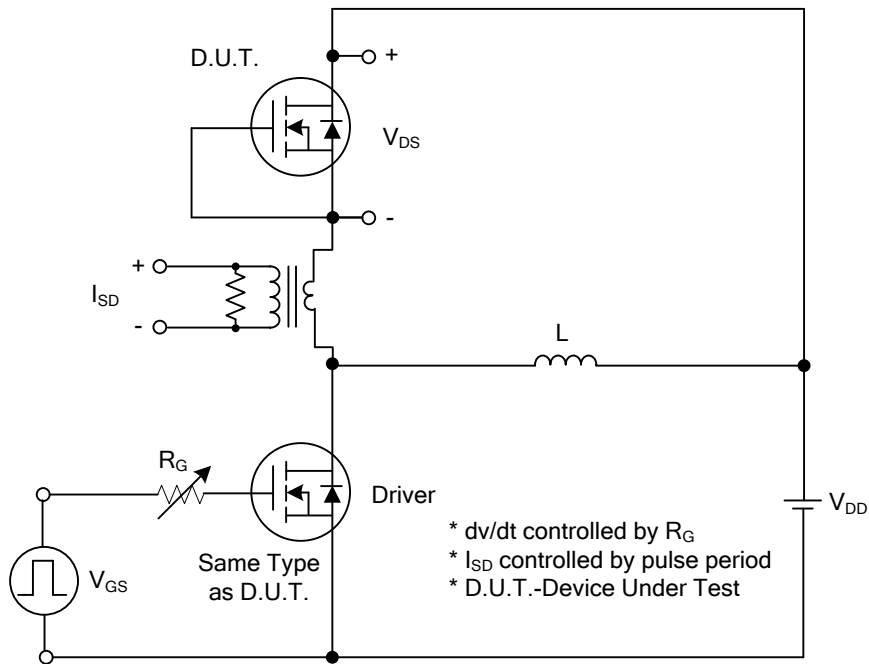
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	$V_{GS}=+30\text{V}$, $V_{DS}=0\text{V}$			+100	nA
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4.0\text{A}$			1.0	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		1020		pF
Output Capacitance	C_{OSS}			108		pF
Reverse Transfer Capacitance	C_{RSS}			12		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=8\text{A}$, $I_G=1\text{mA}$ (Note 1,2)		25		nC
Gate to Source Charge	Q_{GS}			8		nC
Gate to Drain Charge	Q_{GD}			6		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=8\text{A}$, $R_G=25\Omega$ (Note 1, 2)		22		ns
Rise Time	t_R			19		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			52		ns
Fall-Time	t_F			26		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				7	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				14	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=7\text{A}$			1.4	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0\text{V}$, $I_S=7\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		350		ns
Reverse Recovery Charge	Q_{rr}			3.5		μC

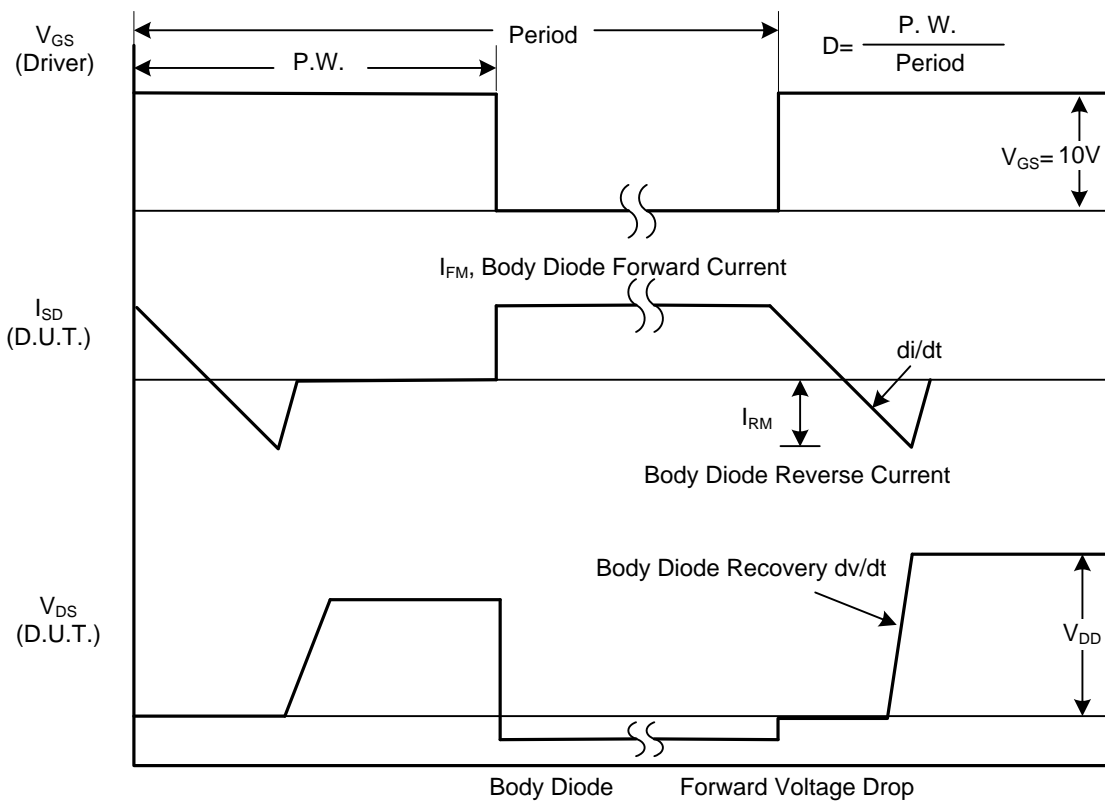
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

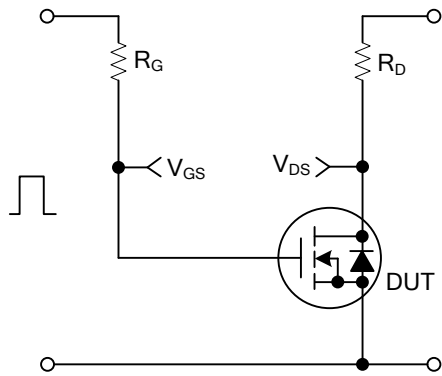


Peak Diode Recovery dv/dt Test Circuit

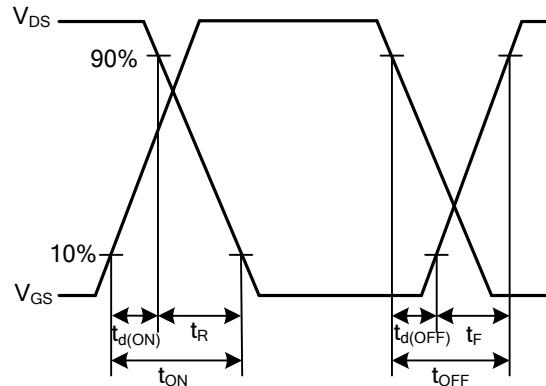


Peak Diode Recovery dv/dt Waveforms

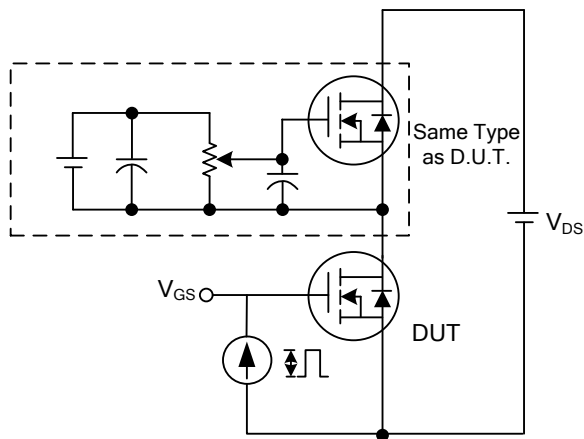
TEST CIRCUITS AND WAVEFORMS



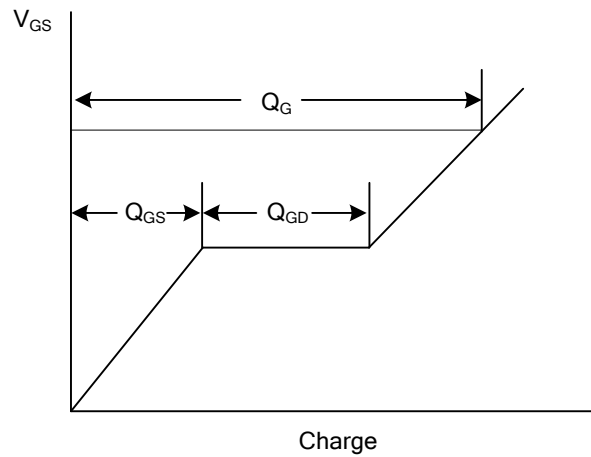
Switching Test Circuit



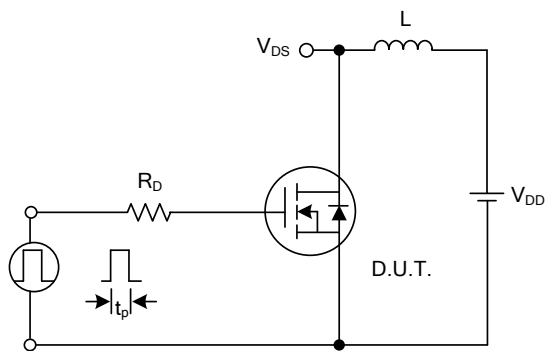
Switching Waveforms



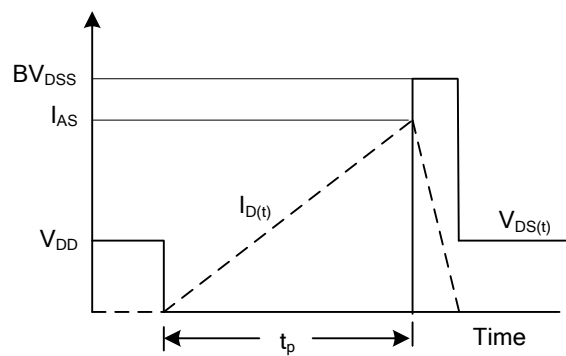
Gate Charge Test Circuit



Gate Charge Waveform

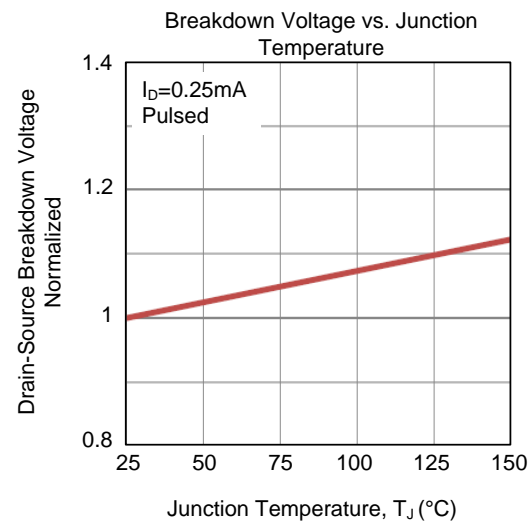
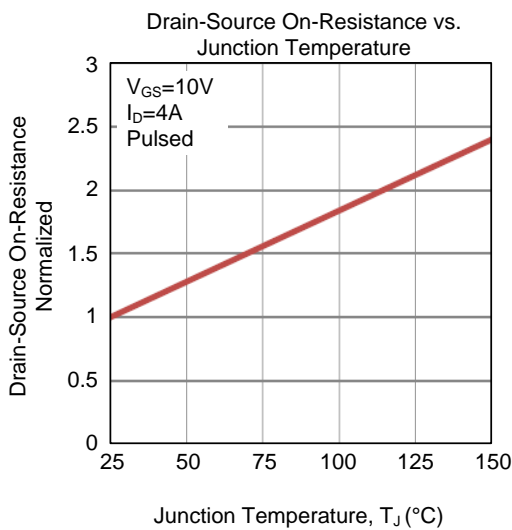
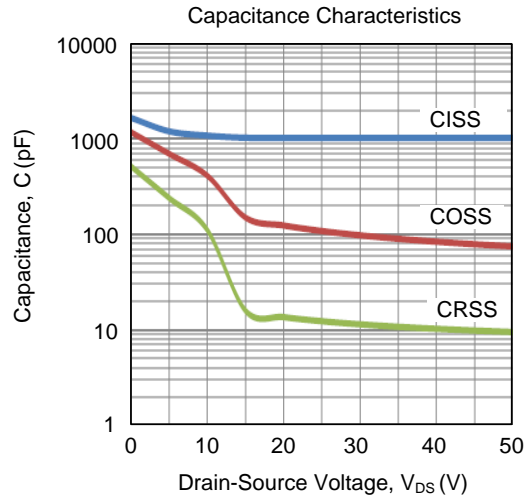
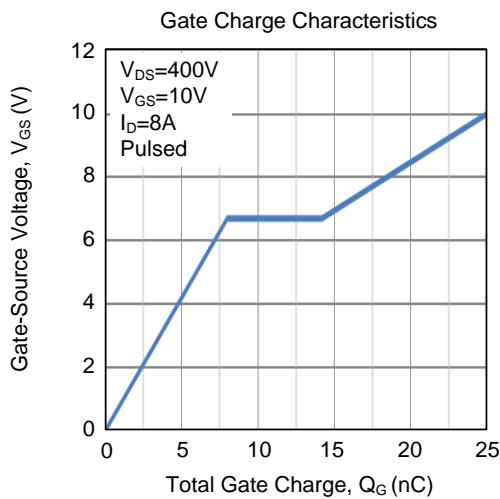
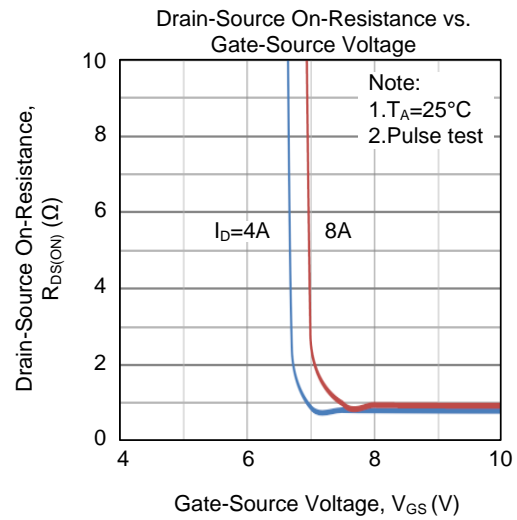
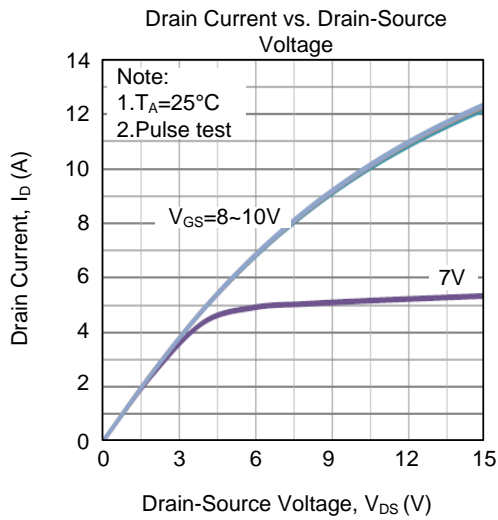


Unclamped Inductive Switching Test Circuit

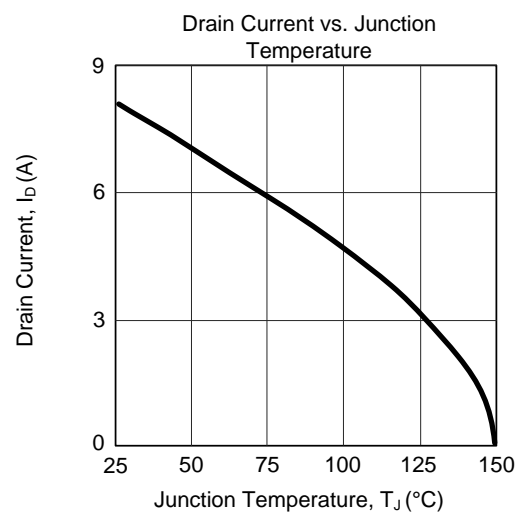
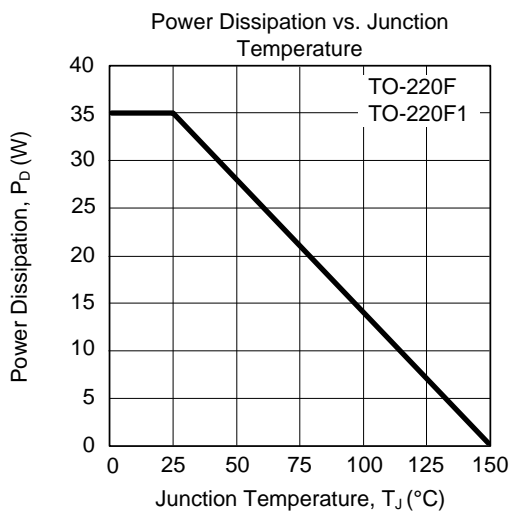
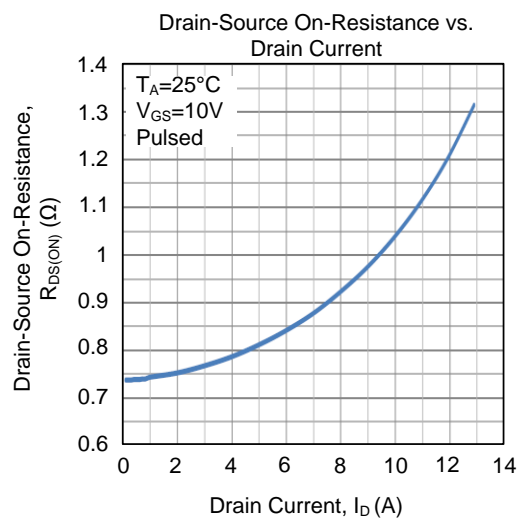
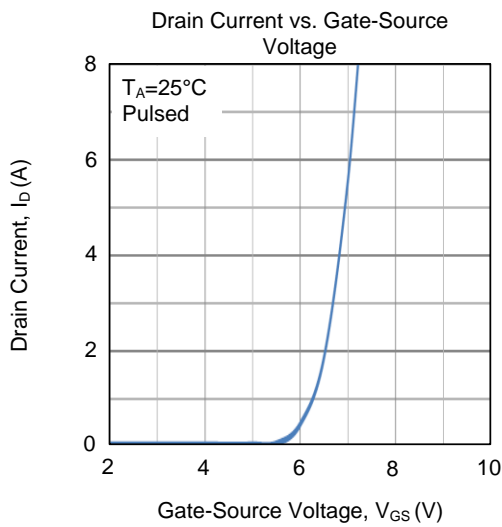
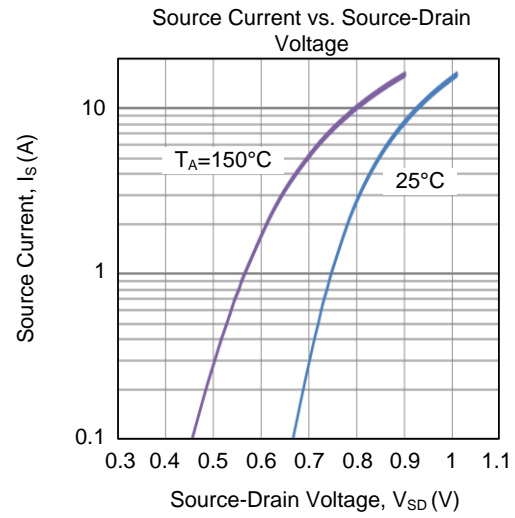
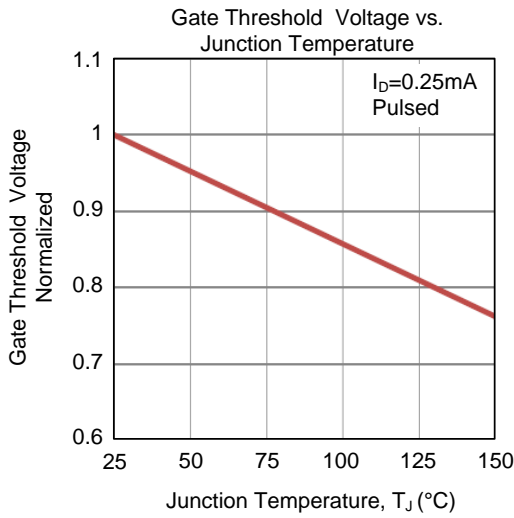


Unclamped Inductive Switching Waveforms

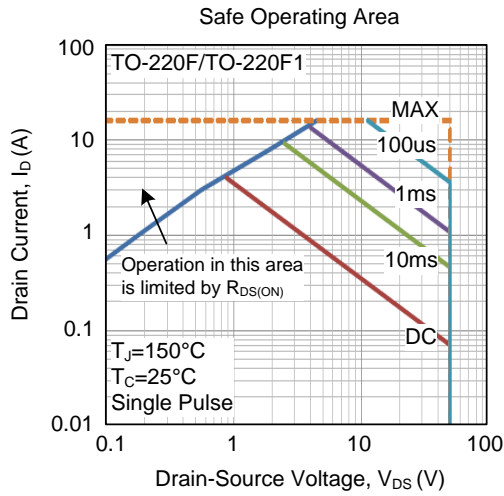
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ **TYPICAL CHARACTERISTICS (Cont.)**



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