Low Phase Noise, 2:4, 3.3V, 2.5V LVPECL Output Fanout Buffer

8SLVP1204

DATASHEET

Description

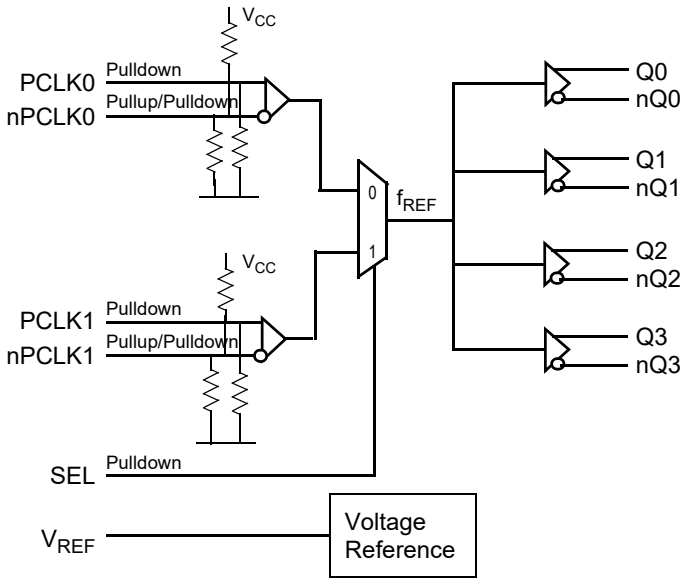
The 8SLVP1204 is a high-performance differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8SLVP1204 is characterized to operate from a 3.3V or 2.5V power supply.

Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVP1204 ideal for clock distribution applications that demand well-defined performance and repeatability. Two selectable differential inputs and four low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

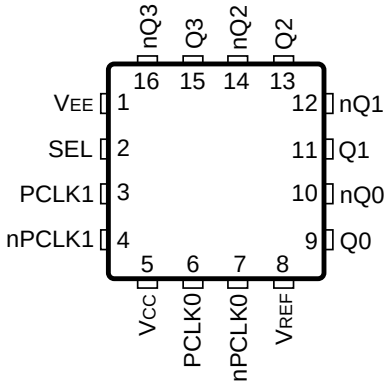
Features

- Four low skew, low additive jitter LVPECL output pairs
- Two selectable, differential clock input pairs
- Differential PCLKx pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Differential PCLKx pairs can also accept single-ended LVCMOS levels. See Applications Information, "Wiring the Differential Input to Accept Single-Ended Levels" (Figures 1A and 1B)
- Maximum input clock frequency: 2GHz
- LVCMOS interface levels for the control input, (input select)
- Output skew: 5ps (typical), at 3.63V
- Propagation delay: 200ps (typical), at 3.63V
- Low additive phase jitter, RMS; f_{REF} = 156.25MHz, V_{PP} = 1V, 12kHz - 20MHz: 40fs (maximum), at 3.63V
- Maximum device current consumption (I_{EE}): 60mA (maximum), at 3.63V
- Full 3.3V±5%, 3.3V±10% or 2.5V±5% supply
- Lead-free (RoHS 6), 16-Lead VFQFPN packaging
- -40°C to 85°C ambient operating temperature
- Supports case temperature ≤ 105°C operations

Block Diagram



Pin Assignment



8SLVP1204

16-Lead, 3mm x 3mm VFQFPN Package

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	SEL	Input	Pulldown	Reference select control pin. See Table 3 for function. LVCMOS/LVTTL interface levels.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. $V_{CC}/2$ default when left floating.
5	V_{CC}	Power		Power supply pins.
6	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
7	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. $V_{CC}/2$ default when left floating.
8	V_{REF}	Output		Bias voltage reference for the PCLK inputs.
9, 10	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
11, 12	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
13, 14	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
15, 16	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. SEL Input Selection Function Table

Input	
SEL	**Operation**
0 (default)	PCLK0, nPCLK0 is the selected differential clock input.
1	PCLK1, nPCLK1 is the selected differential clock input.

NOTE: SEL is an asynchronous control.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Input Sink/Source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	150°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model, NOTE 1	2000V
ESD - Charged Device Model, NOTE 1	1500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C

NOTE 1: It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.

NOTE 2: All conditions in the table must be met to guarantee device functionality.

NOTE 3: The device is verified to the maximum operating junction temperature through simulation.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.97	3.3V	3.63	V
I_{EE}	Power Supply Current			53	60	mA
I_{CC}	Power Supply Current	Q0 to Q3 terminated 50Ω to V_{CC} – 2V		170	204	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current			53	60	mA
I_{CC}	Power Supply Current	Q0 to Q3 terminated 50Ω to V_{CC} – 2V		170	204	mA

Table 4C. Power Supply DC Characteristics, V_{CC} = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
I_{EE}	Power Supply Current			49	55	mA
I_{CC}	Power Supply Current	Q0 to Q3 terminated 50Ω to V_{CC} – 2V		170	199	mA

Table 4D. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.63V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.63V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4E. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4F. LVPECL DC Characteristics, V_{CC} = 3.3V ±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 3.63V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.63V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.63V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias		I_{REF} = ±1mA	V_{CC} – 1.6	V_{CC} – 1.3	V_{CC} – 1.1	V
V_{OH}	Output High Voltage[1]			V_{CC} – 1.1	V_{CC} – 0.9	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage[1]			V_{CC} – 2.0	V_{CC} – 1.65	V_{CC} – 1.5	V

NOTE 1. Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4G. LVPECL DC Characteristics, V_{CC} = 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias		I_{REF} = ±1mA	V_{CC} – 1.6	V_{CC} – 1.3	V_{CC} – 1.1	V
V_{OH}	Output High Voltage[1]			V_{CC} – 1.1	V_{CC} – 0.9	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage[1]			V_{CC} – 2.0	V_{CC} – 1.65	V_{CC} – 1.5	V

NOTE 1. Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4H. LVPECL DC Characteristics, V_{CC} = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias		I_{REF} = ±1mA	V_{CC} – 1.6	V_{CC} – 1.3	V_{CC} – 1.1	V
V_{OH}	Output High Voltage[1]			V_{CC} – 1.1	V_{CC} – 0.9	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage[1]			V_{CC} – 2.0	V_{CC} – 1.6	V_{CC} – 1.5	V

NOTE 1. Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

Table 5A. AC Electrical Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
ΔV/Δt	Input Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay[2]		PCKx, nPCLKx to any Qx, nQx for V_{PP} = 0.1V or 0.3V	120	200	320	ps
*t*sk(o)	Output Skew[3 4]				5	25	ps
*t*sk(i)	Input Skew[4]				5	50	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz		5	20	ps
*t*sk(pp)	Part-to-Part Skew[4 5]				100	200	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 122.88MHz Sine Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		170		fs
			f_{REF} = 122.88MHz Sine Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		114		fs
			f_{REF} = 122.88MHz Sine Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		114		fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		42	51	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		32	40	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		32	40	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 1kHz – 40MHz		51	71	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 10kHz – 20MHz		38	52	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz – 20MHz		38	52	fs
t_R / t_F	Output Rise/ Fall Time		20% to 80%	35	90	180	ps
$MUX_{ISOLATION}$	Mux Isolation[6]		f_{REF} = 100MHz		77		dB
V_{PP}	Peak-to-Peak Input Voltage[7]		f_{REF} < 1.5 GHz	0.1		1.5	V
			f_{REF} > 1.5 GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage[7 8 9]			1.0		V_{CC} – 0.6	V
			V_{PP} = > 247mV	0.8		V_{CC} – 0.6	V
V_O(pp)	Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V, f_{REF} ≤ 2GHz	0.45	0.75	1.0	V
			V_{CC} = 2.5V, f_{REF} ≤ 2GHz	0.4	0.65	1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V, f_{REF} ≤ 2GHz	0.9	1.5	2.0	V
			V_{CC} = 2.5V, f_{REF} ≤ 2GHz	0.8	1.3	2.0	V

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Measured from the differential input crossing point to the differential output crosspoint.

NOTE 3. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.

NOTE 4. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5. Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

NOTE 6. Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

NOTE 7. For single-ended LVCMOS input applications, refer to the Applications section *Wiring the Differential Input Levels to Accept Single-ended Levels* (Figures 1 and 2).

NOTE 8. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.

NOTE 9. Common mode input voltage is defined as the crosspoint.

Table 5B. AC Electrical Characteristics, V_{CC} = 3.3V ±10%, V_{EE} = 0V, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
$\Delta V/\Delta t$	Input[2] Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay[3]		PCKx, nPCLKx to any Qx, nQx for V_{PP} = 0.1V or 0.3V	120	230	325	ps
*t*sk(o)	Output Skew[4 5]				6	30	ps
*t*sk(i)	Input Skew[4]				6	55	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz		7	25	ps
*t*sk(pp)	Part-to-Part Skew[4 6]					200	ps
t_R / t_F	Output Rise/ Fall Time		20% to 80%	35		200	ps
$MUX_{ISOLATION}$	Mux Isolation[7]		f_{REF} = 100MHz		77		dB
V_{PP}	Peak-to-Peak Input Voltage[8]		f_{REF} < 1.5 GHz	0.1		1.5	V
			f_{REF} > 1.5 GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage[7 9 10]			1.0		V_{CC} – 0.6	V
			V_{PP} = > 247mV	0.8		V_{CC} – 0.6	V
V_O(pp)	Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V, $f_{REF} \le$ 2GHz	0.45	0.75	1.0	V
			V_{CC} = 2.5V, $f_{REF} \le$ 2GHz	0.4	0.65	1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V, $f_{REF} \le$ 2GHz	0.9	1.5	2.0	V
			V_{CC} = 2.5V, $f_{REF} \le$ 2GHz	0.8	1.3	2.0	V

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Input Edge Rate is the slope of Δv/Δt at the crosspoint of the differential pair signals. Δt is measured with ΔV = 300mV on one of the single-ended input pair signals.

NOTE 3. Measured from the differential input crossing point to the differential output crosspoint.

NOTE 4. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65

NOTE 6. Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

NOTE 7. Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

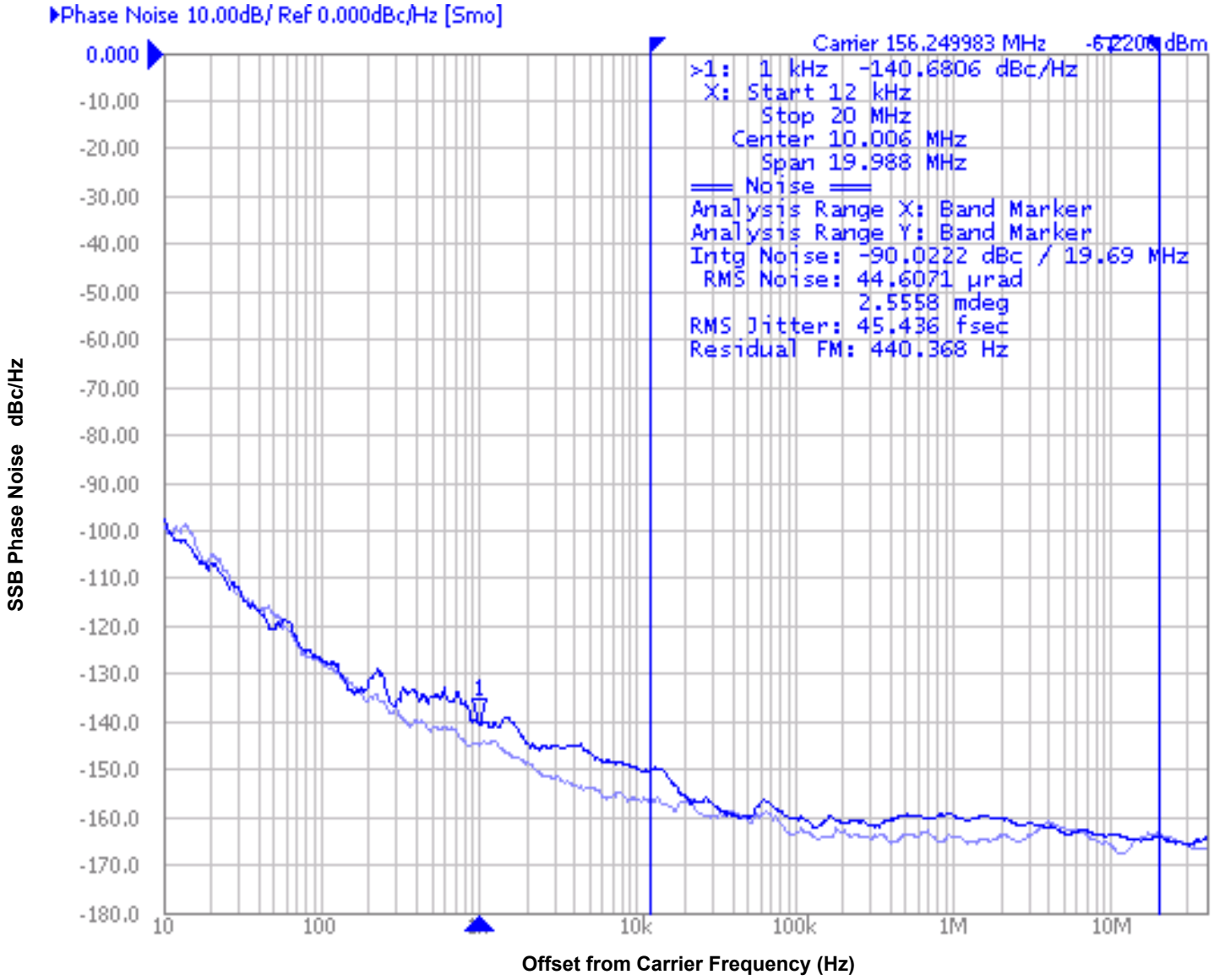
NOTE 8. For single-ended LVCMOS input applications, refer to the Applications section *Wiring the Differential Input Levels to Accept Single-ended Levels* (Figures 1 and 2).

NOTE 9. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.

NOTE 10. Common mode input voltage is defined as the crosspoint.

Additive Phase Jitter

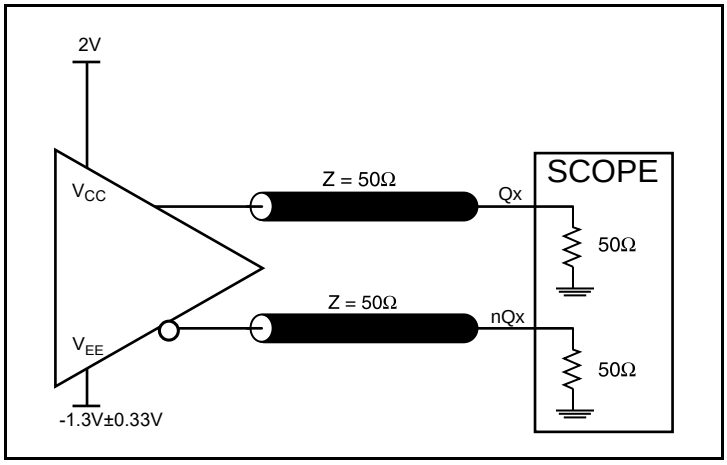
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



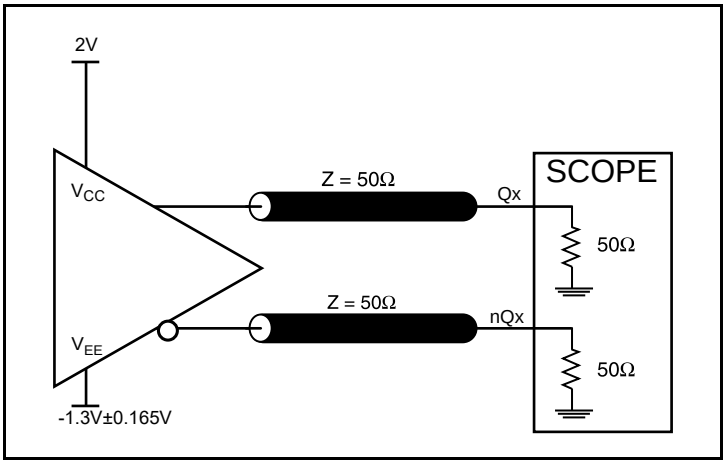
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

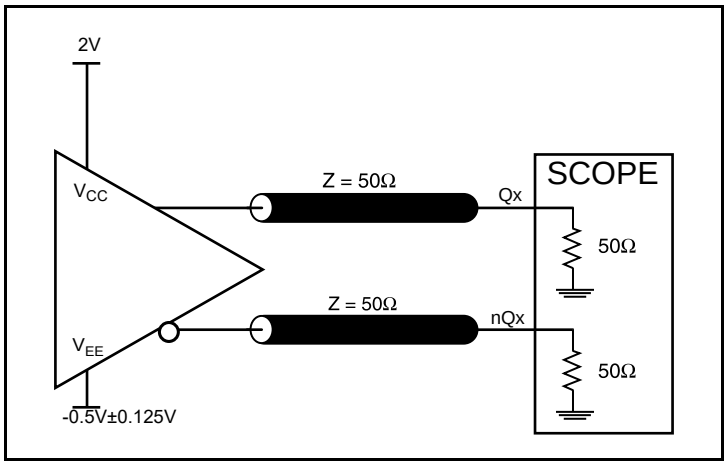
Parameter Measurement Information



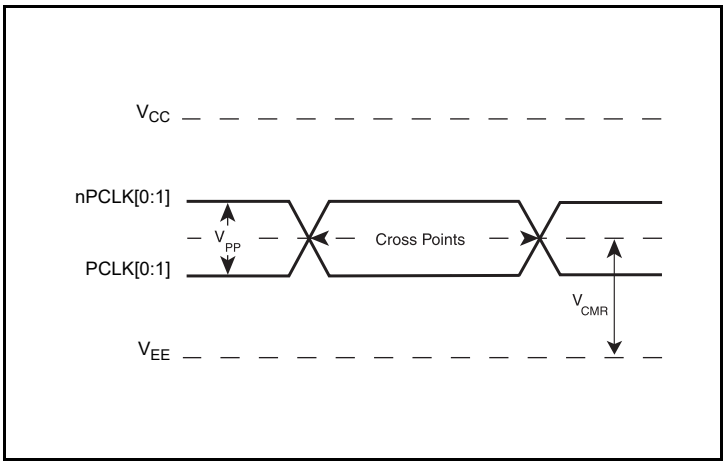
3.3V ±10% LVPECL Output Load Test Circuit



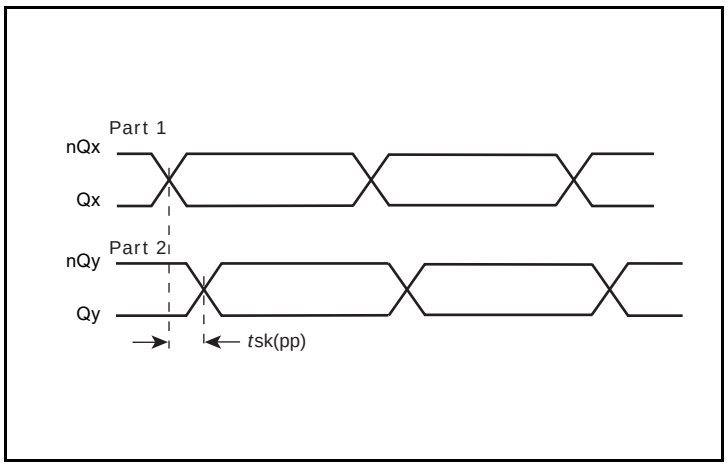
3.3V ±5% LVPECL Output Load Test Circuit



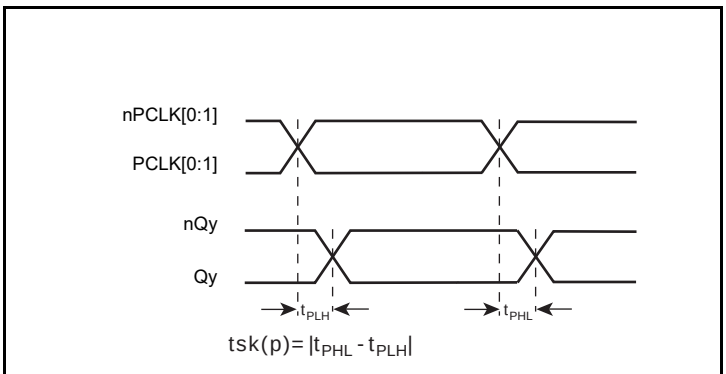
2.5V LVPECL Output Load Test Circuit



Differential Input Level

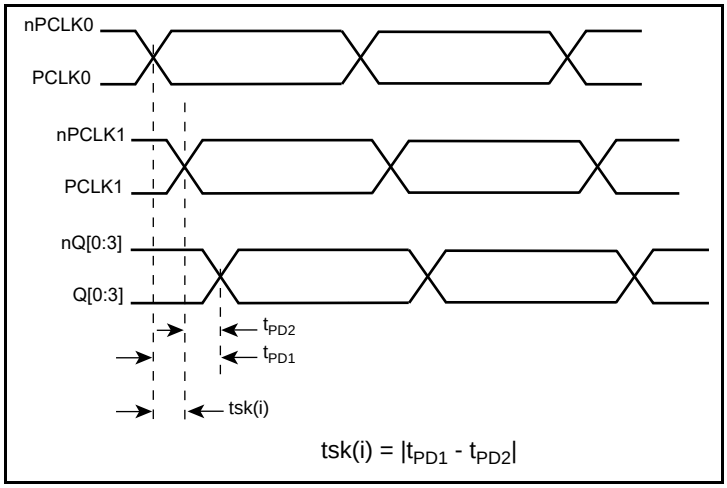


Part-to-Part Skew

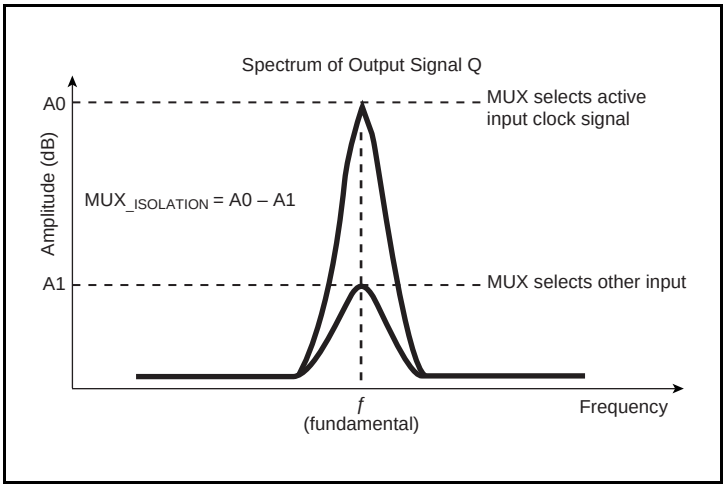


Pulse Skew

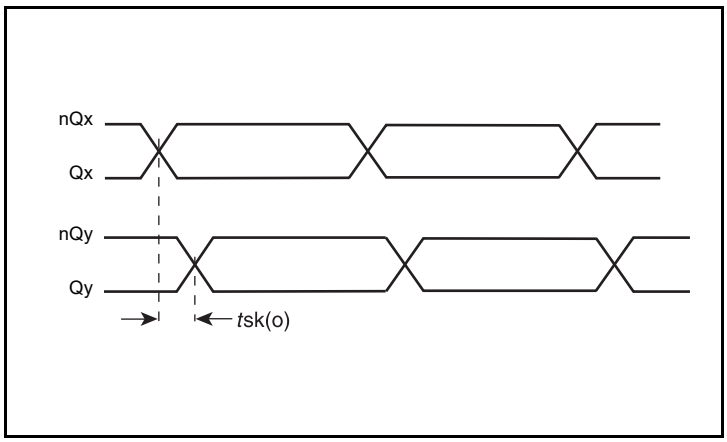
Parameter Measurement Information, continued



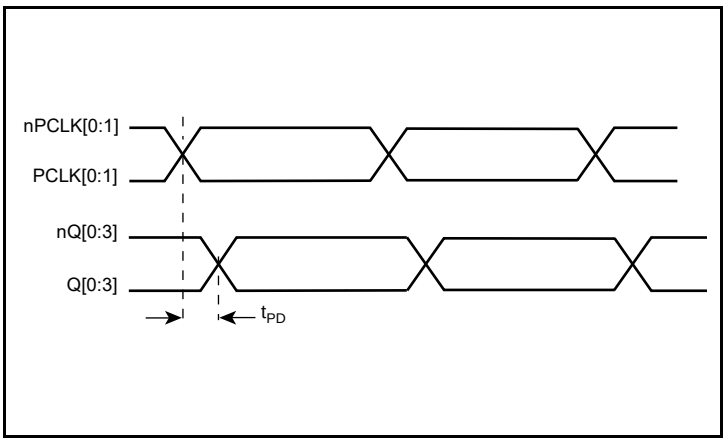
Input Skew



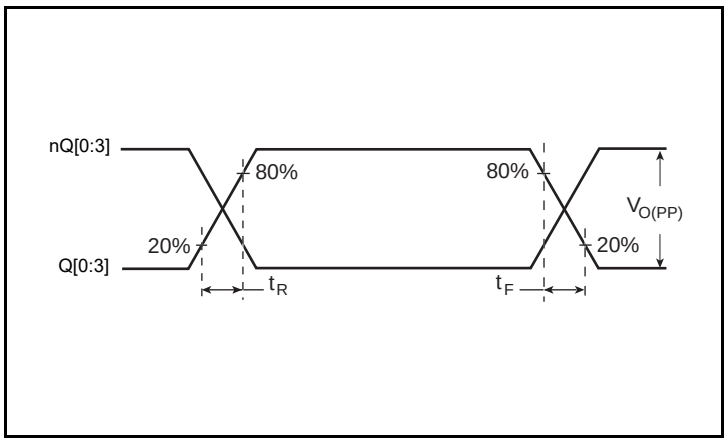
MUX Isolation



Output Skew



Propagation Delay



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

The 8SLVP1204 inputs can be interfaced to LVPECL, LVDS, CML or LVCMOS drivers. *Figure 1A* illustrates how to DC couple a single LVCMOS input to the 8SLVP1204. The value of the series resistance RS is calculated as the difference between the transmission line impedance and the driver output impedance. This resistor should be placed close to the LVCMOS driver. To avoid cross-coupling of single-ended LVCMOS signals, apply the LVCMOS signals to no more than one PCLK input.

A practical method to implement Vth is shown in *Figure 1B* below. The reference voltage Vth = V1 = V_{CC}/2, is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible.

The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below apply when both the single-ended swing and V_{CC} are at the same voltage.

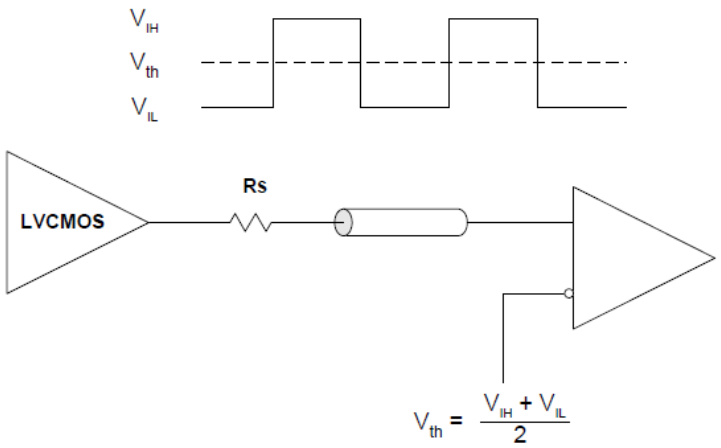


Figure 1A. DC-Coupling a Single LVCMOS Input to the 8SLVP1204

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced, particularly if both input references are LVCMOS to minimize cross talk. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V.

Figure 1B shows a way to attenuate the PCLK input level by a factor of two as well as matching the transmission line between the LVCMOS driver and the 8SLVP1204 at both the source and the load.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. R3 and R4 in parallel should equal the transmission line impedance; for most 50Ω applications, R3 and R4 will be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Though some of the recommended components of Figure 1B might not be used, the pads should be placed in the layout so that they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

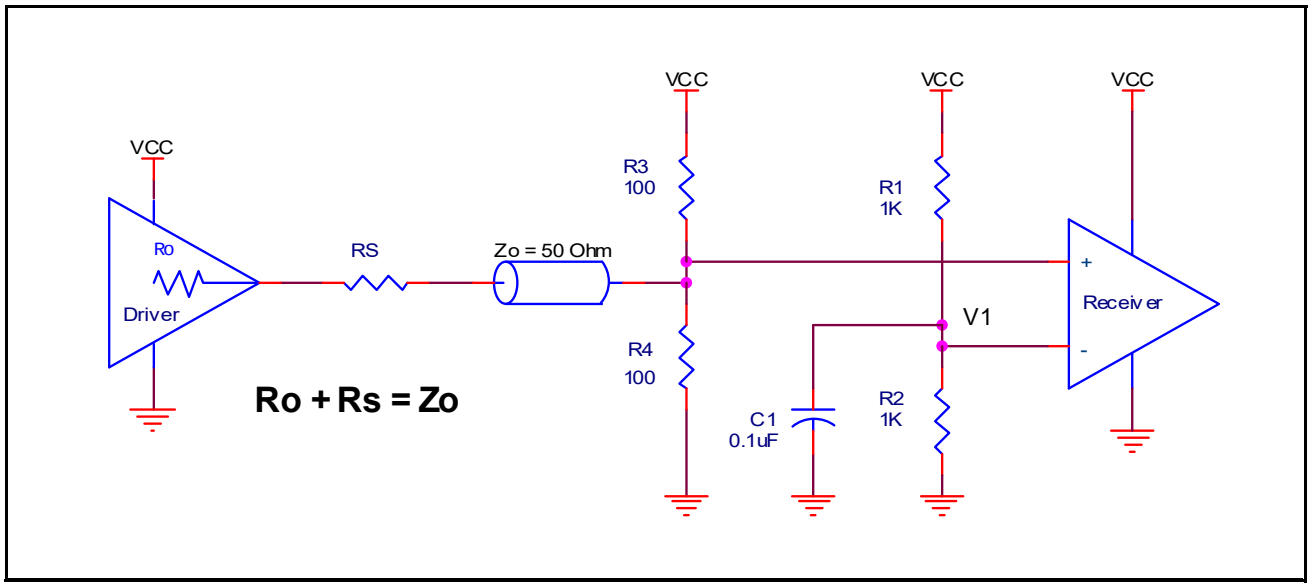


Figure 1B. Alternative DC Coupling a Single LVCMOS Input to the 8SLVP1204

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

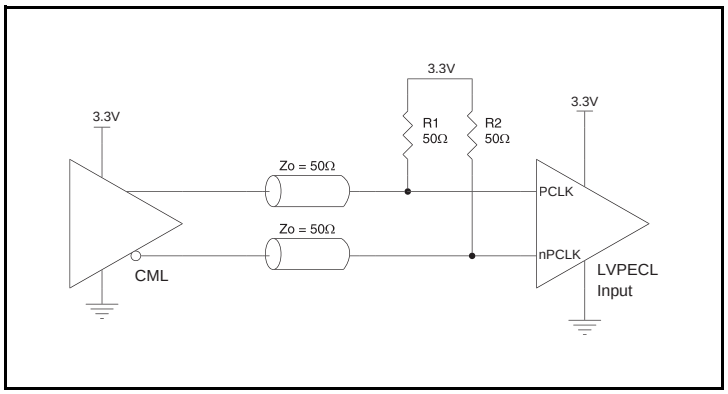


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

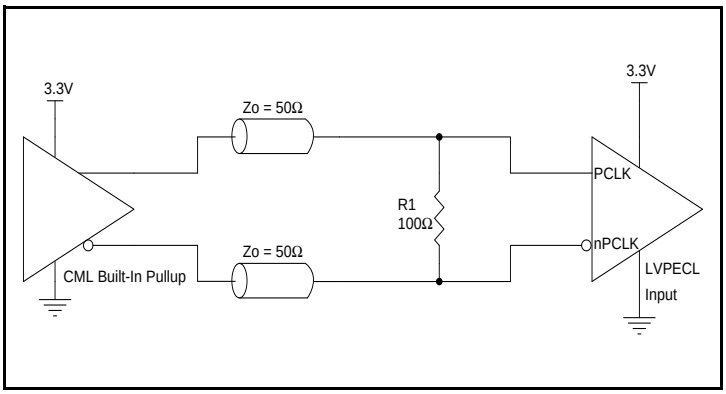


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

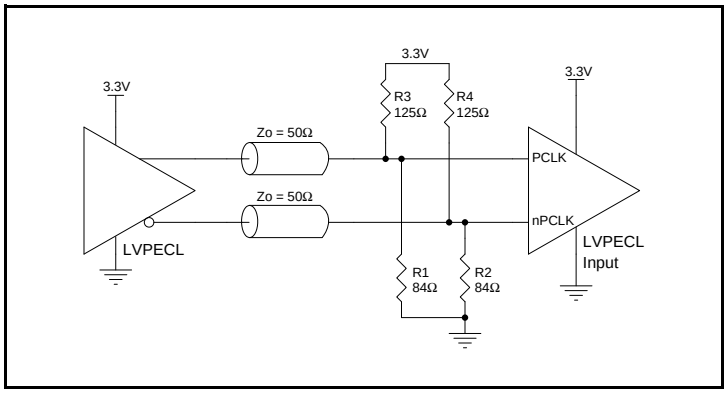


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

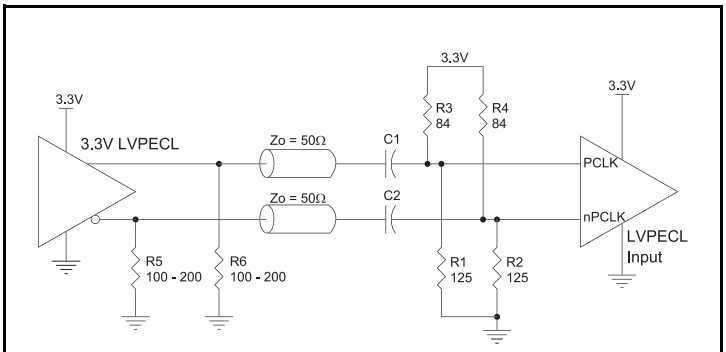


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

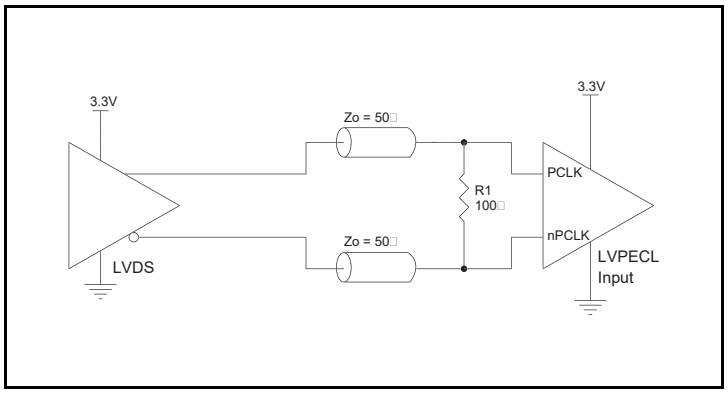


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

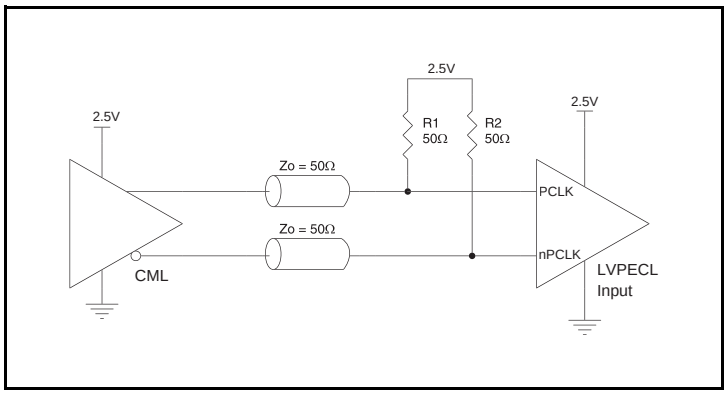


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

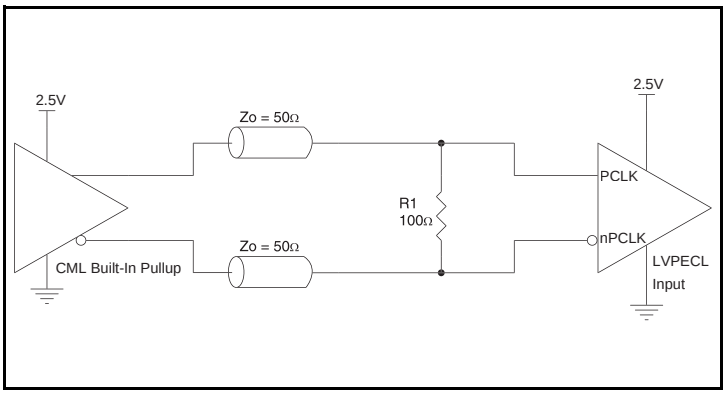


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

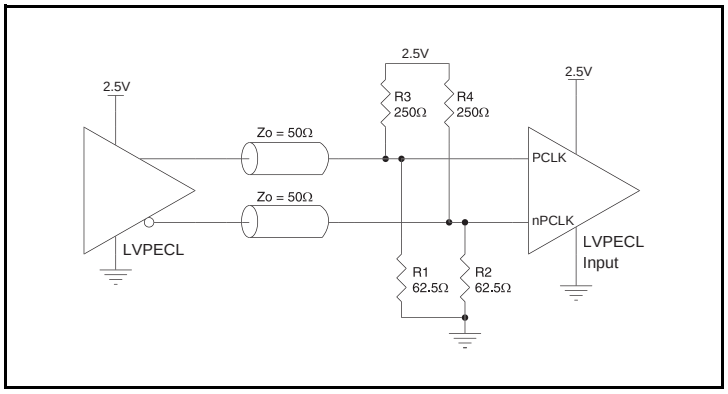


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

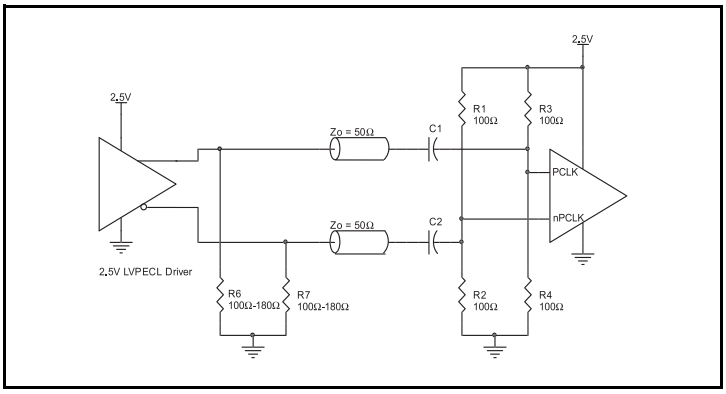


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

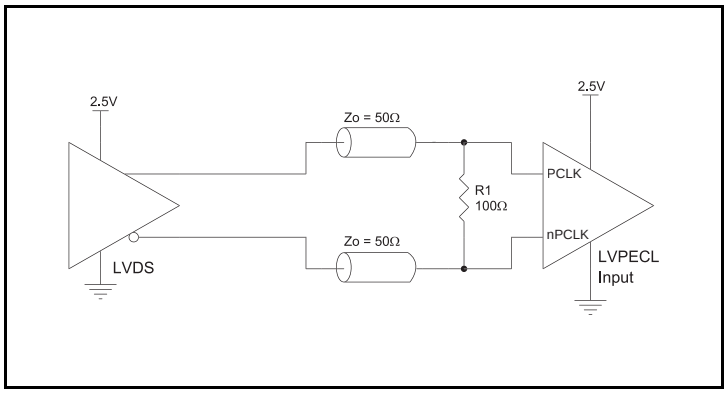


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

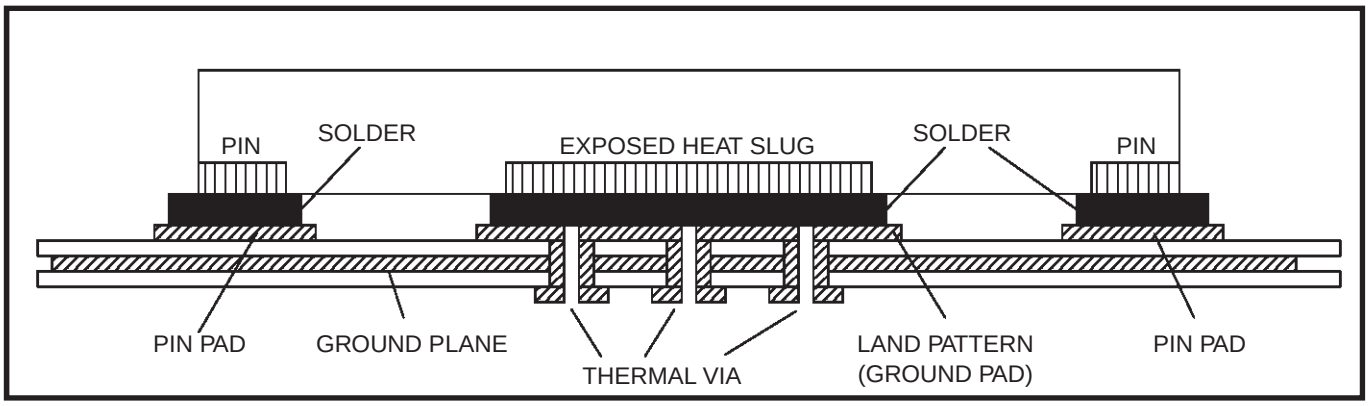


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

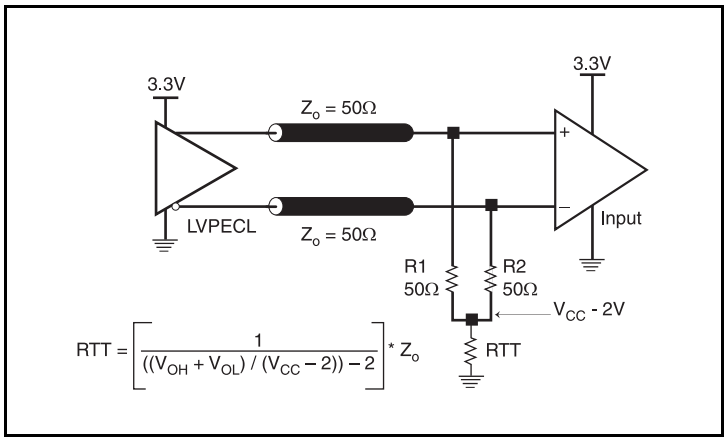


Figure 5A. 3.3V LVPECL Output Termination

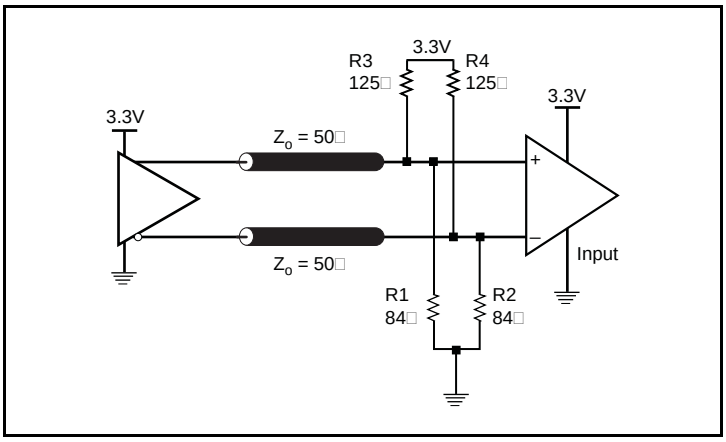


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

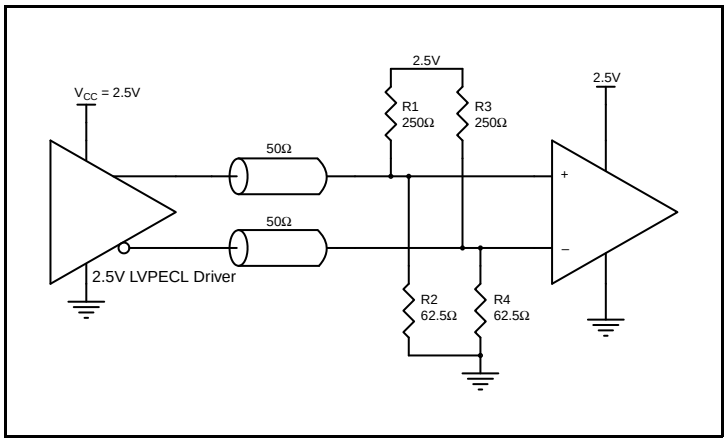


Figure 6A. 2.5V LVPECL Driver Termination Example

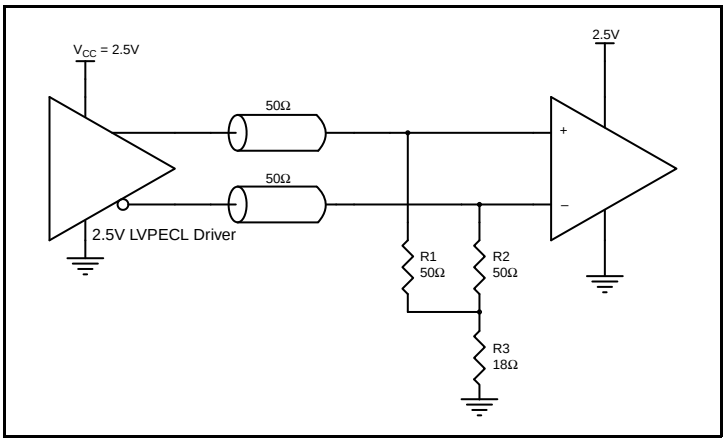


Figure 6B. 2.5V LVPECL Driver Termination Example

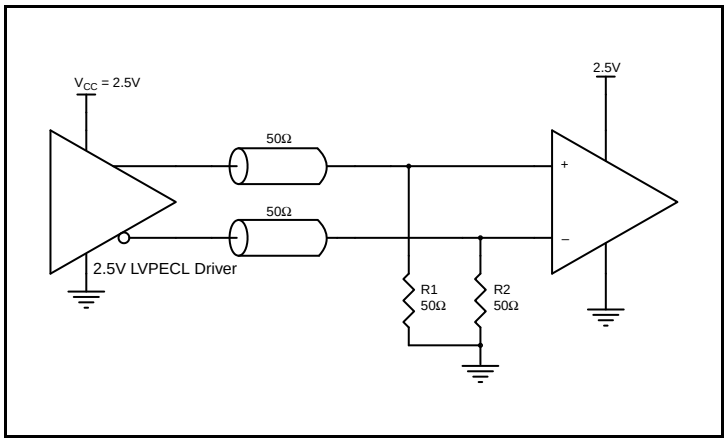


Figure 6C. 2.5V LVPECL Driver Termination Example

3.3V ±10% Power Considerations

This section provides information on power dissipation and junction temperature for the 8SLVP1204.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8SLVP1204 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.63V.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

The maximum current at 85° is as follows:

I_{EE_MAX} = 65mA

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.63V * 60mA = **217.80mW**
- Power (outputs)$_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 33.2mW = **132.8mW**

Total Power_$_{MAX}$ (3.63V, with all outputs switching) = 217.80mW + 132.8mW = **350.60mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.351W * 74.7°C/W = 111.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16-Lead VFQFPN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7.*

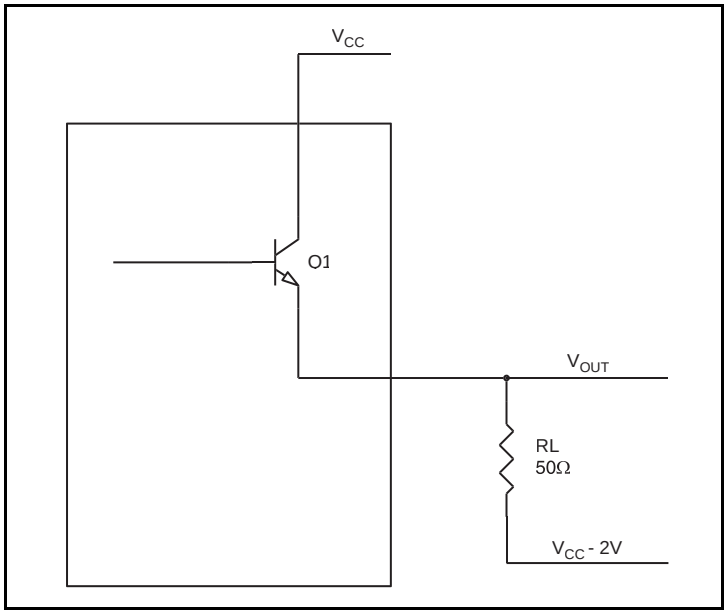


Figure 7. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V. These are typical calculations.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.7V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.7V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.5V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.5V)/50\Omega] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, Ψ_{JB}, is calculated using the following equation:

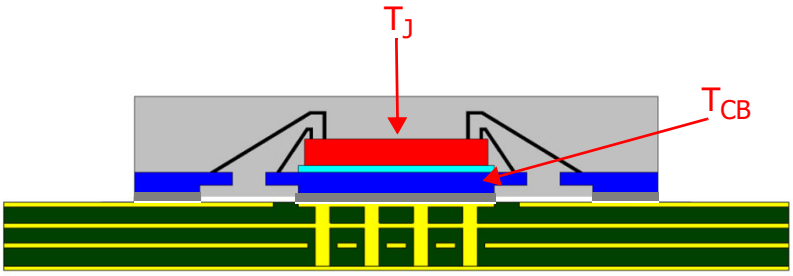
$T_J = T_{CB} + \Psi_{JB} \times P_d$, Where

T_J = Junction temperature at steady state condition in (^oC).

T_{CB} = Case temperature (Bottom) at steady state condition in (^oC).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_d = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_d$

Package type:	16-Lead VFQFPN
Body size:	3mm x 3mm x0.9mm
ePad size:	1.7mm x 1.7mm
Thermal Via:	2 x 2 matrix
Ψ_{JB}	5.1 C/W
T_{CB}	105^{o}C
P_d	0.351 W

For the variables above, the junction temperature is equal to 107^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 111.2^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16-Lead VFQFPN

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for the 8SLVP1204 is: 258

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

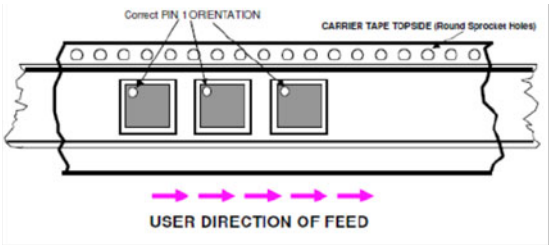
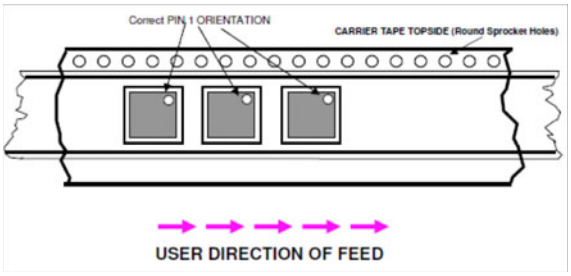
www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nlnlg16p2

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP1204ANLGI	204AI	16-VFQFPN, Lead-Free	Tube	-40°C to 85°C
8SLVP1204ANLGI8	204AI	16-VFQFPN, Lead-Free	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8SLVP1204ANLGI/W	204AI	16-VFQFPN, Lead-Free	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History

Revision Date	Description of Change
November 29, 2018	Updated the description of Absolute Maximum Ratings Added Recommended Operating Conditions
September 13, 2018	Added Note 2 to Table 5B.
March 13, 2018	Updated the package outline drawings; however, no technical changes Completed other minor changes
June 8, 2015	Features Section - Added Case Temperature bullet. Added Case Temperature Considerations.
December 19, 2014	AC Characteristic Tables - added V_{CMR} spec. Updated header/footer throughout the datasheet.
February 25, 2014	Ordering Info: Changed Tray to Tube.
March 20, 2014	V_{PP} Deleted reference to NOTE 5; V_O(pp) corrected typo '≤'; V_{DIFF_OUT} corrected typo '≤' V_{PP} Deleted reference to NOTE 5; V_O(pp) corrected typo '≤'; V_{DIFF_OUT} corrected typo '≤' Output Rise/Fall; changed V_{SWING} to V_O(pp)
January 27, 2014	Changed NOTE 7 to read: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.
September 30, 2013	Features section, 10th bullet; changed 65mA to 60mA. V_{REF}; added Minimum and Maximum values. V_{OH}; added Minimum and Maximum values. V_{OL}; added Minimum and Maximum values.
April 8, 2013	Features section - added Differential PCLK bullet referencing single-ended LVCMOS input. Added 3.3V ±10% Power Supply DC Characteristics Table Added 3.3V ±10% LVCMOS/LVTTL DC Characteristics Table Added 3.3V ±10% LVPECL DC Characteristics Table AC Characteristics Table, added NOTE 6. Added 3.3V ±10% AC Characteristics Table and added NOTE 6. Parameter Measurement Information section - added 3.3V±10% LVPECL Output Load Test Circuit Diagram. Updated application note, *Wiring the Differential Inputs to Accept Single-ended Levels.* Updated Power Considerations section.

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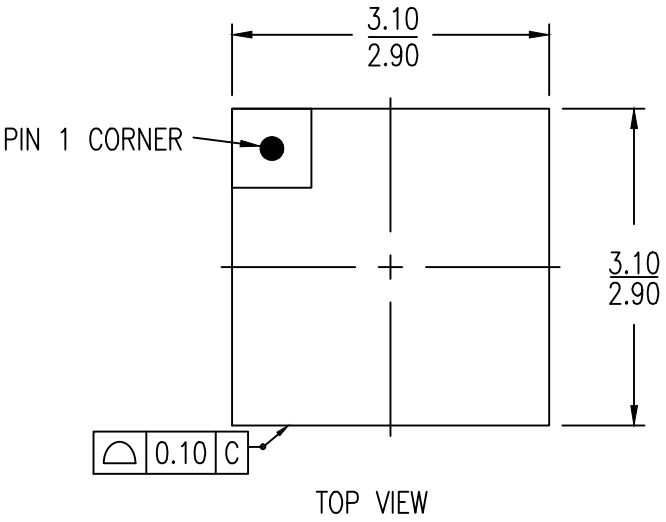
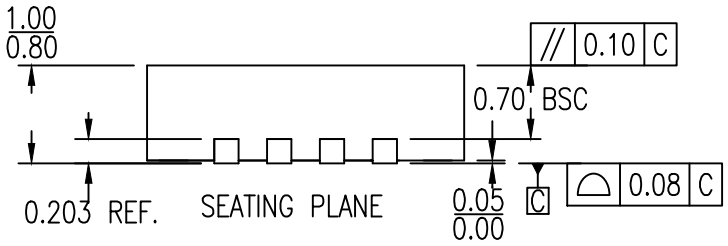
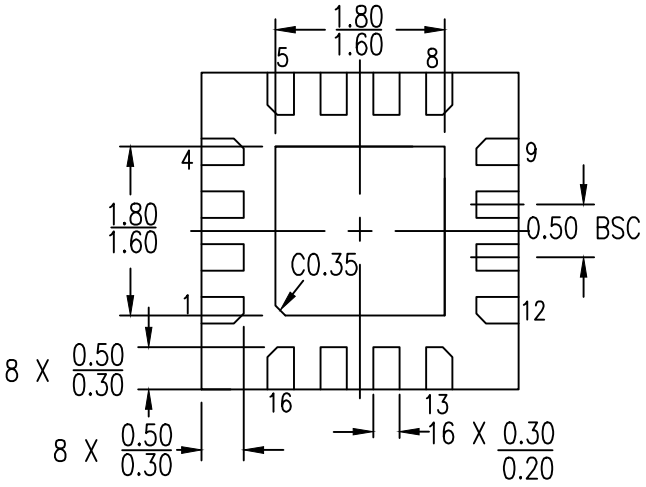


TOP VIEW

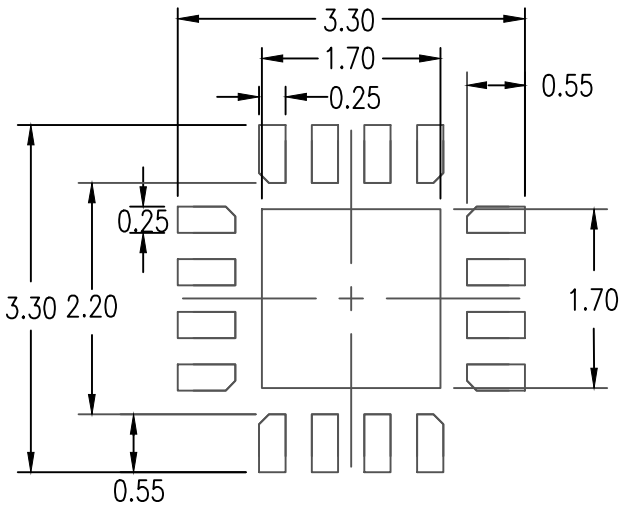


SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Jan 18, 2018	Rev 05	Change QFN to VFQFPN