Clock Synthesizer and Fanout Buffer/Divider

8T49NS010

DATA SHEET

General Description

The 8T49NS010 is a Clock Synthesizer and Fanout Buffer/Divider. When used with an external crystal, the 8T49NS010 generates high performance timing geared towards the communications and data-com markets, especially for applications demanding extremely low phase noise jitter, such as 10, 40 and 100GE.

The 8T49NS010 provides versatile frequency configurations and output formats and is optimized to deliver excellent phase noise performance. The device delivers an optimum combination of high clock frequency and low phase noise performance, combined with high power supply noise rejection.

The 8T49NS010 supports two types of output levels. *FORMAT #1 Outputs* provide an output level with 750mV typical swing, and requires external DC termination. *FORMAT #2 Outputs* provide a similar swing level which does not require DC termination.

The device can be configured through an I^2C serial interface and is offered in a lead-free (RoHS6) 56-pin VFQFN package.

The extended temperature range supports telecommunication and networking end equipment requirements.

Features

- Ten differential outputs
- The input operates in full differential mode (LVDS, LVPECL) or single-ended LVCMOS mode
- Can be driven from a crystal or differential clock
- Support of output power-down
- Excellent clock output phase noise

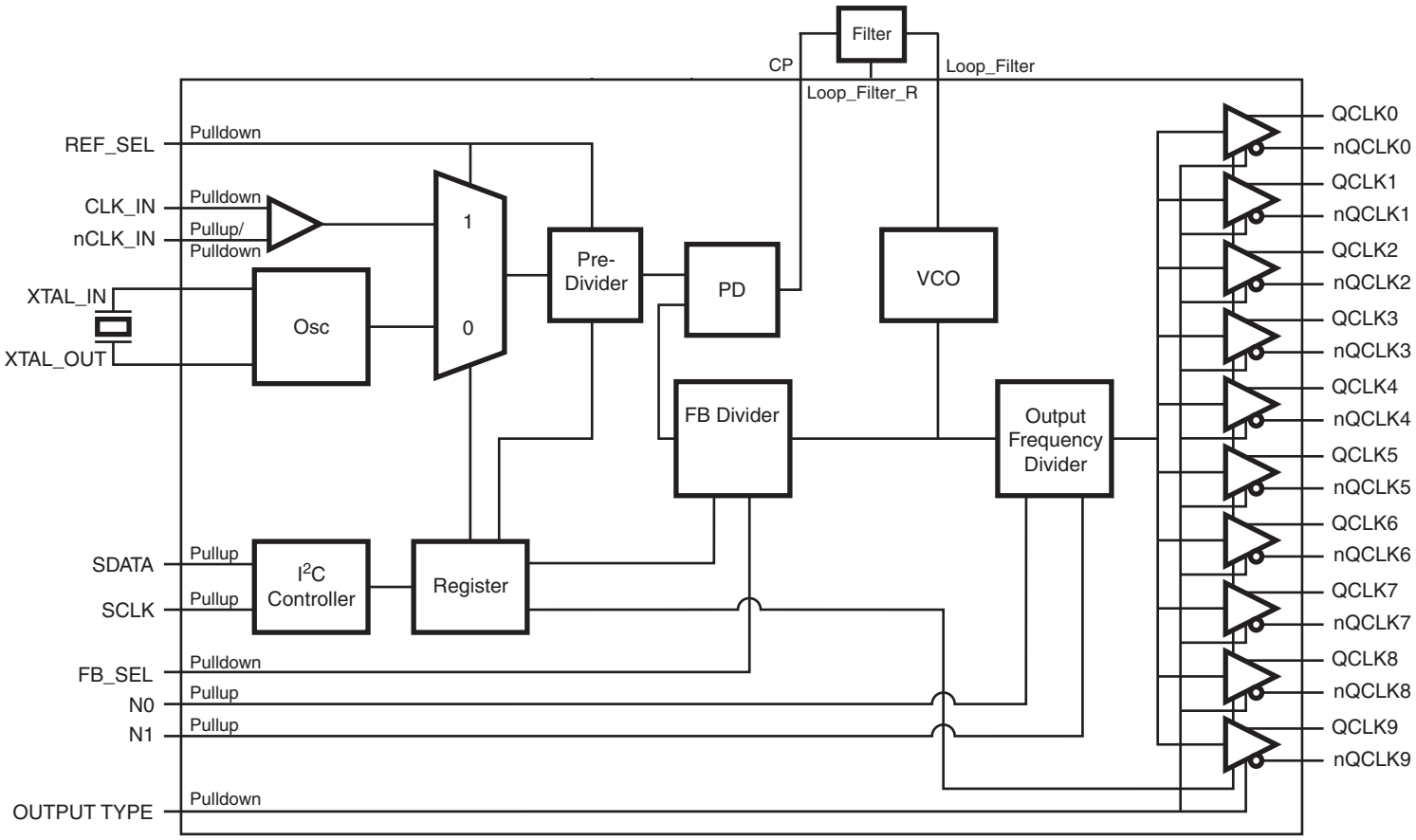
Offset	Output Frequency	Single-side Band Phase Noise
100kHz	156.25MHz	-144 dBc/Hz

- Phase Noise RMS, 12kHz to 20MHz integration range: 84fs (typical)
- LVCMOS compatible I^2C serial interface
- I^2C control inputs are 3.3V tolerant
- Full 3.3V supply voltage
- Lead-free (RoHS 6) 56-pin VFQFN packaging
- -40°C to 85°C ambient operating temperature

Additional Ordering Information

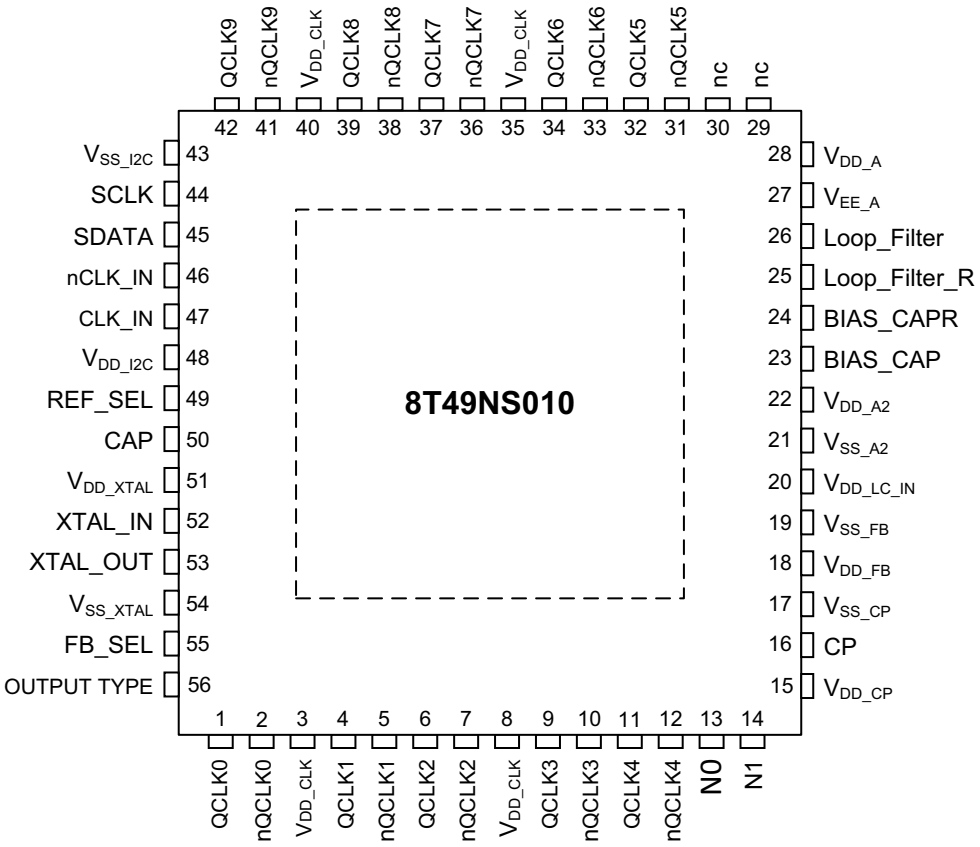
Part/Order Number	Package	Output Frequency (MHz)
8T49NS010-156NLGI	56-pin VFQFN	156.25, 312.5, 625, 1250

Block Diagram



8T49NS010 Functional Block Diagram

Pin Assignment



56-pin 8mm x 8mm VFQFN Package

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	QCLK0	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
2	nQCLK0	Output		
3	V_{DD_CLK}	Power		Power Supply Voltage (3.3V).
4	QCLK1	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
5	nQCLK1	Output		
6	QCLK2	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
7	nQCLK2	Output		
8	V_{DD_CLK}	Power		Power Supply Voltage (3.3V).
9	QCLK3	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
10	nQCLK3	Output		
11	QCLK4	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
12	nQCLK4	Output		

Table 1. Pin Descriptions[1] (Continued)

Number	Name	Type		Description
13	N0	Input	Pullup	Output Divider. Refer to *Table 4C*.
14	N1	Input	Pullup	Output Divider. Refer to *Table 4C*.
15	V_{DD_CP}	Power		Power Supply Voltage to Charge Pump (3.3V).
16	CP	Output		Charge Pump.
17	V_{SS_CP}	Power		Power Supply Ground for Charge Pump - Return for V_{DD_CP}.
18	V_{DD_FB}	Power		Power Supply Voltage to Feedback Divider (3.3V).
19	V_{SS_FB}	Power		Power Supply Ground to Feedback Divider (3.3V). Return for V_{DD_FB}.
20	$V_{DD\_LC\_IN}$	Power		Power Supply Voltage for LC Interface. (3.3V).
21	V_{SS_A2}	Power		Power Supply Ground for VCO.
22	V_{DD_A2}	Power		Power Supply Voltage for VCO.
23	BIAS_CAP			Bias Capacitor.
24	BIAS_CAPR			Bias Capacitor Return.
25	Loop_Filter_R			Loop Filter Return.
26	Loop_Filter			Loop Filter Capacitor.
27	V_{EE_A}	Power		Power Supply ground for VCO. Return for V_{DD_A} pin 28.
28	V_{DD_A}	Power		Power Supply for VCO.
29	NC	Unused		No internal connection.
30	NC	Unused		No internal connection.
31	nQCLK5	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
32	QCLK5	Output		
33	nQCLK6	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
34	QCLK6	Output		
35	V_{DD_CLK}	Power		Power Supply Voltage (3.3V).
36	nQCLK7	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
37	QCLK7	Output		
38	nQCLK8	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
39	QCLK8	Output		
40	V_{DD_CLK}	Power		Power Supply Voltage (3.3V).
41	nQCLK9	Output		Differential clock output pair. FORMAT #1 or FORMAT #2 output levels.
42	QCLK9	Output		
43	V_{SS_I2C}	Power		Power Supply Ground for I^2C. Return for Pin 48 V_{DD_I2C}.
44	SCLK	Input	Pullup	I^2C clock input. LVCMOS interface levels.
45	SDATA	I/O	Pullup	I^2C data Input/Output: LVCMOS interface levels. Open Drain Pin.

Table 1. Pin Descriptions[1] (Continued)

Number	Name	Type		Description
46	nCLK_IN	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD\_x}/2$.
47	CLK_IN	Input	Pulldown	Non-inverting differential clock input.
48	V_{DD_I2C}	Power		Power Supply Voltage for I^2C.
49	REF_SEL	Input	Pulldown	Selects between XTAL and CLK. 0 select Xtal (with x2)and 1 selects CLK input. Refer to *Table 4A*. LVCMOS interface levels.
50	CAP			Bypass capacitor for internal reference. Should connect cap between this pin and V_{DD_I2C} pin 48.
51	V_{DD_XTAL}	Power		Power Supply for crystal.
52	XTAL_IN			Crystal oscillator interface, XTAL_IN is the input.
53	XTAL_OUT			Crystal oscillator interface, XTAL_OUT is the output.
54	V_{SS_XTAL}	Power		Power Supply Ground for XTAL circuit. Return for pin 51
55	FB_SEL	Input	Pulldown	Feedback Divider select. Refer to *Table 4B*. LVCMOS interface levels.
56	OUTPUT TYPE	Input	Pulldown	Selects between FORMAT #1 or FORMAT #2 (with no DC termination) output levels. “0” selects FORMAT #2 and “1” selects FORMAT #1 type output structure. Refer to *Table 5K*. LVCMOS interface levels.
ePad	V_{EE_EP}	Power		Negative supply. Exposed pad must be connected to ground. Return for all outputs and core supplies Pins 3, 8, 20, 35, 40.

NOTE 1. *Pulldown* and *Pullup* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values

Table 2. Input Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3. Output Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{OUT}	Output Impedance	SDATA	V_{DD_I2C} = 3.3V ± 5%		60		Ω

Principles of Operation

Depending on the input used, the 8T49NS010's low phase noise integer-N PLL can multiply the reference to 2400MHz to 2500MHz.

The device offers ten clock outputs (QCLK[9:0]/nQCLK[9:0]). Each output can be disabled individually through registers. With ÷2, ÷4, ÷8 and ÷16 values one can get output frequencies of 156.25MHz, 312.5MHz, 625MHz and 1250MHz when driven from a 25MHz input, for example. *Table 4A* to *Table 4C* show functions of the hardware pin settings. The input select pin REF_SEL will choose either XTAL input or CLK_IN input and this pin also set the pre-divider PRE to either x2 or ÷1. Feedback divider FB_SEL pin will set the feedback divider to either ÷50, ÷25. The VCO of this device is 2.5GHz. The feedback divider should be properly set to assure the PLL lock for VCO=2.5GHz. N1 and N0 are pins for output frequency divider setting. *Table 4D* provide some examples of setting output to 156.25MHz. N1 and N0 can be set for other output frequencies. Additional divider values are available through registers that can be programmed with I^2C interface. *Table 4C* lists the frequencies available with select pins on the device, while *Table 4E* lists all available divider configurations via I^2C.

The 8T49NS010 operates over the industrial temperature range of -40°C to +85°C.

The outputs are compatible with LVPECL-type logic levels, described as FORMAT #1 or FORMAT #2 (see *Termination for QCLKn Outputs*) and the DC characteristics for these two formats in the *DC Electrical Characteristics* (*Table 6D* and *Table 6E*). *Table 4C*, below, shows an example using a 2500MHz VCO frequency input with the selected output dividers shown, resulting in the listed output frequencies. The output divider N can also be set via internal registers. The configuration and re-configuration of any of the output dividers requires an I^2C write sequence.

Each QCLK output can be individually disabled through an I^2C command.

Table 4A. REF_SEL Input Pin Setting

REF_SEL	INPUT	÷PRE
0 (Default)	XTAL_IN	X2
1	CLK_IN	÷1

Table 4B. FBSEL Feedback divider Pin Setting

FB_SEL	Feedback Divider
0 (Default)	÷50
1	÷25

Table 4C. Hardware Pins N1 and N0 Output Frequency Divider Setting

N[1:0]	Output Divider N	Output Frequency (F_{VCO} = 2500MHz)
00	÷2	1250MHz
01	÷4	625MHz
10	÷8	312.5MHz
11 (Default)	÷16	156.25MHz

Table 4D. Hardware Pin Setting Examples

Input (MHz)	REF_SEL	FB_SEL	N[1:0]	Output (VCO=2500MHz)	Comments
XTAL_IN=25	0, [PRE=x2]	0[÷50]	11[÷16]	156.25MHz	Default
XTAL_IN=50	0, [PRE=x2]	1[÷25]	11[÷16]	156.25MHz	Recommended
CLK_IN=50	1, [PRE=÷1]	0[÷50]	11[÷16]	156.25MHz	
CLK_IN=100	1, [PRE=÷1]	1[÷25]	11[÷16]	156.25MHz	

Table 4E. Output Frequency Divider Settings, I^2C Only

N[3:0]	Divider Value
0000	÷1
0001	÷2
0010	÷3
0011	÷4
0100	÷5
0101	÷6
0110	÷8
0111	÷10
1000	÷12
1001	÷16
1010	÷20
1011	÷24

Reference Clock Inputs

The 8T49NS010 features one differential reference clock input (CLK_IN, nCLK_IN) and a crystal input. This input can be configured to operate in full differential mode (LVDS or LVPECL) or single-ended 3.3V CMOS mode.

(The input signal frequency is divided down through a prescaler function (PV).)

The reference input divider (PV) provides division ratios as shown in *Table 4F*.

This divider setting may be adjusted via the PV bit in the *Reference Control Register.*

Table 4F. Available Pre-Divider Settings (PV), I^2C Only

Register Bits PDIV[1:0]	Pv Divider Settings
00	x2
01	÷1
10	÷2
11	÷4

Table 5A. Register Bits

Register	Defaults	D7	D6	D5	D4	D3	D2	D1	D0
0	0011 0010	MDIV[7]	MDIV[6]	MDIV[5]	MDIV[4]	MDIV[3]	MDIV[2]	MDIV[1]	MDIV[0]
1	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK0	OE_QCLK0	PWD_EF_QCLK0
2	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK1	OE_QCLK1	PWD_EF_QCLK1
3	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK2	OE_QCLK2	PWD_EF_QCLK2
4	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK3	OE_QCLK3	PWD_EF_QCLK3
5	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK4	OE_QCLK4	PWD_EF_QCLK4
6	0000 0011	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CP_CUR_C[1]	CP_CUR_C[0]
7	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
8	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10	XXXX XXXX	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
12	0000 1111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
13	1000 0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
14	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0
15	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK5	OE_QCLK5	PWD_EF_QCLK5
17	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK6	OE_QCLK6	PWD_EF_QCLK6
18	0000 1001	Reserved	Reserved	Reserved	Reserved	N[3]	N[2]	N[1]	N[0]
19	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
20	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDIV[1]	PDIV[0]
21	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	HF_XTAL	SEL_VREG2P5	REF_SEL
22	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RELOCK
23	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK7	OE_QCLK7	PWD_EF_QCLK7
24	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK8	OE_QCLK8	PWD_EF_QCLK8
25	0000 0010	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLK9	OE_QCLK9	PWD_EF_QCLK9
26	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
27	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PIN_OVERRIDE
28	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
29	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
30	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

PLL Control Register

The PLL control register contains the settings for the PLL reference divider and feedback dividers.

Table 5B. PLL Pre-Divider Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDIV[1]	PDIV[0]

Table 5C. PLL Pre-Divider Register Function Description

Bits	Name	Factory Default	Function
PDIV[1:0]	Pre-Divider (P)	00	00 = x 2 (Default) 01 = ÷1 10 = ÷2 11 = ÷4

Table 5D. PLL FB Divider Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
0	MDIV[7]	MDIV[6]	MDIV[5]	MDIV[4]	MDIV[3]	MDIV[2]	MDIV[1]	MDIV[0]

Table 5E. PLL FB Divider Register Function Description

Bits	Name	Factory Default	Function
MDIV[7:0]	FB Divide (M)	0011 0010	0000 0000 = Reserved 0000 0001 = Reserved 0000 0010 = Reserved 0000 0011 = Reserved 0000 1000 = ÷8 … 0011 0010 = ÷50 (Default) … 1111 1111 = ÷255

PLL Charge Pump Control Register

The PLL control register contains the PLL charge pump settings.

Table 5F. PLL Charge Pump Control Register Bit Allocations

	Register Bit							
Register	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CP_CUR_C[1]	CP_CUR_C[0]

Table 5G. PLL Charge Pump Control Register Function Description

Bits	Name	Factory Default	Function
CP_CUR_C[1:0]	Charge Pump Current	11	Controls the charge pump current of the PLL. Charge pump current is the binary value of this register plus one multiplied by 1.4 mA. ICP = 1.4 mA x (CP_CUR_C[1:0] + 1). Default setting is 5.6 mA; (4 x 1.4 mA)

NOTE: Charge Pump current (I_{CP}) values are typical numbers.

QCLK[0:9] Clock Divider and Output Control

Table 5H. QCLK[0:9] Clock Divider Register Bit Allocations

		Register Bit							
Register	**Bits**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18	N[3:0]	Reserved	Reserved	Reserved	Reserved	N[3]	N[2]	N[1]	N[0]

Table 5I. QCLK[0:9] Clock Divider Register Function Descriptions

Bits	Name	Factory Default	Function	
N[3:0]	Divider Settings	1001	0000	÷1
			0001	÷2
			0010	÷3
			0011	÷4
			0100	÷5
			0101	÷6
			0110	÷8
			0111	÷10
			1000	÷12
			1001	÷16 (Default)
			1010	÷20
			1011	÷24
			1100 – 1111	Reserved

Table 5J. QCLK[0:9] Output Control Register Bit Allocations

	Register Bit							
Register	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1, 2, 3, 4, 5, 16, 17, 23, 24, 25	Reserved	Reserved	Reserved	Reserved	Reserved	PWD_QCLKn	OE_QCLKn	PWD_EF_QCLKn

Table 5K. QCLK[0:9] Output Control Register Function Description

Bits	Name	Factory Default	Function
PWD_QCLKn	Output Buffer Power Down State	0	0 = Output buffer is powered-on (Default) 1 = Output buffer is powered-down
OE_QCLKn	Output Buffer Enable	1	0 = Output buffer is disabled
			1 = Output buffer is enabled (Default)
PWD_EF_QCLKn	Output Buffer Format	0	0 = QCLKn is FORMAT #2 (Requires FORMAT #2 100Ω output termination across a QCLKn, nQCLKn pair). 1 = QCLKn is FORMAT #1 (Requires FORMAT #1 50Ω output termination of the QCLKn, nQCLKn output pair to the specified recommended termination voltage).

PLL Control Register

Table 5L. PLL Control Register

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
22	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RELOCK

Table 5M. PLL Control Register Function Descriptions

Bits	Name	Factory Default	Function
RELOCK	PLL Relock	0	0 = no effect 1 = Creates a pulse that forces a re-lock on the PLL. Bit auto-clears.

Table 5N. Reference Configuration Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
21	Reserved	Reserved	Reserved	Reserved	Reserved	HF_XTAL	SEL_VREG2P5	REF_SEL

Table 5O. Reference Configuration Control Register Function Descriptions

Bits	Name	Factory Default	Function
HF_XTAL	High-Frequency XTAL	0	0 = 10MHz-70MHz XTAL (Default) 1 = 10MHz-40MHz XTAL (Low Drive Level)
SEL_VREG2P5	XTAL Amplification	0	0 = 2V Regulated Voltage (Default)
			1 = 1.75V Regulated Voltage
REF_SEL	Reference Input Selection	0	0 = XTAL_IN Reference 1 = CLK_IN, nCLK_IN

Table 5P. Programming Selection Control Register Bit Allocation

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PIN_OVERRIDE

Table 5Q. Programming Selection Control Register Function Description

Bits	Name	Factory Default	Function
PIN_OVERRIDE	Programming Source Selection	0	0 = Programming from Pins (Default) 1 = Programming from I^2C Bits

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	 -0.5V to 3.6V -0.5V to 3.6V
Outputs, V_O (LVCMOS)	-0.5V to 3.6V
Outputs, I_O (FORMAT #1) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (FORMAT #2) Continuous Current Surge Current	 50mA 100mA
Maximum Junction Temperature, t_{JMAX}	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

DC Electrical Characteristics

Table 6A. Power Supply DC Characteristics, V_{DD_x} = 3.3V±5%, T_A = -40°C to +85°C, V_{SS_x} = 0V[1 2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_x}	Core Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Total Supply Current for V_{DD_x}	FORMAT #1: All Outputs Enabled & Terminated		780	870	mA
		FORMAT #2: All Outputs Enabled & Terminated		710	785	mA
		FORMAT #1: All Outputs Disabled & not Terminated		390	450	mA
		FORMAT #2: All Outputs Disabled & not Terminated		390	435	mA
I_{DD_CLK}	Supply Current per Output	FORMAT #1: Output Enabled & Terminated		39		mA
		FORMAT #2: Output Enabled & Terminated		32		mA
I_{SS_x}	Power Supply Current for V_{SS_x}	FORMAT #1: Output Enabled & Terminated		445	565	mA
		FORMAT #2: Output Enabled & Terminated		710	785	mA

NOTE 1. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 2. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

Table 6B. LVCMOS DC Characteristics, V_{DD_x} = 3.3V±5%, T_A = -40°C to +85°C, V_{SS_x} = 0V[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		3.3	V
V_{IL}	Input Low Voltage			-0.3		0.63	V
I_{IH}	Input High Current	SCLK, N0, N1 SDATA	$V_{DD\_x} = V_{IN}$ = 3.465V			5	µA
		FB_SEL, REF_SEL, OUTPUT TYPE	$V_{DD\_x} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	SCLK, SDATA N0, N1	V_{DD_x}= 3.465V, V_{IN} = 0V	-150			µA
		FB_SEL, REF_SEL, OUTPUT TYPE	V_{DD_x} = 3.465V, V_{IN} = 0V	-5			µA
V_{OL}	Output Low Voltage	SDATA	I_{OL} = 4mA			0.45	V

NOTE 1. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 2. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

Table 6C. Differential Input DC Characteristics, V_{DD_x} = 3.3V±5%, T_A = -40°C to +85°C. V_{SS_x} = 0V[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK_IN, nCLK_IN	$V_{DD\_x} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_IN	V_{DD_x} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK_IN	V_{DD_x} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage[3, 4]	CLK_IN, nCLK_IN		0.2		1.4	V
V_{CMR}	Common Mode Input Voltage[3, 4]	CLK_IN, nCLK_IN		V_{SS_x} + 1.1		V_{DD_x} – 0.3	V

NOTE 1. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 2. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

NOTE 3. Common mode voltage is defined as the cross point.

NOTE 4. Input voltage cannot be less than V_{SS_x} - 300mV or more than V_{DD_x}.

Table 6D. FORMAT #1 DC Characteristics (QCLKn), V_{DD_x} = 3.3V±5%, V_{SS_x} = 0V, T_A = -40°C to +85°C, V_{SS_x} = 0V[1 2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[3]		V_{DD_x} – 1.2		V_{DD_x} – 0.65	V
V_{OL}	Output Low Voltage[3]		V_{DD_x} – 1.8		V_{DD_x} – 1.15	V
V_{SWING}	Single-ended Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 2. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

NOTE 3. Outputs terminated with 50Ω to V_{DD_x} – 2V.

Table 6E. FORMAT #2 DC Characteristics (QCLKn), V_{DD_x} = 3.3V±5%, V_{SS_x} = 0V, T_A = -40°C to +85°C, V_{SS_x} = 0V[1 2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[3 4]		V_{DD_x} – 1.2		V_{DD_x} – 0.65	V
V_{OL}	Output Low Voltage[3 4]		V_{DD_x} – 1.8		V_{DD_x} – 1.15	V
V_{SWING}	Single-ended Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 2. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

NOTE 3. No external DC pulldown resistor.

NOTE 4. Loading condition is with 100Ω across the differential output.

AC Electrical Characteristics

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Table 7A. AC Characteristics, V_{DD_x} = 3.3V+5%, T_A = -40°C to +85°C, V_{SS_x} = 0V[1 2 3]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency		8T49NS010-156	2400		2500	MHz
f_{OUT}	Output Frequency	QCLK[0:9], nQCLK[0:9]		100		2500	MHz
*t*sk(o)	Output Skew[4 5]	QCLK[0:9], nQCLK[0:9]	Same Frequency and Output Type		25	55	ps
t_R / t_F	Output Rise/Fall Time	QCLK[0:9] nQCLK[0:9]	30% to 70%		65	130	ps
odc	Output Duty Cycle	QCLK[0:9], nQCLK[0:9]	f_{OUT} = 156.25, 312.5, 625 & 1250MHz	45		55	%
t_{LOCK}	PLL Lock Time[6]				150		ms

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL}, V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 3. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

NOTE 4. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6. PLL Lock Time is defined as time from input clock availability to phase locked output. The following loop filter component values may be used: R_Z = 208Ω, C_Z = 4.7µF C_P = 30pf. Refer to *Applications Information*.

Table 7B. QCLK[0:9] Phase Noise and Jitter Characteristics, V_{DD_x} = 3.3V+5%, T_A = -40°C to +85°C[1 2 3 4 5 6 7 8 9]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tjit(Ø)	RMS Phase Jitter Random; QCLKn = 156.25MHz	Integration Range: 12kHz – 20MHz		84	128	fs
	RMS Phase Jitter Random; QCLKn = 312.5MHz	Integration Range: 12kHz – 20MHz		66	98	fs
Φ_N(10)	Single-Side Band Noise Power, 10Hz from Carrier	QCLKn = 156.25MHz		-77		dBc/Hz
Φ_N(100)	Single-Side Band Noise Power, 100Hz from Carrier	QCLKn = 156.25MHz		-107		dBc/Hz
Φ_N(1k)	Single-Side Band Noise Power, 1kHz from Carrier	QCLKn = 156.25MHz		-124		dBc/Hz
Φ_N(10k)	Single-Side Band Noise Power, 10kHz from Carrier	QCLKn = 156.25MHz		-136		dBc/Hz
Φ_N(100k)	Single-Side Band Noise Power, 100kHz from Carrier	QCLKn = 156.25MHz		-144		dBc/Hz
Φ_N(1M)	Single-Side Band Noise Power, 1MHz from Carrier	QCLKn = 156.25MHz		-156		dBc/Hz
Φ_N(10M)	Single-Side Band Noise Power, 10MHz from Carrier	QCLKn = 156.25MHz		-160		dBc/Hz
Φ_N(∝)	Noise Floor (≥30MHz from Carrier)	QCLKn = 156.25MHz		-161		dBc/Hz
Φ_N(10)	Single-Side Band Noise Power, 10Hz from Carrier	QCLKn = 312.5MHz		-67		dBc/Hz
Φ_N(100)	Single-Side Band Noise Power, 100Hz from Carrier	QCLKn = 312.5MHz		-98		dBc/Hz
Φ_N(1k)	Single-Side Band Noise Power, 1kHz from Carrier	QCLKn = 312.5MHz		-118		dBc/Hz
Φ_N(10k)	Single-Side Band Noise Power, 10kHz from Carrier	QCLKn = 312.5MHz		-130		dBc/Hz
Φ_N(100k)	Single-Side Band Noise Power, 100kHz from Carrier	QCLKn = 312.5MHz		-138		dBc/Hz
Φ_N(1M)	Single-Side Band Noise Power, 1MHz from Carrier	QCLKn = 312.5MHz		-151		dBc/Hz
Φ_N(10M)	Single-Side Band Noise Power, 10MHz from Carrier	QCLKn = 312.5MHz		-159		dBc/Hz
Φ_N(∝)	Noise Floor (≥30MHz from Carrier)	QCLKn = 312.5MHz		-160		dBc/Hz

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Characterized using (FX325BS) 50MHz, CL = 12pF crystal.

NOTE 3. V_{DD_x} denotes V_{DD_CLK}, V_{DD_CP}, $V_{DD\_LC\_IN}$, V_{DD_I2C}, V_{DD_XTAL} V_{DD_FB}, V_{DD_A}, V_{DD_A2}.

NOTE 4. V_{SS_x} denotes V_{SS_CP}, V_{SS_I2C}, V_{SS_FB}, V_{SS_A2}, V_{EE_A}, V_{SS_XTAL}, V_{EE_EP}.

NOTE 5. Measured on QCLKn configured as ÷16 and ÷8.

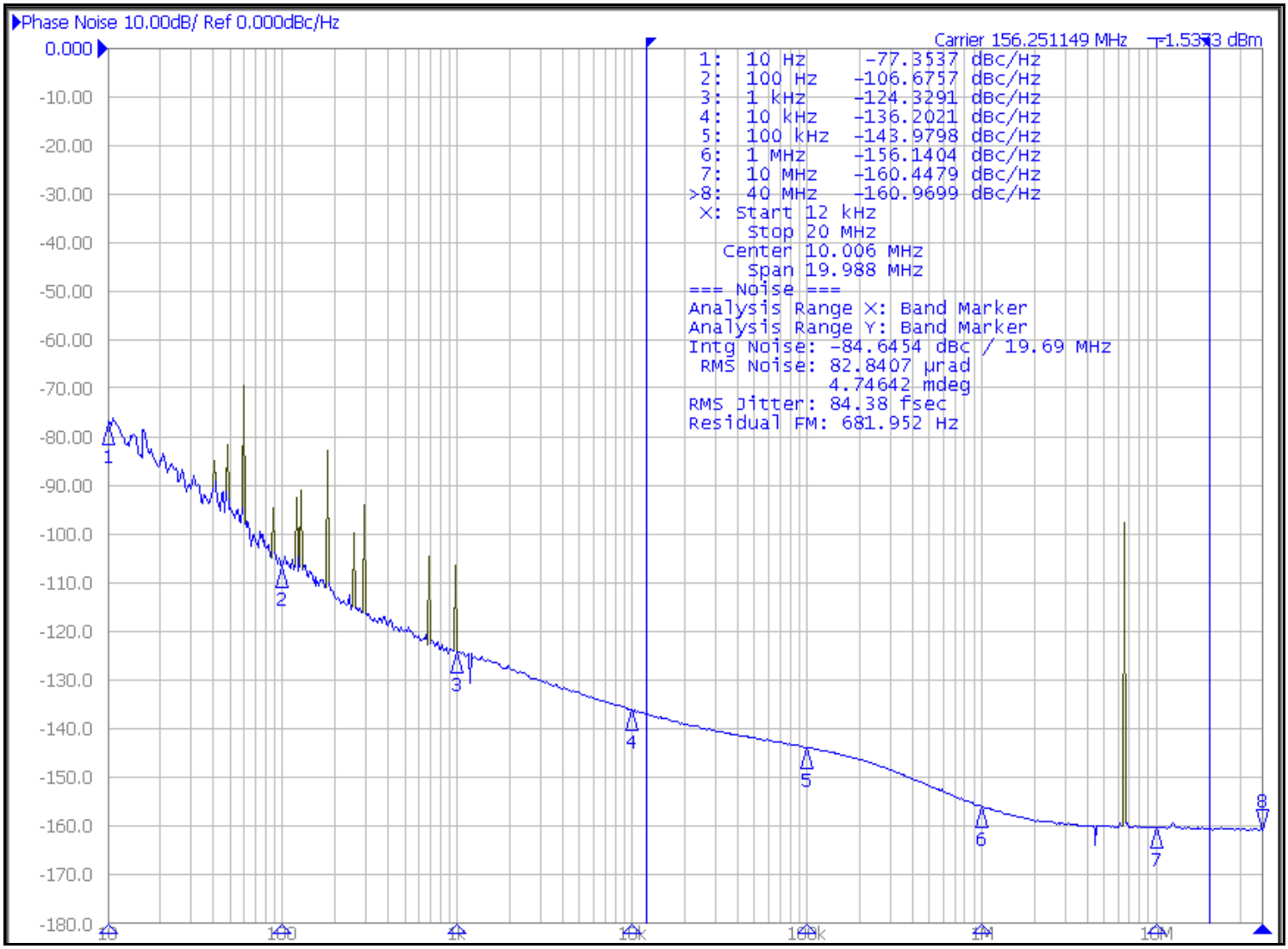
NOTE 6. Phase noise and spurious specifications apply for device operation with QCLKn outputs active.

NOTE 7. V_{DD_A} requires a voltage regulator. Voltage supplied to V_{DD_A} should be derived from a regulator with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/√Hz at 10kHz and 7nV/√Hz at 1kHz.

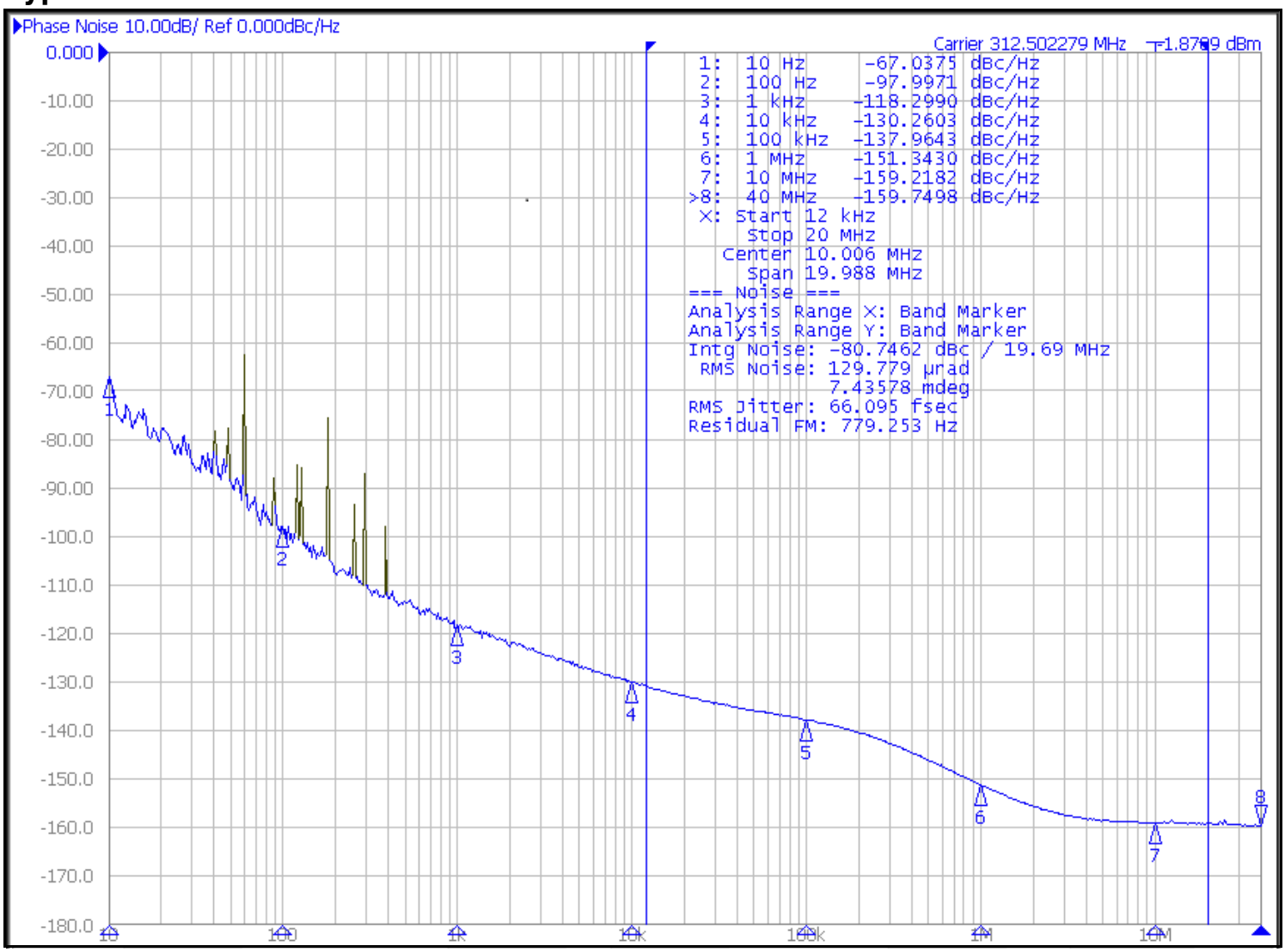
NOTE 8. The following loop filter component values may be used: R_Z = 208Ω, C_Z = 4.7µF CP = 30pF. See *Figure 5*.

NOTE 9. The phase noise was measured up to 40MHz offset and assumed the noise floor remains same until 61.44MHz offset.

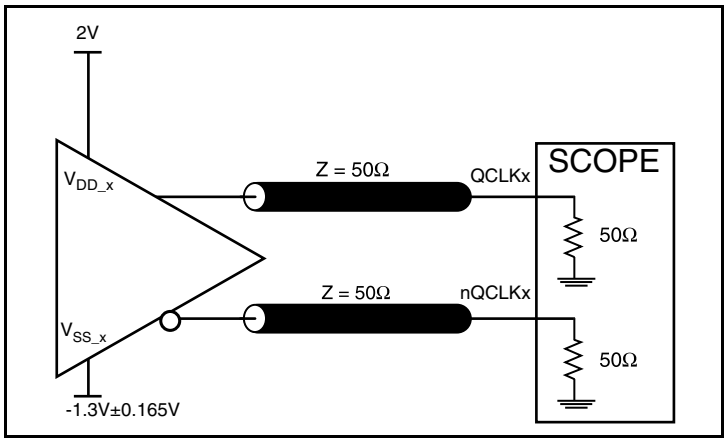
Typical Phase Noise at 156.25MHz



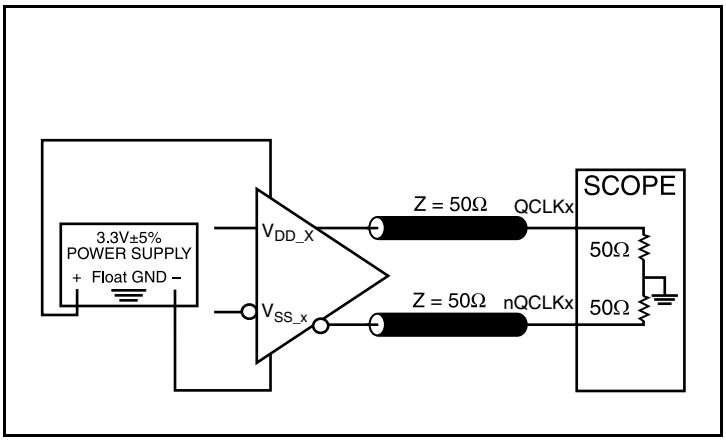
Typical Phase Noise at 312.5MHz



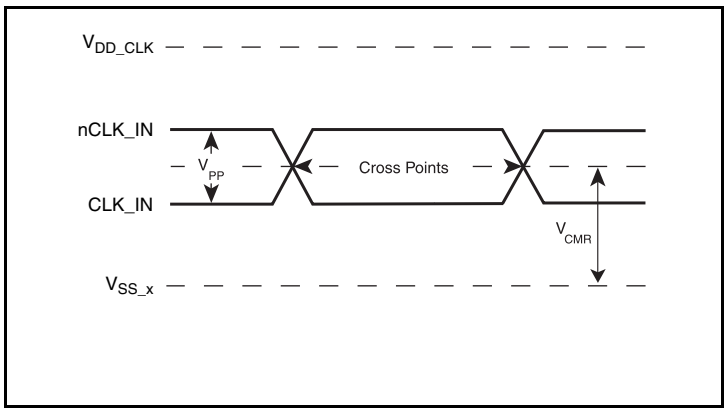
Parameter Measurement Information



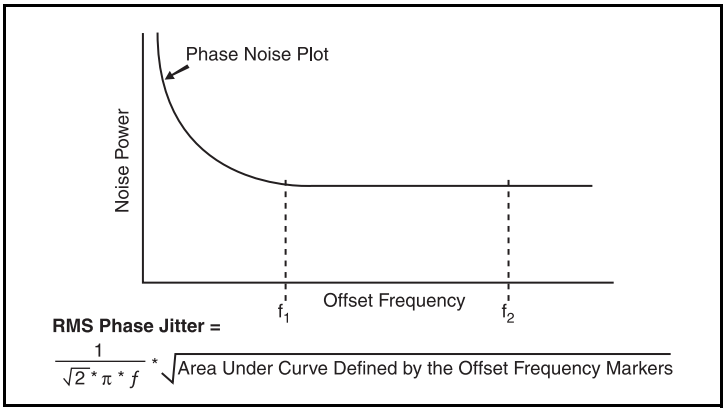
3.3V FORMAT #1 Output Load Test Circuit



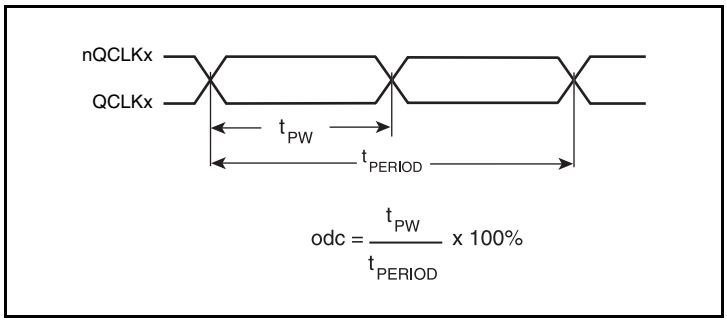
3.3V FORMAT #2 Output Load Test Circuit



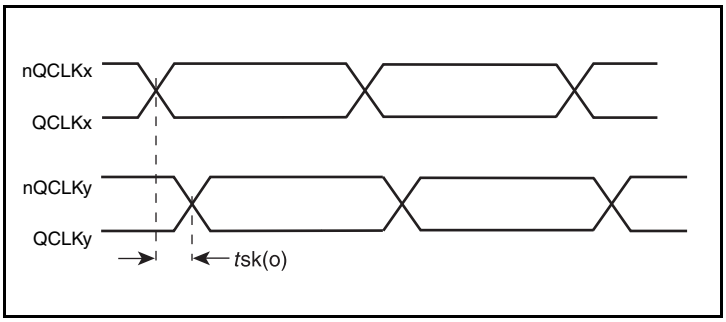
Differential Input Levels



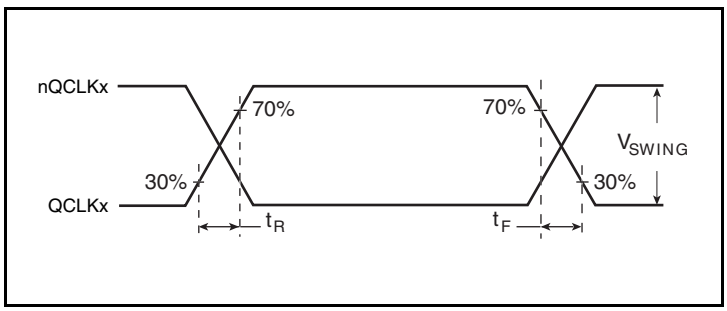
RMS Phase Jitter



Differential Output Duty Cycle



Differential Output Skew



Differential Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

FORMAT #1 Outputs

All unused FORMAT #1 outputs should be left floating. It is recommended that there is no trace attached.

FORMAT #2 Outputs

All unused FORMAT #2 output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

3.3V Differential Clock Input Interface

The CLK_IN /nCLK_IN accepts LVDS, LVPECL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 1A to Figure 1C* show interface examples for the CLK_IN/nCLK_IN input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 1A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

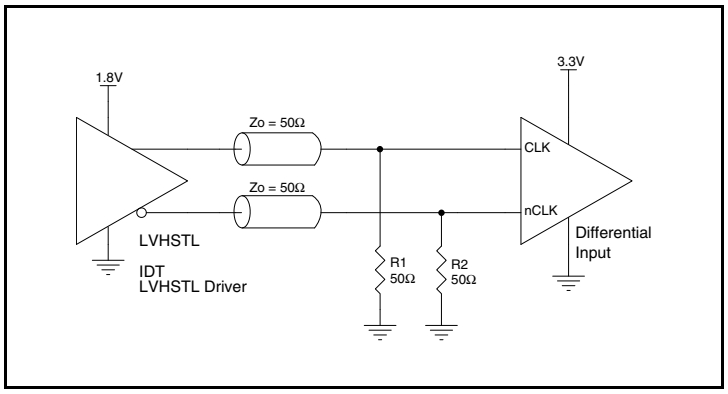


Figure 1A. CLK_IN/nCLK_IN Input Driven by a 3.3V LVPECL Driver

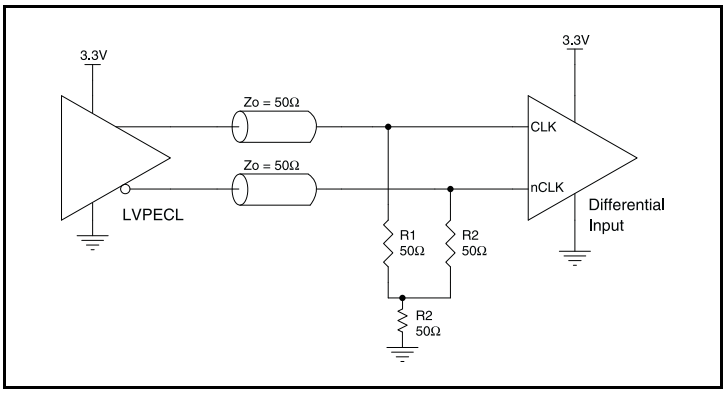


Figure 1C. CLK_IN/nCLK_IN Input Driven by a 3.3V LVPECL Driver

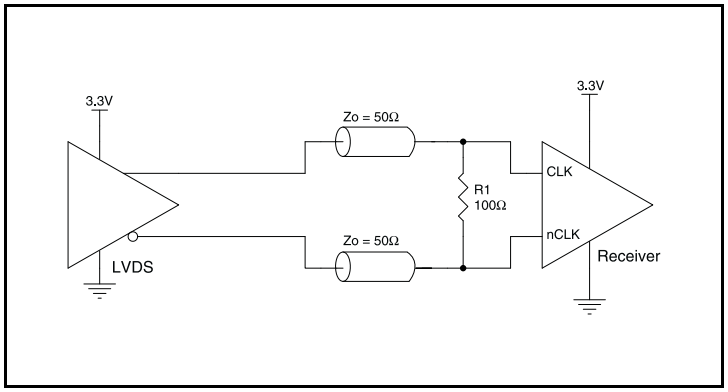


Figure 1B. CLK_IN/nCLK_IN Input Driven by a 3.3V LVDS Driver

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

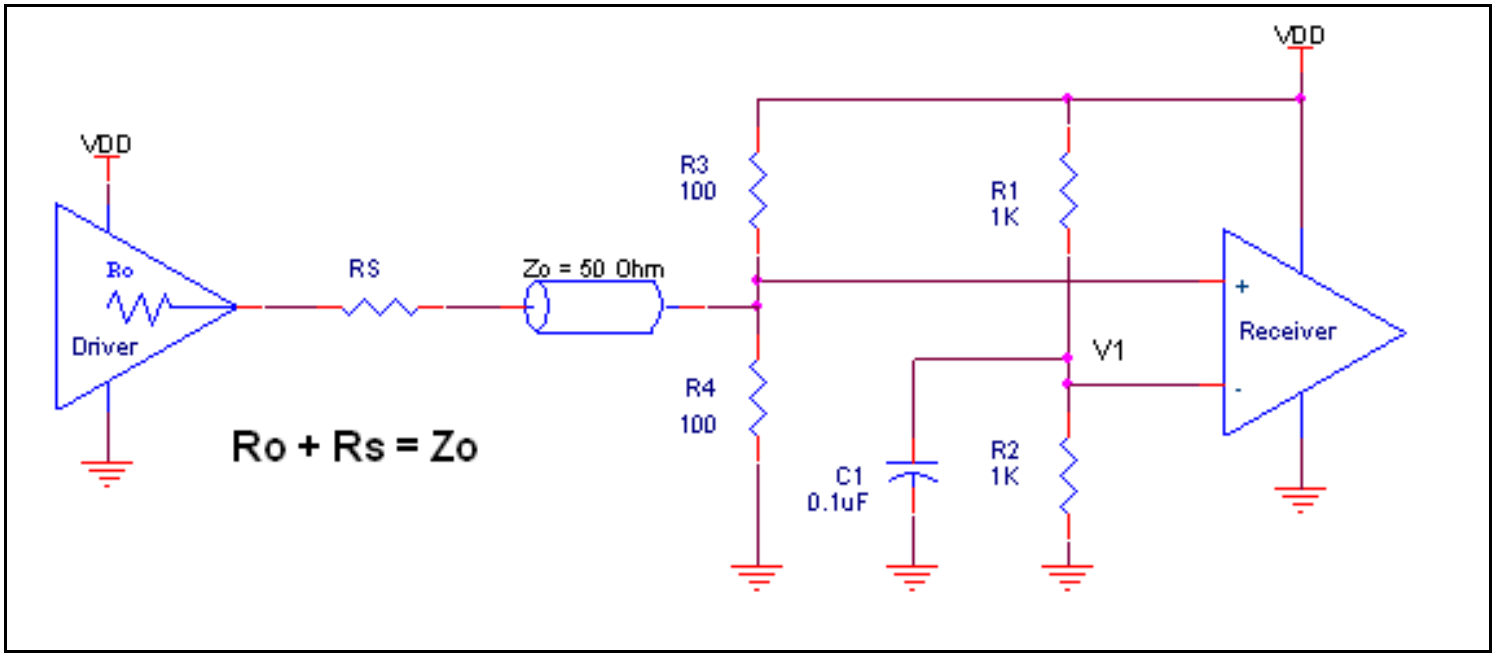


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Termination for QCLKn Outputs

FORMAT #2:
The recommended value for the termination impedance (ZT) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z0) of your transmission line. A typical point-to-point design using the QCLKn Output format uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. This output format has a voltage source output structure. The termination schematic as shown in *Figure 3A* can be used. *Figure 3B* is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output. Refer to *Figure 3E and Figure 3F* for more details about the termination schemes.

If using a non-standard termination, it is recommended to contact IDT and confirm if the output termination is adequate.

FORMAT #1:
The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential output is a low impedance follower output that generates ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 3C and Figure 3D* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

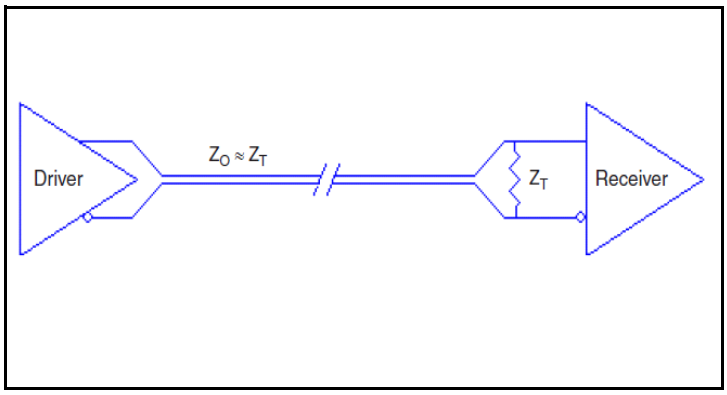


Figure 3A. FORMAT #2 Standard Termination

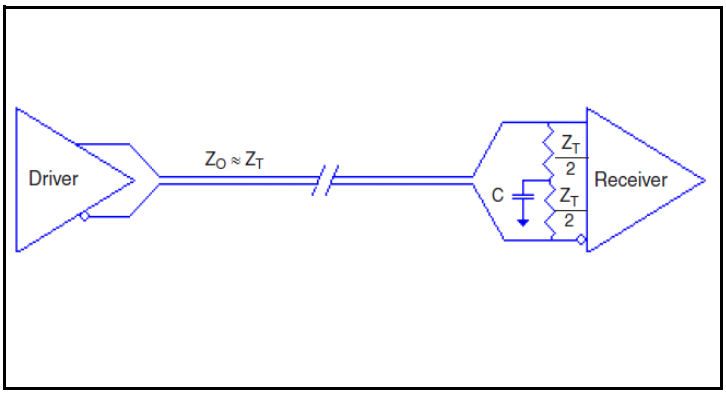


Figure 3B. FORMAT #2 Optional Termination

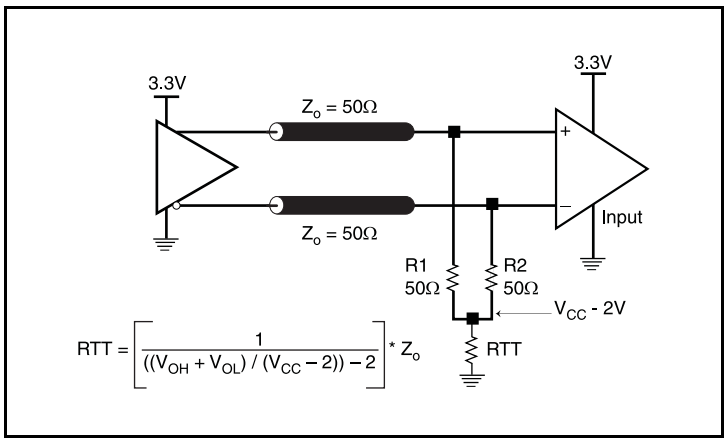


Figure 3C. 3.3V FORMAT #1 Output Termination

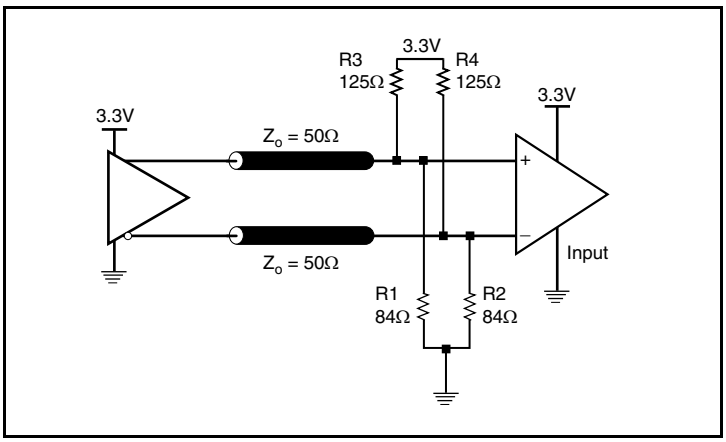


Figure 3D. 3.3V FORMAT #1 Output Termination

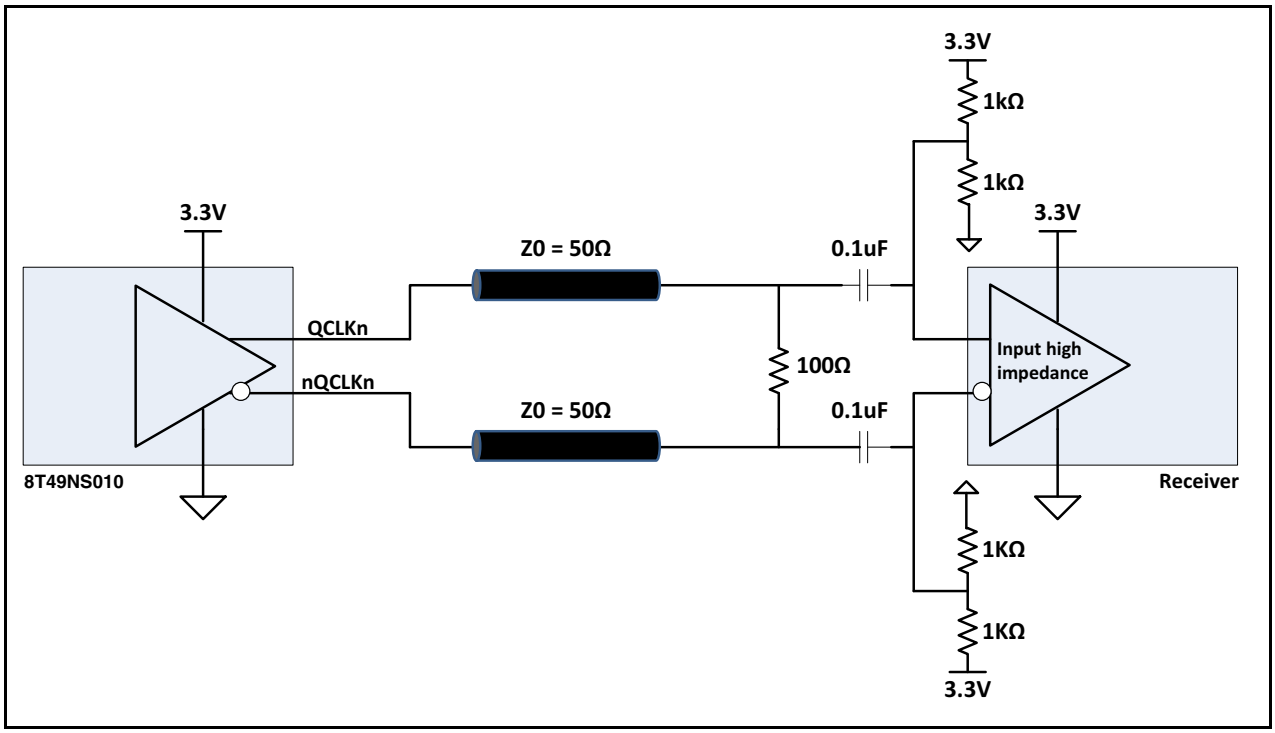


Figure 3E. AC Termination for FORMAT #2

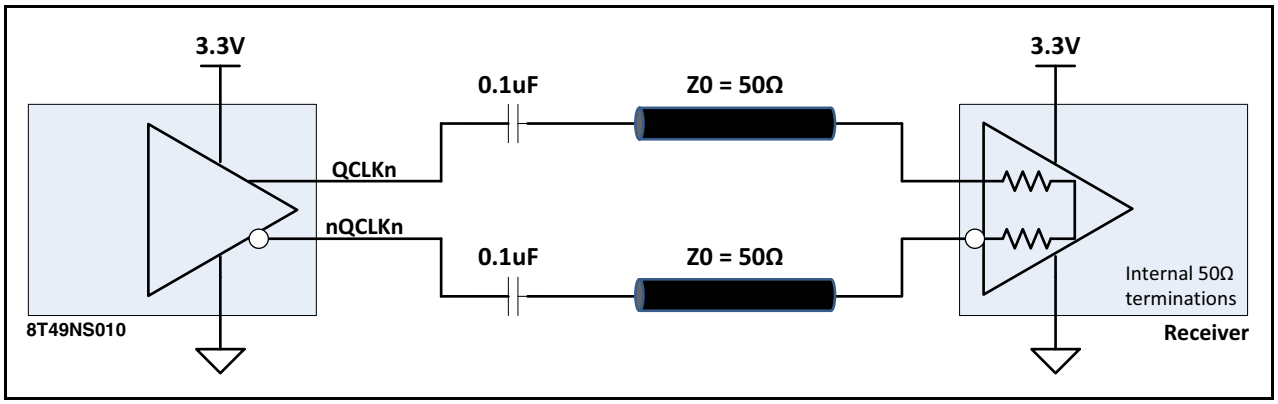


Figure 3F. AC Termination for FORMAT #2 used with an Input Clock Receiver with Internal 50Ω Terminations.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

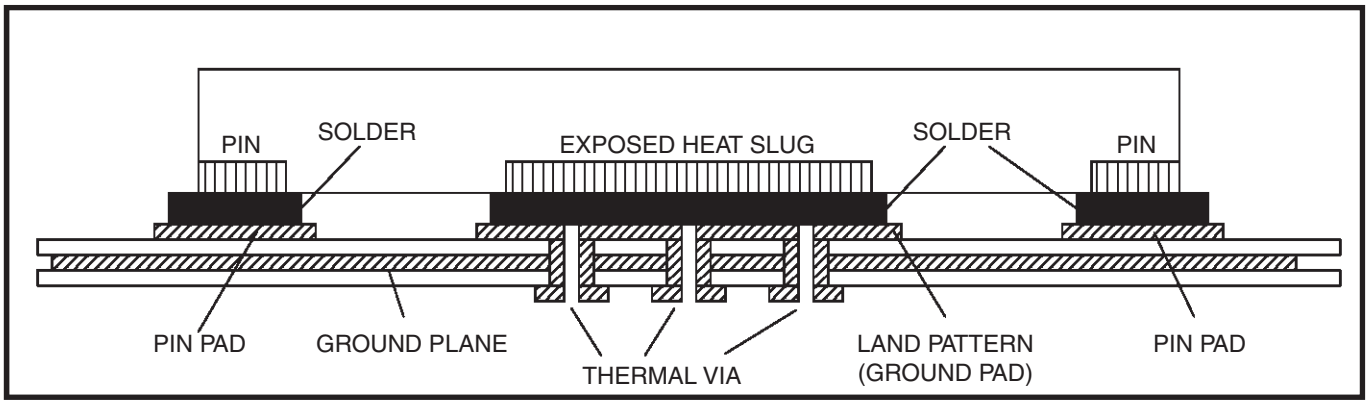


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 5 shows an example 8T49NS010 application schematic operating the device at V_{DD} = 3.3V. This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

To demonstrate the range of output stage configurations possible, the application schematic assumes that the 8T49NS010 is programmed over I^2C. Specifically the QCLK0 and QCLK9 outputs are configured by PWD_EF_QCLK0 and PWD_EF_QCLK9 respectively for an LVDS like output with internal biasing. On the other hand, the QCLK4 is configured by PWD_EF_QCLK4 for the reduced swing LVPECL output. For alternative DC coupled LVPECL options please see IDT AN-828; for AC coupling options use IDT AN-844.

The 12pF parallel resonant Fox FX325BS 50MHz crystal is used with tuning capacitors C1 = C2 = 2pF recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal tuning capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal-oscillator loop if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8T49NS010. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8T49NS010 as possible as shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8T49NS010 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 10Ω V_{DDA} resistor and the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull up and pull down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

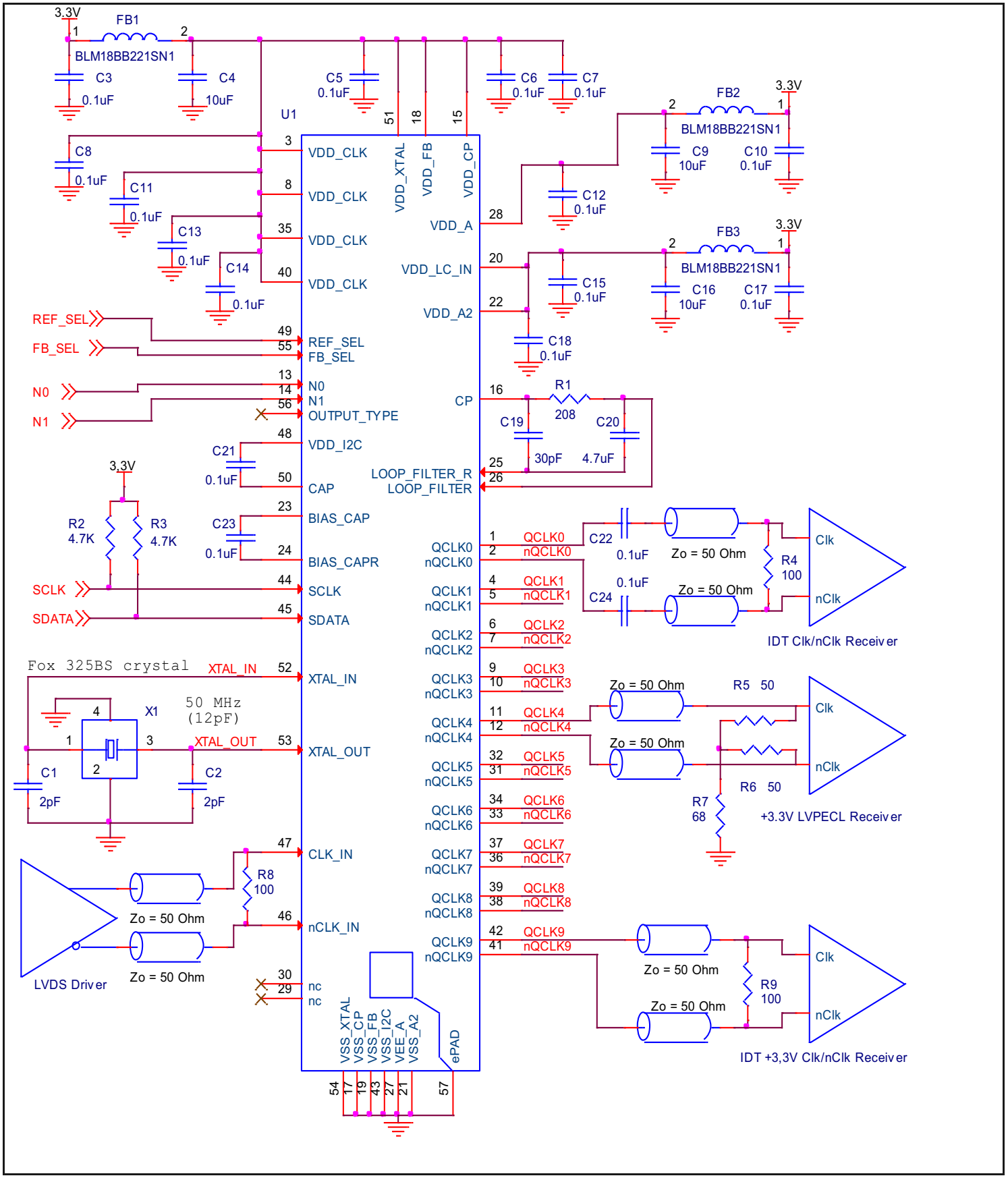


Figure 5. 8T49NS010 Application Schematic

Loop Filter Calculation

2nd Order Loop Filter

This section helps design a 2nd order loop filter for 8T49NS010. A general 2nd order loop filter is shown in *Figure 6.* Below will show step by step calculation to determine Rz, Cz and Cp values for desire loop bandwidth. The required parameters are also provided. A spread sheet for calculating the loop filter values is also available.

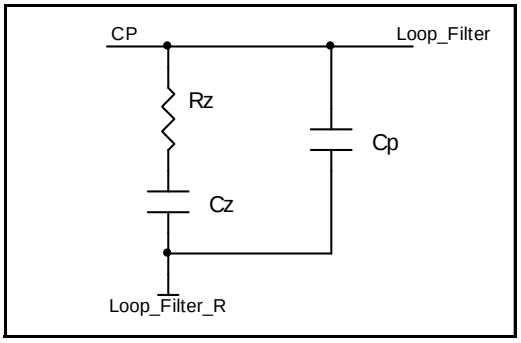


Figure 6. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth fc.
2. Calculate Rz:

$$Rz = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Where,

Icp is charge pump current. For this part, the charge pump current can be programmed to I_{CP} = 1.4mA, 2.8mA, 4.2mA, or 5.6mA.

K_{VCO} is VCO gain. For this part, K_{VCO} = 29MHz/V.

N is effective feedback divider. N must be programmed into the following value.

$$N = \frac{Fvco}{Fpd}$$

F_{VCO} is VCO frequency. For this part, F_{VCO} = 2500MHz.

fpd is phase detector input frequency.

$$fpd = \frac{F\_ref}{Pv}$$

F_ref is Reference CLK_IN input frequency

Pv is pre-divider setting, user can program Pv to 1, 2, 4, x2

3. Calculate Cz:

$$Cz = \frac{\alpha}{2 * \pi * fc * Rz}$$

Where, α = fc/ fz, user can determine an α number. It is recommend α > 6.

fz is frequency at zero

4. Calculate Cp:

$$Cp = \frac{Cz}{\alpha * \beta}$$

Where

β = fp/fc, user can determine β number. It is recommend $\beta > 4$

fp is frequency at pole

5. Verify maximum Phase Margin, PMmax

$$PM\ \max = \arctan(\frac{b-1}{2*\sqrt{b}})$$

Where,

$$b = 1 + \frac{Cz}{Cp}$$

The maximum phase margin, PMmax, should be greater than 50°.

A spread sheet for calculating the loop filter component values is provided. To use the spread sheet, user simply enters the following parameters:

fc, F_ref, PV, Icp, F_{VCO}, α and β.

The spread sheet will provide the component values, Rz, Cz and Cp as result. The spread also calculate maximum phase noise margin for verification.

3rd Order Loop Filter

This section helps design a 3rd order loop filter for IDT8T49NS010. A general 3rd order loop filter is shown in *Figure 7*

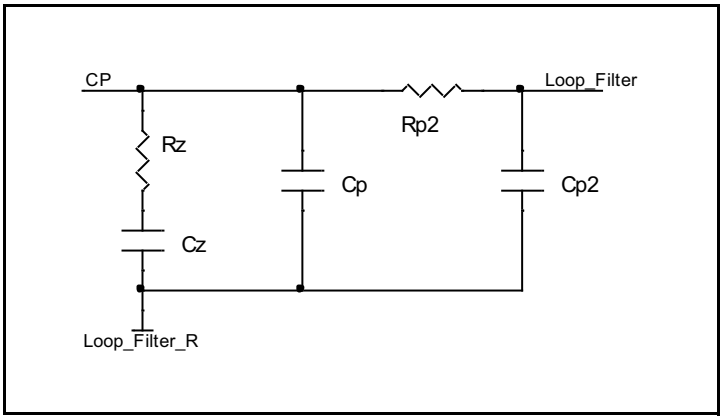


Figure 7. Typical 3rd Order Loop Filter

The Rz, Cz and Cp can be calculated as 2nd order loop filter. The following equation help determine the 3rd order loop filter Rp2 and Cp2

Pick an Rp2 value. Suggest Rp2 ~ 1.5xRz. calculate Cp2 as follows:

$$Cp2 = \frac{Rz * Cp}{Rp2 * \gamma}$$

Where γ is ratio between the 1st pole frequency and the 2nd pole frequency. Suggest γ=10.

Power Considerations

The 8T49NS010 device was designed and characterized to operate within the ambient extended temperature range of -40°C to 85°C.The ambient temperature represents the temperature around the device, not the junction temperature. When using this device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding the 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage with all outputs enabled and terminated. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Equations and example calculations are also provided below.

Power Dissipation

1. FORMAT #1 Output Style.

The power dissipation for the 8T49NS010 is the product of supply voltage and total I_{DD} (for FORMAT #1 output style).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V at ambient temperature of 85°C.

Maximum current at 85°C, I_{DD_MAX} = 870mA

- Total Power Dissipation: $P_D = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 870mA = **3002.64mW**

Junction Temperature.

Junction temperature, T_J, signifies the hottest point on the device and exceeding the specified limit could cause device reliability issues. The maximum recommended junction temperature is 125°C.

For devices like this and in systems where most heat escapes from the bottom exposed pad of the package, θ_{JB} is the primary thermal resistance of interest.

The equation to calculate T_J using θ_{JB} is: $T_J = \theta_{JB} * P_D + T_B$

T_J = Junction Temperature

θ_{JB} = Junction-to-Board Thermal Resistance

P_D = Device Power Dissipation (example calculation is in section 1 above)

T_B = Board Temperature

In order to calculate junction temperature, the appropriate junction-to-board thermal resistance θ_{JB} must be used. Assuming a 2-ground plane board, the appropriate value of θ_{JB} is 0.707°C/W per *Table 8*.

Therefore, T_J for a PCB maintained at 100°C with the outputs switching is:

100°C + 3.0W * 0.707°C/W = 102.12°C which is below the limit of 125°C.

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, heat transfer method, the type of board (multi-layer) and the actual maintained board temperature. *Table 8* is for two ground planes. The thermal resistance will change as the number of layers in the board changes or if the board size change and other changes in other factors impacts heat dissipation in the system.

2. FORMAT #2 Output Style

The power dissipation for the 8T49NS010 is the product of supply voltage and total I_{DD} (for FORMAT #2 output style).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V at ambient temperature of 85°C.

Maximum current at 85°C, I_{DD_MAX} = 725mA

- Total Power Dissipation: $P_D = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 725mA = **2509.17mW**

Junction Temperature.

Junction temperature, T_J, signifies the hottest point on the device and exceeding the specified limit could cause device reliability issues. The maximum recommended junction temperature is 125°C.

For devices like this and in systems where most heat escapes from the bottom exposed pad of the package, θ_{JB} is the primary thermal resistance of interest.

The equation to calculate T_J using θ_{JB} is: $T_J = \theta_{JB} * P_D + T_B$

Tj = Junction Temperature

θ_{JB} = Junction-to-Board Thermal Resistance

P_D = Device Power Dissipation (example calculation is in section 1 above)

T_B = Board Temperature

In order to calculate junction temperature, the appropriate junction-to-board thermal resistance θ_{JB} must be used. Assuming a 2-ground plane board, the appropriate value of θ_{JB} is 0.707°C/W per *Table 8* below.

Therefore, Tj for a PCB maintained at 100°C with the outputs switching is:

100°C + 2.51W * 0.707°C/W = 101.8°C which is below the limit of 125°C.

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, heat transfer method, the type of board (multi-layer) and the actual maintained board temperature. *Table 8* is for two ground planes. The thermal resistance will change as the number of layers in the board changes or if the board size change and other changes in other factors impacts heat dissipation in the system.

Table 8. Thermal Resistances for 56-Lead VFQFN Package[1 2 3]

Air Flow (m/s)	0	1	2
θ_{JB}	0.707°C/W	0.707°C/W	0.707°C/W
θ_{JA}	17.02°C/W	13.75°C/W	12.57°C/W

NOTE 1.Applicable to PCB's with 2-ground planes.

NOTE 2.ePAD size is 6.05mm x 6.05mm and connected to ground plane in PCB through 8 x 8 Thermal Via Array.

NOTE 3.θ_{JB} is applicable to use for junction temperature calculations in board designs where the majority of the heat dissipated through the device is the through the ePad and into the subsequent ground layer(s) within the PCB.

Reliability Information

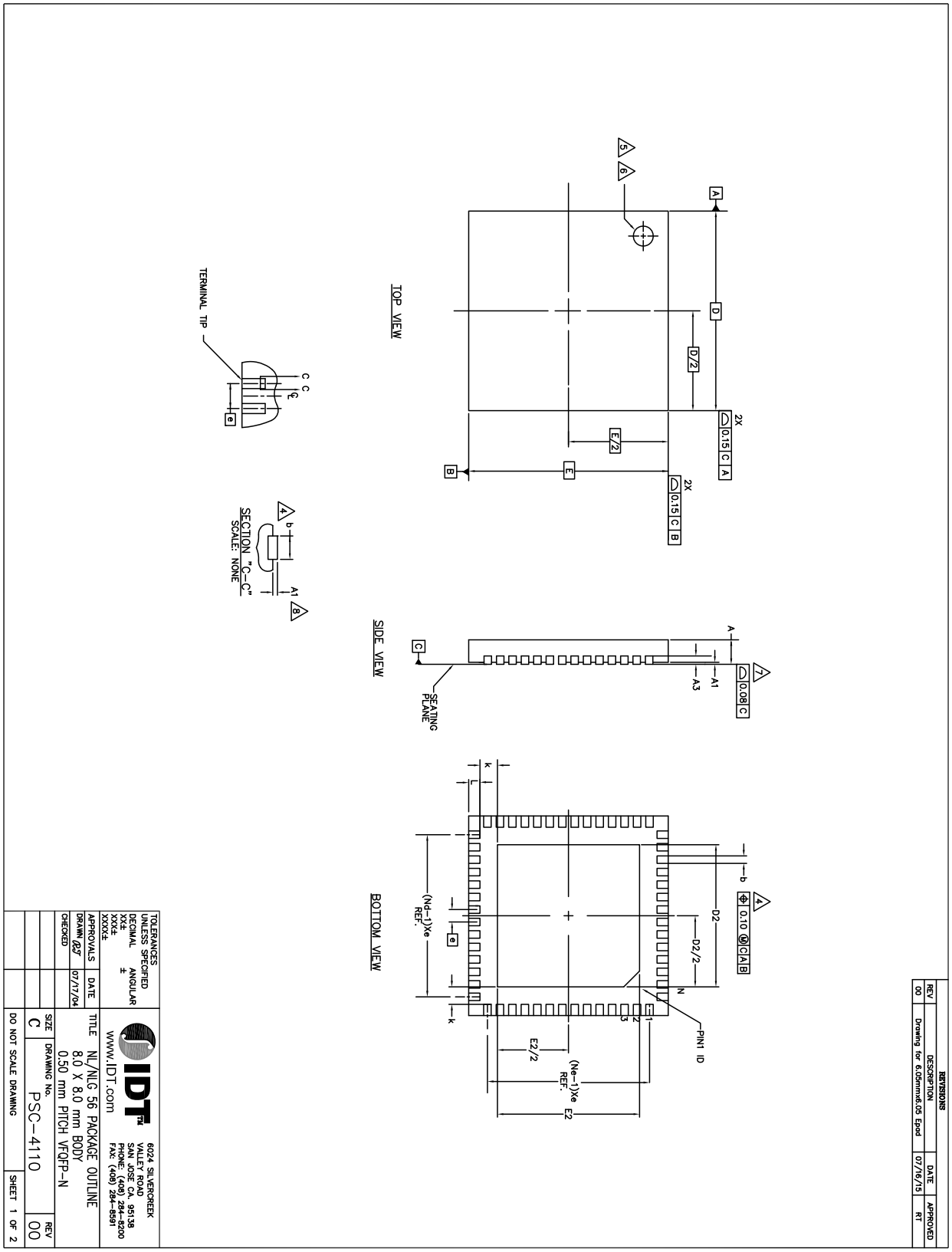
Table 9. Thermal Resistance vs. Air Flow Table for a 56-pin VFQFN

Air Flow (m/s)	0	1	2
θ_{JB}	0.707°C/W	0.707°C/W	0.707°C/W
θ_{JA}	17.02°C/W	13.75°C/W	12.57°C/W

Transistor Count

The transistor count for the 8T49NS010 is: 28,480

56-pin VFQFN Package Outline



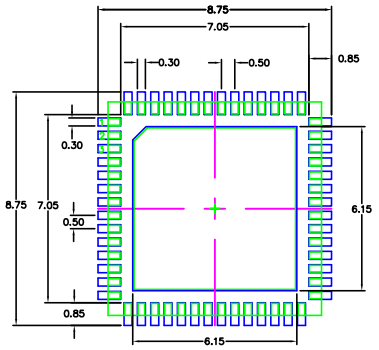
56-pin VFQFN Package Outline, Continued

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	Drawing for 6.05mmx6.05 Epad	07/16/15	RT

SYMBOL	DIMENSION			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		56		2
Nd		14		2
Ne		14		2
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	4
D2	5.95	6.05	6.15	
E2	5.95	6.05	6.15	
A	0.80	0.9	1.00	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
D		8.00 BSC		
E		8.00 BSC		
k	0.20	–	–	

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.

LAND PATTERN RECOMMENDATION



EPAD 6.05 mm SQ

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 SILVERCREEK VALLEY ROAD SAN JOSE CA. 95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
APPROVALS	DATE	TITLE	NL/NLG 56 PACKAGE OUTLINE 8.0 X 8.0 mm BODY 0.50 mm PITCH VFQFP–N
DRAWN RT	07/17/14		
CHECKED			
		SIZE C	DRAWING No. PSC–4110 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49NS010-156NLGI	IDT8T49NS010-156NLGI	56-pin VFQFN, Lead-Free	Tray	-40°C to +85°C
8T49NS010-156NLGI8	IDT8T49NS010-156NLGI	56-pin VFQFN, Lead-Free	Tape & Reel	-40°C to +85°C

NOTE: Parts that are ordered with a “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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