

Description

The 8V19N880 is a fully integrated FemtoClock® NG jitter attenuator and clock synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, LTE-A, and 5G radio board implementations. The device supports JESD204B (subclass 0 and 1) and JESD204C.

The 8V19N880 has a two-stage PLL architecture that supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the PLL-0 output signal and synthesizes the target frequency. The second stage PLL can use the internal or an external high-frequency VCO.

The 8V19N880 supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for additional flexibility.

The 8V19N880 is configured through a 3/4-wire SPI interface and reports lock and signal loss status in internal registers and via the GPIO[1:0] outputs. Internal status bit changes can also be reported via a GPIO output. The device is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The 8V19N880 is a member of the high-performance clock family from IDT.

Typical Applications

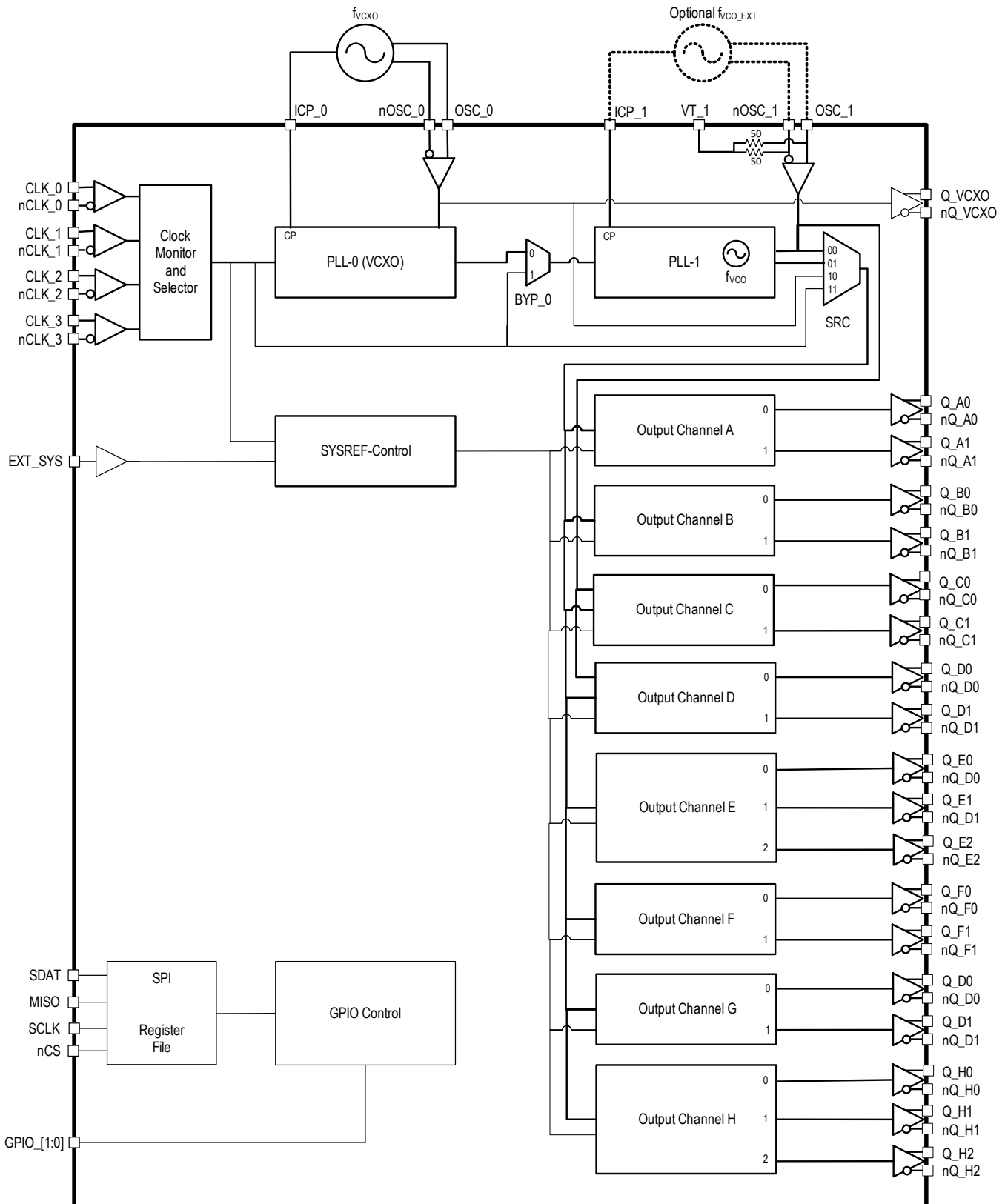
- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A, and 5G
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

Features

- High-performance clock RF-PLL with support for JESD204B/C
- Optimized for low phase noise: -150dBc/Hz (800kHz offset; 245.76MHz clock)
- Integrated phase noise of $< 80\text{fs RMS}$ typical (12k–20MHz)
- Dual-PLL architecture with optional external VCO
- 1st-PLL stage with external VCXO for clock jitter attenuation
- 2nd-PLL with internal FemtoClockNG PLL: 3932.16MHz
 - Optional external VCO frequency range: 700MHz–6GHz
- Nine output channels with a total of 19 outputs, organized in:
 - Two RF clock channels each consisting of two device clocks ($\leq 4\text{GHz}$)/SYSREF outputs; each output can buffer external VCO clocks up to 6GHz
 - Six device clock/SYSREF channels (2 or 3 outputs, $\leq 4\text{GHz}$)
 - One VCXO-PLL (PLL-0) output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include:
 - From internal VCO: 3932.16, 1966.08, 983.04, 491.52, and 245.76MHz
 - From external VCO: $\leq 6\text{GHz}$
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling, and LVPECL, LVDS line terminations techniques
- Phase delay circuits
 - PLL feedback phase delay for output-to-input alignment
 - Channel phase delay with 512 steps of 127ps
 - Individual output phase delay with four steps of 127ps and additional four steps of 32ps delay for clock/SYSREF alignment
- Redundant input clock architecture with four inputs and
 - Input activity monitoring
 - Manual and automatic, fault-triggered clock selection modes
 - Priority-controlled clock selection
 - Digital holdover and hitless switching
 - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B/C
- SPI 3/4 wire configuration interface
- Supply voltage: 1.8V (core, output) and 3.3V (oscillator interfaces, 6GHz output supply)
- SPI and control I/O voltage: 1.8V
- Package: 100-CABGA (11x11 mm²)
- Temperature range: -40°C to $+95^{\circ}\text{C}$ (case)

Block Diagram

Figure 1. Block Diagram ($f_{VCO} = 3932.16\text{MHz}$)





Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as "IDT") reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary. Integrated Device Technology, Inc. All rights reserved.