

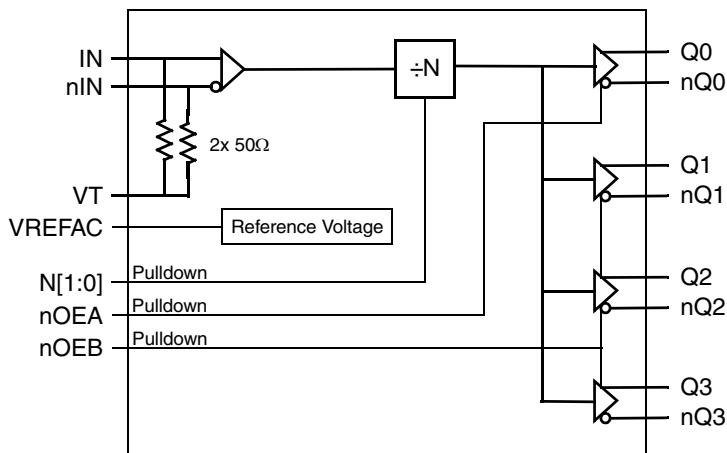
### General Description

The 8V79S674 is a clock divider and fanout buffer. The device has been designed for clock signal division in wireless base station radio equipment boards. The device is optimized to deliver excellent additive phase jitter performance. The 8V79S674 uses SiGe technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection. The device offers the frequency division by  $\div 1$ ,  $\div 2$ ,  $\div 4$  and  $\div 8$ . Four low-skew LVPECL outputs are available and support clock output frequencies up to 2500MHz ( $\div 1$  frequency division). Outputs can be disabled to save power consumption if not used. The device is packaged in a lead-free (RoHS 6) 20-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

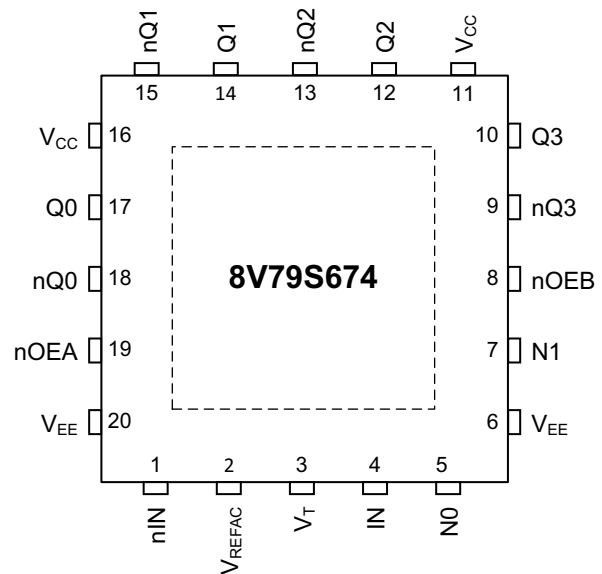
### Features

- Clock signal division and distribution
- SiGe technology for high-frequency and fast signal rise/fall times
- Four low-skew LVPECL clock outputs
- Supports frequency division of  $\div 1$ ,  $\div 2$ ,  $\div 4$  and  $\div 8$
- Maximum frequency: 2500MHz
- Maximum output skew: 50ps (maximum)
- Maximum LVPECL output rise/fall time: 200ps (maximum)
- 3.3V or 2.5V core and output supply mode
- Supports 1.8V I/O logic levels for all control pins
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment



20-pin, 4mm x 4mm VFQFN Package

## Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	nIN	Input		Inverting differential clock signal input. Internal termination 50Ω to V <sub>T</sub> .
2	V <sub>REFAC</sub>	Output		Reference voltage for AC-coupled applications of IN, nIN.
3	V <sub>T</sub>			Leave open if IN, nIN is used with LVDS signals. Connect 50Ω to V <sub>EE</sub> if IN, nIN is used with LVPECL signals.
4	IN	Input		Non-inverting differential clock signal input. Internal termination 50Ω to V <sub>T</sub> .
5, 7	N0, N1	Input	Pulldown	Frequency divider controls. 1.8V LVCMOS/LVTTL interface levels.
6, 20	V <sub>EE</sub>	Power		Negative power supply voltage (ground).
8	nOEB	Input	Pulldown	Output enable control for the Q1, Q2 and Q3 outputs. 1.8V LVCMOS/LVTTL interface levels.
9, 10	nQ3, Q3	Output		Differential clock output pair. LVPECL output levels.
11, 16	V <sub>CC</sub>	Power		Power supply voltage.
12, 13	Q2, nQ2	Output		Differential clock output pair. LVPECL output levels
14, 15	Q1, nQ1	Output		Differential clock output pair. LVPECL output levels
17, 18	Q0, nQ0	Output		Differential clock output pair. LVPECL output levels
19	nOEA	Input	Pulldown	Output enable control for the Q0 output. 1.8V LVCMOS/LVTTL interface levels.
—	V <sub>EE_EP</sub>	Power		Exposed package pad negative supply voltage (ground). Return current path for the Q0, Q1, Q2 and Q3 outputs. This pin must be connected to ground.

NOTE: *Pulldown* refers to an internal input resistor. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			2		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Truth Tables

**Table 3A. Nx Clock Divider Function Table**

Input		Divider Value
N1	N0	
0 (default)	0 (default)	÷1
0	1	÷2
1	0	÷4
1	1	÷8

**Table 3B. nOEA Output Enable Function Table**

Input	Output Operation
nOEA	
0 (default)	Q0 is enabled
1	Q0 is disabled in logic Low state

**Table 3C. nOEB Output Enable Function Table**

Input	Output Operation
nOEB	
0 (default)	Q1, Q2 and Q3 are enabled
1	Q1, Q2 and Q3 are disabled in logic Low state

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Input Current, $I_{IN}$ , $nIN$	$\pm 50mA$
$V_T$ Current, $I_{VT}$	$\pm 100mA$
Input Sink/Source, $I_{REF\_AC}$	$\pm 2mA$
$T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current	Outputs Unloaded		80	90	mA

**Table 4B. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current	Outputs Unloaded		75	85	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	1.2		$V_{CC}$	V
		$V_{CC} = 2.5V$	1.2		$V_{CC}$	V
$V_{IL}$	Input Low Voltage	1.8V logic	-0.3		0.3	V
$I_{IH}$	Input High Current	N[1:0], nOEA, nOEB $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	N[1:0], nOEA, nOEB $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-10			$\mu A$

**Table 4D. Differential DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Input Resistance	IN, nIN	IN to VT, nIN to VT	40	50	60	$\Omega$
$I_{IN}$	Input Current	IN, nIN				30	mA
$V_{REFAC}$	Bias Voltage		$V_{CC} = 2.5V$ or $3.3V$ $I_{REFAC} = \pm 1mA$	$V_{CC} - 1.5$	$V_{CC} - 1.28$	$V_{CC} - 1.0$	V

**Table 4E. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage <sup>1</sup>		$V_{CC} - 1.1$		$V_{CC} - 0.7$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 1.8$		$V_{CC} - 1.4$	V
$V_{OUT}$	Output Voltage Swing		0.5		1	V
$V_{DIFF\_OUT}$	Differential Output Voltage Swing		1		2	V

 NOTE 1. Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 4F. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage <sup>1</sup>		$V_{CC} - 1.1$		$V_{CC} - 0.7$	V
$V_{OL}$	Output Low Voltage <sup>1</sup>		$V_{CC} - 1.8$		$V_{CC} - 1.4$	V
$V_{OUT}$	Output Voltage Swing		0.5		1.0	V
$V_{DIFF\_OUT}$	Differential Output Voltage Swing		1		2	V

 NOTE 1. Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ <sup>1</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	$N = \div 1$			2500	MHz
		$N = \div 2$			1250	MHz
		$N = \div 4$			625	MHz
		$N = \div 8$			312.5	MHz
$f_{IN}$	Input Frequency				2500	MHz
$V_{CMR}$	Common Mode Input Voltage <sup>2</sup>	IN, nIN	1.0		$V_{CC} - V_{PP}/2$	V
$V_{PP}$	Input Voltage Swing		0.15		1.3	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing		0.3		2.6	V
tsk(o)	Output Skew <sup>3, 4</sup>			22	50	ps
tsk(pp)	Part-to-Part Skew <sup>3, 5</sup>				200	ps
	Noise Floor <sup>6</sup>	100kHz Offset, $f_{OUT} = 1228.8MHz$		-146		dBc/Hz
$f_{jit}(\theta)$	Buffer Additive Phase Jitter	$f_{REF} = f_{OUT} = 156.25MHz$ , Integration Range: 12kHz to 20MHz		42	60	fs
	Output Isolation	$f_{OUT} = 1228.8MHz$		90		dBc
		$f_{OUT} = 614.4MHz$		90		dBc
		$f_{OUT} = 307.2MHz$		90		dBc
		$f_{OUT} = 153.6MHz$		95		dBc
odc	Output Duty Cycle	50% Input Duty Cycle	44	50	56	%
$t_R / t_F$	Output Rise/Fall Time	20% to 80%			200	ps
$t_{PD}$	Propagation Delay		200		550	ps

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Common mode input voltage is defined as the signal cross point.

NOTE 3. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

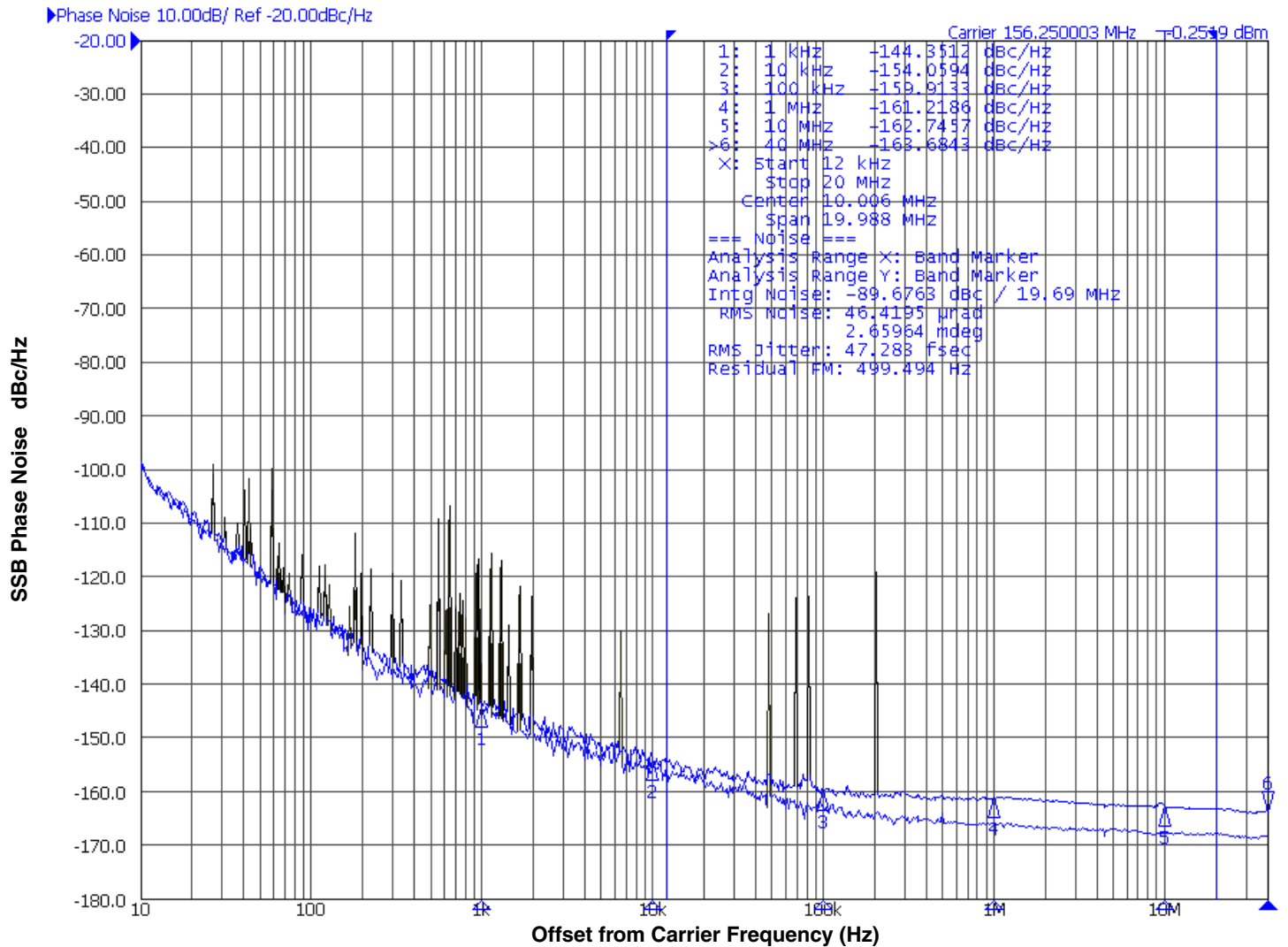
NOTE 5. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 6. The phase noise at 100kHz offset of the applied input clock is -146 dBc/Hz.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

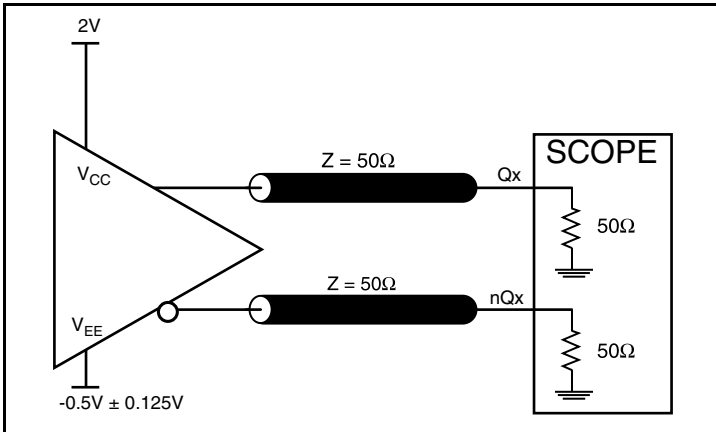
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



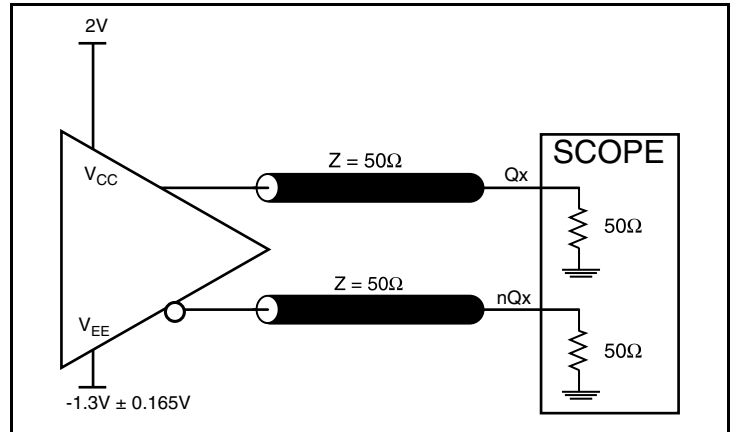
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using a 156.25 MHz Wenzel oscillator as input clock source and an Agilent E5052 Phase noise analyzer.

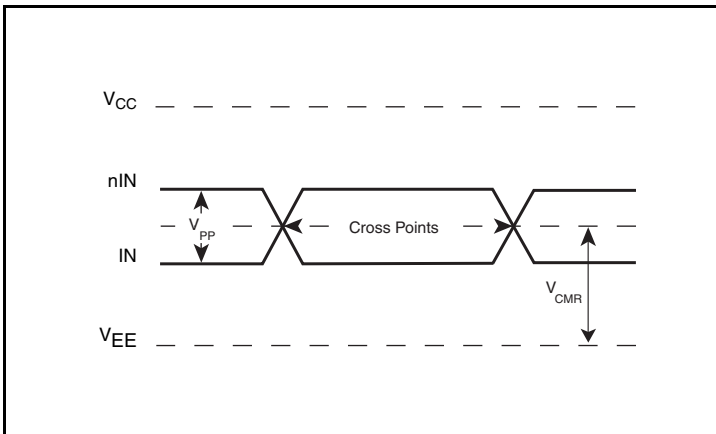
## Parameter Measurement Information



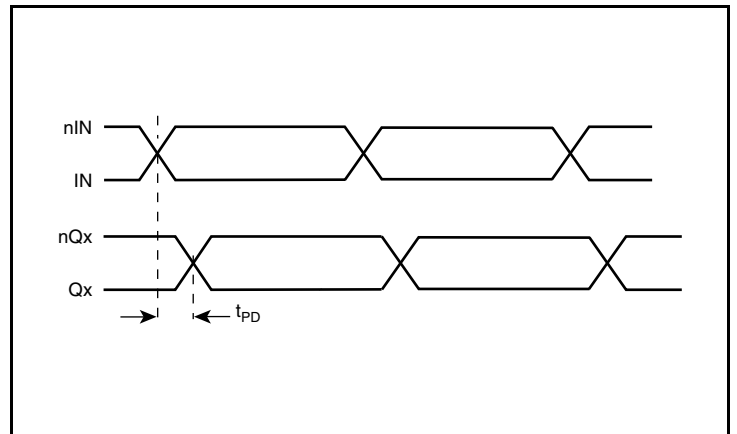
**2.5V Output Load AC Test Circuit**



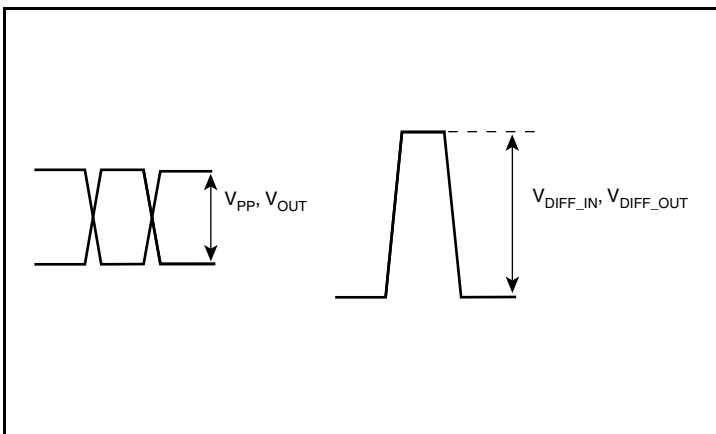
**3.3V Output Load AC Test Circuit**



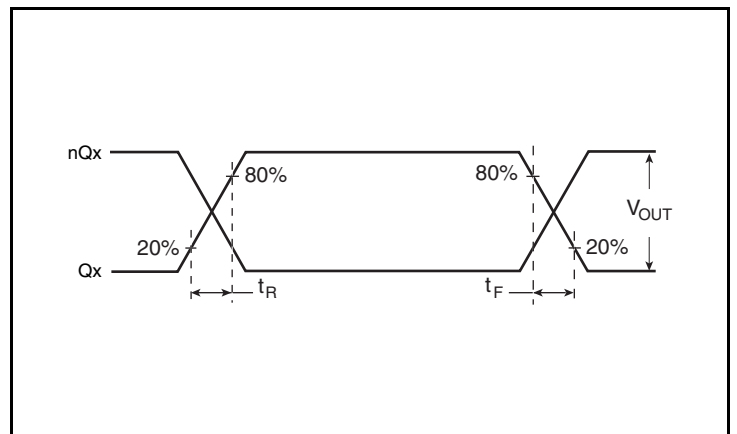
**Input Levels**



**Propagation Delay**



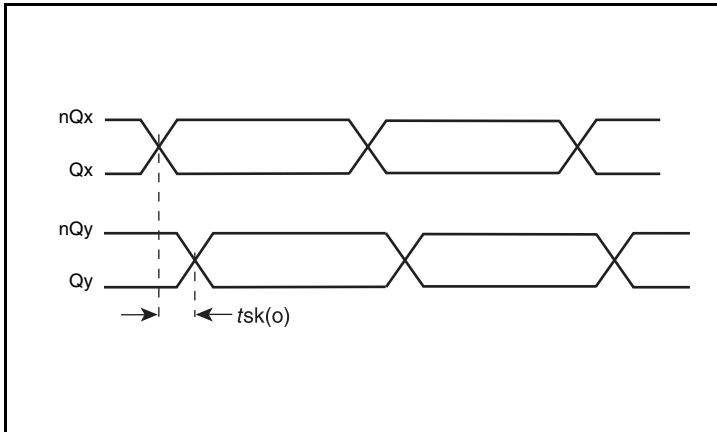
**Single-Ended & Differential Input Swing**



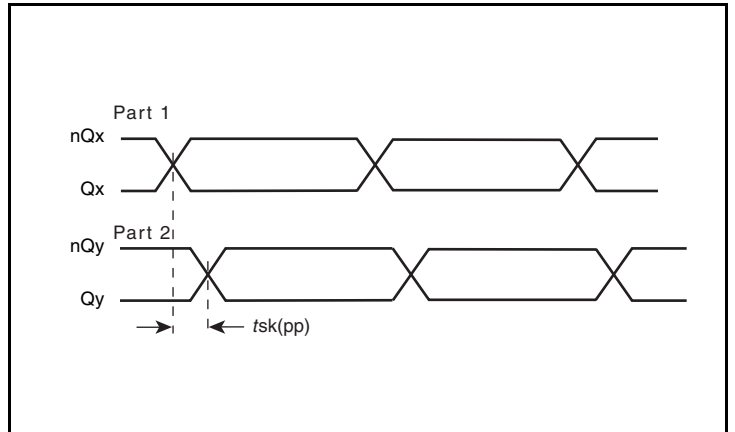
**Output Rise/Fall Time**



## Parameter Measurement Information, continued



**Output Skew**



**Part-to-Part Skew**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVCMOS Select Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

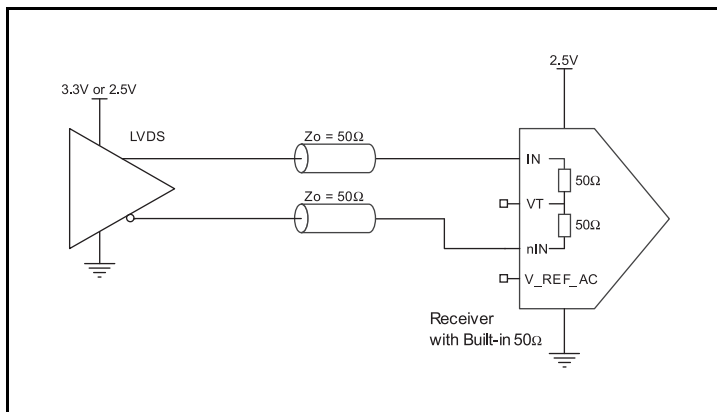
##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

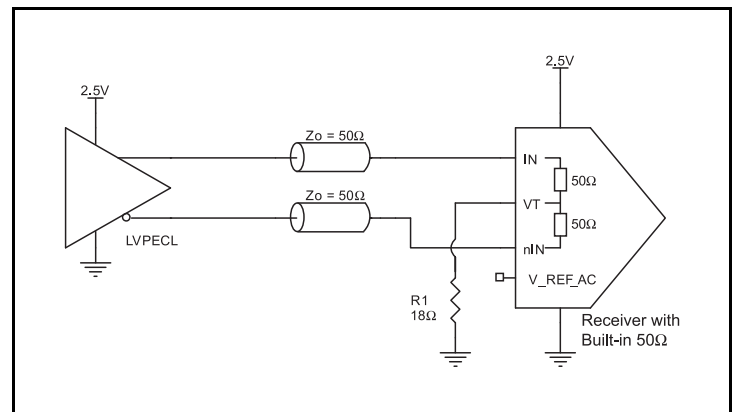
### 2.5V LVPECL Input with Built-In 50 $\Omega$ Termination Interface

The IN/nIN with built-in 50 $\Omega$  terminations accept LVDS, LVPECL, CML and other differential signals. Both  $V_{OH}$  and  $V_{OL}$  must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. *Figures 1A to 1D* show interface examples for the IN/nIN with built-in 50 $\Omega$  termination input driven by

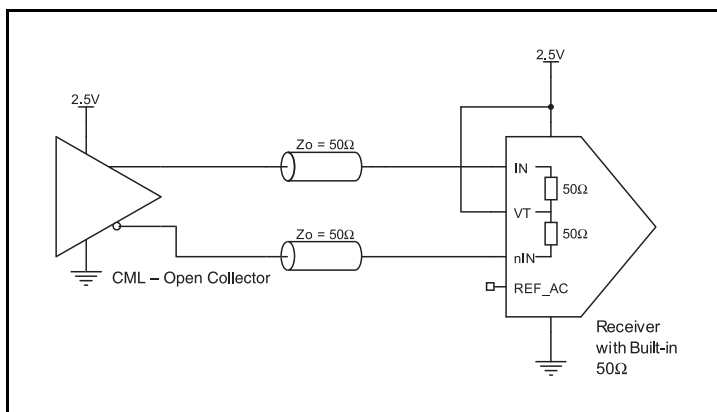
the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



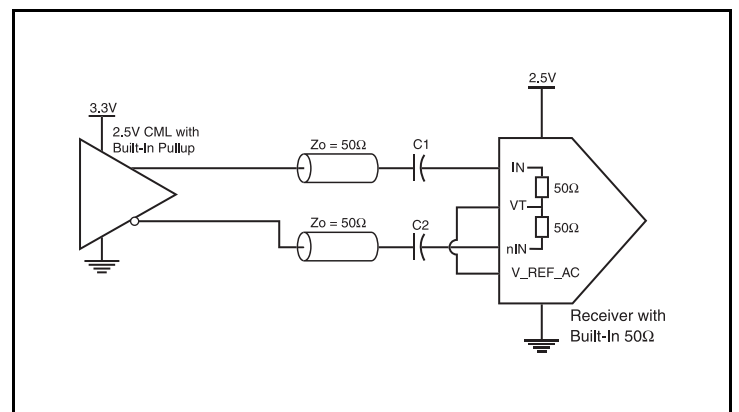
**Figure 1A. IN/nIN Input with Built-In 50 $\Omega$  Driven by an LVDS Driver**



**Figure 1B. IN/nIN Input with Built-In 50 $\Omega$  Driven by an LVPECL Driver**



**Figure 1C. IN/nIN Input with Built-In 50 $\Omega$  Driven by a CML Driver**

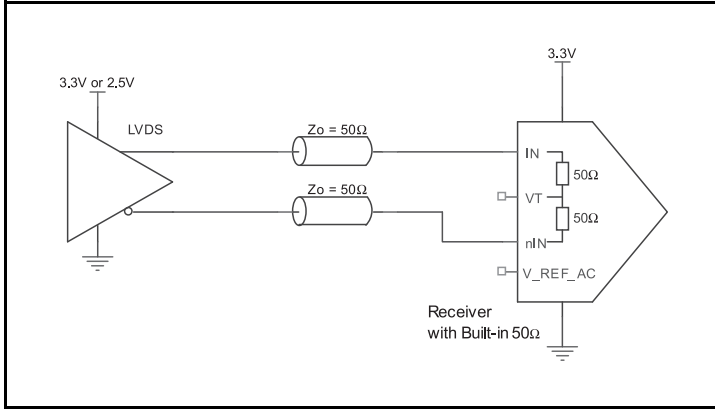


**Figure 1D. IN/nIN Input with Built-In 50 $\Omega$  Driven by a CML Driver with Built-In 50 $\Omega$  Pullup**

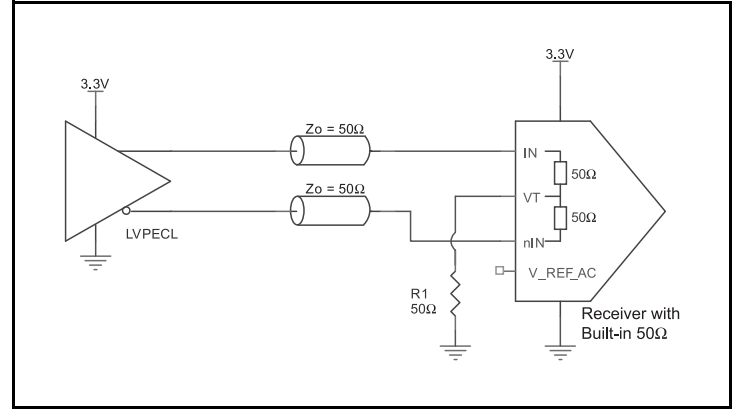
### 3.3V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both  $V_{OH}$  and  $V_{OL}$  must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by

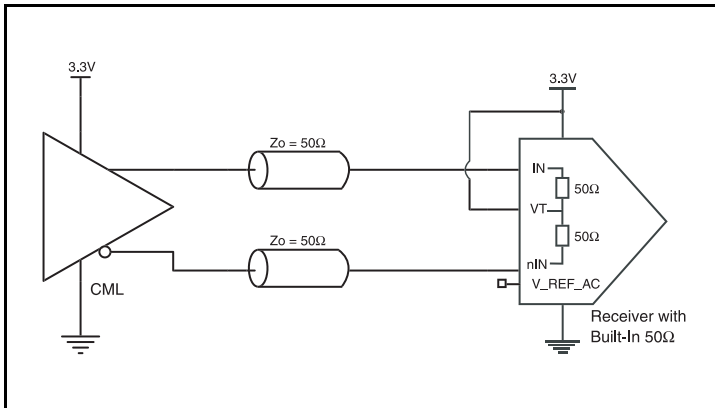
the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



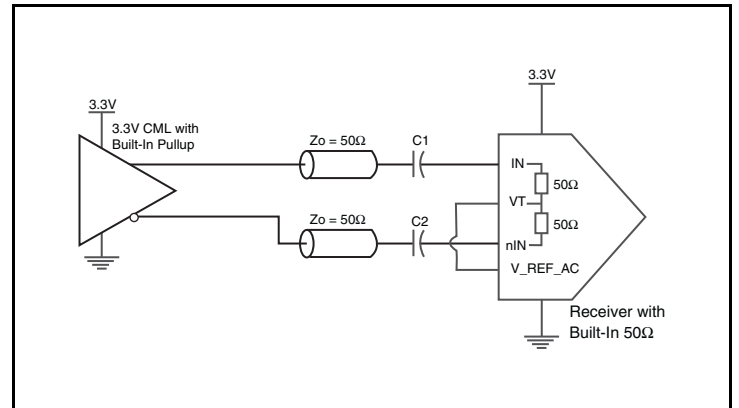
**Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



**Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



**Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector**



**Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup**



### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

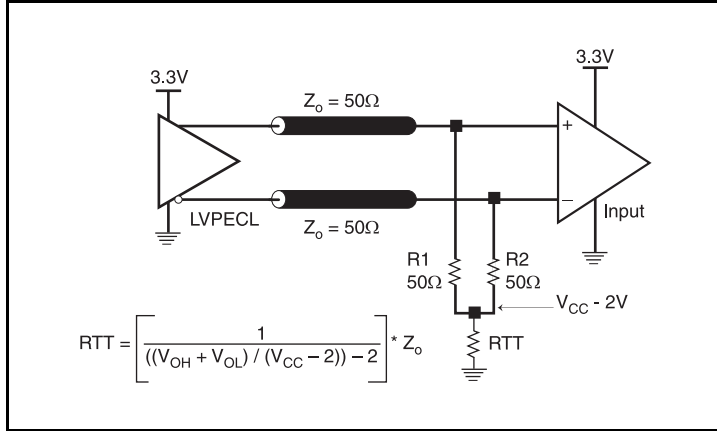


Figure 4A. 3.3V LVPECL Output Termination

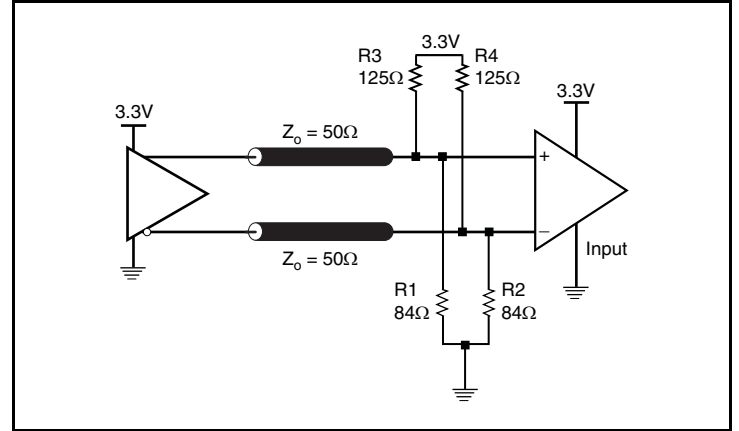


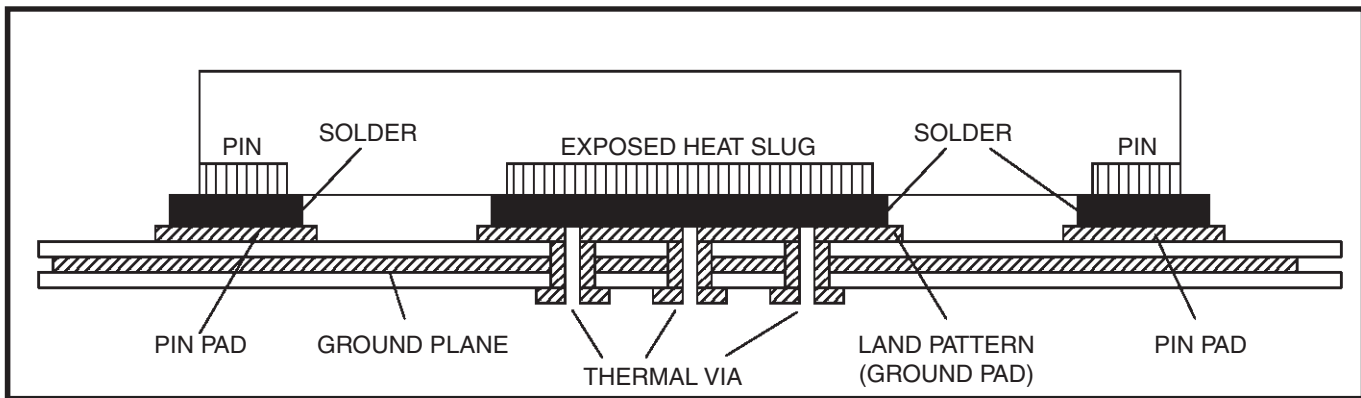
Figure 4B. 3.3V LVPECL Output Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

### 1. Power Dissipation

The total power dissipation for the 8V79S674 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

#### Core

- The maximum current at 85°C,  $I_{max} = 90mA$
- Power(core) =  $V_{CC\_MAX} * (I_{EE}) = 3.465V * 90mA = 311.9mW$

#### LVPECL Output

LVPECL driver power dissipation is 35mW/Loaded output pair, total LVPECL output dissipation:

- Power (outputs)<sub>MAX</sub> = **35mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 35mW = 140mW$

#### Total Power Dissipation

- Total Power**  
= Power (core) + Power(LVPECL)  
=  $311.9mW + 140mW$   
= **451.9mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70.7°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.452W * 70.7^\circ C/W = 117^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

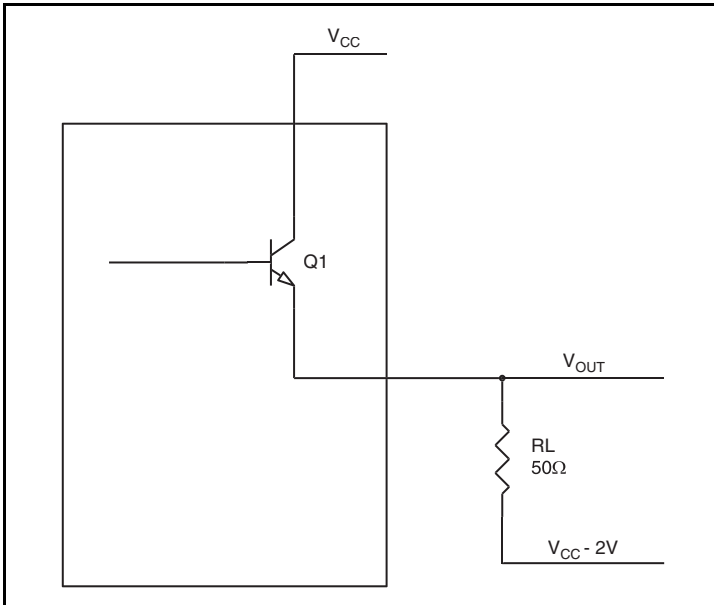
**Table 6. Thermal Resistance  $\theta_{JA}$  for for a 20-Lead VFQFN**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	70.7°C/W	67.0°C/W	65.3°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.7V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.7V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.4V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.4V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$\begin{aligned} Pd\_H &= [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) \\ &= [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) \\ &= [(2V - 0.7V)/50\Omega] * 0.7V = \mathbf{18.2mW} \end{aligned}$$

$$\begin{aligned} Pd\_L &= [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) \\ &= [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) \\ &= [(2V - 1.4V)/50\Omega] * 1.4V = \mathbf{16.8mW} \end{aligned}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{35mW}$$



## Reliability Information

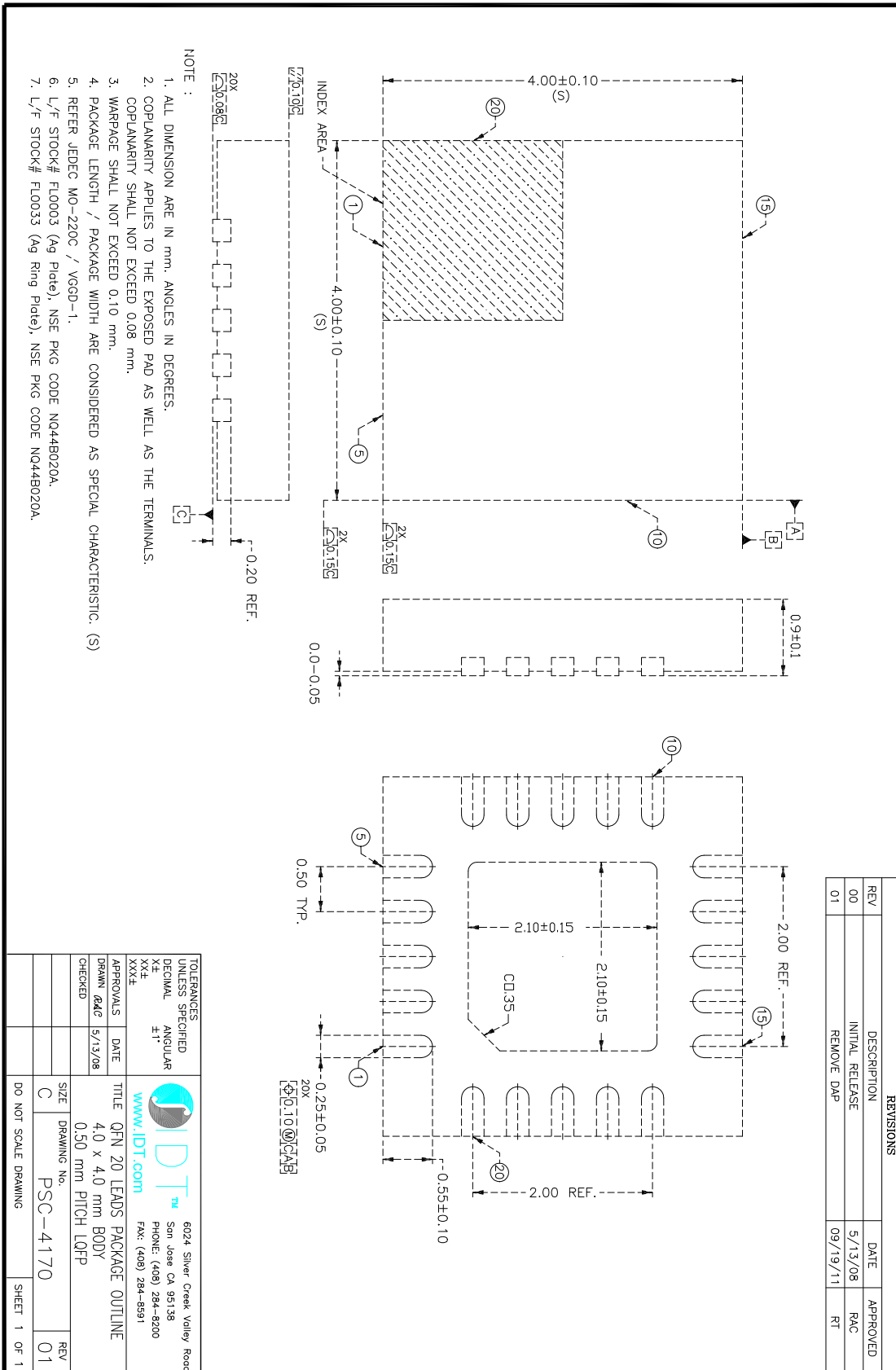
Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20-Lead VFQFN

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	70.7°C/W	67.0°C/W	65.3°C/W

## Transistor Count

The transistor count for 8V79S674: 1255

# 20-Lead VFQFN Package Outline and Package Dimensions



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/13/08	RAC
01	REMOVE DAP	09/19/11	RT

TOLERANCES UNLESS SPECIFIED		APPROVALS		DATE	
DECIMAL	ANGULAR	DATE	DATE	DATE	DATE
XXX	±1	5/13/08			
XXX					
DRAWN R44G		CHECKED		SIZE	
C		C		DO NOT SCALE DRAWING	
DRAWING No. PSC-4170		REV 01		SHEET 1 OF 1	

6024 Silver Creek Valley Road  
 San Jose CA 95138  
 PHONE: (408) 284-8200  
 FAX: (408) 284-9991  
[www.IDT.com](http://www.IDT.com)

## Ordering Information

**Table 8. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V79S674NLGI	8V79S674NLGI	“Lead-Free” 20-Lead VFQFN	Tray	-40°C to 85°C
8V79S674NLGI8	8V79S674NLGI	“Lead-Free” 20-Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
2	T5	6	AC Characteristics Table - corrected frequencies for $F_{OUT}$ $N\div 2$ , $N\div 4$ , $N\div 8$ . $f_{IN}$ changed from 2.5GHz to 2500MHz.	4/10/15



**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
www.IDT.com

**Tech Support**  
email: [clocks@idt.com](mailto:clocks@idt.com)

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2015 Integrated Device Technology, Inc.. All rights reserved.