National Semiconductor

93479
256 x 9-Bit Static Random Access Memory

General Description

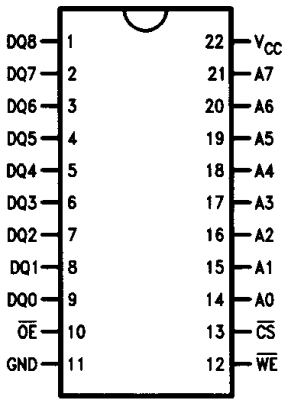
The 93479 is a 2304-bit read/write Random Access Memory (RAM), organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

Features

- Commercial address time
  93479—45 ns max
  93479A—35 ns max
- Military address access time
  93479—60 ns max
  93479A—45 ns max
- Common data input/output
- Features TRI-STATE® output

Connection Diagrams

22-Pin Ceramic DIP



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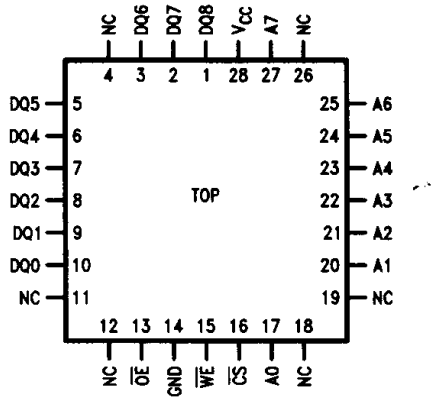
Top View

Order Number 93479DC, 93479ADC, 93479DMQB or 93479ADMQB
See NS Package Number J22A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn In

28-Pin LCC



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Top View

Order Number 93479LMQB or 93479ALMQB
See NS Package Number E28A*

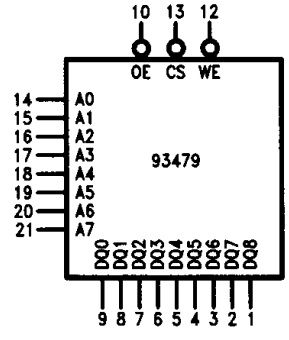
*For most current package information, contact product marketing.

Optional Processing QR = Burn In

Pin Names

A0–A7	Address Inputs
DQ0–DQ8	Data Input Outputs
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
NC	No Connect

Logic Symbol



V_{CC} = Pin 22
GND = Pin 11

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Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Notes 1, 2)	−0.5V to V_{CC} (RAMs) −1.5V to V_{CC} (PROMs)
Voltage Applied to Outputs (Notes 2, 3) (Output HIGH)	−0.5V to +5.5V (RAMs) −1.5V to +5.5V (PROMs)
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V. T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = $V_{OL\ (Max)}$ (0.45V), V_{IH} = $V_{OH\ (Min)}$ (2.4V).

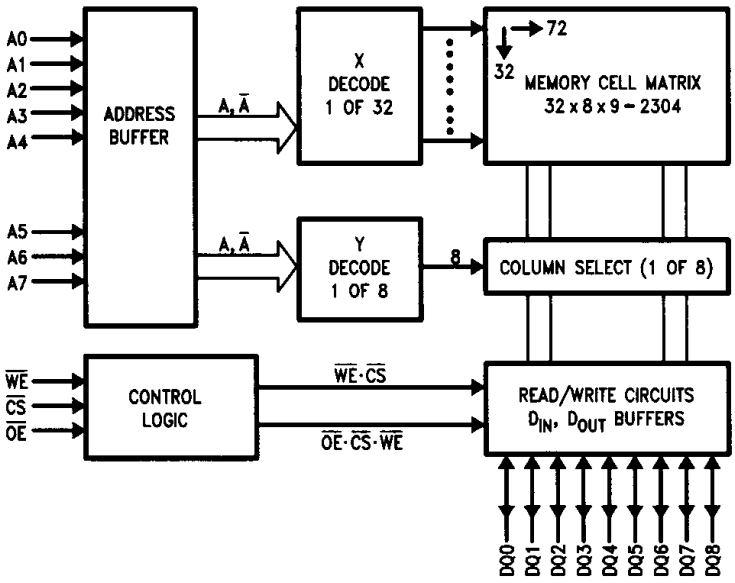
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



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Functional Description

The 93479 is a fully decoded 2304-bit random access memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address A0–A7.

The Chip Select input provides for memory array expansion. For larger memories the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected and the output disabled, the data at DQ0–DQ8 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected and the output enabled. Non-inverted data is then presented at the outputs DQ0–DQ8.

The 93479 has TRI-STATE outputs which provide an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-ups provide drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Data In/Out DQ0–DQ8	Mode
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$		
X	H	X	HIGH Z	Output Disabled
H	X	X	HIGH Z	R W Disabled
L	L	H	Data Out	Read
L	H	L	Data In	Write

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.5V
X = Don't Care HIGH or LOW
HIGH Z = High Impedance State

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA				0.5	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)		2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−250	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V			1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V			 −50	50 −400	μA μA
V_C	Input Diode Clamp Voltage	V_{CC} = Max, V_{IN} = −10 mA			−1.0	−1.5	V
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max, (Note 7)				−70	mA
I_{CC}	Power Supply Current	Commercial Military	V_{CC} = Max All Inputs GND			185 200	mA

Commercial

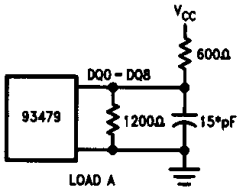
AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		25		25	ns
t_{ZRCS}	Chip Select to HIGH Z			25		25	ns
t_{AOS}	Output Enable Access Time			25		25	ns
t_{ZROS}	Output Enable to HIGH Z			25		25	ns
t_{AA}	Address Access Time (Note 8)			35		45	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	25		25		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		25		25		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns

Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%. GND = 0V. T_C = −55°C to +125°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		30		40	ns
t_{ZRCS}	Chip Select to HIGH Z			30		40	ns
t_{AOS}	Output Enable Access Time			30		40	ns
t_{ZROS}	Output Enable to HIGH Z			30		40	ns
t_{AA}	Address Access Time (Note 8)			45		60	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	40		40		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		50		50		ns
t_{WHD}	Data Hold Time after Write		10		10		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		10		10		ns
t_{WHA}	Address Hold Time after Write		10		10		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		10		10		ns
t_{WHCS}	Chip Select Hold Time after Write		10		10		ns



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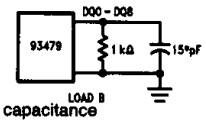

*Includes jig and probe capacitance

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Note: Load A is used for all production testing.

FIGURE 1. AC Test Load Output Load

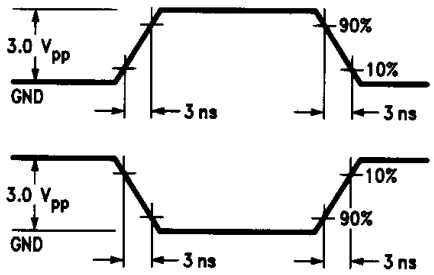

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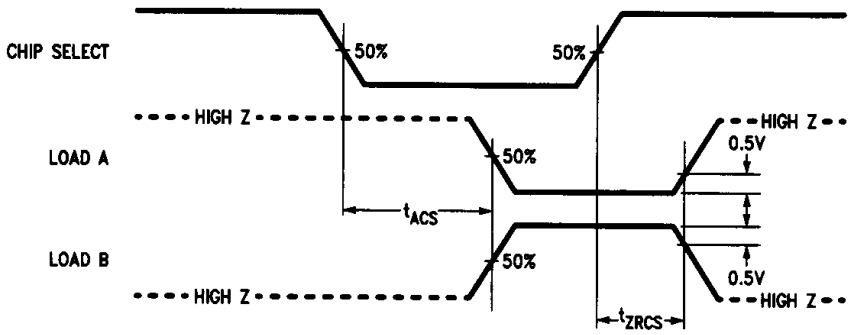
FIGURE 2. AC Test Input Levels



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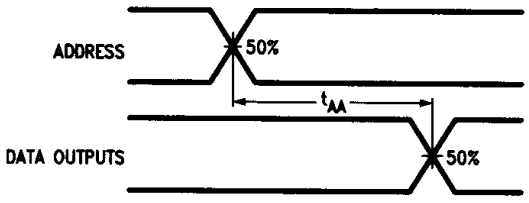
a. Read Mode Propagation Delay from Chip Select to Output



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b. Read Mode Propagation Delay from Address to Output

FIGURE 3. Read Mode Timing

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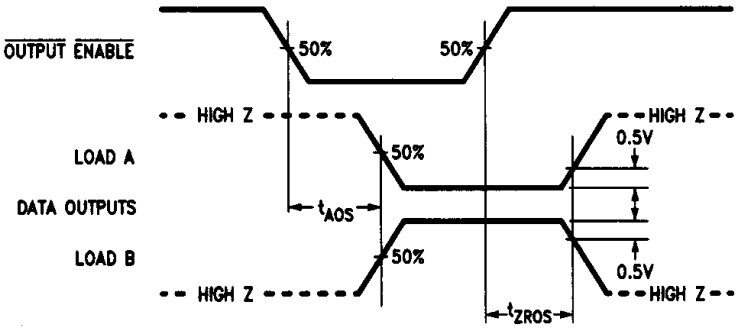

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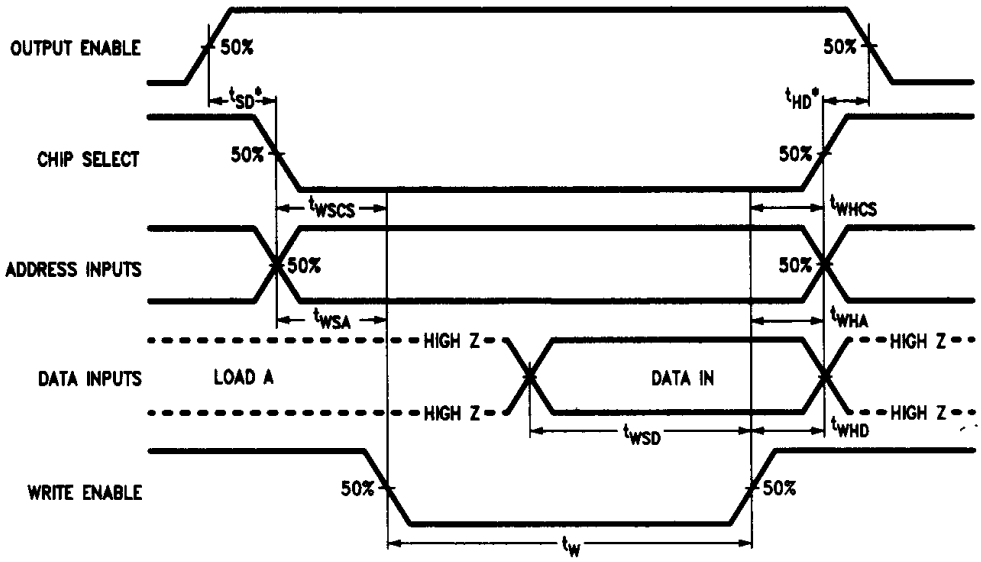
c. Read Mode Propagation Delay from Output Enable
FIGURE 3. Read Mode Timing (Continued)



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*These timing parameters are only necessary to guarantee High Z state during the entire write cycle.

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0/0.0V.