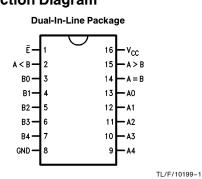


93L24 **5-Bit Comparator**

General Description

The 93L24 expandable comparator provides comparison than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

Connection Diagram



Order Number 93L24DMQB or 93L24FMQB See NS Package Number J16A or W16A

Pin Names	Description
Ē	Enable Input (Active LOW)
A0-A4	Word A Parallel Inputs
B0-B4	Word B Parallel Inputs
A <b< td=""><td>A Less than B Output (Active HIGH)</td></b<>	A Less than B Output (Active HIGH)
A>B	A Greater than B Output (Active HIGH)
A=B	A Equal to B Output (Active HIGH)

Features

- Three separate outputs: A<B, A>B, A=B
- Easily expandable

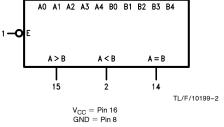
Logic Symbol

Active low enable input



13 12 11 10 9 3 4 5 6 7

June 1989



Truth Table

Inputs			Outputs		
Ē	An	Bn	A <b< th=""><th>A>B</th><th>$\mathbf{A} = \mathbf{B}$</th></b<>	A>B	$\mathbf{A} = \mathbf{B}$
н	Х	Х	L	L	L
L	Word A =	Word B	L	L	н
L	Word A >	Word B	L	н	L
L	Word B <	Word A	н	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage 7V

7V
5.5V
-55°C to +125°C
$-65^{\circ}C$ to $+150^{\circ}C$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	93L24 (MIL)			Units
Cymbol	i aranieter	Min	Nom	Max	onita
V _{CC}	Supply Voltage	4.5	5	5.5	V
VIH	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.7	v
I _{OH}	High Level Output Current			-400	μA
I _{OL}	Low Level Output Current			4.8	mA
T _A	Free Air Operating Temperature	-55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Мах	Units
VI	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -10 \text{ mA}$			-1.5	V
V _{OH}	High Level Output Voltage	$V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min$	2.4			V
V _{OL}	Low Level Output Voltage	$\label{eq:V_CC} \begin{split} V_{CC} &= \text{Min, } I_{OL} = \text{Max,} \\ V_{IH} &= \text{Min, } V_{IL} = \text{Max} \end{split}$			0.3	V
lı	Input Current @ Max Input Voltage	$V_{CC} = Max, V_1 = 5.5V$			1	mA
I _{IH}	High Level Input Current	$V_{CC} = Max, V_I = 2.4V$			40	μA
IIL	Low Level Input Current	$V_{CC} = Max, V_I = 0.3V$			-0.8	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	-2.5		-25	mA
ICC	Supply Current	V _{CC} = Max			21	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

O y III DOI	Parameter	C _L =	C _L = 15 pF	
Symbol		Min	Max	Units
t _{PLH} t _{PHL}	Propagation Delay \overline{E} to A=B; \overline{E} to A <b, a="">B</b,>		32 35	ns
t _{PLH} t _{PHL}	Propagation Delay An to $A>B$; Bn to $A>B$		54 75	ns
t _{PLH} t _{PHL}	Propagation Delay An to A <b; a<b<="" bn="" td="" to=""><td></td><td>70 77</td><td>ns</td></b;>		70 77	ns

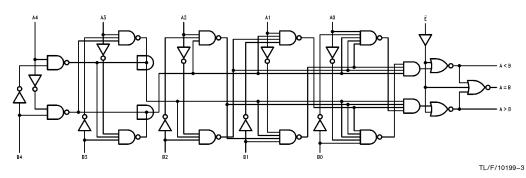
Functional Description

The 93L24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these ouptuts are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input (E).

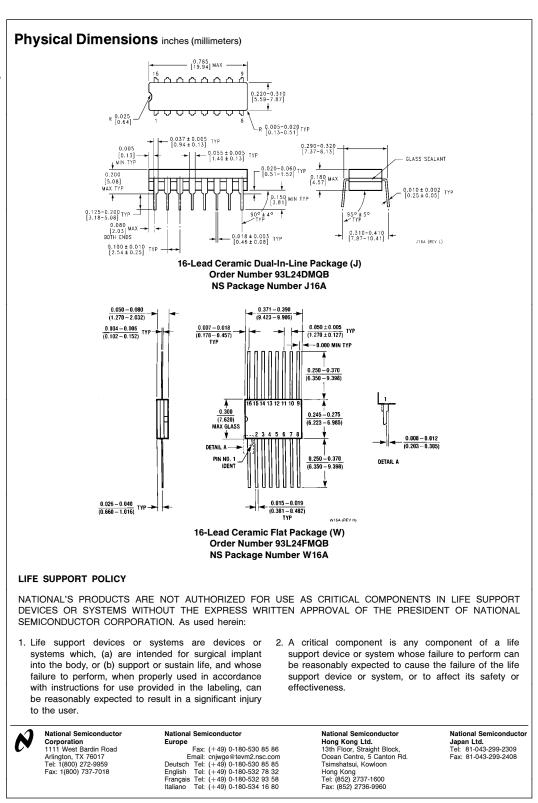
Tying the A>B output from one device into an A input on another device and the A< B output into the corresponding B input permits easy expansion.

The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A>B output will be HIGH regardless of all other inputs except \overline{E} .

Logic Diagram







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